Circulating Current Suppression of Current-Fed Push–Pull DC–DC Converter With Natural Commutation Strategy

Zhifeng Sun, Yankun Chen, Jinhui Zeng, Qunfang Wu, *Member, IEEE*, Jiangli Ren, Wei Su, and Pengfei Yu

***Abstract*—In low-voltage high-current applications, the current-fed push–pull (CFPP) converter stands as one of the promising topological candidates. However, voltage spikes will occur when input inductor current and leakage inductor current become mismatched. Natural commutation techniques have attracted significant attention due to their ability to mitigate voltage spikes without requiring additional clamping circuits. Nevertheless, existing natural commutation strategies still exhibit limitations in terms of excessive current stress and substantial circulating current. To address these challenges, this article proposes a circulating current suppression (CCS) modulation strategy. The fundamental principle involves strictly controlling both duty cycle and phase shift angle of the CFPP converter to minimize current mismatch duration, thereby significantly reducing current stress and circulating current. First, this article elaborates on the operational principles of the proposed CCS strategy and derives mathematical expressions for its transmission power, current stress, circulating power, and loss model. Furthermore, to highlight the advantages of proposed CCS strategy, mathematical models for current stress and circulating power in existing natural commutation strategies are systematically established, followed by comprehensive comparative analysis and simulation validation. Finally, a 500 W CFPP prototype is constructed for experimental validation. Experimental results demonstrate that compared with state-of-the-art strategies, the proposed CCS strategy achieves at least a 35.21% reduction in current stress and at least a 67.26% reduction in circulating power. On the other hand, it also shows advantages in terms of cost and compactness.**

***Index Terms*—Circulating current suppression (CCS), current-fed push–pull (CFPP) converter, dc–dc converter, natural commutation.**

Received 11 March 2025; revised 5 July 2025; accepted 18 August 2025. Date of publication 25 August 2025; date of current version 13 November 2025. This work was supported in part by the National Natural Science Foundation of China under Grant 52407206 and Grant 52377185, in part by the Scientific Research Project of Hunan Provincial Department of Education under Grant 24B0545, and in part by Steady Support Fund for State Key Laboratory under Grant JBS242800150 and Grant JSZL2023610B001-066. Recommended for publication by Associate Editor S. K. Mishra. *(Corresponding author: Qunfang Wu.)*

Zhifeng Sun, Yankun Chen, and Jinhui Zeng are with the Hunan University of Technology, Zhuzhou 412007, China (e-mail: sunzhifeng@hut.edu.cn; m24085800086@stu.hut.edu.cn; zjh@hut.edu.cn).

Qunfang Wu and Jiangli Ren are with the Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China (e-mail: wuqunfang@nuaa.edu.cn; sx2103048@nuaa.edu.cn).

Wei Su and Pengfei Yu are with the Laboratory of Science and Technology on Reliability Physics and Application of Electronic Component, Guangzhou 511370, China (e-mail: suwei@ceprei.com; yupengfei@ceprei.com).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3602280.

Digital Object Identifier 10.1109/TPEL.2025.3602280

I. Introduction

RENEWABLE energy sources such as solar photovoltaic and fuel cells exhibit low-voltage high-current output characteristics. The current-fed isolated bidirectional dc–dc converter (CF-IBDC) has been widely employed in scenarios interconnecting renewable energy systems with high-voltage dc buses [1], [2], owing to its advantages including low input current ripple, high voltage gain, and electrical isolation [3], [4]. Established CF-IBDC topologies encompass half-bridge [5], L-L type [6], [7], resonant [8], full-bridge [9], [10], [11], [12], and push–pull configurations [13], [14]. Compared with other topologies, push–pull and full-bridge converters demonstrate significant advantages in design cost and compactness [4]. Studies demonstrate that mismatch between input inductor current and leakage inductor current triggers high-voltage spikes across primary-side switches in current-fed push–pull (CFPP) converter [13], [15], [16]. Additionally, current mismatch induces significant circulating currents between primary and secondary sides, increasing device current stress and conduction losses.

To address voltage spikes, existing research primarily focuses on two categories: 1) clamping techniques and 2) natural commutation techniques. Clamping techniques suppress voltage spikes through additional circuits, including passive and active clamping methods. In passive clamping techniques, dissipative *RC* [17], [18], and RCD [19] snubbers offer structural simplicity but suffer from low efficiency due to resistive energy dissipation. Nondissipative *LC* snubbers [20] recycle energy through resonance, yet face challenges in resonant parameter design and limited soft-switching ranges. Active clamping techniques construct an energy transfer path by adding power transistors and high-frequency capacitors [21], [22], leveraging the charging/discharging characteristics of high-frequency capacitors to suppress voltage spikes. For example, in [21], a clamp circuit consisting of power transistors and capacitors was added to the LL type current-fed full bridge converter, effectively reducing the problem of voltage spikes. Wu et al. [22] proposed an active clamp three switch push–pull full bridge bidirectional dc–dc converter (TPFBC) topology based on a TPFBC. By adding a capacitor clamp circuit, not only is the voltage spike of the converter effectively suppressed, but the soft switching range is also expanded. Additionally, the study in [23] and [24] reconstruct the circuit based on the single half-bridge structure [5] to obtain an LL type DAB topology, recognized as a special active-clamped

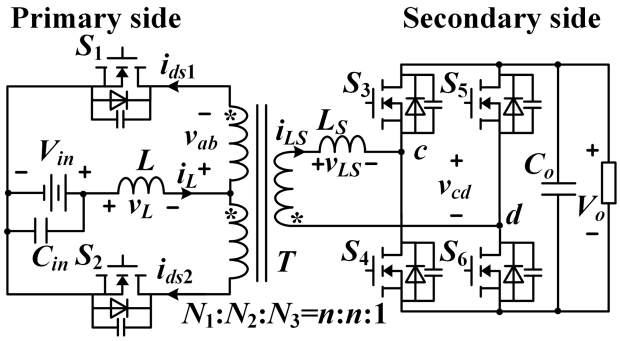

Fig. 1. Topology configuration of CFPP converter.

LL type topology. By adopting pulsewidth modulation combined with phase-shift control, it addresses high circulating current losses while maintaining the advantages of active clamping. However, after fixing the pulse width on the high-voltage side, the circulating current remains relatively large, and it still relies on the clamping circuit to suppress voltage spikes. In summary, active clamping techniques increase system volume and cost but cannot effectively suppress circulating current.

Natural commutation techniques achieve zero-current commutation by optimizing switching sequences or duty cycles, enabling primary current reversal through body diodes at current zero-crossing instants. Specifically, during switch turn-OFF, the primary reverse current freewheels through body diodes. As junction capacitors cannot charge during switch turn-OFF but only after current freewheeling concludes, voltage spikes are effectively suppressed [25], [26]. Established natural commutation strategies include single-PWM (SP), dual-PWM (DP), and PWM plus phase-shift (PPS), currently applied to L-L type, full-bridge, and push–pull topologies [6], [7], [9], [10], [11], [13], [14]. In [6], [9], and [13], the SP strategy is proposed where primary switch gate signals adopt variable-duty-cycle square waves. This method generates bipolar voltage waveforms at secondary bridge midpoints, achieving ZCC and voltage spike suppression. However, reduced input voltage or low power transfer significantly increases primary switch reverse current, leading to excessive current stress and circulating currents. To mitigate circulating currents and current stress, in [7] and [10], the DP strategy is introduced incorporating additional duty cycle control for full-bridge rectification. However, discontinuous series inductor current causes voltage/current oscillations, increasing system losses and impeding soft-switching realization. In [11] and [14], the PPS strategy is proposed by introducing phase-shift angles between secondary bridge arms on the basis of SP, generating triple level voltage waveforms at bridge midpoints. The added phase shift transforms primary switch reverse current and leakage current from triangular to trapezoidal profiles, thereby reducing current stress and circulating currents. Nevertheless, current stress remains suboptimal. Furthermore, existing strategies exhibit prolonged current mismatch duration when primary inductor current reaches its peak, resulting in substantial residual circulating currents.

To reduce circulating currents and current stress in CFPP converters, this article proposes a circulating current suppression (CCS) strategy. Its core principle lies in minimizing circulating power by reducing both current mismatch duration and current stress. Compared with existing natural commutation strategies, the proposed approach achieves significantly lower circulating power and current stress while enhancing system efficiency.

The contributions are as follows.

1) A novel CCS strategy is proposed, along with detailed implementation principles. Compared with the state-of-the-art PPS strategy, the proposed CCS strategy reduces the total circulating power by 78.41% and 67.26% under half-load and full-load conditions, respectively.
2) Operational modes of the proposed CCS strategy are analyzed. Mathematical expressions for transmission power, current stress, and circulating power are derived, enabling quantitative analysis characteristics of CFPP converter.
3) Detailed mathematical models of current stress, circulating power, and loss of CFPP with the existing SP, DP, and PPS strategies are rigorously derived. A comprehensive comparative analysis is conducted to validate the superiority of the proposed circulating current suppression strategy in terms of efficiency, cost, and compactness.

This article presents the operating principles and development process of the proposed strategy, accompanied by experimental validation. The rest of this article is organized as follows. Section II performs steady-state analysis of the proposed CCS strategy, derives control variable mathematical models, and explains implementation principles. Section III presents a characteristic analysis of the proposed CCS strategy, derives expressions for CFPP characteristics, including models of voltage gain, transmission power, current stress, circulating power, and loss. Section IV conducts a comprehensive comparison between the existing strategies and the proposed CCS strategy in terms of current stress, circulating power, losses, cost, and compactness. Section V presents the PLECS simulation results and experimental results of the 500 W prototype to validate the effectiveness of the proposed CCS strategy. Finally, Section VI concludes this article.

II. Operational Principle

Fig. 1 illustrates the topological configuration of the CFPP converter. The converter consists of a primary-side push–pull circuit, a high-frequency transformer, and a secondary-side full-bridge circuit, where L denotes the primary-side input inductor, L_S represents the equivalent total leakage inductance referred to the secondary side, and the transformer turns ratio is defined as $N_1 : N_2 : N_3 = n : n : 1$. $V_{\rm in}$ and V_o correspond to the input and output voltages, respectively. $v_{\rm ab}$ and $v_{\rm cd}$ indicate the voltages across winding N_1 and the midpoint voltage of the secondary full-bridge legs, respectively. v_L and v_{LS} denote the input inductor voltage and leakage inductor voltage, with i_L and i_{LS} being their respective currents. i_{ds1} and i_{ds2} characterize the drain-source currents of switches S_1 and S_2. The transmission power is defined as P, and the voltage gain is expressed as $M = nV_o/V_{\rm in}$.

Fig. 2 provided the key waveforms of the proposed CCS strategy, which include two control variables D and D_2. Here, D

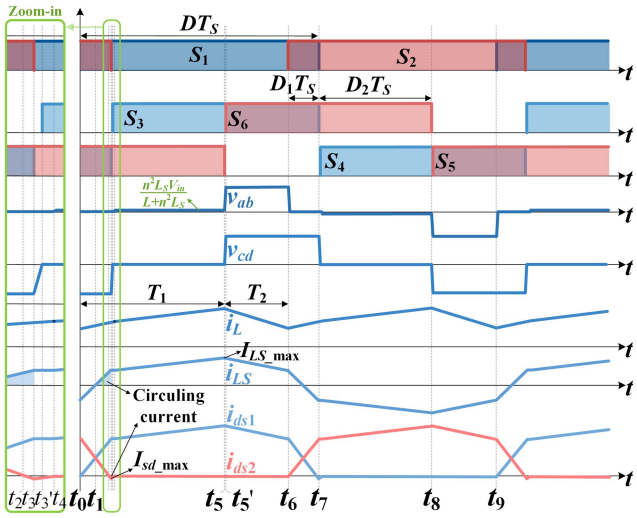

Fig. 2. Operation waveforms of the proposed CCS strategy.

denotes the duty cycle of primary switches S_1 and S_2, while D_2 represents the inner phase-shift angle between the bridge arms of the secondary full bridge. The overlapping part of the duty cycles of S_1 and S_2 is defined as D_1, satisfying $D_1 + 0.5 = D$. Furthermore, the driving signals of S_1 and S_2 are 180° out of phase. The driving signals of the switches in the same bridge arm of the secondary full bridge are also 180° out of phase, with dead times incorporated.

A. Mode Analysis

The proposed CCS strategy has symmetrical waveforms in both half-cycles. Therefore, only the operational modes in the first half-cycle are analyzed. The half-cycle operation is divided into eight intervals, and the equivalent circuits corresponding to each mode are shown in Fig. 3. Here, T_S denotes the duration of a half-cycle.

Interval 1 [see Fig. 3(a), $t_0 \le t \le t_1$]: Before t_0, switches S_2, S_4, and S_5 are conducting. The input inductor current matches the secondary-side leakage inductance current, and the converter transfers energy between the primary and secondary sides. At t_0, switch S_1 is turned ON with zero-voltage switching (ZVS), resulting in a mismatch between the input inductor current and leakage inductance current. During this interval, the input inductor L is charged, and the transformer leakage inductance L_S discharges to the V_2-side. The voltage and current expressions of the input inductor L and leakage inductance L_S can be expressed as

$$\begin{cases} v_L(t) = V_{\text{in}} \\ v_{LS}(t) = V_o \\ i_L(t) = \frac{1}{L}\int_{t_0}^{t} V_L(t)dt = i_L(t_0) + \frac{V_{\text{in}}(t-t_0)}{L} \\ i_{LS}(t) = \frac{1}{L_S}\int_{t_0}^{t} V_{LS}(t)dt = i_{LS}(t_0) + \frac{MV_{\text{in}}(t-t_0)}{nL_S}. \end{cases} \tag{1}$$

Interval 2 [see Fig. 3(b), $t_1 \le t \le t_2$]: At t_1, i_{LS} crosses zero and reverses polarity, causing the leakage inductance to transition from a discharging state to a charging state. The states of all other devices remain identical to those in Interval 1.

Interval 3 [see Fig. 3(c), $t_2 \le t \le t_3$]: At t_2, i_{ds2} crosses zero and reverses polarity, reaching its peak value at t_3. The states of all other devices remain identical to those in Interval 2.

Interval 4 [see Fig. 3(d), $t_3 \le t \le t_3'$]: At t_3, switch S_2 turns OFF, and the reverse current freewheels through its body diode, causing i_{ds2} to decrease from its peak value. For the secondary-side full-bridge circuit, the junction capacitance of switch S_3 discharges, while that of S_4 charges.

Interval 5 [see Fig. 3(e), $t_3' \le t \le t_4$]: At t_3', switch S_3 is turned ON with ZVS. During this interval, i_{LS} remains constant, and the states of the primary-side push–pull circuit are identical to those in Interval 4.

Interval 6 [see Fig. 3(f), $t_4 \le t \le t_5$]: At t_4, the drain current i_{ds2} is zero. The input inductor current matches the leakage inductance current, enabling energy transfer from the primary to the secondary side. Both the input inductor L and leakage inductance L_S are in a charging state. Additionally, since the input inductance L is significantly larger than L_S, the charging slope of the input inductor is approximated as V_{in}/L. The key expressions in this interval are

$$\begin{cases} v_L(t) = \frac{LV_{\text{in}}}{L+n^2L_S} \\ v_{LS}(t) = \frac{nL_SV_{\text{in}}}{L+n^2L_S} \\ i_L(t) = \frac{1}{L}\int_{t_4}^{t} V_L(t)dt = i_L(t_4) + \frac{V_{\text{in}}(t-t_4)}{L} \\ i_{LS}(t) = \frac{1}{L_S}\int_{t_0}^{t} V_{LS}(t)dt = i_{LS}(t_4) + \frac{nV_{\text{in}}(t-t_4)}{L+n^2L_S}. \end{cases} \tag{2}$$

Interval 7 [see Fig. 3(g), $t_5 \le t \le t_5'$]: At t_5, the junction capacitance of switch S_2 charges, enabling S_2 to achieve zero-current switching (ZCS). For the secondary-side full-bridge circuit, the junction capacitances of switches S_5 and S_6 are in discharging and charging states, respectively.

Interval 8 [see Fig. 3(h), $t_5' \le t \le t_6$]: At t_5', switch S_6 is turned ON with ZVS, and i_L reaches its peak value. The V_{in} source, input inductor L, and leakage inductance L_S collectively discharge to the V_o-side. The key expressions in this interval are

$$\begin{cases} v_L(t) = \frac{V_{\text{in}}(1-M)L}{L+n^2L_S} \\ v_{LS}(t) = \frac{nV_{\text{in}}(1-M)L_S}{L+n^2L_S} \\ i_L(t) = \frac{1}{L}\int_{t_5'}^{t} v_L(t)dt = i_L(t_{5prime}) + \frac{V_{\text{in}}(1-M)(t-t_5')}{L+n^2L_S} \\ i_{LS}(t) = \frac{1}{L_S}\int_{t_5'}^{t} v_{LS}(t)dt = i_{LS}(t_5') + \frac{nV_{\text{in}}(1-M)(t-t_5')}{L+n^2L_S}. \end{cases} \tag{3}$$

B. Realization Mechanism of Proposed CCS Method

Existing SP, DP, and PPS natural commutation techniques can achieve matching between input inductor current and leakage inductor current by controlling duty cycle and phase-shift angle, thus effectively eliminating voltage spikes. We find that in one switching cycle, the current matching time points of SP, DP, and PPS strategies are relatively lagging, leading to issues of large current stress and circulating current. To address the abovementioned problems, by advancing the current matching time point, we propose a CCS strategy with low current stress and circulating current, as shown in Fig. 2. The implementation of the CCS modulation strategy under different operating conditions lies in the precise coordination of duty cycle D and phase-shift angle D_2. Next, based on the modulation waveform of CCS

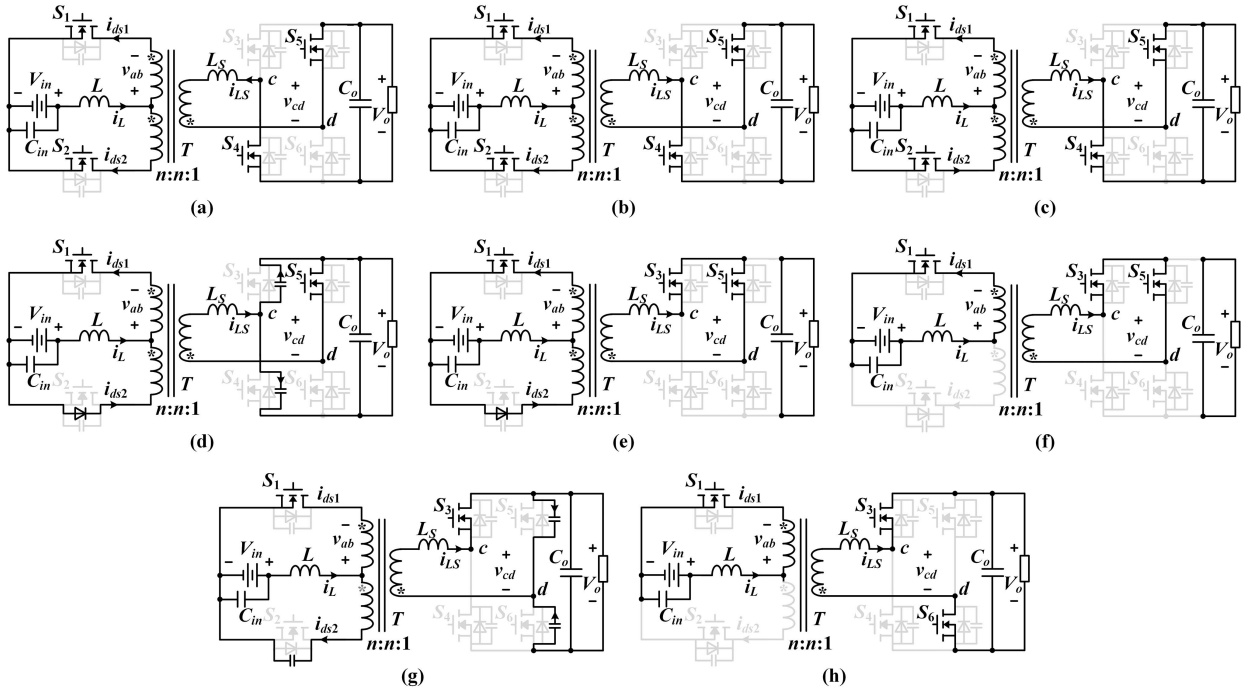

Fig. 3. Equivalent circuit for half a cycle of the proposed CCS strategy (Interval 1–8). (a) Interval 1. (b) Interval 2. (c) Interval 3. (d) Interval 4. (e) Interval 5. (f) Interval 6. (g) Interval 7. (h) Interval 8.

and combined with the circuit principle of CFPP, we derive the expressions for the control variables D and D_2. It should be noted that under different operating conditions, substituting circuit parameters into the control variable expressions can realize the CCS modulation waveform, and the converter can operate in a low current stress and circulating current mode.

Based on the modal analysis in the previous section, Intervals 4 and 5 are significantly shorter than the switching period and, thus, can be neglected. The duration of Interval 6 is defined as D_2T_S. According to (1), (2), and (3), the instantaneous leakage inductor currents at t_3, t_5, and t_6, denoted as $i_{LS}(t_3)$, $i_{LS}(t_5)$, and $i_{LS}(t_6)$ are, respectively, derived as

$$\begin{cases} i_{LS}(t_3) = i_{LS}(t_0) + \frac{MV_{\text{in}}D_1T_S}{nL_S} \\ i_{LS}(t_5) = i_{LS}(t_3) + \frac{nV_{\text{in}}D_2T_S}{L+n^2L_S} \\ i_{LS}(t_6) = i_{LS}(t_5) + \frac{nV_{\text{in}}(1-M)(0.5-D_1-D_2)T_S}{L+n^2L_S}. \end{cases} \tag{4}$$

The leakage inductor current i_{LS} exhibits symmetry between positive and negative half-cycles, satisfying $i_{LS}(t_0) = -i_{LS}(t_6)$. Substituting this condition into (4) yields the leakage inductor current magnitude at t_0 can be expressed as

$$i_{LS}(t_0) = \frac{nV_{\text{in}}(M-1)(0.5-D_1-D_2)T_S}{2L+2n^2L_S} - \frac{MV_{\text{in}}D_1T_S}{2nL_S} - \frac{nV_{\text{in}}D_2T_S}{2L+2n^2L_S}. \tag{5}$$

Furthermore, based on the transformer primary-secondary current conversion relationship, we have $i_L(t_0) = -i_{LS}(t_0)/n$, the input inductor current magnitude at t_0 can be calculated as

$$i_L(t_0) = \frac{MV_{\text{in}}D_1T_S}{2n^2L_S} + \frac{V_{\text{in}}D_2T_S}{2L+2n^2L_S}$$

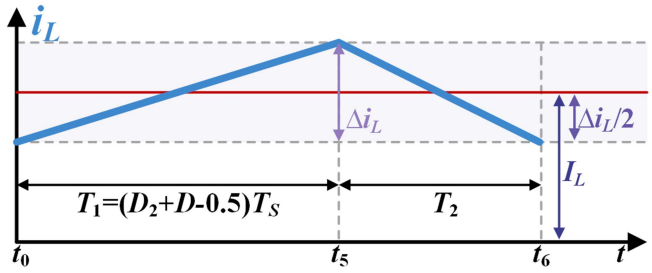

Fig. 4. Zoomed waveform of input inductor current.

$$+ \frac{(V_{\text{in}} - MV_{\text{in}})(0.5-D_1-D_2)T_S}{2L+2n^2L_S}. \tag{6}$$

For the CFPP converter, the average inductor current over a half-cycle equals the input current, we obtain

$$I_L = I_{\text{in}} = P/V_{\text{in}}. \tag{7}$$

Fig. 4 presents a zoom in view of the input inductor current i_L from Fig. 2, where T_1 and T_2, respectively, denote the charging and discharging durations of the input inductor.

As derived from Fig. 4, the variation of the input inductor current during the charging duration Δi_L is expressed as

$$\Delta i_L = \frac{V_{\text{in}}(D_1+D_2)T_S}{L}. \tag{8}$$

Furthermore, the expression for the input inductor current at t_0 is given by

$$i_L(t_0) = I_L - \frac{\Delta i_L}{2}. \tag{9}$$

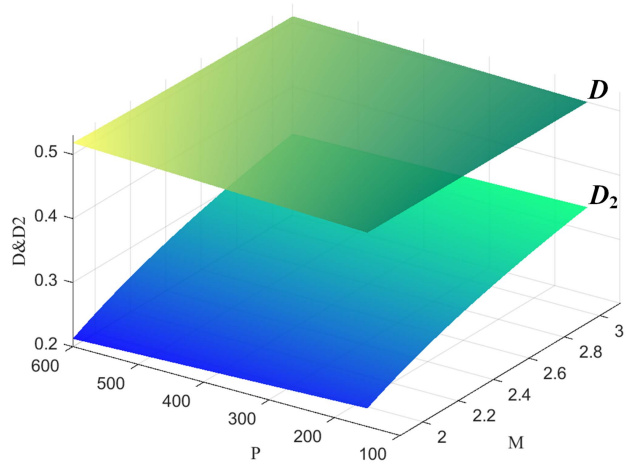

Fig. 5. Three-dimensional graph of D and D_2.

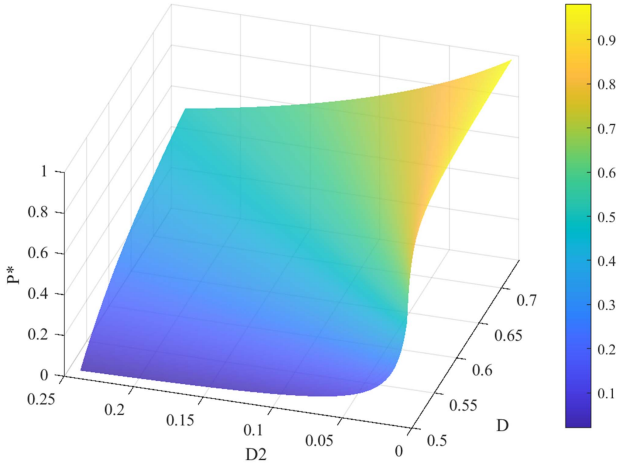

Fig. 6. Three-dimensional graph of the transmission power.

By substituting (7) and (8) in (9), we obtain

$$i_L(t_0) = \frac{P}{V_{\text{in}}} - \frac{V_{\text{in}}(D_1 + D_2)T_S}{2L}. \tag{10}$$

For the proposed CCS strategy, the mathematical relationship between D and D_1 is given by $D = 0.5 + D_1$, i.e., $D_1 = D - 0.5$. Substituting this condition into (6) and (10), and simultaneously solving the equation to eliminate $i_L(t_0)$, we derive as

$$\frac{P}{V_{\text{in}}} - \frac{V_{\text{in}}(D_1 + D_2)T_S}{2L} = \frac{(V_{\text{in}} - MV_{\text{in}})(0.5 - D_1 - D_2)T_S}{2L + 2n^2L_S} + \frac{MV_{\text{in}}D_1T_S}{2n^2L_S} + \frac{V_{\text{in}}D_2T_S}{2L + 2n^2L_S}. \tag{11}$$

Based on Fig. 4, the volt-second balance equation for the input inductor current is established as follows:

$$\frac{V_{\text{in}}(D_2 + D - 0.5)T_S}{L} + \frac{V_{\text{in}}(1 - M)(1 - D_2 - D)T_S}{L + n^2L_S} = 0. \tag{12}$$

By combining (11) and (12), the calculation model for the two key control variables D and D_2 of proposed CCS strategy can be obtained as

$$\begin{cases} D = \frac{1}{2} + \frac{L_S n^2 \left(4L_S^2 P n^4 + 4L_S L P n^2 (M+1) + 4L^2 M P + T_S V_{\text{in}}^2 L(1-M)\right)}{2T_S V_{\text{in}}^2 (L_S n^2 + LM)(L_S n^2 (M-1) + LM)} \\ D_2 = \frac{L(M-1)}{2L_S n^2 + 2LM} - (D - 0.5). \end{cases} \tag{13}$$

Obviously, by substituting different circuit parameters (V_{in}, L, L_S, n, T_S) and operating conditions (M, P) into (13), a set of control variables D and D_2 can be obtained. This set of control variables enables the implementation of the proposed CCS modulation strategy. Fig. 5 illustrates the three-dimensional (3-D) relationship surfaces among voltage gain M, power P, and the control variables D/D_2. As shown in the figure, the duty cycle D is directly proportional to transmission power P but inversely proportional to voltage gain M, while the phase-shift angle D_2 is inversely proportional to P and directly proportional to M.

III. Theoretical Characterization

To comprehensively evaluate the performance of the proposed CCS strategy, this section conducts an in-depth analysis of the converter's key characteristics, including voltage gain, transmission power, current stress, and circulating power, as detailed below.

A. Voltage Gain and Transmission Power

From (12), the voltage gain M can be derived as

$$M = \frac{2(D_2 + D - 0.5)L_S n^2 + L}{(1 - 2(D_2 + D - 0.5))L}. \tag{14}$$

From (14), when circuit parameters are fixed, the sum of control variables D and D_2 remains constant, thereby ensuring the voltage gain M remains invariant.

Substituting (14) into (11), the expression for transmission power P can be derived as

$$P = \frac{T_S V_{\text{in}}^2 \left(\left(2D_2^2 + (2D-2)D_2 - D + 0.5\right)n^2 L_S - (D - 0.5)L\right)}{4n^2 L_S (D_2 + D - 1)(n^2 L_S + L)} - \frac{(D - 0.5)T_S V_{\text{in}}^2 (D_2 + D - 0.5)}{2L(D_2 + D - 1)}. \tag{15}$$

Based on Fig. 2, the duty cycle D of the CFPP converter operating in continuous conduction mode must satisfy

$$D \in \left(0.5, 0.5 + \frac{T_1}{T_S}\right) \tag{16}$$

where

$$\frac{T_1}{T_S} = \frac{L(M-1)}{2L_S n^2 + 2LM}. \tag{17}$$

Since the transmission power P is proportional to the duty cycle D, when $D = 0.5$, the minimum transmission power $P_{\min}$ is defined. When $D = 0.5 + T_1/T_S$, the maximum transmission power $P_{\max}$ is achieved. We have

$$\begin{cases} P_{\min} = \frac{T_S V_{\text{in}}^2 L(M-1)}{4(L_S n^2 + L)(L_S n^2 + LM)} \\ P_{\max} = \frac{T_S V_{\text{in}}^2 LM(M-1)}{4L_S n^2 (L_S n^2 + LM)}. \end{cases} \tag{18}$$

To facilitate analysis, the normalized expression of transmission power in this article is defined as

$$P^* = \frac{P - P_{\min}}{P_{\max} - P_{\min}}. \tag{19}$$

By substituting (15) and (18) into (19), the normalized transmission power expression of CFPP can be derived as

$$P^* = \frac{D - 0.5}{D_2 + D - 0.5}. \tag{20}$$

Fig. 6 presents the 3-D graph of transmission power versus control variables D and D_2. It can be observed that the transferred power P increases with the rise in duty cycle D and the decrease in phase-shift angle D_2.

B. Current Stress

This section will analyzes current stresses, including the maximum leakage inductor current stress $I_{LS\_\max}$ and maximum the reverse current stress $I_{sd\_\max}$ of primary-side switch S_2. Derivation procedures are as follows.

From Fig. 2, the leakage inductor current reaches its peak at t_5. Substituting (5) into (4), the leakage inductor current stress $I_{LS\_\max}$ can be expressed as

$$I_{LS\_\max} = i_{LS}(t_5) = \frac{T_S V_{\text{in}} \left(\left((1-2D_2) L_S M + (2D_1+4D_2-1) L_S\right) n^2 + 2D_1 LM\right)}{4L_S n \left(L_S n^2 + L\right)} \tag{21}$$

i_{ds2} reaches its reverse peak value at t_2. From Fig. 1, based on Kirchhoff's current law and the transformer primary-secondary current conversion relationship, the drain-source current expression of switch S_2 can be derived as

$$i_{ds2}(t) = \frac{i_L(t)}{2} - \frac{i_{LS}(t)}{2n}. \tag{22}$$

According to (4) and (5), $I_{sd\_\max}$ can be expressed as

$$I_{sd\_\max} = i_{ds2}(t_2) = \frac{T_S V_{\text{in}} \left((2D_1 + 2D_2 - 1) M + 1 - 2D_1\right)}{4L_S n^2 + 4L} + \frac{D_1 T_S V_{\text{in}}}{2L}. \tag{23}$$

C. Circulating Power

Circulating power is caused by circulating current. During the power transmission process of the converter, circulating power occurs in the phase where the current is in opposite phase with the primary/secondary side voltage. The primary circulating power P_{c_pri} of the CFPP converter is defined as the power generated in the phase where the drain-source current i_{ds} of the primary switch is in opposite phase with the input voltage V_{in}. The secondary circulating power P_{c_sec} of the CFPP converter is defined as the power generated in the phase where the secondary leakage inductor current i_{LS} is in opposite phase with the midpoint voltage v_{cd} of the secondary full-bridge arm.

Based on Fig. 2, primary-side circulating power can be given by

$$P_{c\_pri} = \frac{2V_{\text{in}}}{T_S} \int_{t_2}^{t_4} i_{ds2}(t)\, dt = -\frac{V_{\text{in}} I_{sd\_\max} T_{24}}{T_S} \tag{24}$$

where

$$T_{24} = \frac{T_S LM \left(2n^2 L_S D_1 + (2D_2 + 2D_1 - 1) LM + L\right)}{2\left(n^2 L_S - LM\right)\left(n^2 L_S + L\right)}. \tag{25}$$

Similarly, secondary-side circulating power can be given by

$$P_{c\_\text{sec}} = \frac{2V_o}{T_S} \int_{t_1}^{t_3} i_{LS}(t)\, dt = \frac{T_S V_{\text{in}}^2 \left(\begin{pmatrix} (2D_2 - 1) M \\ +1 - 2D_1 \end{pmatrix} L_S n^2 - 2D_1 LM\right)^2}{16 L_S n^2 (L_S n^2 + L)^2}. \tag{26}$$

D. Loss Model

The losses of the CFPP converter mainly include key components such as conduction loss, switching loss, and transformer loss. Next, we will establish detailed mathematical models for various losses.

1) Conduction Loss: Conduction losses are mainly caused by the parasitic resistances of the switches and body diodes. Assuming both parameters are R_{ON}, the loss can be expressed as

$$P_{\text{on}} = I_{ds\_\text{rms}}^2 R_{\text{on}} \tag{27}$$

where I_{ds_rms} represents the root-mean-square (rms) value of the power switch conduction current. For S_1-S_2, this value can be calculated as

$$I_{ds1\_\text{rms}} = \sqrt{\frac{\left(i_{ds1}^2(t_3) + i_{ds1}^2(t_6)\right) D_1 + \left(i_{ds1}^2(t_3) + i_{ds1}^2(t_5) + i_{ds1}(t_3)\, i_{ds1}(t_5)\right) D_2 + \left(i_{ds1}^2(t_5) + i_{ds1}^2(t_6) + i_{ds1}(t_5)\, i_{ds1}(t_6)\right)(0.5 - T_1/T_S)}{3}}. \tag{28}$$

For S_3–S_6, this value can be calculated as

$$I_{ds3\_\text{rms}} = \frac{I_{LS\_RMS}}{\sqrt{2}} = \sqrt{\frac{\left(i_{LS}^2(t_0)\right) + \left(i_{LS}^2(t_3) + i_{LS}(t_0)\, i_{LS}(t_3)\right) D_1 + \left(i_{LS}^2(t_3) + i_{LS}^2(t_5) + i_{LS}(t_3)\, i_{LS} + i_{LS}(t_5)\right) D_2 + \begin{pmatrix} i_{LS}^2(t_5) + i_{LS}^2(t_6) \\ + i_{LS}(t_5)\, i_{LS}(t_6) \end{pmatrix}(0.5 - T_1/T_S)}{3}}. \tag{29}$$

2) Switching Loss: Switching loss mainly includes turn-ON loss and turn-OFF loss. Since the proposed CCS strategy can achieve ZVS-ON for all switches and ZCS-OFF for primary-side switches, the turn-ON loss and primary-side turn-OFF loss can be neglected. The secondary-side turn-OFF loss can be calculated as

$$P_{\text{off}} = \frac{I_{\text{off}}^2 t_{\text{off}}^2 f_s}{24 C_{oss}} \tag{30}$$

TABLE I
MATHEMATICAL MODELS OF CURRENT STRESS AND CIRCULATING POWER FOR EXISTING MODULATION STRATEGIES

	SP strategy	DP strategy	PPS strategy
$I_{LS\_\max}$	$\frac{T_S V_{in}(M-1)}{4nL_S}$	$\frac{D_2 T_S V_{in} M}{nL_S}$	$-\frac{T_S V_{in}\left((2D_2-1)M+1\right)}{4nL_S}$
$I_{sd\_\max}$	$\frac{T_S V_{in}\left((D-0.5)n^2L_S+(D-1)LM+0.5L\right)}{2n^2L_S L}$	$\frac{P}{2V_{in}}+\frac{V_{in}(D-0.5)T_S}{2L}-\frac{D_2 T_S V_{in} M}{2n^2L_S}-\frac{T_S V_{in}(M-1)}{8n^2L_S+8LM}$	$\frac{T_S V_{in}\left(2D_1n^2L_S+(2D_2+2D_1-1)LM+L\right)}{4n^2L_S L}$
P_{c_pri}	$\frac{-T_S V_{in}^2 M\left((D-0.5)n^2L_S+(D-1)LM+0.5L\right)}{n^2L_S\left(n^2L_S-LM\right)\left(n^2L_S+LM\right)}$	$\begin{pmatrix}(D-0.5)-\frac{L(M-1)}{2n^2L_S+2LM}\\ -\frac{2I_{sd\_\max}L^2M}{V_{in}T_S\left(n^2L_S-LM\right)}-\frac{2I_{sd\_\max}L}{V_{in}T_S}\end{pmatrix}V_{in}I_{sd\_\max}$	$\left(\frac{I_{sd\_\max}T_{02'}-i_{ds2}(t_4')T_{04}}{T_S}+D_1 i_{ds2}(t_4')-(D_2+D_1)I_{sd\_\max}\right)V_{in}$ where $i_{ds2}(t_4')=-\frac{I_{LS\_\max}}{n}+\frac{T_S V_{in}\left((D_2+D_1)n^2L_S+D_1LM\right)}{2n^2L_S L}$, $T_{01z}=\frac{-T_S L\left((2D_2+4D_1-1)M+1\right)}{2n^2L_S-2LM}$, $T_{04}=\frac{T_S L(M-1)}{2n^2L_S+2LM}$
P_{c_sec}	$\frac{T_S V_{in}^2(M-1)^2}{16L_S n^2}$	$\frac{D_2^2 T_S V_{in}^2 M^2}{L_S n^2}$	$\frac{T_S V_{in}^2\left((2D_2-1)M+1\right)^2}{16L_S n^2}$

where t_{off} denotes the turn-OFF time of the power switch, C_{oss} represents the output junction capacitance, and I_{OFF} is the turn-OFF current of the secondary switch. As shown in Fig. 2, the turn-OFF current I_{OFF} under the proposed CCS strategy is $I_{LS\_\max}$.

3) Transformer Losses: Transformer losses mainly include winding losses and core losses. The winding losses can be expressed as

$$P_{\text{wind}} = I_{LS\_\text{rms}}^2\left(\frac{R_{pri}}{n^2}+R_{sec}\right) \tag{31}$$

where R_{pri} and R_{sec} refer to the equivalent resistance of the primary and secondary windings of the transformer.

The core losses can be expressed as

$$P_{\text{core}} = P_V V_e \tag{32}$$

where V_e is the core volume, P_V (W/m^3) is the core loss per unit volume, which can be expressed as

$$P_V = aB^x \tag{33}$$

where a and x are coefficients of the core material, and B is the flux density. For the 3C95 core material, the parameters are $a = 1.627 \times 107$, $x = 2.73$, and the magnitude of B is

$$B = \frac{U}{K_f f_s A_e N} \tag{34}$$

where U is the rms voltage across the primary winding, K_f is the waveform coefficient of the primary winding voltage, f_s is the switching frequency, A_e is the effective cross-sectional area of the core, and N is the number of primary turns.

IV. COMPREHENSIVE COMPARATIVE ANALYSIS OF DIFFERENT STRATEGIES

A. Comparison of Current Stress and Circulating Power

To facilitate quantitative comparison between the proposed CCS strategy and existing natural commutation strategies, this section derives the current stress and circulating power

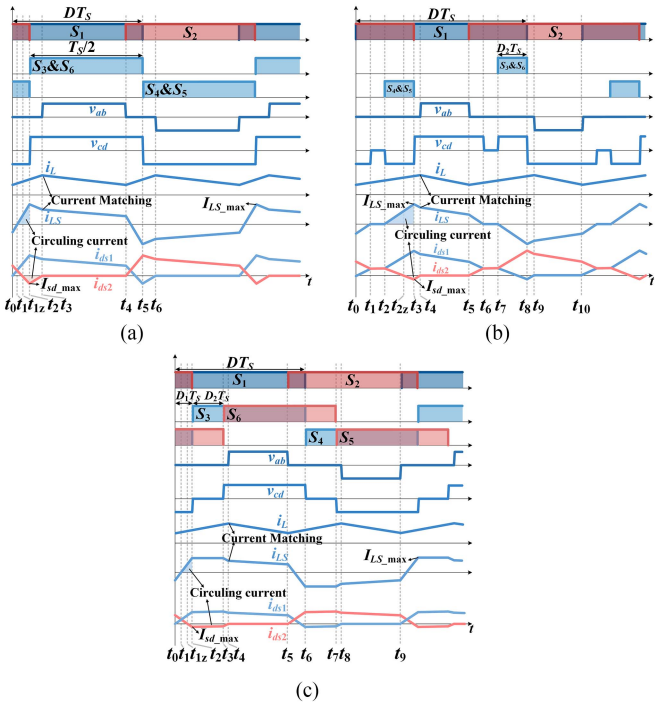

Fig. 7. Operational waveforms of existing strategies. (a) SP strategy. (b) DP strategy. (c) PPS strategy.

expressions of existing SP, DP, and PPS strategies. Fig. 7(a), (b), and (c) presents the modulation waveforms of these three strategies. Following similar derivation procedures as in Sections II and III, we derive the primary-side switch's reverse current stress $I_{sd\_\max}$, leakage inductor current stress $I_{LS\_\max}$, primary-side circulating power P_{c_pri}, and secondary-side circulating power P_{c_sec} for all three strategies. The derivation results are summarized in Table I.

Furthermore, Fig. 8 provides zoomed-in views of current stress profiles and current matching points under identical scales for SP, DP, PPS, and proposed CCS strategies, which obtained

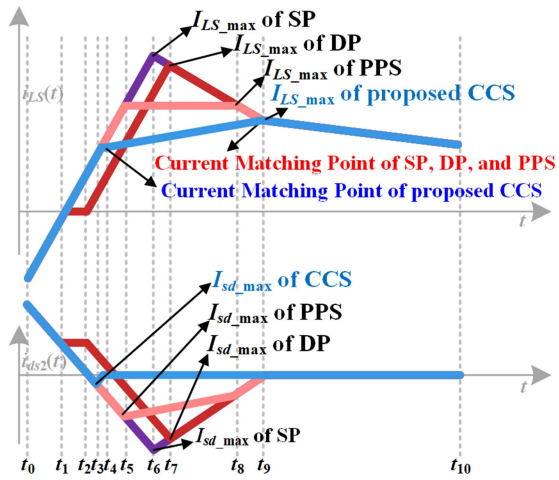

Fig. 8. Comparison of current stress (I_{sd_max}, $I_{LS\_,max}$) and matching time.

from Figs. 8 and 2. By observing Fig. 8, we can draw the following conclusions.

1) Compared to SP, DP, and PPS strategies, the proposed CCS strategy achieves minimum reverse current stress I_{sd_max} and peak leakage inductor current stress I_{LS_max}.
2) SP, DP, and PPS strategies achieve current matching at t_9, while the proposed CCS strategy significantly reduces circulating currents and current stress by adjusting the current matching point from t_9 to t_4.

To intuitively compare the effects, the current stresses and circulating powers of the four strategies are subjected to normalized processing (Divide by the maximum value of SP). Fig. 9 provides the comparison results of current stresses ($I_{sd\_max}*$, $I_{LS\_max}*$) or circulating power ($P_{c\_pri}*$, $P_{c\_sec}*$) of SP, DP, PPS, and the proposed CCS with respect to voltage gain M and transmission power P. The results demonstrate that under various operating conditions, the proposed CCS strategy achieves significant reductions in primary-side switch's reverse current stress I_{sd_max}, leakage inductance current stress I_{LS_max}, primary-side circulating power P_{c_pri}, and secondary-side circulating power P_{c_sec}.

B. Losses Comparison

Following the same procedures as in Section III-D, the loss models for the existing SP, DP, and PPS strategies can be derived, and a comparison is made among these three strategies and the proposed CCS strategy. Fig. 10 presents the 3-D relationship curves of conduction loss, switching loss, transformer loss, and total loss versus voltage gain M and transmitted power P for the four strategies. Since the circulating current and current stress of the proposed CCS strategy are significantly reduced compared with other strategies, the losses of each converter component and the total loss are minimized among the four strategies.

C. Comparison of Cost and Compactness

This article primarily focuses on the modulation strategies of CFPP converters, and the proposed strategy demonstrates advantages in cost, compactness, and weight density. The following density between the proposed CCS and existing SP, DP, and PPS strategies.

Under the same voltage rating and load conditions, the proposed CCS shows significant advantages in current stress compared with other modulation strategies. Low current stress can effectively reduce the cost of MOSFET devices. Additionally, since the proposed CCS strategy achieves the highest efficiency, which implies lower losses, the size of the heat sink can be minimized. As the cost of heat sinks accounts for a smaller proportion of the converter design cost compared with power devices, only the size comparison is provided here. Overall, the cost advantage of the proposed CCS strategy is mainly reflected in the power device section. Table II presents the component selection and cost comparison of power switches for CFPP converters under different modulation strategies, indicating that the proposed CCS has the lowest cost.

Furthermore, a detailed comparison of compactness and weight density is conducted between the proposed CCS strategy and existing SP, DP, and PPS strategies. Since the proposed CCS strategy exhibits the minimum leakage inductance current stress, lower current stress is beneficial for the design of transformer windings and cores. The highest efficiency of the proposed CCS strategy→higher efficiency implies lower losses→smaller heat sink volume→lighter heat sink weight. Overall, the advantages of the proposed CCS strategy in compactness and weight density are mainly reflected in two aspects: 1) transformers and 2) heat sinks. Table II also provides the comparison results of heat sink area, core volume, and weight density of CFPP converters under different modulation strategies. It can be seen that the heat sink area (calculated based on the thermal resistance model) and core volume of the proposed CCS are the smallest, and the converter has the highest weight density.

V. Simulation and Experimental Validation

A. Simulation Validation

To validate the correctness of the proposed CCS strategy, simulation verification is performed on four modulation strategies: SP, DP, PPS, and proposed CCS. The simulation parameters are listed in Table III.

Under operating conditions of input voltage $V_{\text{in}} = 48$ V, output voltage $V_o = 180$ V, and load power $P = 500$ W, Fig. 11(a)–(d) presents simulated operational waveforms for SP, DP, PPS, and proposed CCS strategies under identical parameter settings. Test results reveal that as follows.

1) Primary-side switch's reverse current stresses I_{sd_max} for SP, DP, PPS, and proposed CCS strategies are measured at −31.37 A, −13.09 A, −4.82 A, and −0.08 A, respectively.
2) Leakage inductor current stresses I_{LS_max} are recorded as 36.26 A, 19.12 A, 9.21 A, and 6.01 A, respectively.

These simulation experimental results demonstrate significant reductions in both current stress and circulating currents (as circulating currents are proportional to current stress) with the proposed CCS strategy, thereby validating its effectiveness.

B. Experimental Validation

A CFPP experimental prototype is developed with an input

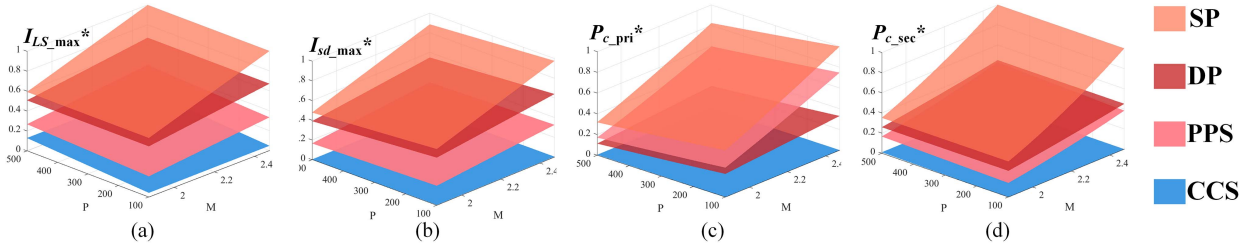

Fig. 9. Quantitative comparison of existing method and proposed CCS strategy. (a) Leakage inductance current stress $I_{LS\_max}*$. (b) Reverse current stress $I_{sd\_max}*$. (c) Primary-side circulating power $P_{c\_pri}*$. (d) Secondary-side circulating power $P_{c\_sec}*$.

TABLE II
COMPARISON OF COST, COMPACTNESS, AND WEIGHT DENSITY OF CFPP CONVERTER UNDER DIFFERENT MODULATION STRATEGIES

	SP	DP	PPS	Proposed CCS
No. of switches	Primary: 2; Secondary: 4			
Rms currents of switches	Primary: 2 × 12.805 A Secondary: 4 × 8.263 A	Primary: 2 × 10.89 A Secondary: 4 × 6.759 A	Primary: 2 × 9.495 A Secondary: 4 × 5.601 A	Primary: 2 × 7.333 A Secondary: 4 × 3.632 A
Peak currents of switches	Primary: 33.382 A Secondary: 28 A	Primary: 30.056 A Secondary:24.484 A	Primary: 17.936 A Secondary: 12.027 A	Primary: 12.139 A Secondary: 6.087 A
Voltage stresses of switches	Primary: 180 V Secondary: 180 V	Primary: 180 V Secondary: 180 V	Primary: 180 V Secondary: 180 V	Primary: 180 V Secondary: 180 V
MOSFETS	41.19 $	34.29 $	28.79 $	17.79 $
	2 × IPB407N30N (300 V, 44 A) 4 × IRFP4137PBF (300 V, 38 A)	2 × IRFP4137PBF (300 V, 38 A) 4 × IRFI4229PBF (300 V, 32 A)	2 × IRFI4229PBF (300 V, 32 A) 4 × IPP60R070CFD7 (600 V, 20 A)	2 × IPP60R070CFD7 (600 V, 20 A) 4 × IRFP360PBF (400 V, 14 A)
Conduction loss	2 × 6.559 W 4 × 3.824 W	2 × 5.641 W 4 × 2.635 W	2 × 3.926 W 4 × 2.396 W	2 × 1.625 W 4 × 1.274 W
Heat sink area of MOSFET (Natural cooling)	2 × 20 cm^2 4 × 11 cm^2 Aluminum heat sink	2 × 20 cm^2 4 × 5 cm^2 Aluminum heat sink	2 × 10 cm^2 4 × 7 cm^2 Aluminum heat sink	2 × 5 cm^2 4 × 4 cm^2 Aluminum heat sink
Rms currents of leakage inductor	11.686 A	9.558A	7.921 A	5.137 A
Peak currents of leakage inductor	28 A	24.484A	12.027 A	6.087 A
Transformer	Core: PQ40/40-3C95 (V_e=20.5 cm^3) winding length: 3 × 0.796 m (primary) 1.591 m (secondary)	Core: PQ35/35-3C95 (V_e=16.3 cm^3) winding length: 3 × 0.672 m (primary) 1.343 m (secondary)	Core: PQ32/30-3C95 (V_e=12.5 cm^3) winding length: 3 × 0.509 m (primary) 1.017 m (secondary)	Core: PQ32/30-3C95 (V_e=12.5 cm^3) winding length: 3 × 0.416 m (primary) 0.832 m (secondary)
Transformer weight	Core: 92.25 g Winding: 91.35 g	Core: 73.35 g Winding:77.12 g	Core: 56.25 g Winding: 58.41 g	Core: 56.25 g Winding: 47.75 g
Other gate drive/ capacitor/ PCB/ inductor	390–399.4 g			
Total Weight	591 g	558 g	512g	502 g
Weight Density	846.02 W/kg	896.06 W/kg	976.56W/kg	996.02 W/kg

TABLE III
PARAMETERS OF CFPP CONVERTER

Parameter	Value
Input voltage V_{in}	48 V
Output voltage V_o	180 – 300 V
Rated power P	500 W
Switching frequency f_s	50 kHz
Input inductor L	60 μH
capacitor C_{in}, C_o	480 μF
HF transformer	$N_1 : N_2 : N_3 = 5:5:10$; $L_S = 6$ μH

a rated power of 500 W. The test environment and prototype configuration are shown in Fig. 12, while the detailed circuit parameters align with those listed in Table III.

Experimental validation is conducted under the following four operating conditions.

Case 1: Input voltage $V_{\text{in}} = 48$ V, output voltage $V_o = 180$ V.
Case 2: Input voltage $V_{\text{in}} = 48$ V, output voltage $V_o = 220$ V.
Case 3: Input voltage $V_{\text{in}} = 48$ V, output voltage $V_o = 260$ V.
Case 4: Input voltage $V_{\text{in}} = 48$ V, output voltage $V_o = 300$ V.

1) Comparison of Current Stress With State-of-the-Art Strategy: To verify the superiority of the proposed CCS strategy, the current stress of the proposed CCS and the state-of-the-art PPS strategy are compared under the Case 1 operating condition.

Fig. 13 shows the key test waveforms of the PPS strategy under half-load and full-load conditions. Fig. 14 shows the key test waveforms of the proposed CCS strategy under half-load and full-load conditions. It can be observed that the primary-side

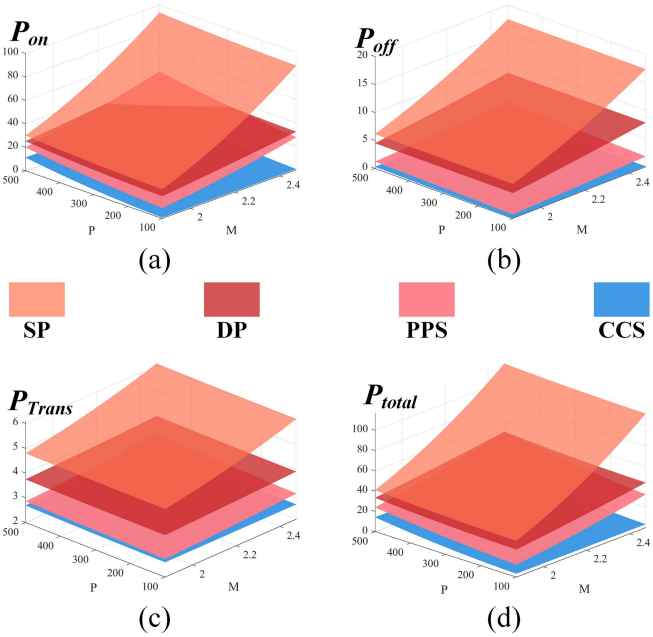

Fig. 10. Losses comparison. (a) Conduction loss P_{ON}. (b) Switching loss P_{OFF}. (c) Transformer loss P_{trans}. (d) Total loss P_{total}.

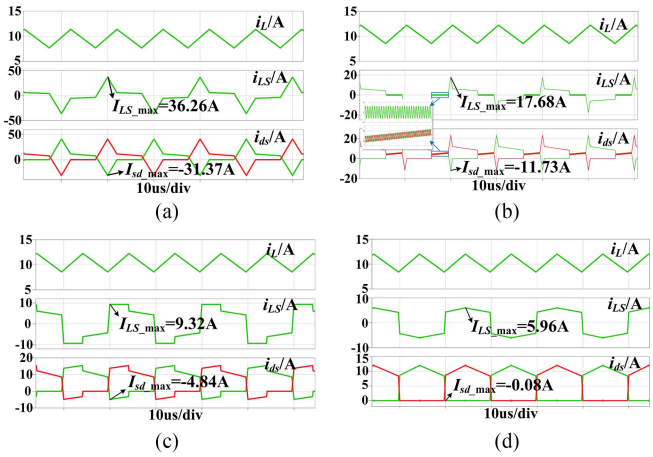

Fig. 11. Simulated waveform comparison results. (a) SP. (b) DP. (c) PPS. (d) Proposed CCS.

switch's reverse current stress $I_{sd\_\max}$ of the PPS strategy is −3.68 A and −4.45 A under half-load and full-load conditions, respectively, and the leakage inductance current stress $I_{LS\_\max}$ is 5.56 A and 8.72 A, respectively. The primary-side switch's reverse current stress $I_{sd\_\max}$ of the proposed CCS strategy is −0.73 A and −0.57 A under half-load and full-load conditions, respectively, and the leakage inductance current stress $I_{LS\_\max}$ is 3.52 A and 5.56 A, respectively. The test results indicate that the current stress of the proposed CCS strategy is significantly lower than that of the PPS strategy. Specifically, compared with the PPS strategy, the proposed CCS strategy reduces the primary-side switch's reverse current stress $I_{sd\_\max}$ and leakage inductance current stress $I_{LS\_\max}$ by 80.16% and 40.94% under

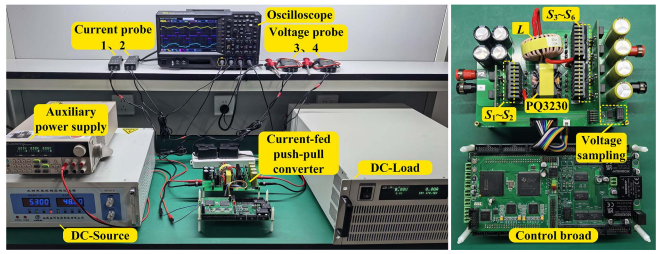

Fig. 12. Experimental prototype and testing environment.

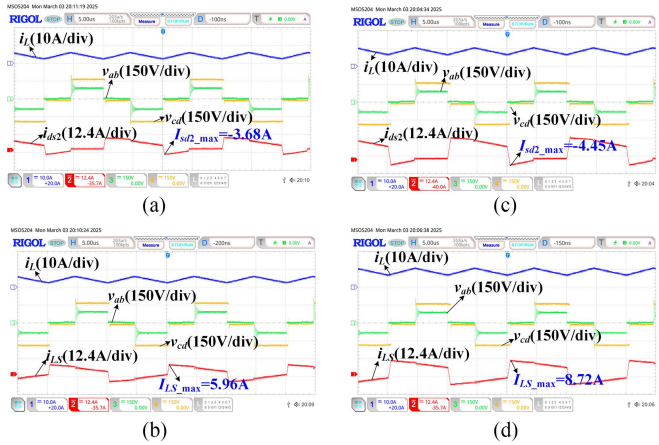

Fig. 13. Experimental waveforms of the PPS strategy under Case 1. (a) and (b) Half-load (250 W). (c) and (d) Full-load (500 W).

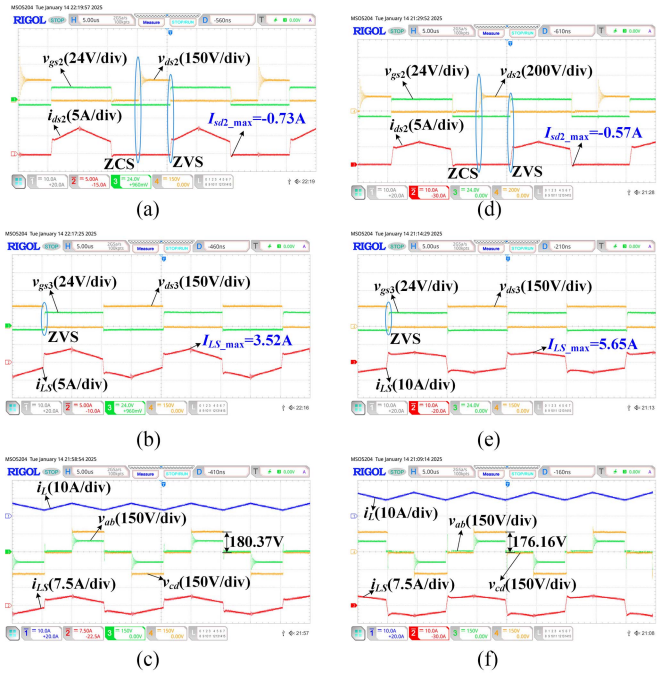

Fig. 14. Experimental waveforms of the proposed CCS strategy under Case 1. (a)–(c) Half-load. (d)–(f) Full-load.

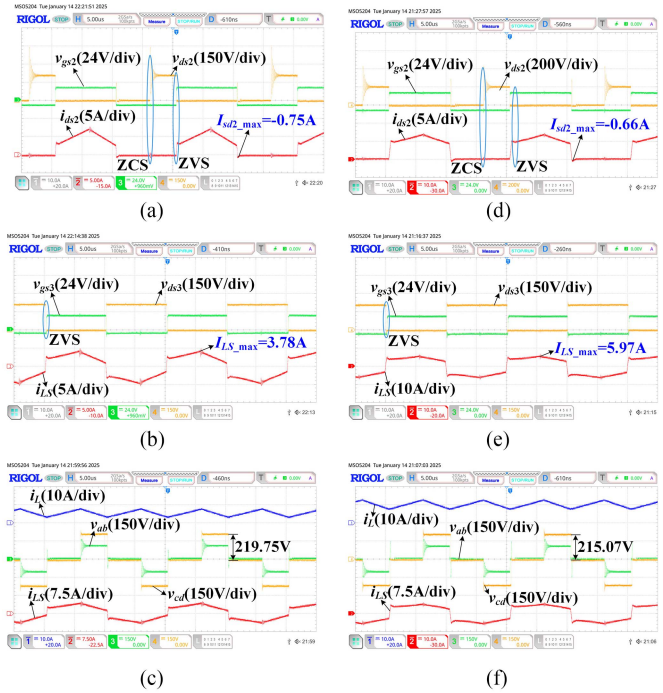

Fig. 15. Experimental waveforms of the proposed CCS strategy under Case 2. (a)–(c) Half-load. (d)–(f) Full-load.

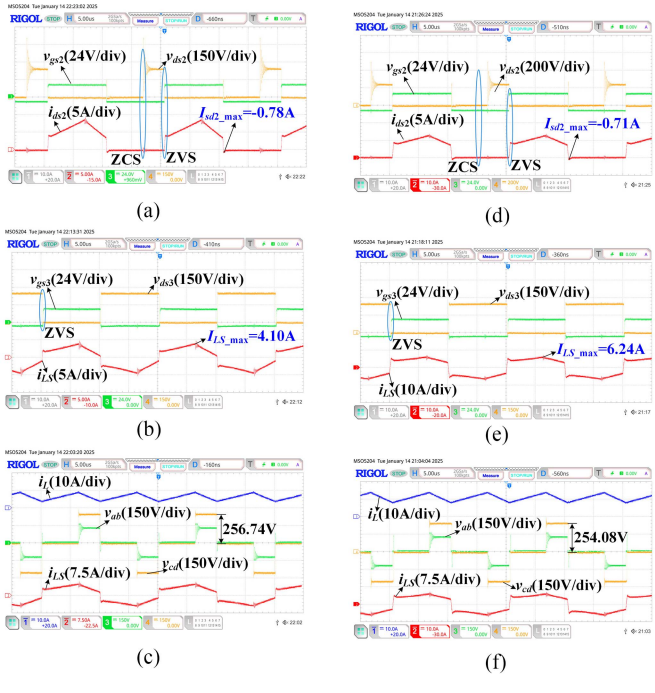

Fig. 16. Experimental waveforms of the proposed CCS strategy under Case 3. (a)–(c) Half-load. (d)–(f) Full-load.

TABLE IV
ACCURATE DATA FOR CURRENT STRESS

Load		Case1	Case2	Case3	Case4
Half load	I_{sd_max}	–0.73 A	–0.75 A	–0.78 A	–0.80 A
	I_{LS_max}	3.52 A	3.78 A	4.10 A	4.33 A
Full load	I_{sd_max}	–0.57 A	–0.66 A	–0.71 A	–0.76 A
	I_{LS_max}	5.65 A	5.97 A	6.34 A	6.47 A

half-load conditions, and by 87.91% and 35.21% under full-load conditions, respectively.

Additionally, based on experimental measurement data and the circulating current power model, the proposed CCS strategy reduces the total circulating power ($P_{c\_\mathrm{pri}} + P_{c\_\mathrm{sec}}$) by 78.41% and 67.26% at half load and full load, respectively, compared with the state-of-the-art PPS strategy.

2) CCS Performance Under Different Operation Condition: To verify the performance of the proposed CCS strategy under different operating conditions, Figs. 15–17 present the key test waveforms for Case 2 to Case 4, respectively. Combine Fig. 13, Table IV records the experimental data of $I_{sd\_\max}$ and $I_{LS\_\max}$ for the proposed CCS strategy under Case 1–Case 4.

The test results demonstrate that the proposed CCS strategy achieves $I_{sd\_\max}$ values below 1 A across all cases, while $I_{LS\_\max}$ closely matches theoretical predictions. This experimentally validates the effectiveness of the proposed CCS strategy. Additionally, under all tested operating conditions, all power switches achieve ZVS, and the primary-side switches further realize ZCS.

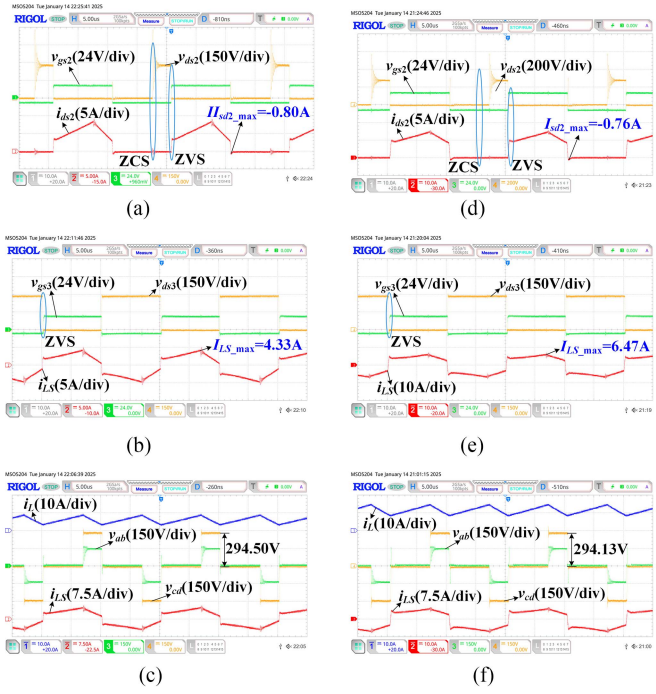

Fig. 17. Experimental waveforms of the proposed CCS strategy under Case 4. (a)–(c) Half-load. (d)–(f) Full-load.

C. Efficiency Comparison

Taking the operating condition with input voltage $V_{\mathrm{in}} = 48$ V and output voltage $V_o = 180$ V($M = 1.875$) as an example, Fig. 18(a) presents the efficiency comparison curves of the SP, DP, PPS, and proposed CCS strategies. It can be observed that

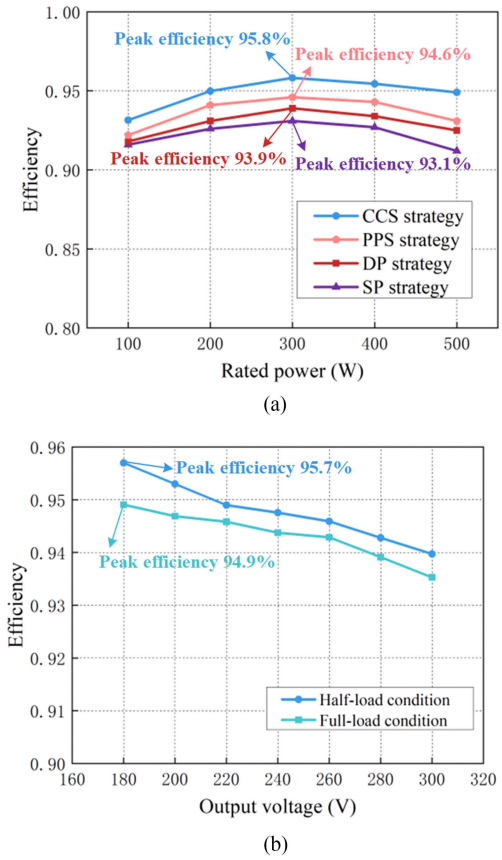

Fig. 18. Efficiency characterization of proposed CCS strategy. (a) Efficiency curves of different strategies under the condition at $M = 1.875$. (b) Efficiency curve of the proposed CCS strategy with varying output voltage under fixed input voltage and load conditions.

the proposed CCS strategy achieves a peak efficiency of 95.8%, with overall efficiency consistently higher than SP, DP, and PPS strategies. This is attributed to the significant reduction in current stress and circulating power in the proposed CCS strategy.

Fig. 18(b) further shows the 2-D efficiency curves of the proposed CCS strategy with varying output voltage under fixed input voltage and load conditions. The results indicate that the efficiency gradually increases as the output voltage decreases. Specifically, the peak efficiency reaches 94.3% at full load and 95.7% at half load.

VI. Conclusion

To address the issue of high current stress and circulating power in existing natural commutation strategies, this article proposes a CCS modulation strategy for CFPP converters. Through theoretical analysis and experimental validation, the following conclusions are drawn.

1) A detailed analysis of the operational modes of the CFPP converter is conducted, and a computational model for control variables under the proposed CCS strategy is derived. This model adaptively solves the duty cycle and phase-shift angle based on different operating conditions and circuit parameters, enabling the converter to operate in low current stress and circulating power modes.
2) Mathematical models for current stress, circulating power, and loss models are systematically derived for the existing SP, DP, PPS, and proposed CCS strategies, followed by comprehensive quantitative comparisons. Theoretical results confirm that the proposed CCS strategy achieves the lowest current stress, circulating power, and losses under all tested operating conditions compared with existing methods.
3) A 500-W CFPP prototype is developed. Experimental results demonstrate that the proposed CCS strategy effectively reduces current stress and circulating power across all test cases. All switches achieve ZVS, and primary-side switches additionally realize ZCS. Compared with state-of-the-art strategies, the proposed CCS strategy achieves at least a 35.21% reduction in current stress and at least a 67.26% reduction in circulating power, along with a 1.2% improvement in peak efficiency.
4) Owing to the low current stress and circulating current characteristics of the proposed CCS strategy, under the same voltage and load conditions, adopting the proposed CCS strategy can effectively reduce design costs and improve compactness or weight density compared with existing SP, DP, and PPS strategies.

References

[1] Y. Shi, R. Li, Y. Xue, and H. Li, "High-frequency-link-based grid-tied PV system with small DC-link capacitor and low-frequency ripple-free maximum power point tracking," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 328–339, Jan. 2016.

[2] A. K. Rathore, "Current-fed DC/DC converters for high voltage gain and low voltage high current applications: An overview of topologies and modulation techniques," in *Proc. IEEE Int. Conf. Power Electron., Drives Energy Syst.*, 2016, pp. 1–6.

[3] A. K. Rathore and U. Prasanna, "Comparison of soft-switching voltage-fed and current-fed bi-directional isolated DC/DC converters for fuel cell vehicles," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2012, pp. 252–257.

[4] X. Pan, H. Li, Y. Liu, T. Zhao, C. Ju, and A. K. Rathore, "An overview and comprehensive comparative evaluation of current-fed-isolated-bidirectional DC/DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2737–2763, Mar. 2020.

[5] H. Li, F. Zheng Peng, and J. S. Lawler, "A natural ZVS medium-power bidirectional DC-DC converter with minimum number of devices," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 525–535, Mar./Apr. 2003.

[6] A. K. Rathore and U. R. P., "Analysis, design, and experimental results of novel snubberless bidirectional naturally clamped ZCS/ZVS current-fed half-bridge DC/DC converter for fuel cell vehicles," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4482–4491, Oct. 2013.

[7] U. R. Prasanna, A. K. Rathore, and S. K. Mazumder, "Novel zero-current-switching current-fed half-bridge isolated DC/DC converter for fuel-cell-based applications," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1658–1668, Jul./Aug. 2013.

[8] Y. Li, Y. Xing, Y. Lu, H. Wu, and P. Xu, "Performance analysis of a current-fed bidirectional LLC resonant converter," in *Proc. 42nd Annu. Conf. IEEE Ind. Electron. Soc.*, 2016, pp. 2486–2491.

[9] P. Xuewei and A. K. Rathore, "Novel bidirectional snubberless naturally commutated soft-switching current-fed full-bridge isolated DC/DC converter for fuel cell vehicles," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2307–2315, May 2014.

[10] Y. Zhang, Z. Wang, Y. W. Li, N. Hou, and M. Cheng, "Decoupled dual-PWM control for naturally commutated current-fed dual-active-bridge DC/DC converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 4246–4259, Dec. 2020.

[11] S. Bal, A. K. Rathore, and D. Srinivasan, "Comprehensive study and analysis of naturally commutated current-fed dual active bridge PWM DC/DC converter," in *Proc. 42nd Annu. Conf. IEEE Ind. Electron. Soc.*, 2016, pp. 4382–4388.

[12] G. Xu, Y. Lin, L. Yuan, W. Xiong, and Y. Sun, "Dead-time optimization and magnetizing current design for a current-fed dual active bridge DC–DC converter to secure full load range ZVS in wide voltage range," *IEEE Trans. Transp. Electrific.*, vol. 9, no. 2, pp. 2164–2176, Jun. 2023.
[13] P. Xuewei and A. K. Rathore, "Naturally clamped zero-current commutated soft-switching current-fed push–pull DC/DC converter: Analysis, design, and experimental results," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1318–1327, Mar. 2015.
[14] J. Ren et al., "A method for reducing voltage spikes and circulating current of current-fed push-pull DC/DC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2023, pp. 2542–2545.
[15] S. S. Nag and S. Mishra, "Current-fed switched inverter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 9, pp. 4680–4690, Sep. 2014.
[16] H. Shi, H. Wen, Y. Hu, and L. Jiang, "Reactive power minimization in bidirectional DC–DC converters using a unified-phasor-based particle swarm optimization," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10990–11006, Dec. 2018.
[17] K. Harada and H. Sakamoto, "Switched snubber for high frequency switching," in *Proc. 21st Annu. IEEE Conf. Power Electron. Specialists*, 1990, pp. 181–188.
[18] A. Algaddafi and K. Elnaddab, "Modelling and designing the RC snubber circuit for a buck converter and testing its effectiveness," in *Proc. Int. Renewable Sustain. Energy Conf.*, 2016, pp. 554–559.
[19] L. Zhu, "A novel soft-commutating isolated boost full-bridge ZVS-PWM DC–DC converter for bidirectional high power applications," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 422–429, Mar. 2006.
[20] E.-S. Kim, K.-Y. Joe, H.-Y. Choi, Y.-H. Kim, and Y.-H. Cho, "An improved soft switching bi-directional PSPWM FB DC/DC converter," in *Proc. 24th Annu. Conf. IEEE Ind. Electron. Soc.*, 1998, pp. 740–743.
[21] M. Schulz and S. Ditze, "Analysis and experimental verification of an isolated half-bridge bidirectional DC−DC converter," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5089–5106, May 2022.
[22] Q. Wu, S. Xue, H. Xi, J. Ren, Z. Sun, and Q. Wang, "Active-clamp soft-switching push-pull full-bridge bidirectional DC–DC converter over a wide load range," *IEEE Trans. Power Electron.*, vol. 39, no. 11, pp. 14862–14876, Nov. 2024.
[23] H. Xiao and S. Xie, "A ZVS bidirectional DC–DC converter with phase-shift plus PWM control scheme," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 813–823, Mar. 2008.
[24] D. Sha, X. Wang, and D. Chen, "High-efficiency current-fed dual active bridge DC–DC converter with ZVS achievement throughout full range of load using optimized switching patterns," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1347–1357, Feb. 2018.
[25] S. Bal, A. K. Rathore, and D. Srinivasan, "Modular snubberless bidirectional soft-switching current-fed dual 6-pack (CFD6P) DC/DC converter," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 519–523, Feb. 2015.
[26] Y. Zhang, L. Ding, N. Hou, and Y. Li, "A dual-current-fed dual-active-bridge DC/DC converter with high-frequency current-ripple-friendly ports," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 15084–15098, Dec. 2022.

Zhifeng Sun received the Ph.D. degree in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2024.

Since March 2024, he is currently a Lecturer with the College of Electrical Engineering, Hunan University of Technology, Zhuzhou, China. He was awarded the 2020 high impact paper by the *Journal of Proceedings of the CSEE* (Chinese). His research interests include dc–dc and Multiphase dc–dc converter.

Yankun Chen received the B.S. degree in electrical engineering and automation from the Huizhou University, Huizhou, China, in 2024. He is currently working toward the M.S. degree in electrical engineering with the Hunan University of Technology, Zhuzhou, China.

His current research interests include the natural commutation technology of current-fed isolated dc–dc converters and soft-switching dc–dc converters.

Jinhui Zeng received the B.S. and Ph.D. degrees in electrical engineering from the College of Electrical and Information Engineering, Hunan University, Changsha, China, in 2009 and 2013, respectively.

Since 2013, he has been a Professor with Hunan University of Technology. His research interests include power electronic transformation, power quality control, and control methods of renewable energy grid connection.

Qunfang Wu (Member, IEEE) received the Ph.D. degree in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2018.

From 2018 to 2020, he has been a Postdoctoral Research Fellow with the Department of Electrical and Computer Engineering, University of Michigan, Dearborn, MI, USA. Since September 2020, he has been an Associate Professor with the College of Automation Engineering, Nanjing University of Aeronautics and Astronautics. He has authored or coauthored more than 80 technical papers in international journals and conference proceedings. He is the holder of more than 40 Chinese patents. His research interests include dc–dc and dc–ac power conversions, power electronics reliability, and wideband-gap semiconductor power device applications.

Jiangli Ren received the B.S. degree in electrical engineering and automation from Nanjing Agricultural University, Nanjing, China, in 2019, and the M.S. degree in electrical engineering from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2024.

His current research interests include soft switching dc–dc converters and current push–pull converters.

Wei Su received the B.S. degree from Shandong Agriculture University, Taian, China, in 2005, and the M.S. and Ph.D. degrees from Jinan University, Guang Zhou, China, in 2009 and 2013, respectively. He was a Professor-level Senior Engineer with the Laboratory of Science and Technology on Reliability Physics and Application of Electronic Component, Guangzhou, China. His research interests include mechanical reliability design, numerical simulation, experimental testing, and failure analysis of electronic devices and components.

Pengfei Yu received the B.S. degree in automation from Huazhong University of Science and Technology, Wuhan, China, in 2013, the M.S. degree in detection technology and automation devices from Jiangsu Automation Research Institute, Lianyungang, China, in 2016, and the Ph.D. degree in energy and environment from South China University of Technology, Guangzhou, China, in 2025.

Since 2016, he has been with Laboratory of Science and Technology on Reliability Physics and Application of Electronic Component, China Electronic Product Reliability and Environmental Testing Research Institute, Guangzhou, China. His research interests include power conversion system and component reliability, prognostic and health management, and digital twin.