Letters

An Enhanced Characterization Method of SiC MOSFETs in the High-Voltage Saturation Region With Reduced Self-Heating

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***Abstract*—Accurate device modeling, short-circuit prediction, and protection for silicon carbide (SiC) MOSFETs require accurate measurement of their saturation characteristics under high drain-source voltages. However, conventional curve tracers are limited by power constraints, parasitic elements, and especially the device's intrinsic turn-ON time, which together constrain di/dt. This makes it difficult to characterize behavior in high-voltage, high-current regions, since the long duration required to reach steady state can cause significant self-heating, reducing accuracy or even damaging the device. This letter proposes a test topology using multiple parallel devices as auxiliary switches to control the measurement and accelerate the turn-ON transient while keeping the device under test normally ON. To accurately measure the internal gate voltage during an ultra-narrow pulse, we propose a high-impedance gate drive circuit, eliminating the influence of the voltage drop across the device's intrinsic gate resistance. The measured results capture the full range of transfer and output characteristics of the SiC MOSFET and show good agreement with curve tracer data in the low-voltage region. At $V_{ds} = 20$ V and $V_{gs} = 20$ V under room temperature, the proposed method limits the temperature rise to within 4 °C, compared to nearly 100 °C with a power device analyzer, thereby enabling more accurate device characterization and modeling.**

***Index Terms*—Characterization, MOSFETs, self-heating, silicon carbide (SiC).**

I. Introduction

ACCURATE characterization of silicon carbide (SiC) devices, particularly in the saturation region, is essential for ensuring reliability, modeling short-circuit (SC) behavior, designing protection, and defining the safe operating area.

Power device datasheets typically include transfer and output characteristics, often measured using curve tracers (CT, e.g., Keysight B1505 A). However, these tests are usually conducted at a relatively low V_{ds}, e.g., 20 V for transfer curves and below 30 V for output curves, even for 1200 V rated SiC MOSFETs. Such conditions do not reflect actual switching behavior in the high-voltage/high-current (HVHC) region, as shown in Fig. 1. This limitation is critical for short-channel SiC MOSFETs, where drain-induced barrier lowering (DIBL) increases current with rising V_{ds} [1], especially at the high V_{ds} levels typical in practical applications. The absence of SC region data hinders accurate SC behavior analysis. A key challenge in high-voltage characterization is self-heating caused by the prolonged duration required to reach steady state, and the theoretical minimum duration is determined by the device's intrinsic turn-ON time. Due to 5–15 times higher saturation current and 5–8 times higher current density than SiC MOSFETs, prolonged measurement causes heating and leads to measurement inaccuracies [2].

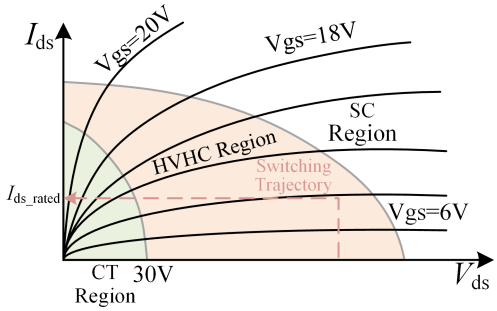

Fig. 1. Measurement regions of a curve tracer, HVHC, and SC.

Methods targeting HVHC region characterization are broadly divided into Miller effect-based and SC-based approaches. In [3], a double-pulse test extracts $V_{gs,plateau}$ under a given V_{ds} and I_d, inferring the internal gate voltage from the external V_{gs}, I_g, and $R_{g,int}$ to reduce measurement error from the voltage drop across $R_{g,int}$. A large gate resistance enhances plateau clarity, but prolonged turn-ON causes excessive self-heating at high current. To mitigate this, Nakamura et al. [4] introduced an auxiliary switch that carries the first pulse to raise current, allowing the device under test (DUT) to handle only the second pulse, thereby reducing the thermal stress. Similarly, Salcines et al. [5] exploited the near-constant V_{ds} during load current transitions to extract multiple I_d–V_{gs} points. Multipulse operation provides cooling intervals to limit self-heating. Gate charging current and C_{gs} are used to correct internal–external gate voltage differences, although modeling nonlinear capacitance, particularly in SiC MOSFETs, is complex due to its dependence on V_{gs}, V_{ds}, and frequency [6]. Miller effect-based testing is limited by the

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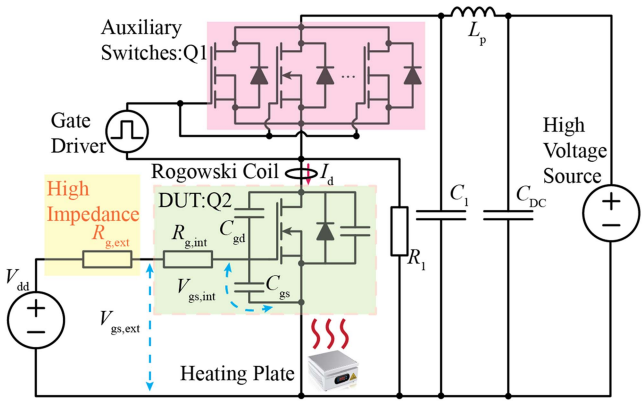

Fig. 2. Proposed measurement topology for characterization in HVHC and SC regions.

typically low Miller voltage and self-heating, which constrain the measurement range and current.

Unlike Miller-based methods, SC testing measures the saturation current under SC conditions. To reduce self-heating, parasitic inductance must be minimized to achieve a fast current rise. Mukunoki et al. [7] applied this method to low-current devices. Deboi et al. [8] introduced an auxiliary switch to eliminate V_{th} hysteresis but neglected the voltage drop across the internal gate resistance, where displacement current through C_{gd} flows into the gate loop, creating a voltage drop across $R_{g,int}$ and causing a notable offset between internal and external gate voltages.

This letter tackles saturation current and gate voltage measurement errors in SiC MOSFETs caused by self-heating and internal gate resistance.

II. Proposed HVHC Characterization Platform

This letter presents a method for measuring the high-voltage saturated I_d–V_{gs} characteristics of high-power SiC MOSFETs. To shorten the time required to reach steady state and reduce self-heating, a precharged gate voltage is applied to the DUT, and multiple parallel auxiliary switches accelerate transitions. Importantly, a high-impedance gate drive loop is employed to ensure accurate internal V_{gs} measurement.

A. SC Test Platform

Fig. 2 shows the measurement topology of the proposed method. Similar to a half-bridge configuration, the DUT (Q2) forms the lower side, while the upper side comprises auxiliary switches Q1. In this letter, as an example, the DUT is the IMZA120R014M1H from Infineon CoolSiC, packaged in TO-247 with a Kelvin source connection. The same device type is also used for the auxiliary switches. The auxiliary switches are driven by a powerful gate driver that generates an ultra-narrow pulse (typically <1 μs), minimizing the total time HVHC is applied to the DUT and effectively reducing self-heating. The parallel connection of multiple switches, combined with a higher gate voltage (20 V), accelerates the turn-ON transient to reach steady state within the ultra-narrow pulse. This approach also prevents any single auxiliary switch from saturating. Since Q1 is implemented in a multidevice parallel configuration, it is necessary to design the printed circuit board (PCB) with a highly symmetrical layout and to carefully select devices of the same type with matched parameters to ensure balanced branch impedances and prevent adverse effects, such as local overheating or overstress caused by uneven current sharing during transient events. A constant precharged gate voltage, denoted as V_{dd} in Fig. 2, is applied between the gate and Kelvin source of Q2 for each measurement. This prevents the influence of V_{th} hysteresis on the DUT during turn-ON [8]. An adjustable gate driver supplies the gate bias, allowing V_{gs} to be tuned for different test conditions. Since this test involves relatively high dv/dt, effective isolation of both the driver and the measurement equipment is required to suppress common-mode noise and high-frequency transients. Table I summarizes the employed components and their key parameters. An auxiliary resistor R_1 is placed in parallel with the DUT, with its value chosen to be much higher than the ON-state resistance of the DUT and much lower than the OFF-state resistance of the auxiliary switch. This ensures that the V_{ds} of the DUT is clamped near 0 V or V_{dc} during auxiliary switch transitions, even when V_{dd} is below the DUT threshold voltage. Parasitic inductance L_p in the power loop limits the current rise rate. A 5 μF capacitor C_1 is soldered to the SiC MOSFET pins to supply instantaneous current and reduce stray inductance. A Rogowski coil is used to measure the drain current, and V_{ds} is also measured simultaneously. Due to the presence of other impedances in the circuit, the actual V_{ds} is slightly lower than the intended supply voltage V_{dc}, which requires compensation. The heating plate is used to heat the DUT to the set temperature.

TABLE I
Devices and Equipment Used in the Experiment

Devices	Model	Key Parameters
SiC MOSFET	IMZA120R014M1H	$V_{DS,max} = 1200$ V
Gate driver	1ED3122MC12H	CMTI $> 200\,\text{kV}\,\mu\text{s}^{-1}$
Isolated source	WE-HIDA 750319177	$C_{parasitic} = 0.68$ pF
Oscilloscope	WaveSurfer 4034HD	Bandwidth: 350 MHz
Current probe	CWT MiniHF 15	Peak $di/dt = 80\,\text{kA}\,\mu\text{s}^{-1}$
Voltage probe	Micsig DP3002	CMRR > 40 dB (20 MHz)
Voltage source	SM1500-CP-30	$V_{max} = 1500$ V

B. Intrinsic Gate-Source Voltage Measurement

One of the key challenges in device characterization is accurately measuring the gate-source voltage V_{gs} due to the presence of internal gate resistance. When Q1 switches ON rapidly, the V_{ds} of Q2 rises sharply. This rapid change induces a displacement current I_{gd} through the gate-drain capacitance C_{gd}. In a typical gate driver configuration, I_{gd} splits into two paths: the gate-source capacitance C_{gs} and the internal gate resistance $R_{g,int}$. The I_{gd} can be expressed, as shown in (1). To demonstrate the principle, the following is a reasonable simplification. During the turn-ON transient of Q1, the rising edge of Q2's V_{ds} can be approximated as linear. As illustrated in Fig. 3(a), this allows I_{gd} to be modeled as a pulse current. I_{gd} is calculated using the

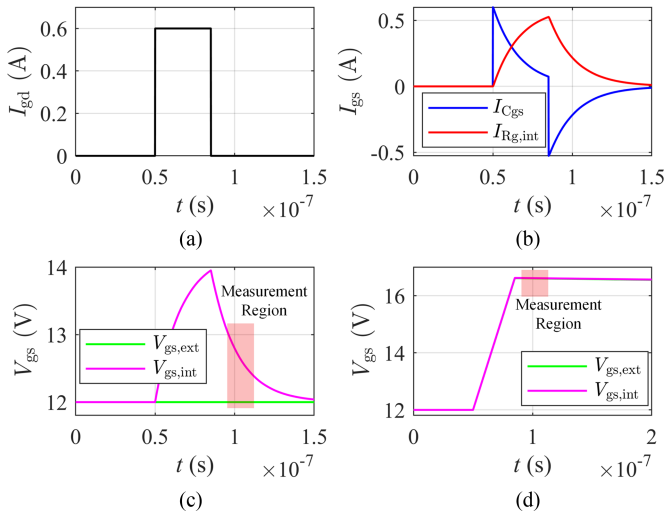

Fig. 3. Relative waveform of I_{gd} in the gate loop with initial $V_{gs} = 12\,\text{V}$ and $V_{dc} = 600\,\text{V}$ from linear technology (LT) spice simulation. (a) Displacement current of C_{gd}. (b) Current through C_{gs} and $R_{g,int}$. (c) Comparison of external and internal V_{gs}. (d) External versus internal V_{gs} in a high-R_g gate loop.

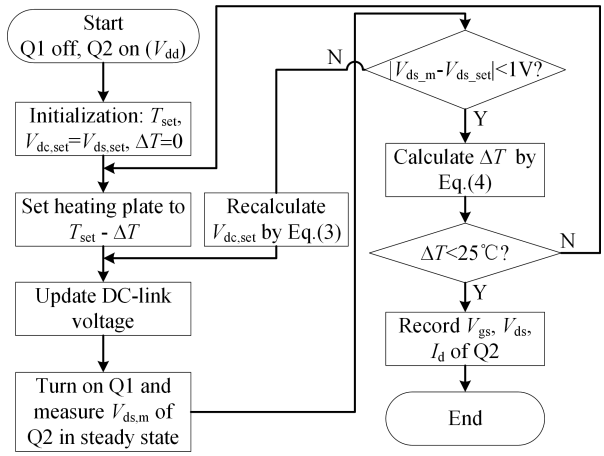

Fig. 4. Flowchart for extracting saturation characteristics.

maximum voltage slew rate at $V_{dc} = 600\,\text{V}$, yielding $600\,\text{mA}$. Due to its high frequency, I_{gd} initially flows through C_{gs} and subsequently through $R_{g,int}$, as shown in Fig. 3(b). Fig. 3(c) shows that the voltage drop across $R_{g,int}$ causes a mismatch between the externally measured gate voltage $V_{gs,ext}$ and the actual internal gate voltage $V_{gs,int}$

$$I_{gd,Q2} = C_{gd}\frac{dV_{gd}}{dt} \approx C_{gd}\frac{dV_{ds}}{dt}. \tag{1}$$

Since $R_{g,int}$ is the intrinsic gate resistance of the device, it cannot be bypassed and is nonnegligible. For the DUT, $R_{g,int}$ is $3.7\,\Omega$. To ensure an accurate measurement of V_{gs}, a large external gate resistor ($R_{g,ext} = 2\,\text{k}\Omega$) is employed in this letter. This high resistance ensures that during the test pulse, the I_{gd} is almost entirely directed into C_{gs} with negligible discharge. As a result, $V_{gs,int}$ rises and remains steady throughout the pulse, ensuring $V_{gs,ext} \approx V_{gs,int}$, as shown in Fig. 3(d). The steady-state $V_{gs,ext}$ can be expressed as follows:

$$V_{gs,steady} = V_{gs,precharge} + \int_0^{V_{ds,set}} \frac{C_{gd}(V_{ds})}{C_{gs}(V_{ds})}\,dV_{ds} \tag{2}$$

where $V_{gs,precharge}$ is the precharged gate voltage applied before testing, and $V_{ds,set}$ denotes the drain-source voltage at which the saturation current is extracted. The capacitances C_{gd} and C_{gs} can be modeled by fitting measurement data. Under this configuration, the measured *I–V* data are at $V_{gs,steady}$ instead of $V_{gs,precharge}$.

III. HVHC Characteristics Extraction Method

A. Procedure

Fig. 4 shows a flowchart of the method proposed in this letter, which is described as follows:

1) Initially, Q1 is turned OFF. A predefined constant gate bias voltage V_{dd} is applied to Q2.
2) Set $\Delta T = 0$. Set the temperature of the heating plate to $T_{set} - \Delta T$. The high-voltage power supply is turned ON to charge the dc-link to $V_{dc,set} = V_{ds,set}$.
3) Turn ON Q1 with a short pulse, applying the dc-link voltage across the DUT. The current and voltage rise rapidly, reach their peaks, and then settle into steady state. The saturation current $I_{d,m}$, corresponding $V_{ds,m}$, and external gate voltage $V_{gs,m}$ are measured. Since $di/dt \approx 0$, parasitic inductance introduces no voltage drop. In addition, $dv/dt \approx 0$ eliminates displacement currents through junction capacitances, ensuring the measured current flows entirely through the channel.
4) After Q1 is turned OFF, it is verified whether $V_{ds,m}$ has reached $V_{ds,set}$. If not, the loop resistance is estimated based on the measured $V_{ds,m}$, and the power supply voltage is updated according to (3). The measurement is then repeated to achieve $V_{ds,m} \approx V_{ds,set}$. It is assumed that after adjusting the dc-link voltage, the equivalent resistance of the DUT and the loop, as well as $V_{gs,ext}$, remain constant

$$V_{dc,set} \approx \frac{V_{ds,set}^2}{V_{ds,m}}. \tag{3}$$

5) Calculate the temperature rise ΔT in the extraction region and compare it against a predefined threshold. This threshold is empirically determined based on experimental results. If the threshold is exceeded, apply temperature compensation by changing the presetting temperature of the heating plate and repeat the process. Otherwise, record V_{gs}, V_{ds}, and I_d of Q2.

B. Consideration of Self-Heating Effects

To reduce self-heating, a fast current rise is essential. A 5 μF capacitor (C_1) is soldered to the leads to minimize stray inductance. Temperature compensation is employed to align the extraction region temperature with the target temperature as closely as possible. While ensuring a sufficient number of samples within the data extraction window, its length is minimized

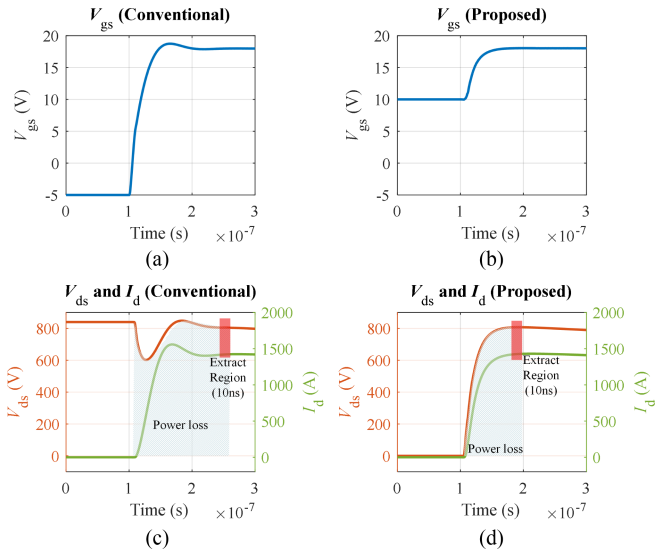

Fig. 5. Comparison between the proposed method and conventional single-device testing under $V_{gs} = 18\,\text{V}$, $V_{ds} = 800\,\text{V}$, and $60\,^{\circ}\text{C}$: (a) V_{gs} with the conventional method. (b) V_{gs} with the proposed method. (c) V_{ds} and I_d with the conventional method. (d) V_{ds} and I_d with the proposed method.

(10 ns in this work) to ensure that the temperature rise within the window does not exceed 5 °C. Fig. 5 presents a comparison of the simulated waveforms between the conventional single-device SC testing method and the proposed method; thanks to the gate precharge design, the proposed method reaches the saturation steady state more quickly. The overlap areas in Fig. 5(c) and (d) represent the power loss. In the proposed method, both voltage and current rise from zero simultaneously to their saturation values, whereas in the conventional method, the device voltage remains close to the dc bus level during the current rise, leading to significantly higher power loss. With V_{ds} and I_d measured, power loss (P_{loss}) can be calculated. The junction temperature is estimated using a fourth-order Foster model, as shown in (4), where $R_{th,i}$ and τ_i are the thermal resistance and time constant, respectively. Based on calculations, the temperature rise under the test conditions shown in Fig. 5 is reduced by 50% when using the proposed method compared to the conventional testing method

$$\Delta T(t) = P_{loss} \cdot \sum_{i=1}^{4} R_{th,i} \left(1 - e^{-t/\tau_i}\right). \tag{4}$$

Since the testing method involves SC tests, some performance degradation is inevitable. According to the study in [9], reducing the SC pulsewidth to below 1 μs helps mitigate degradation. However, we recommend replacing the device with a new one after a certain number of tests, as determined by lifetime characterization, to ensure measurement accuracy.

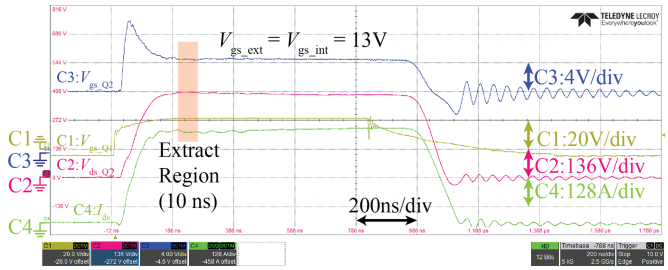

Fig. 6. Measurement waveforms at $V_{dc} = 400\,\text{V}$ and $70\,^{\circ}\text{C}$.

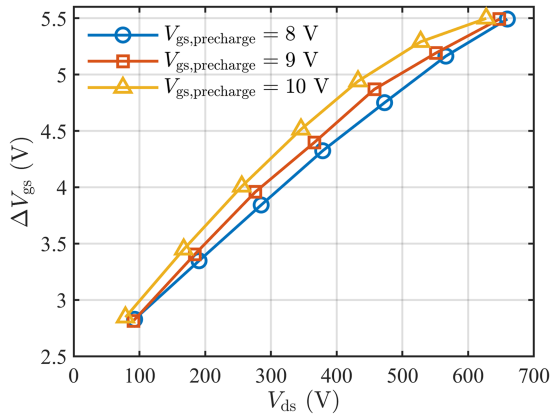

Fig. 7. ΔV_{gs} dependence on $V_{gs,precharge}$ and V_{ds}.

IV. Experimental Validation

A. Internal Gate-Source Voltage and Temperature Rise

Fig. 6 presents a test example under a 400 V dc-link voltage. $V_{gs,Q2}$ represents the gate voltage of the DUT, and $V_{gs,Q1}$ represents the gate voltage of the auxiliary switch. The precharged value of $V_{gs,Q2}$ is 8.3 V, and $V_{gs,Q1}$ initially starts at -5 V. Once $V_{gs,Q1}$ exceeds its threshold voltage, the drain current I_d and V_{ds} of the DUT rapidly rise from zero. Due to the high dV_{ds}/dt and the large gate resistance $R_{g,ext}$, displacement current charges C_{gs} through C_{gd}, causing $V_{gs,Q2}$ to rise to a steady-state value of 13 V. The red-shaded area in the figure indicates the time window during which the saturation current is extracted. V_{gs}, V_{ds}, and I_d are extracted after V_{ds} recovers to the target voltage and reaches a stable state. In this steady-state region, both di/dt and dV/dt of the DUT approach zero, so the influence of parasitic parameters on the measurement accuracy can be neglected. ΔV_{gs} is defined as the difference between the V_{gs} in this time window and its precharged voltage. It is worth noting that while (2) provides an approximation of $V_{gs,steady}$, an accurate calculation should also account for the voltage dependence of C_{gs} and C_{gd}. Fig. 7 illustrates the variation of the V_{gs} increment with respect to V_{ds} under different precharged V_{gs} conditions. When the precharged V_{gs} is relatively low, ΔV_{gs} exhibits an approximately linear relationship with V_{ds}. In contrast, at higher $V_{gs,precharge}$, the relationship between ΔV_{gs} and V_{ds} follows a power-law behavior.

TABLE II
TEMPERATURE RISE EVALUATION AT $T_{SET} = 70\,^{\circ}\mathrm{C}$

$V_{gs,steady}$ (V)	V_{ds} (V)	$V_{gs,precharge}$ (V)	ΔT (°C)
9	600	4.2	4.7
14	600	8.6	14.5
15	600	9.9	22.5
18	600	13.0	35.6

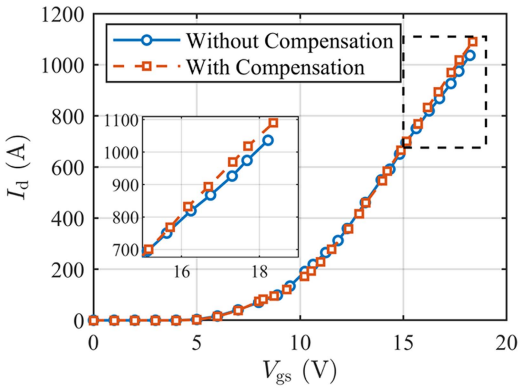

Fig. 8. Comparison of transfer characteristics with and without temperature compensation at $T_{set} = 70\,^{\circ}\mathrm{C}$ and $V_{ds} = 600\,\mathrm{V}$.

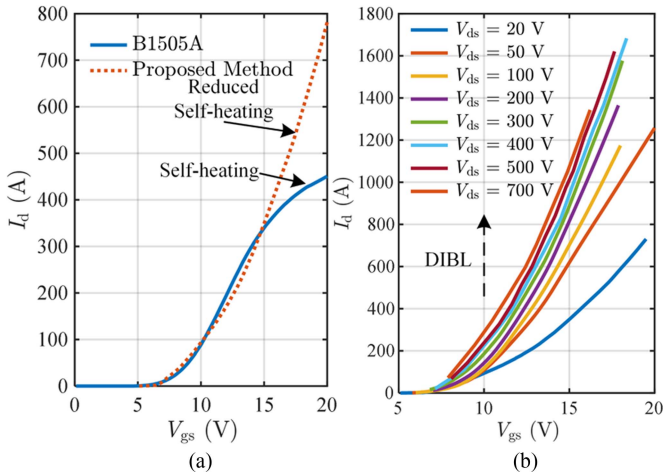

Fig. 9. (a) Transfer curve comparison between B1505 A (measurement delay 25 μs, measurement window = 10 μs) and the proposed method at $V_{ds} = 20\,\mathrm{V}$ and $T_{set} = 25\,^{\circ}\mathrm{C}$. (b) Transfer curves at V_{ds} from 20 to 700 V at $T_{set} = 25\,^{\circ}\mathrm{C}$.

The temperature rise caused by power loss is primarily determined by the current and the internal resistance. Two conditions are most likely to result in a significant temperature rise: high V_{ds} with low V_{gs} (corresponding to high internal resistance), and high V_{ds} with high V_{gs} (corresponding to high current). Table II summarizes the temperature rise under several representative conditions. Under gate-source voltage settings below 15 V, the device self-heating induced by the proposed method is controlled to within 25 °C, which can be considered negligible in the HVHC and SC regions. Since this study uses discrete devices, the relatively high parasitic inductance of the package limits the current rise rate. If power modules with lower parasitic inductance or ultra-fast switching devices are used for testing, the self-heating effect can be further suppressed. At the same time, measurement equipment with sufficient bandwidth and a higher common-mode rejection ratio (CMRR) is required. However, the influence of temperature rise can be compensated by adjusting the heating plate's setpoint. Fig. 8 compares the transfer characteristics with and without temperature compensation at a target test temperature of 70 °C. When $V_{gs} < 15\,\mathrm{V}$, the presence or absence of temperature compensation has little impact on the saturation current. However, when $V_{gs} > 15\,\mathrm{V}$, the device generates more heat, which increases the equivalent resistance. As a result, the compensated saturation current becomes noticeably higher.

B. HVHC and SC Region I–V Characteristics of SiC MOSFETs

Manufacturers typically only provide transfer characteristics at $V_{ds} = 20\,\mathrm{V}$. The proposed method is particularly suitable for measuring transfer characteristics under high drain-source voltages, offering conditions that better reflect real operating scenarios. Fig. 9(a) shows the transfer characteristics measured at $V_{ds} = 20\,\mathrm{V}$ using both the proposed method and the Keysight B1505A. It can be observed that when V_{gs} is below 15 V, the results from both methods are in close agreement, as the current is relatively low and self-heating is minimal. However, when V_{gs} exceeds 15 V, the longer test pulse used by the B1505A (20 μs) generates more heat and causes a significant temperature rise ($\Delta T \approx 100\,^{\circ}\mathrm{C}$ at $V_{gs} = 20\,\mathrm{V}$), driving the ON-state resistance into its positive temperature coefficient region and resulting in a lower saturation current. In contrast, with the proposed method, owing to the faster steady-state attainment, reduced power dissipation, and shorter data extraction window, the temperature rise can be limited to about 4 °C at $V_{gs} = 20\,\mathrm{V}$, thereby yielding a higher saturation current. Since the DUT features an extremely low ON-resistance (typical $R_{ds(on)}$ of 14 mΩ), the saturation current is highly sensitive to temperature variations. Fig. 9(b) shows the transfer characteristic curves at higher V_{ds} levels of several hundred volts. It is evident that the DIBL effect in SiC MOSFETs becomes more pronounced under these conditions, as the saturation current exhibits an increase with rising V_{ds}.

V. CONCLUSION

This letter introduces a new topology for characterizing the saturation behavior of SiC MOSFETs. The proposed topology resolves critical inaccuracies in HVHC regions, where conventional methods suffer from substantial errors from self-heating due to the long measurement duration required to reach steady state. The proposed approach employs an auxiliary switch with multiple parallel-connected devices to quickly apply voltage to the DUT while keeping the DUT turned ON throughout the test, significantly shortening the duration required for measurement and reducing self-heating. To mitigate V_{gs} errors caused by high dv/dt, a high-impedance gate circuit is used to accurately measure the internal gate voltage, further improving precision. The method is simple, low-cost, and easy to implement, providing a practical solution for HVHC device characterization.

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