A Single-Mode Buck–Boost Converter With Always-Dual-Path Operation for Inductor Current Reduction

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***Abstract*—This article presents a battery-to-3.4 V buck–boost converter designed for mobile devices. The converter employs two flying capacitors (C_{F1} and C_{F2}), one inductor (L) and six switches. C_{F1} operates in parallel with the inductor to distribute input current during inductor energizing phase, while C_{F2} assists the inductor in transferring output current during the inductor de-energizing phase, ensuring the inductor current (I_L) is always lower than the output current (I_{OUT}). This configuration results in a single-mode controlled buck–boost converter, allowing smooth voltage conversion over the entire battery voltage range. Additionally, the maximum voltage stress on switches is limited to either V_{IN} or V_{OUT}, enabling the use of 5-V devices for all power switches. Furthermore, the continuous output current delivery alleviates the right-half-plane zero effect, leading to fast transient responses. The converter was fabricated in a 0.18-μm BCD process. Measurement results demonstrate that the converter achieves a peak efficiency of 97.3% using a bulky inductor with a DCR of 18 mΩ. The peak efficiency remains at 96.4% using a compact inductor with a DCR of 200 mΩ.**

***Index Terms*—Always-dual-path, buck–boost converter, flying capacitor, inductor current reduction, single-mode.**

I. Introduction

FOR portable applications to fully benefit from the compact size and high energy density of modern battery technology, they must operate efficiently across the entire battery voltage range (e.g., from 4.2 V to 2.7 V). This presents a design challenge for generating a mid-3-V supply voltage for many function blocks, such as power amplifiers in Wi-Fi front-end modules [1], [2]. As illustrated in Fig. 1, buck–boost converters offer a feasible solution for these applications [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15]. The conventional buck–boost converter (CBBC) is favored for its simple structure and short time-to market, but it suffers from two main issues [3], [4], [5], [6]. First, conduction loss is high due to the large inductor current (I_L) and the presence of two power switches connected in series with the inductor, resulting in poor efficiency and power density. Second, in the boost mode, the discontinuous output current delivery results in a load-dependent right-half-plane (RHP) zero, degrading transient responses performance, and complicating loop compensation design. To tackle these challenges, various hybrid buck–boost converters with flying capacitors have been explored in recent years [7], [8], [9], [10], [11], [12], [13], [14], [15].

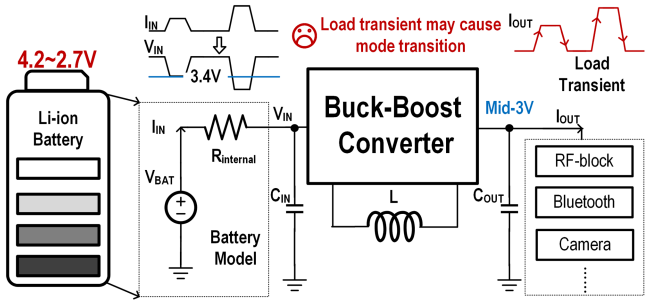

Fig. 1. Diagram of lithium-ion battery powered mobile devices.

To ensure that only one power switch is in the main current path, thereby reducing the conduction loss, a hybrid boost mode was introduced to a two-switches buck converter [7], [8], [9] [see Fig. 2(a)], and the inductor current is reduced in boost mode of [8]. However, the inductor current remains the same as CBBC in [3], [4], [5], and [6] and one switch suffers voltage stress problem, leading to high silicon cost and reduced efficiency. To further reduce conduction loss, an improved topology that combines a dual-path buck and a dual-path boost mode was proposed in [10]. By using four low-voltage switches and one C_F with always reduced I_L, this design achieves both high efficiency and high power density. However, these structures face a common problem during the mode transition. As shown in Fig. 2(a), due to the discontinuous voltage across flying capacitor in buck and boost modes and, thus, large dV_{CF}/dt during mode transition, a large inrush current will be generated that may cause reliability problem.

Fig. 2(b) illustrates buck-like buck–boost converters based on charge pumps developed in [11], [12], and [13] to mitigate the mode transition issue and improve transient responses. These converters operate similarly to a buck converter, with the switching node V_{SW} capable of being higher, equal to,

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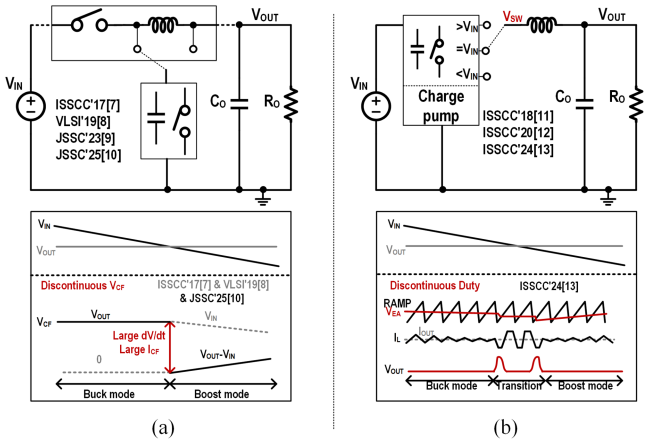


Fig. 2. Existing multimode hybrid buck–boost converters face challenge during mode transition because of the discontinuous V_{CF} or duty cycle. (a) Buck–boost converters with only one power switch on the main current path. (b) Buck-like buck–boost converters based on charge pump.

or lower than V_{IN}, thus achieving buck or boost operations. Due to the continuous output current delivery, the RHP zero is avoided and fast transient responses can be achieved. With the flying capacitors act as voltage source throughout operation, the maximum voltage stress on the power switches is either V_{IN} or $V_{IN}/2$. However, in [13], the discontinuity in duty cycle during mode changes results in voltage overshoot on V_{OUT} [see Fig. 2(b)]. Additionally, the increased complexity due to the addition of more switches and capacitors, along with the need for dedicated mode transition control circuits, complicates the design and limits efficiency improvement.

Although the above designs have improved efficiency and transient performance, the mode transition issue remains challenging. In mobile devices, dynamic load currents from various functions powered by the battery can cause unpredictable fluctuations in battery voltage (see Fig. 1). This necessitates robust mode transition capabilities in buck–boost converters. Therefore, hybrid single-mode buck–boost converters with dual-path operation were proposed [14], [15], offering simple control circuit designs. However, both designs suffer from poor switch utilization due to the requirement for high-voltage devices, which increases silicon cost and limits efficiency. To achieve optimized performance in a hybrid single-mode buck–boost converter, it is essential to reduce the voltage stress on the power switches [16], [17], [18].

To further enhance the power efficiency of single-mode buck–boost converters while maintaining seamless mode transition, this article, an extended version of the conference paper presented in [18], proposes a single-mode, always-dual-path buck–boost converter. The proposed design minimizes the inductor current (I_L) to below the output current (I_{OUT}) across the entire battery voltage range, while ensuring that all power switches are immune to voltage stress issues. In addition to the previously presented work, this article includes a comprehensive loss analysis and transfer function analysis, demonstrating that constructing highly efficient power delivery paths not only improves power efficiency but also enables faster transient responses. Furthermore, a discussion is provided on the performance trade-offs between single-mode and multimode configurations of the proposed topology. Detailed circuit implementations of both the power stage and controller are also presented to enable a thorough analysis and characterization of the proposed converter.

The rest of this article is organized as follows. Section II introduces the operation principle of the proposed converter and provides a performance analysis. Circuit implementations are discussed in Section III, and measurement results are presented in Section IV. Finally, Section V concludes this article.

II. Proposed Buck–Boost Converter

A. Operation Principle of the Proposed Always-Dual-Path Single-Mode Buck–Boost Converter

Fig. 3 reviews the dual-path buck–boost converter proposed in [10]. In the buck mode, during phase 1, the inductor is connected in series with the flying capacitor C_F, accumulating a charge of $\Delta Q = I_L D_S T$ on C_F, where $D_S T$ represents the duration of L and C_F is in series. During phase 2, the output is supplied by both L-path and C_F-path, ensuring the I_L is less than I_{OUT}. It is evident that the charge transferred by C_F-path is $Q_C = \Delta Q$. Then, we have

$$\frac{I_L}{I_O} = \frac{Q_L}{Q_O} = \frac{Q_L}{Q_L + Q_C} = \frac{I_L T}{I_L T + D_S I_L T} = \frac{1}{1 + D_S} \quad (1)$$

where Q_L is the charge transferred by L, while Q_O represents the charge delivered to output.

Note that the inductor handles I_O in a conventional buck ($I_{L,\text{buck}} = I_O$) and I_{IN} in a conventional boost ($I_{L,\text{boost}} = I_{IN}$). To reduce I_L in a boost converter, a C_F-path should be introduced to assist the inductor in distributing the input current, as depicted in Fig. 3(b). Similarly, the I_L/I_{IN} ratio is given by

$$\frac{I_L}{I_{IN}} = \frac{Q_L}{Q_{IN}} = \frac{Q_L}{Q_L + Q_C} = \frac{I_L T}{I_L T + D_S I_L T} = \frac{1}{1 + D_S}. \quad (2)$$

According to (1) and (2), I_L can be reduced across the entire battery range by introducing dual-path operations for the output current in buck mode and for the input current in the boost mode. As illustrated in Fig. 4, during Φ_1, the C_{F1} is connected in series with the inductor while C_{F2} is parallel, transferring charge to the output. In Φ_2, the C_{F2} is connected in series with the inductor while the C_{F1} is in parallel for input current distribution. Building on this concept, a single-mode always-dual-path buck–boost converter is devised, which consists of one inductor, two flying capacitors and six switches.

Fig. 5 illustrates the operation principle of the proposed converter, which operates in a single mode with two operation phases, Φ_1 and Φ_2. During Φ_1, S_1, S_4, and S_5 are ON, energizing L and discharging C_{F1} and C_{F2}. The C_{F2}-path and L-path form a dual-path for the output. During Φ_2, S_2, S_3, and S_6 are ON, the L is de-energized and the C_{F1} and C_{F2} are charged. The L-path and C_{F1}-path then form a dual-path for the input. It can be observed that the voltage across C_{F1} (V_{CF1}) and C_{F2} (V_{CF2}) are V_{IN} and V_{OUT}, respectively. The voltage across L is $2V_{IN} - V_{OUT}$ during Φ_1 and $2V_{OUT} - V_{IN}$ during Φ_2. Using inductor voltage-second balance principle, the voltage conversion ratio

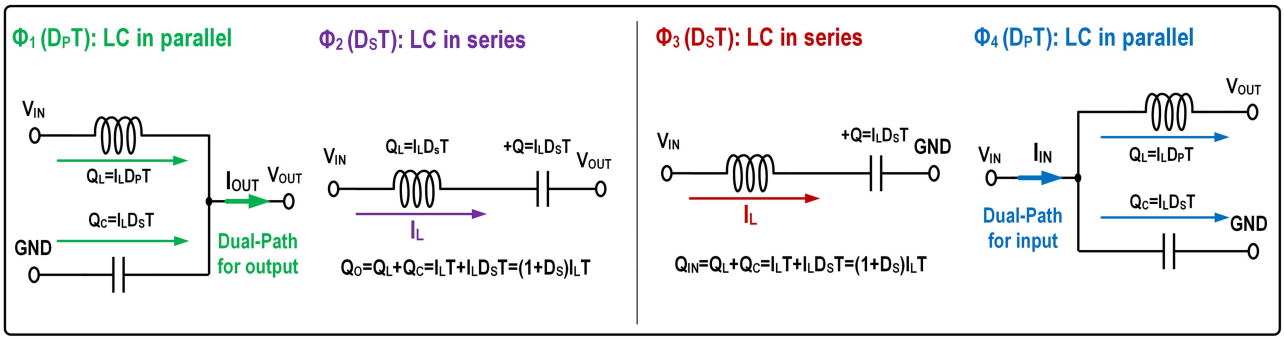


Fig. 3. Prior inductor current reduction methods in [10]. (a) Dual-path for output in buck converter. (b) Dual-path for input in boost converter.

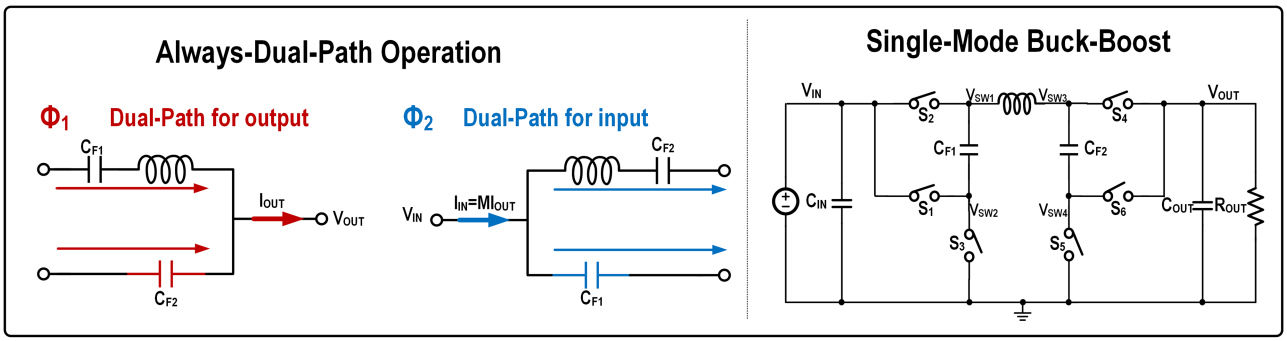


Fig. 4. Proposed single-mode buck–boost converter with always-dual-path operation.

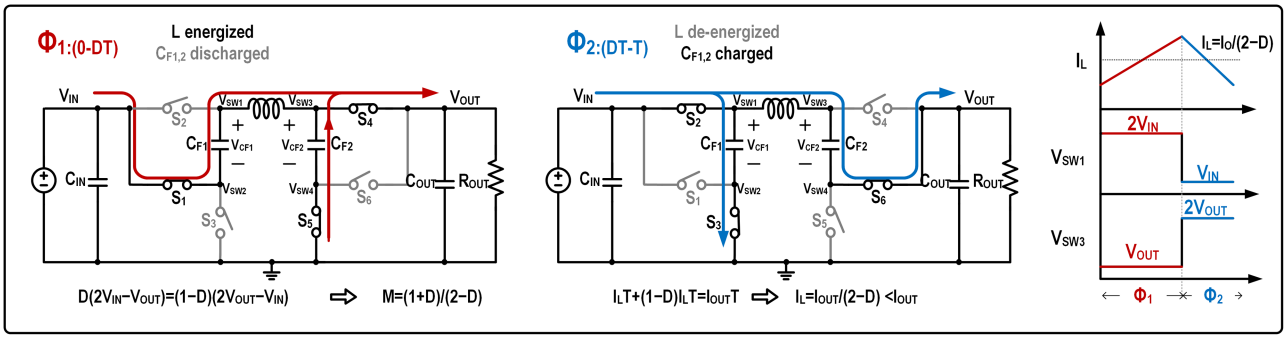


Fig. 5. Operation principle of the proposed buck–boost converter.

is derived as

$$\mathrm{D}\left(2V_{\mathrm{IN}}-V_{\mathrm{OUT}}\right)=(1-D)\left(2V_{\mathrm{OUT}}-V_{\mathrm{IN}}\right) \tag{3}$$

$$\mathrm{M}=\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}}=\frac{1+D}{2-D}\epsilon\,(0.5,2) \tag{4}$$

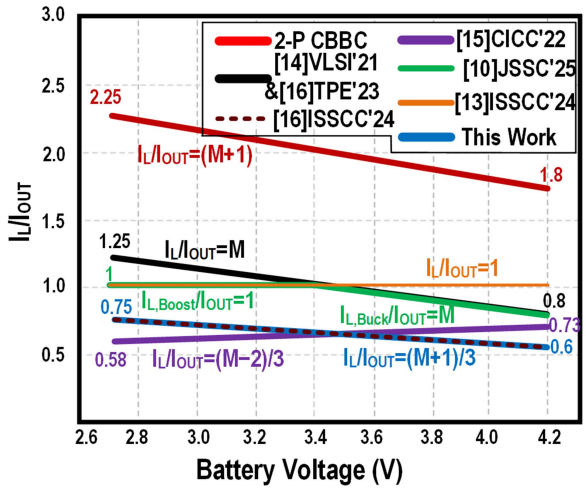
where D denotes the duty cycle of Φ_1, varying from 0 to 1, thus, M varies from 0.5 to 2. Although the voltage conversion ratio is limited, the converter meets the requirement of battery-to-3.4-V applications. Since V_{CF1} and V_{CF2} are continuous and a single mode covers both down and up conversion across the entire input voltage range, smooth voltage conversion can be easily realized when V_{IN} changes without complex control circuits. Thanks to the always-dual-path operation, the I_L is significantly reduced, and the I_L/I_O ratio is given by

$$\frac{I_L}{I_O}=\frac{Q_L}{Q_O}=\frac{I_LT}{I_LT+(1-D)\,I_LT}=\frac{1}{2-D}. \tag{5}$$

Substituting (4) into (5), we have

$$\frac{I_L}{I_O}=\frac{M+1}{3}. \tag{6}$$

As shown in Fig. 6, compared with the topology in [10], which has the lowest I_L among multimode buck–boost converters, the I_L in this work is further reduced by adopting both methods in [10]. Compared with the single-mode topologies, the I_L in this design is much lower than that in [14] and [19] and comparable to that in [15] and [18].



*2-P CBBC: Conventional buck-boost converter w/ 2-phase operation

Fig. 6. Comparison of normalized inductor current between this work and prior designs.

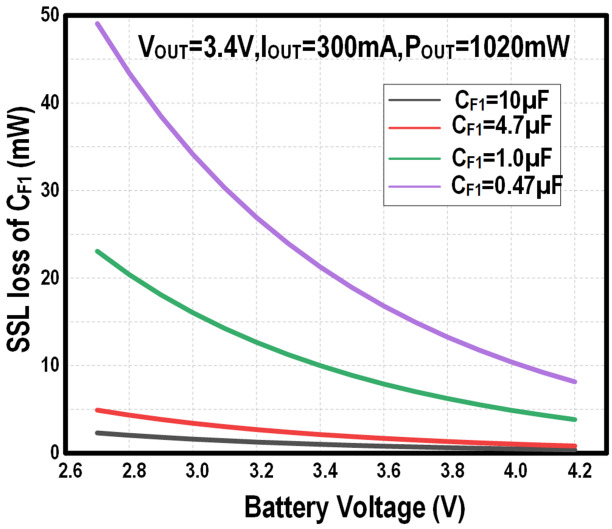


Fig. 7. SSL loss varies with different C_{F1} when V_{OUT} = 3.4 V, I_{OUT} = 300 mA.

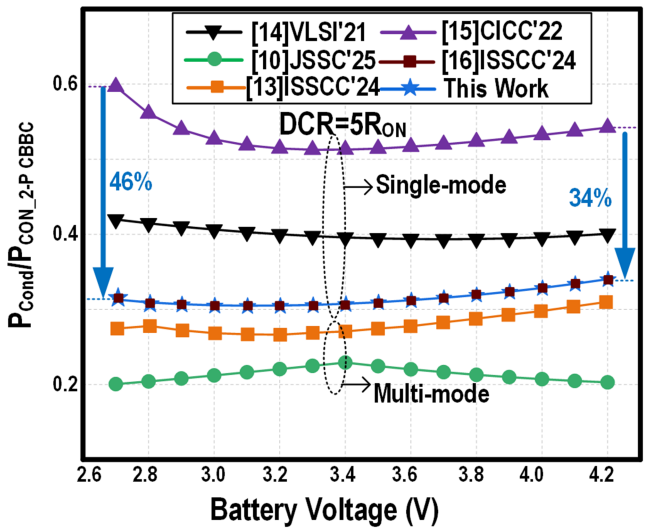


Fig. 8. Comparison of normalized conduction loss between this work and prior designs.

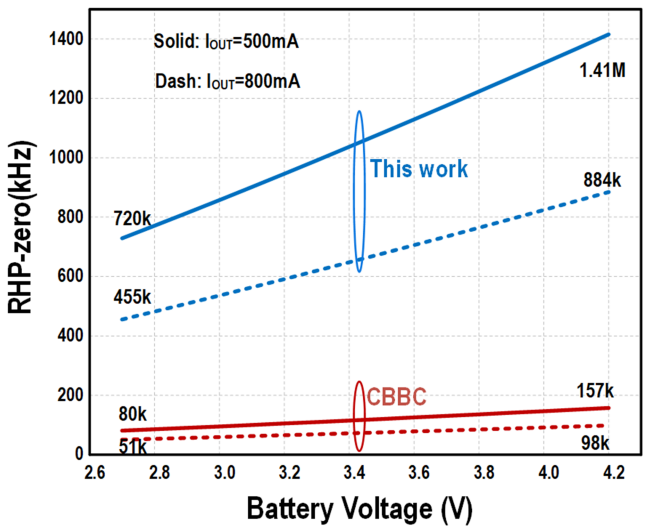


Fig. 9. Comparison of RHP zero between CBBC and the proposed converter.

B. Loss Analysis

While hybrid converters offer advantages in balancing efficiency and power density by leveraging the relatively high energy density of capacitors [19], [20], [21], and [22], these tradeoffs still have inherent limitations. These constraints include slow-switching limit (SSL) losses, primarily caused by charge-sharing between capacitors, and fast-switching limit (FSL) losses, which are mainly due to the resistance of switches, capacitors, and inductors, if present. To evaluate the performance of hybrid converter, a framework has been proposed that compares different topologies using a minimum power loss figure of merit when considering cost constraints [23], [24].

1) SSL Loss: In this design, charge-sharing losses occur due to the charge distribution between C_{F1} and C_{IN} during Φ_1, and between C_{F2} and C_{OUT} during Φ_2. For instance, I_L softly

TABLE I
PARAMETERS OF POWER SWITCHES

Condition: V_{IN} = (2.7-4.2 V), V_{OUT} = 3.4 V, 5-V devices are used				
Architecture	Sw	V_i	$I_{rms,i}$	G_i @D=0.5
Single-mode CBBC I_L=$(M+1)I_O$	S_1	V_{IN}	$I_L\sqrt{D}$	G_{ON}
	S_2	V_{IN}	$I_L\sqrt{1-D}$	G_{ON}
	S_3	V_{OUT}	$I_L\sqrt{D}$	G_{ON}
	S_4	V_{OUT}	$I_L\sqrt{1-D}$	G_{ON}
Proposed converter I_L=$(M+1)/3I_O$	S_1	V_{IN}	$I_L\sqrt{D}$	$G_{ON}/2$
	S_2	V_{IN}	$I_L\sqrt{1/(1-D)}$	G_{ON}
	S_3	V_{IN}	$I_L\sqrt{D^2/(1-D)}$	$G_{ON}/2$
	S_4	V_{OUT}	$I_L\sqrt{1/D}$	G_{ON}
	S_5	V_{OUT}	$I_L\sqrt{(1-D)^2/D}$	$G_{ON}/2$
	S_6	V_{OUT}	$I_L\sqrt{1-D}$	$G_{ON}/2$

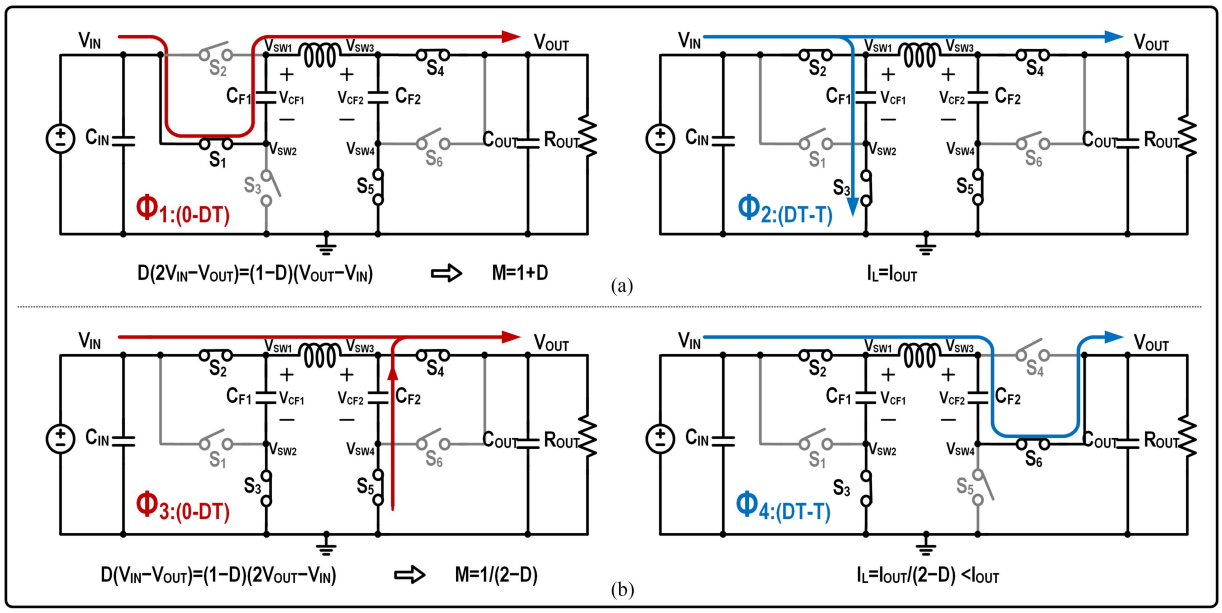


Fig. 10. Multimode operation of the proposed converter. (a) Boost mode. (b) Buck mode.

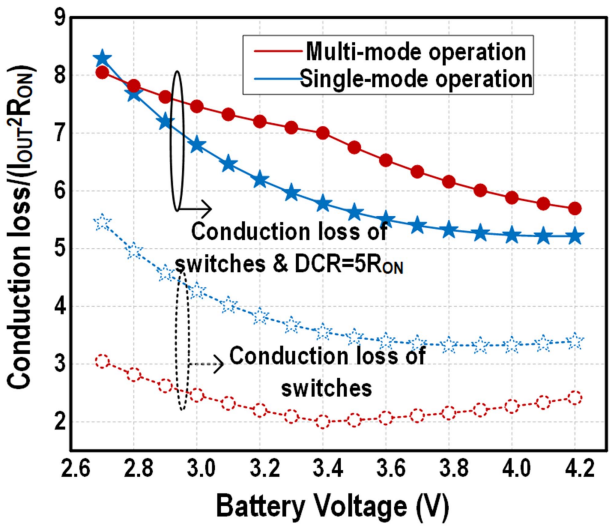


Fig. 11. Comparison of normalized conduction loss and inductor current of the proposed converter operating with single-mode and multimode.

discharges $C_{\rm F1}$ during Φ_1, with the amount of transferred charge given by

$$\Delta Q_{CF1} = I_L\ DT \tag{7}$$

During Φ_2, to maintain charge balance in $C_{\rm F1}$, it is hard-charged by $C_{\rm IN}$ with ΔQ_{CF1}. To simplify the analysis of the SSL losses, we assume that the inductor behaves as a current source and the input and output capacitors have large capacitance values. Then, the charge-sharing loss of $C_{\rm F1}$ can be calculated as

$$P_{CF1} = \frac{1}{2}\ C_{F1}\left(\frac{\Delta Q_{CF1}}{C_{F1}}\right)^2 \frac{1}{T}. \tag{8}$$

Combining (5), (7), and (8) yields

$$P_{CF1} = \frac{(I_O D)^2 T}{(2-D)^2 C_{F1}}. \tag{9}$$

From (9), it is evident that a larger $C_{\rm F1}$ results in smaller charge-sharing loss. Fig. 7 illustrates the charge-sharing loss associated with different $C_{\rm F1}$ capacitances when $I_{\rm OUT} = 300$ mA, showing that capacitance of 4.7 μF or greater effectively reduces the SSL loss to a negligible level. Accordingly, this design adopts two 4.7 μF flying capacitors in compact 0603 packages to ensure both performance and integration efficiency. With $V_{\rm IN} = 3.7$ V, $V_{\rm OUT} = 3.4$ V, $I_O = 0.3$ A, $C_{\rm F1} = 4.7$ μF, and $f_{sw} = 1$ MHz ($T = 1$ μs), $\rm P_{CF1}$ is approximately 1.2 mW, accounting for 4.2% of the total power loss. This indicates that SSL losses in this design are not dominant, and are considered negligible in the subsequent analysis.

2) FSL Losses: Assuming that all capacitors function as voltage sources, FSL losses are primarily related to conduction losses in resistive elements. The conduction loss (P_{cond}) for a given architecture can be expressed as

$$P_{Cond} = \sum_{i=1}^{k} I_{{\rm rms},i}^2 R_i\ + I_{{\rm rms},L}^2 {\rm DCR} \tag{10}$$

where $I_{{\rm rms},i}$ is the root-mean-square (rms) current of switch i with resistance R_i, $I_{{\rm rms},L}$ is the rms current of the inductor, and k is the number of switches. In (10), the first term corresponds to the loss of active devices (switches), while the second term represents the loss from passive device (inductor). In a practical design, to minimize the P_{Cond} while maintaining a small form factor, the area of each switch should be optimized individually within a total active area constraint, and $\rm I_L$ should be minimized, as bulky inductors with low DCR are typically not allowed.

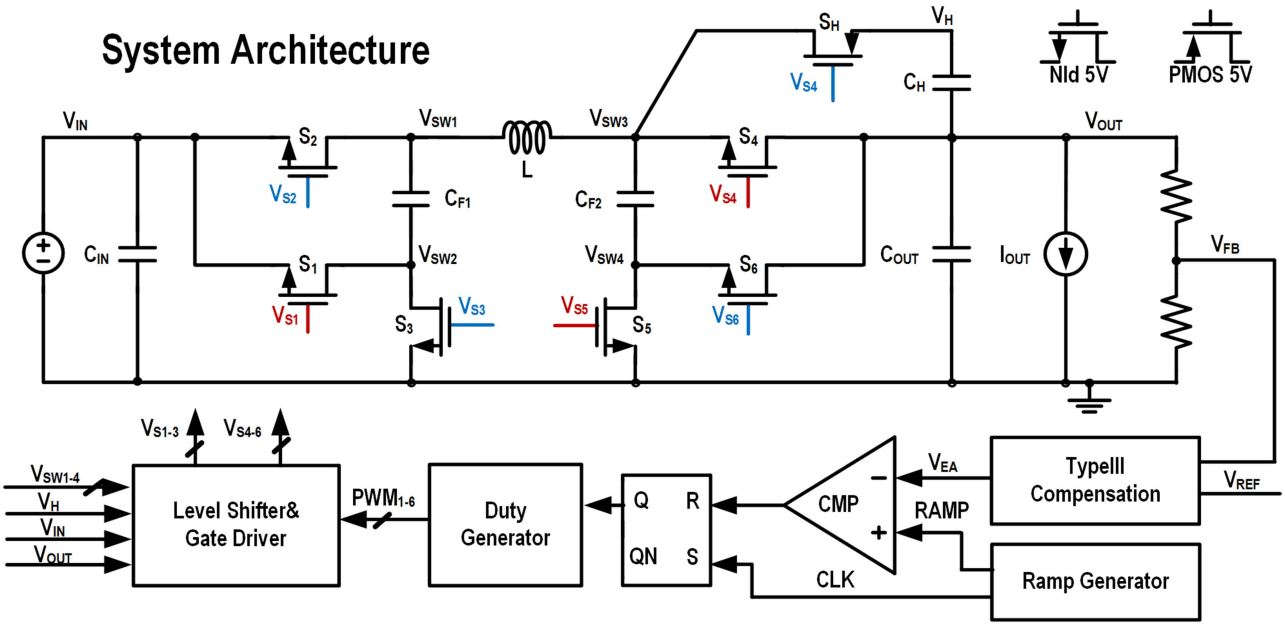


Fig. 12. System architecture of the proposed converter.

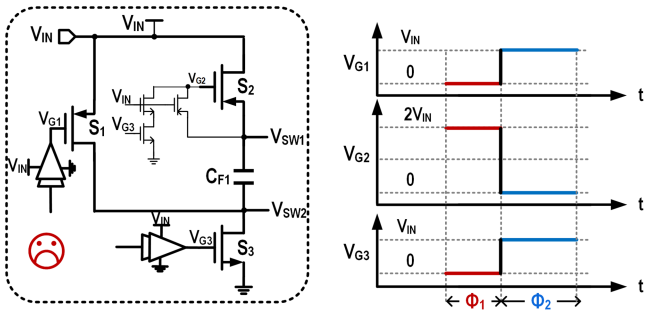


Fig. 13. Optional implementations where S_1 and S_2 are PMOS transistors, and S_3 is NMOS transistor.

For simplicity, the inductor current ripple is ignored in the subsequent analysis. The conduction loss of the inductor is given by

$$P_{Cond,\mathrm{DCR}} = I_L^2 \mathrm{DCR} = \frac{(M+1)^2}{9} I_O^2 \mathrm{DCR}. \tag{11}$$

For a fair comparison, the sum of G-V^2 products of all switches in a power converter is used as a cost-based constraint [23], which can be written as

$$A_{tot} = \sum_{i=1}^{k} G_i V_i^2 \tag{12}$$

where G_i and V_i represent the conductance and rated voltage of switch i. To minimize the conduction loss of switches under the area constraint in (12), an auxiliary function is obtained using the Lagrange multiplier optimization as follows:

$$\mathcal{L}(G_i, \lambda) = \sum_{i=1}^{k} \frac{I_{\mathrm{rms},i}^2}{G_i} + \lambda \left(\sum_{i=1}^{k} G_i V_i^2 - A_{tot} \right) \tag{13}$$

where the first term of (13) represents the conduction loss of the proposed converter and λ is the Lagrange multiplier. Then, the conduction loss is minimized by taking the partial derivatives of $\mathcal{L}$ with respect to G_i and then setting it to zero.

Then, the optimal conductance of each switch is derived as

$$G_i = \frac{I_{\mathrm{rms},i}}{V_i} \frac{A_{tot}}{\sum_{j=1}^{k} I_{\mathrm{rms},j} V_j}. \tag{14}$$

It is evident that each switch is sized proportional to its I_{rms}/V_i ratio with a given total area. With all switches having the same stress voltages, (14) is simplified as

$$G_i = \frac{I_{\mathrm{rms},i}}{\sum_{j=1}^{k} I_{\mathrm{rms},j}} G_{tot}. \tag{15}$$

Table I lists the rms currents and rated voltages of the power switches of CBBC and the proposed converter. It is worth noting that the voltage stress across switches is either V_{IN} or $\mathrm{V_{OUT}}$ in the proposed converter, avoiding the use of high-voltage devices.

Since all switches in CBBC have equal rms current and the same stress voltage when $\mathrm{D} = 0.5$, they have the same area, and conductance ($G_{\mathrm{ON}} = 1/R_{\mathrm{ON}}$). Therefore, the total conductance, G_{tot}, amounts to $4G_{\mathrm{ON}}$. In the proposed converter, the optimized conductance for each switch is determined based on their respective rms currents, as listed in Table I. Specifically, S_2 and S_4 are sized twice as large as the other switches to accommodate their doubled rms current when $D = 0.5$. This sizing strategy is consistently applied across other designs for a fair comparison, using a compact inductor with a large DCR of $5R_{\mathrm{ON}}$. As illustrated in Fig. 8, the proposed converter achieves the lowest conduction loss among single-mode buck–boost converters, owing to the absence of the voltage stress problem. However, due to the increased number of switches or voltage stress on power switches, its conduction loss is higher than that

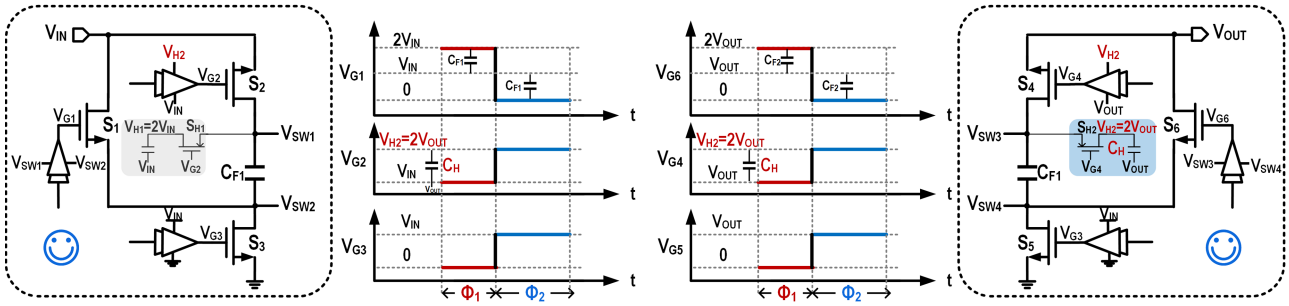


Fig. 14. Adopted implementations using NLDMOS transistors for S_{1-6} and corresponding gate drivers.

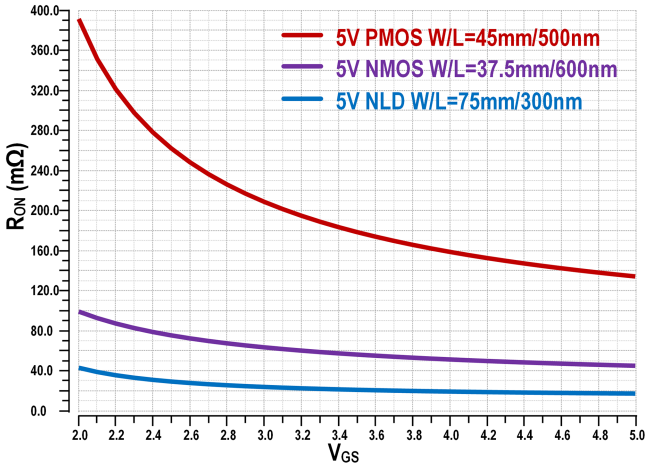


Fig. 15. Comparison of on resistance of 5-V PMOS, 5-V NMOS, 5-V NLDMOS with the same active area ($=W \times L$).

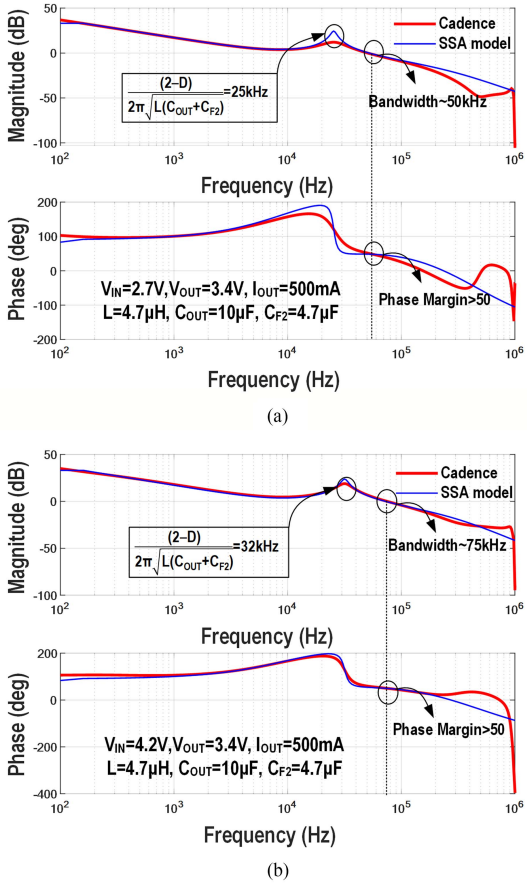


Fig. 16. Bode plots of the converter. (a) $V_{\mathrm{IN}} = 2.7$ V, $I_{\mathrm{OUT}} = 500$ mA. (b) $V_{\mathrm{IN}} = 4.2$ V, $I_{\mathrm{OUT}} = 500$ mA.

in [10] and [13]. Consequently, the power efficiency under heavy load conditions is theoretically expected to be lower compared to [10] and [13], given a comparable chip area.

The above analysis is based on the assumption that the flying capacitor is sufficiently large, allowing SSL losses to be negligible. However, when the flying capacitor is small and SSL losses become significant, a more accurate loss analysis method can be employed that merges aspects of both capacitance and switch utilization [24].

C. Transfer Function Derivation

Using the state-space averaging method, the transfer function of the power stage of the proposed converter has been derived. As discussed in Section II, $V_{\mathrm{CF1}} = V_{\mathrm{IN}}$ and $V_{\mathrm{CF2}} = V_{\mathrm{OUT}}$ in the steady state. Assuming all parasitic resistances (R_{eq}) are negligible, C_{F1} is not considered as a state variable since the variation in v_{IN} is zero [26], while C_{F2} is treated as one. Therefore, there are three state variables: v_{CF2}, i_L, and v_{OUT}. Based on the current and voltage relationships of C_{F2}, L, and C_{OUT}, the control-to-output transfer function is derived as follows:

$$G_{vd}(s)\big|_{v_{\mathrm{in}}=0,\ R_{eq}=0} = G_{vd0}\frac{1-\frac{s}{w_{\mathrm{RHP}-z}}}{1+\frac{s}{Qw_0}+\frac{s^2}{w_0^2}} \tag{16}$$

$$G_{vd0} = \frac{3V_{\mathrm{IN}}}{(2-D)^2} \tag{17}$$

$$w_0 = \frac{2-\mathrm{D}}{\sqrt{L\left(C_{F2}+C_{\mathrm{OUT}}\right)}} \tag{18}$$

$$Q = \frac{(2-\mathrm{D})\,\mathrm{R}}{\sqrt{\left(C_{F2}+C_{\mathrm{OUT}}\right)/L}} \tag{19}$$

$$w_{\mathrm{RHP}-z} = \frac{3(2-D)^2R}{(1+D)\,L} = \frac{9\,R}{M\,(M+1)\,L} \tag{20}$$

where R is load resistance and R_{eq} is all other parasitic resistances. This derivation indicates that the transfer function of the converter is a second-order function with a pair of complex poles, combining C_{F2} and C_{OUT} into a single state element. Moreover, due to the charge transferred to output in one cycle, $(2–D)I_LT$, is disproportional to D, resulting in an RHP zero. However, the continuous output current delivery pushes this zero to a higher frequency, making the RHP zero in this converter nine times higher than that in a CBBC with two-phase operation, where the RHP zero is given by

$$\omega_{\mathrm{RHP}-z,\mathrm{CBBC}} = \frac{(1-D)^2 R}{DL} = \frac{R}{M\,(M+1)\,L}. \tag{21}$$

Fig. 9 compares the RHP zero locations of the proposed and conventional structures under varying input voltages and load currents. At an input voltage of 2.7 V and an output current of 500 mA, the RHP zero of the proposed structure reaches 728 kHz, whereas that of the conventional structure is only 80 kHz. With the RHP zero in the proposed structure being nine times higher than that in the conventional structure, the system can support a higher control bandwidth without sacrificing stability. This indicates that the proposed converter has the potential to achieve faster transient response.

D. Discussion on Different Configurations of the Proposed Converter

Note that the proposed converter also supports multimode operation, similar to the CBBC that can configure from single-mode to multimode operation, including pseudobuck and pseudoboost modes. As illustrated in Fig. 10(a), when switches S_4 and S_5 are always ON and S_6 is OFF, C_{F2} functions as an output capacitor. Under this configuration, the operational principle resembles that of a KY boost converter [27]. During Φ_2, C_{F1} is charged by V_{IN}, while in Φ_2, V_{SW1} is pumped to $2V_{IN}$, achieving boost operation with a voltage conversion ratio defined as $M = 1 + D \in (1, 2)$. The output current delivery is continuous, and $I_L = I_{OUT}$. When S_2 and S_3 are kept ON, C_{F1} acts as an input capacitor, the converter works in the buck region [see Fig. 10(b)] like a SIC converter [27], yielding a voltage conversion ratio of $M = 1/(2–D) \in (0.5, 1)$. Since the inductor is located at the input, the inductor current equals to input current, express as $I_L = 1/(2–D)I_{OUT}$. Compared to conventional multimode buck–boost converter, the inductor current is reduced in both modes like that in [6]. Additionally, the voltage across the flying capacitors is stably defined throughout the entire battery voltage range ($V_{CF1} = V_{IN}$, $V_{CF2} = V_{OUT}$), which enhances the converter's potential for smooth mode transition with dedicated control circuits recommended in [28].

For CBBC, multimode operation is typically employed to enhance efficiency by minimizing inductor current and conduction losses. In this design, losses on the power switches under single-mode operation are larger than those in multimode configurations like CBBC, as shown in Fig. 11, due to the increase number of power switches in the current. However, the always-dual-path operation during single-mode significantly lowers the inductor current, thereby reducing total conduction losses, when using a compact inductor, compared to multimode operation. Given the advantages of single-mode operation and the further reduction in inductor current, we advocate the converter work operate in single-mode for mobile devices with strictly limited space.

III. Circuit Implementation

Fig. 12 presents a detailed circuit diagram of the proposed converter. Loss analysis and small-signal analysis are employed to guide the design of the converter prototype. This design accommodates an input voltage range of 2.7 V to 4.2 V, typical for battery applications, with the output voltage regulated to a fixed 3.4 V. Optimal utilization of active devices is achieved by using 5-V N-type lateral double-diffused MOS (5-V NLDMOS) transistors for $S_{1–6}$, and a 5-V P-type MOS transistor for S_H, all configured with compact sizes and supplemented with appropriate gate drivers, as discussed shortly.

A. Design Considerations of Power Stage

The proposed converter features a symmetrical configuration around the L, which simplifies the power stage design by allowing focus on only half of the circuit. Fig. 13 shows a solution for implementations of $S_{1–3}$ on the left of inductor, where S_1 and S_2 are P-type MOS transistors, and S_3 is an N-type MOS transistor. This approach simplifies the design of gate drivers for $S_{1–3}$, as S_1 and S_3 can be directly powered by V_{IN} and ground, while S_2 can utilize a dynamic driver suggested in [12] without the need for a bootstrap capacitor. However, this configuration involves two power-inefficient P-type switches among the three switches, which significantly decreases both efficiency and power density.

To improve the utilization of active devices, an alternative solution involves using N-type MOS transistors for S_1–S_3 and applying the same implementation to S_4–S_6, as illustrated in Fig. 14. With the 0.18-μm BCD process, the minimum channel length of a 5-V CMOS device (N-type) is 600 nm while of a 5-V NLDMOS is only 300 nm. Fig. 15 compares the ON-resistance of a 5-V PMOS, a 5-V NMOS with a 5-V NLDMOS under the same active area ($=W \times L$), illustrating the NLDMOS as more suitable for use as a switch. To minimize the conduction loss of switches, S_2 and S_4 are sized to be twice as large as other switches, as analyzed in Section II-B.

In this setup, switches S_1 and S_5 have their source terminals connected to the bottom plate of flying capacitors C_{F1} and C_{F2}, respectively, allowing the gate drivers to be directly powered by the corresponding flying capacitor. Meanwhile, switches S_2 and S_4 have their source terminals, respectively, connected to V_{IN} and V_{OUT}, necessitating fixed supplies of $2V_{IN}$ or $2V_{OUT}$, which can be generated from V_{SW1} and V_{SW3}, respectively. To minimize the bill of materials cost, this design aims to use only one OFF-chip bootstrap capacitor, rather than two in [16]. Using $2V_{IN}$ exclusively, the overdriving voltage (V_{OD}) of S_2 is $V_{IN} \in$(2.7 V, 4.2 V), while for S_4 it is $2V_{IN} – V_{OUT} \in$(2 V, 5 V). If $2V_{OUT}$ is used only, the V_{OD} of S_2 is $2V_{OUT} – V_{IN} \in$(2.6 V, 4.1 V). Ultimately, $2V_{OUT}$ is selected to supply both S_2 and S_4 for small variation of V_{OD}. To generate $2V_{OUT}$, a small switch S_{H2} is introduced and activated during Φ_2, charging C_{H1} and regulating V_{H2} to $2V_{OUT}$.

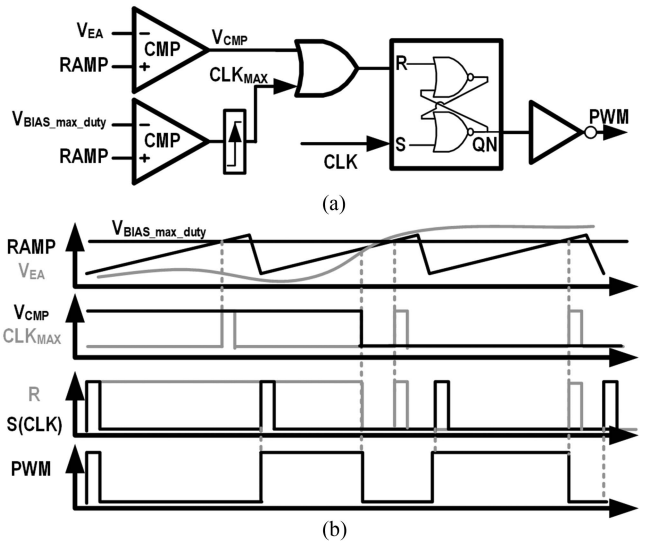


Fig. 17. (a) Schematic of duty cycle limitation. (b) Operation principle of the duty generator.

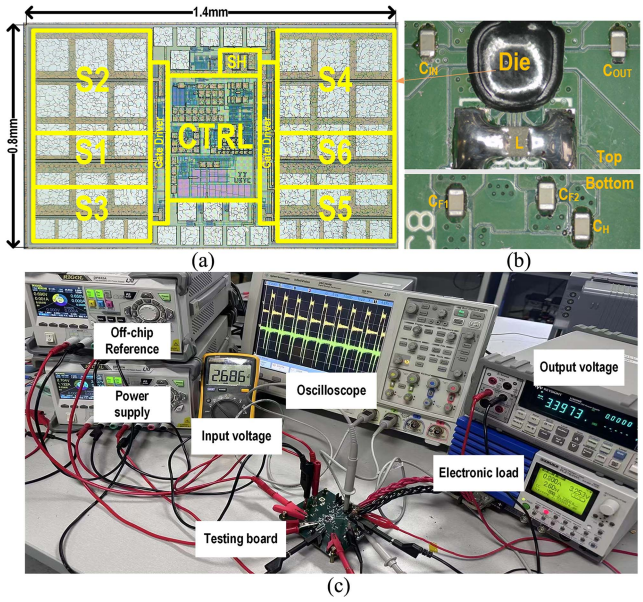


Fig. 18. (a) Die micrograph of the proposed converter. (b) PCB solution. (c) Measurement setup.

Although an external OFF-chip capacitor is required, the efficiency and ON-die current density can be improved by using NLDMOS only instead of CMOS devices.

B. Design Considerations of Control Stage

The control-to-output transfer function of the converter has been derived in Section II-C, revealing the presence of a pair of complex poles and a high frequency RHP zero with. Thereby a voltage mode PWM control with a Type-III compensation is applied for wide loop bandwidth [29]. Fig. 16 shows the bode plots of loop-gain function of the proposed converter. Note that the red lines represent circuit-level periodic stability simulation results using Cadence, while blue lines depict calculated results based on the linear small-signal analysis. With appropriate compensation, the converter achieves a bandwidth of >50 kHz with a phase margin of >50°.

To guarantee robust operation for the level shifters and the power stage, the extremely large or small duty cycles are prohibited. Thus, a duty cycle limiter is incorporated into PWM control logic. As shown in Fig. 17, when V_{EA} is lower than RAMP signal, the minimal duty cycle is determined by the pulsewidth of CLK signal; when V_{EA} exceeds the RAMP signal, the maximum duty cycle is limited by a CLK_{max} signal generated by comparing the RAMP signal with a fixed bias voltage $V_{BIAS\_max\_duty}$, which has a fixed phase delay relative to CLK. In this work, the duty cycle of PWM signal is constrained within 5% to 95%.

IV. Measurement Results

Fig. 18(a) shows the die micrograph of the proposed buck–boost converter. Fabricated in a 0.18-μm BCD process using 5-V devices only, the converter occupies an active area of 1.12 mm^2. Table II shows the type and the size of power switches S_{1-6} and S_H with corresponding drive voltage. The prototype was measured with $V_{IN} = 2.7$ to 4.2 V and $V_{OUT} = 3.4$ V. Fig. 18(b) and (c) presents the PCB solution of the converter and the measurement setup. The setup includes two 4.7 μF flying capacitors, one 10 μF output capacitor, one 4.7 μH inductor and one 100 nF bootstrap capacitor. The power stage switches at 1 MHz.

TABLE II
Size of Power Switches

	Type	W/L	V_{GS}
$S_{1,3}$	5-V NLDMOS	75 mm/300 nm	V_{IN}
S_2	5-V NLDMOS	150 mm/300 nm	$2V_{OUT}$-V_{IN}
S_4	5-V NLDMOS	150 mm/300 nm	V_{OUT}
$S_{5,6}$	5-V NLDMOS	75 mm/300 nm	V_{IN}/V_{OUT}
S_H	5-V PMOS	5 mm/500 nm	V_{OUT}

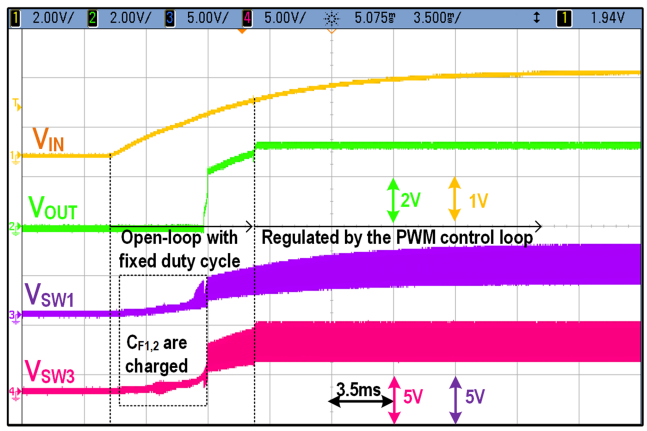


Fig. 19. Measured start-up process.

The measured start-up process is shown in Fig. 19, which indicates a safe start-up. As V_{IN} ramps up, the converter initially

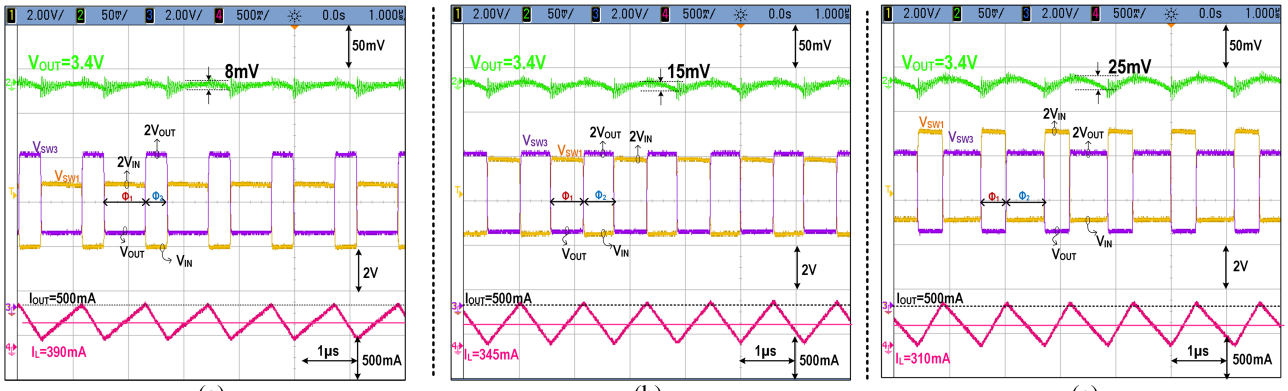


Fig. 20. Measured steady-state waveforms at $I_{\mathrm{OUT}} = 500$ mA. (a) $V_{\mathrm{IN}} = 2.7$ V. (b) $V_{\mathrm{IN}} = 3.4$ V. (c) $V_{\mathrm{IN}} = 4.2$ V.

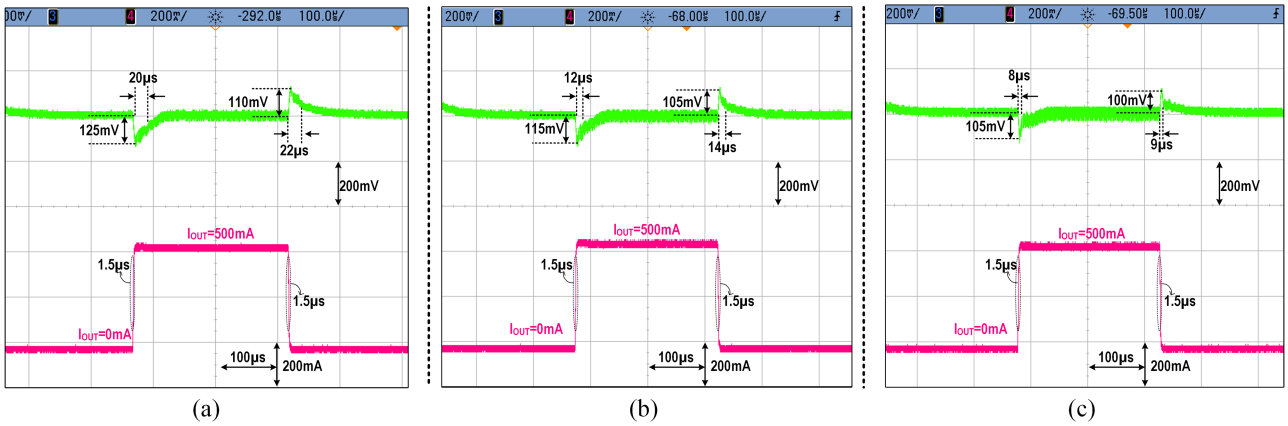


Fig. 21. Measured load transient responses with a load step of 500 mA. (a) $V_{\mathrm{IN}} = 2.7$ V. (b) $V_{\mathrm{IN}} = 3.4$ V. (c) $V_{\mathrm{IN}} = 4.2$ V.

operates in open-loop control with a fixed duty cycle, effectively mitigating the risk of unexpectedly large inrush currents on C_{F}s due to hard charging. As V_{OUT} progresses toward the target level, the converter transitions to PWM control loop regulation. It should be noted that when V_{IN} is below 0.7 V, all power switches are inactive. Once V_{IN} exceeds 0.7 V, the body diode of S_2 conducts, initiating the charging of C_{F1}, C_{F2}, and subsequently C_{OUT} via S_6. When V_{OUT} reaches approximately 2 V, S_2 and S_6, which are powered by V_{H} ($= 2V_{\mathrm{OUT}}$), are then able to switch normally.

Fig. 20 shows the measured steady state waveforms of V_{OUT}, $V_{\mathrm{SW1,3}}$, and I_L at different V_{IN} conditions. When $V_{\mathrm{IN}} = 2.7$ V, 3.4 V and 4.2 V, $I_{\mathrm{OUT}} = 500$ mA, the converter works in the same mode with small output voltage ripples (<1% of 3.4 V). The measured I_L values are 390 mA, 345 mA, 310 mA, respectively, which are always lower than I_{OUT}, resulting in a great reduction of conduction loss. Theoretically, the expected I_L values are 375 mA, 333 mA, and 302 mA, respectively. The observed discrepancies are attributed to the extended duty cycle resulting from losses in the nonideal switches and inductor.

The measured waveforms of load transient responses with a load step of 500 mA within 1.5 μs is shown in Fig. 21. Thanks to the continuous output current delivery, which alleviates the RHP zero effect, the under/overshoot is lower than 125 mV over the whole $\mathrm{V_{IN}}$ range in this design. When $\mathrm{V_{IN}} = 4.2$ V, the under/overshoot is only 100 mV/105 mV with 1% settling time of 8 μs/9 μs.

Fig. 22(a) shows the measured line transient responses of the proposed converter when V_{IN} changes from 4.2 V to 2.7 V or from 2.7 V to 4.2 V over a duration of 10 s. Fig. 22(b) presents a faster transition scenario with a 15 ms input voltage change. In both cases, unnoticeable voltage variation is observed on V_{OUT}, which indicates the seamless mode transition with the single-mode operation.

Fig. 23 presents the measured efficiency of the converter at various V_{IN} and I_{OUT} conditions. Two different inductors, are used to verify the performance of the converter. The peak efficiency reaches 97.3% using a bulky inductor with saturation current of 14 A (max. DCR = 18 mΩ). Thanks to the significantly reduced inductor current, even a compact inductor ($I_{sat} = 1.4$ A, max. DCR = 200 mΩ) is used, the peak efficiency remains at 96.4%.

Fig. 24 shows the estimated power loss breakdown at $V_{\mathrm{IN}} = 2.7$ V, $I_{\mathrm{OUT}} = 800$ mA with a DCR of 18 mΩ. It is evident that under heavy load conditions, conduction losses from power switches and bonding wires dominate the total power loss, thereby limiting overall efficiency. To improve heavy-load efficiency, increasing the area of power switches not only reduces

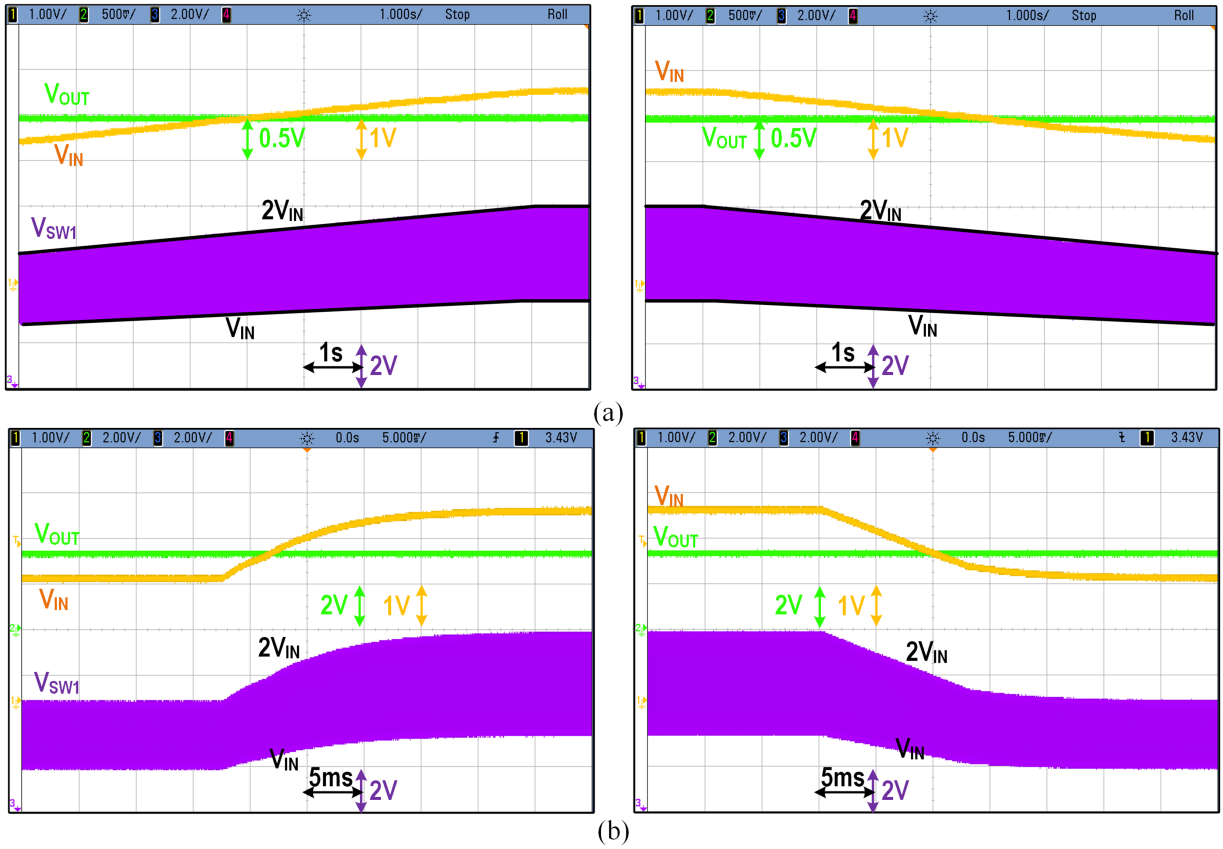


Fig. 22. Measured line transient responses when V_{IN} changes between 2.7 and 4.2 V with in (a) 10 s. (b) 15 ms.

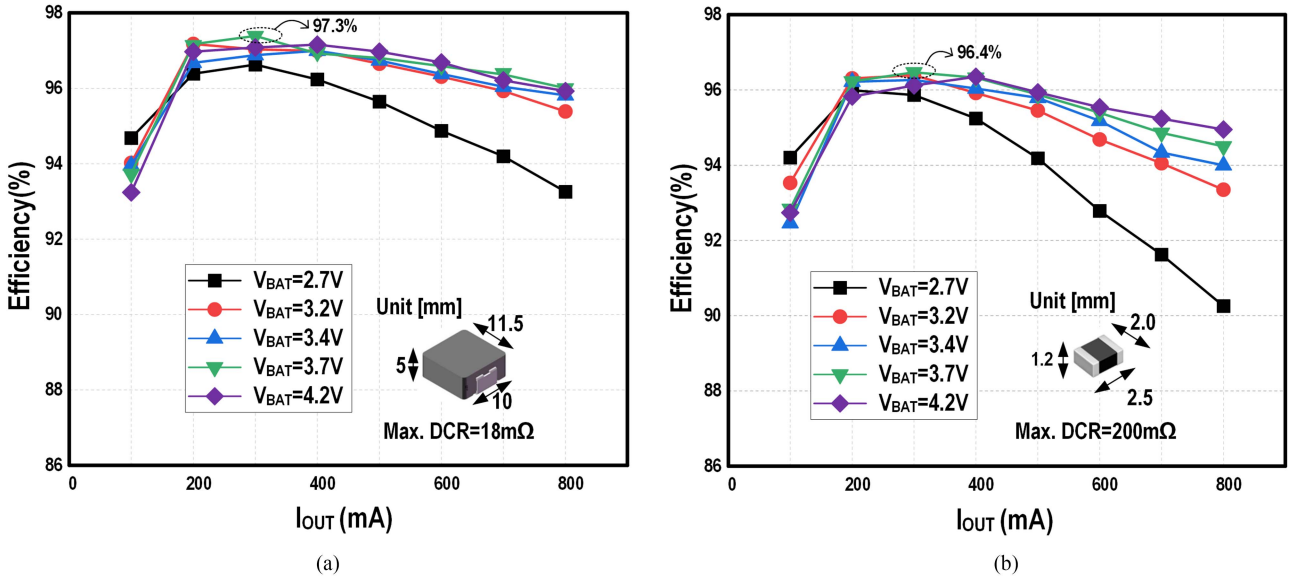


Fig. 23. Measured efficiency with (a) Bulky L. (b) Compact L.

conduction loss and balances gate driver loss of power switches, but also allows for the placement of more PADs. This, in turn, enables more gold bonding wires to be added, further mitigating conduction loss due to parasitic resistances.

Table III summarizes and compares the performance of the proposed converter with state-of-the-art designs. Unlike using high-voltage devices in [7], [14], and [15], the 5-V devices are used only in the proposed converter, so this design occupies the

TABLE III
PERFORMANCE SUMMARY AND COMPARISON

	Multi-Mode				Single-Mode									
Publication	**JSSC'25[10]**		**JSSC'25[13]**		**VLSI'21[14]**		**JSSC'23[15]**		**TPEL'23[17]**		**ISSCC'24[16]**		**This work**	
Technology	0.18-μm		0.18-μm		0.18-μm		0.18-μm		0.18-μm		0.18-μm		**0.18-μm**	
Typical V_{IN}	2.7—4.2 V		2.8—4.2 V		2.8—4.2 V		2.9—4.2 V		2.7—4.2 V		2.7—4.2 V		**2.7—4.2 V**	
Typical V_{OUT}	3.4 V		3.3 V		3.3 V		3.3 V		3.4 V		3.4 V		**3.4V**	
Voltage Conversion Ratio	(0.5,2)		(0.5,1.5)		(0.5, ∞)		(0.5,2)		(0.67,2)		(0.5,2)		**(0.5,2)**	
Load Range (PCE>90%)	0.1-2.5 A		0.05-1 A		0.2-1 A		0.2-1 A		0.02-0.7 A		0-1 A		**0.1-0.8 A**	
Switching Frequency	1 MHz		2 MHz		1 MHz		1 MHz		1 MHz		1 MHz		**1 MHz**	
Flying capacitor	4.7-μF		20 μF×2		10 μF		10 μF×2		10 μF×2		10 μF×2		**4.7 μF×2**	
Output capacitor	10-μF		10 μF		10 μF		4.7 μF		10 μF		10 μF		**10 μF**	
Inductor	2.2 μH		2.2 μH		4.7 μH		4.7 μH		4.7 μH		4.7 μH		**4.7 μH**	
I_L/I_{OUT}(Boost|Buck)	1	M<1	1		M$\in$(0.8,1.3)		(3−M)/3<1		M$\in$(0.8,1.3)		(M+1)/3<1		**(M+1)/3<1**	
I_{OUT} Step @ V_{IN}	500 mA@4.2 V		500 mA@4.2 V		550 mA@ 4.2V		500 mA@4.2 V		500 mA@4.2 V		1 A@4.2 V		**500 mA@4.2 V**	
*Undershoot|Overshoot	155 mV	150 mV	33 mV	26 mV	350 mV	320 mV	320 mV	350 mV	400 mV	400 mV	240 mV	280 mV	**105 mV**	**100 mV**
Recovery Time	23 μs	23 μs	30 μs	17 μs	150 μs	100 μs	60 μs	60 μs	N/A	N/A	40 μs	40 μs	**8 μs**	**9 μs**
Max. V_{DS} of Switch	V_{IN} (4.2 V)		V_{IN}/2(2.1 V)		2V_{OUT} (6.6 V)		3V_{IN}−V_{OUT} (9.3 V)		V_{OUT}/2 (1.7 V)		V_{IN} (4.2 V)		**V_{IN} (4.2 V)**	
*Chip area	2.23 mm^2		2.79 mm^2		8.26 mm^2		5.85 mm^2		6.25 mm^2		3.2 mm^2		**1.12 mm^2**	
**On-die current density	1.12 A/mm^2		0.36 A/mm^2		0.12 A/mm^2		0.17 A/mm^2		0.11 A/mm^2		0.31 A/mm^2		**0.71 A/mm^2**	
*Peak Efficiency /DCR	98.6% 9 mΩ	97.3% 170 mΩ	98.2% 8.5 mΩ	97.2% 110 mΩ	96.6% N/A		96.1% 19 mΩ	94.8% 175 mΩ	96.48% 98 mΩ	95.63% 288 mΩ	96.9% 9 mΩ	95.5% 250 mΩ	**97.3% 18 mΩ**	**96.4% 200 mΩ**
V_{CF}(Boost|Buck)	V_{OUT} −V_{IN}	V_{OUT}	V_{IN}/2		V_{OUT}		V_{CF1}=V_{IN}, V_{CF2}=2V_{IN}−V_{OUT}		V_{CF1}=V_{OUT}/2 V_{CF2}=V_{OUT}/2		V_{CF1}=V_{IN}, V_{CF2}=V_{OUT}		**V_{CF1}=V_{IN}, V_{CF2}=V_{OUT}**	
Mode Transition	Discontinuous V_{CF}		Discontinuous duty		Not Required		Not Required		Not Required		Not Required		**Not Required**	

* Estimated from the paper ** On-die current density = $I_{OUT.max}$ / Chip area

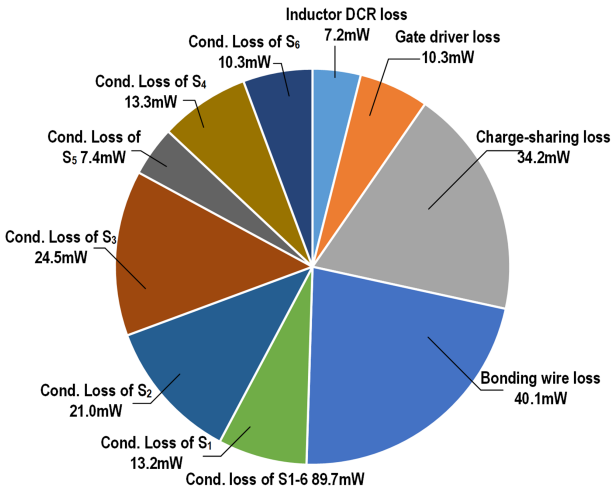


Fig. 24. Estimated power loss breakdown at $V_{IN} = 2.7$ V, $I_{OUT} = 800$ mA using a bulky inductor with DCR = 18 mΩ.

smallest active area of 1.12 mm^2. Thanks to the always-dual-path operation, the I_L is much lower than that in [10], [13], [19], and [14] and comparable to [15] and [17]. The measurement results demonstrate that whether a bulky or compact inductor is used, the converter outperforms other work with single-mode operation both in efficiency and on-die current density, which is attributed to superior performance of the 5-V NLDMOS devices used in this work compared to the high-voltage-devices utilized in [10] and [11], and 5-V CMOS devices used in [16]. Compared to other multimode converters, the efficiency and on-die current density of this design is the second only to that of the structures in [10] and [13], both of which have mode transition issues. Additionally, this work also exhibits smaller under/overshoot and achieves a quicker recovery time, demonstrating fast transient response.

V. CONCLUSION

In this article, a battery-to-3.4-V single-mode buck–boost converter is proposed for seamless mode transition without complex control circuits. Featuring the always-dual-path operation, I_L is reduced to less than I_{OUT} over entire battery voltage range. Although six switches and 2-C_Fs are used, the optimized SSL and FSL losses are studied and compared with other works, indicating that this converter can achieve the best active and passive components utilization owing to the relaxed burden of current stress of inductor and voltage stress of power switches, thus, the highest peak-efficiency with the smallest die size among single-mode buck–boost converters. Experimental results verify the effectiveness of the proposed converter. Moreover, the RHP zero effect is alleviated due to the continuous output current delivery, leading to fast transient responses.

While the proposed structure offers clear benefits in efficiency, size, and dynamic performance, it also presents tradeoffs, including increased gate driver complexity, more OFF-chip interconnections due to external flying capacitors, and a narrower voltage conversion range. These limitations should be weighed in practical applications, though the overall performance makes the converter a strong candidate for battery-powered portable electronics.

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