A Modular Commutated Converter With DC Fault Ride-Through Capability for Overhead-Line-Based VSC-HVDC Application

Ruihang Bai, *Graduate Student Member, IEEE*, Biao Zhao, *Senior Member, IEEE*, Xueyin Zhang, Lin Wang, *Graduate Student Member, IEEE*, Zhanqing Yu, *Member, IEEE*, Qiang Song, *Senior Member, IEEE*, and Rong Zeng, *Senior Member, IEEE*

***Abstract*—VSC-HVDC systems based on overhead transmission lines suffer from transient dc short-circuit faults frequently, for which converters with dc-fault ride-through (DC-FRT) capability are required. This article proposes a hybrid modular commutated converter (H-MCC) with DC-FRT capability. H-MCC applies a hybrid dc switch to isolate fault lines and adopts an energy-absorption branch to facilitate rapid arc quenching. The control sequences and dynamic process of H-MCC during DC-FRT are analyzed in detail, deducing the analytical model of electrical stress. On this basis, the parameter design methodology is presented, and a comprehensive comparison with the conventional hybrid MMC scheme shows that the proposed H-MCC achieves notable improvements in power density, cost-effectiveness, and operational efficiency. Finally, the feasibility of H-MCC is verified by simulation and experiment. The proposal offers a technically and economically attractive solution for power conversion in overhead-line-based VSC-HVDC systems.**

***Index Terms*—Arc mitigation, dc-fault ride-through (DC-FRT), hybrid dc switch, modular commutated converters (MCC), overhead line-based dc transmission.**

I. Introduction

VOLTAGE source converter (VSC)-based high-voltage direct current (HVDC) has a rapidly-growing installed capacity in scenarios such as off-shore wind farm, long-distance power transmission, and multiport dc-grid forming [1], [2], [3]. Modular multilevel converter (MMC) has been widely used in VSC-HVDC for its high efficiency, reliability and easy scalability [4], [5]. Nevertheless, MMC faces limitations in technical economy due to high cost and large physical footprint [6].

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Ruihang Bai, Biao Zhao, Lin Wang, Zhanqing Yu, Qiang Song, and Rong Zeng are with the Department of Electrical Engineering, Tsinghua University, Beijing 100084, China (e-mail: brh20@mails.tsinghua.edu.cn; zhao-biao@tsinghua.edu.cn; l-wang23@mails.tsinghua.edu.cn; yzq@tsinghua.edu.cn; songqiang@tsinghua.edu.cn; zengrong@tsinghua.edu.cn).

Xueyin Zhang is with Tsinghua Sichuan Energy Internet Research Institute, Chengdu 610213, China (e-mail: zhangxueyin@tsinghua-eiri.org).

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In comparison, the modular commutated converter (MCC) brings significant technical benefit. For example, MCC reduces the required support capacitance by more than 70% and the number of fully controlled devices by nearly 20%. These reductions enable 50% optimization in the overall converter footprint and about 30% reduction in total cost [7], [8]. Moreover, the zero-voltage switching characteristics of the commutation bridges in MCC not only optimize the operational power loss by around 20%, but also allow full utilization of the high surge-current capability of integrated gate-commutated thyristors (IGCTs) to enable high-overload operation without a significant increase in the number of power devices, thereby enhancing the capability to provide reactive power support during ac short-circuit faults and improving the robustness of power systems with high penetration of power electronics [9]. Therefore, it represents a feasible and competitive option for VSC-HVDC deployment.

In HVDC applications, protecting the converter and the system during dc short-circuit faults is essential. A half-bridge submodule (HBSM)-based MMC utilizes diodes with higher rated current to handle the surge fault current arising from uncontrolled rectification [10] or bypassing the current by thyristors [11] before opening the ac circuit breaker. These methods prevent damage of the converter with the minimum additional cost, while also leading to long recovery time due to the natural decay of the fault current, during which the converter is out of service and unable to transmit power.

When HVDC systems adopt overhead transmission line or connects to weak ac grid, it is considered valuable to clear the dc fault actively and compensate reactive power to the ac grid during the fault for higher robustness [12], [13]. To this end, the dc-fault ride-through (DC-FRT) techniques of MMC have been widely researched, in which numerous evolved topologies of MMC are proposed and implemented, such as full-bridge submodules (FBSM), hybrid submodules, and clamp-double submodules [14], [15], [16]. They can decouple the control of ac side and the dc side, making it possible to output a negative dc voltage to accelerate the decay of fault current, meanwhile keeping the static-synchronous-compensator (STATCOM) operation toward the ac grid [17], [18]. However, not only do these schemes significantly increase the quantity of devices with additional cost, the current will also flow through more power-electronics

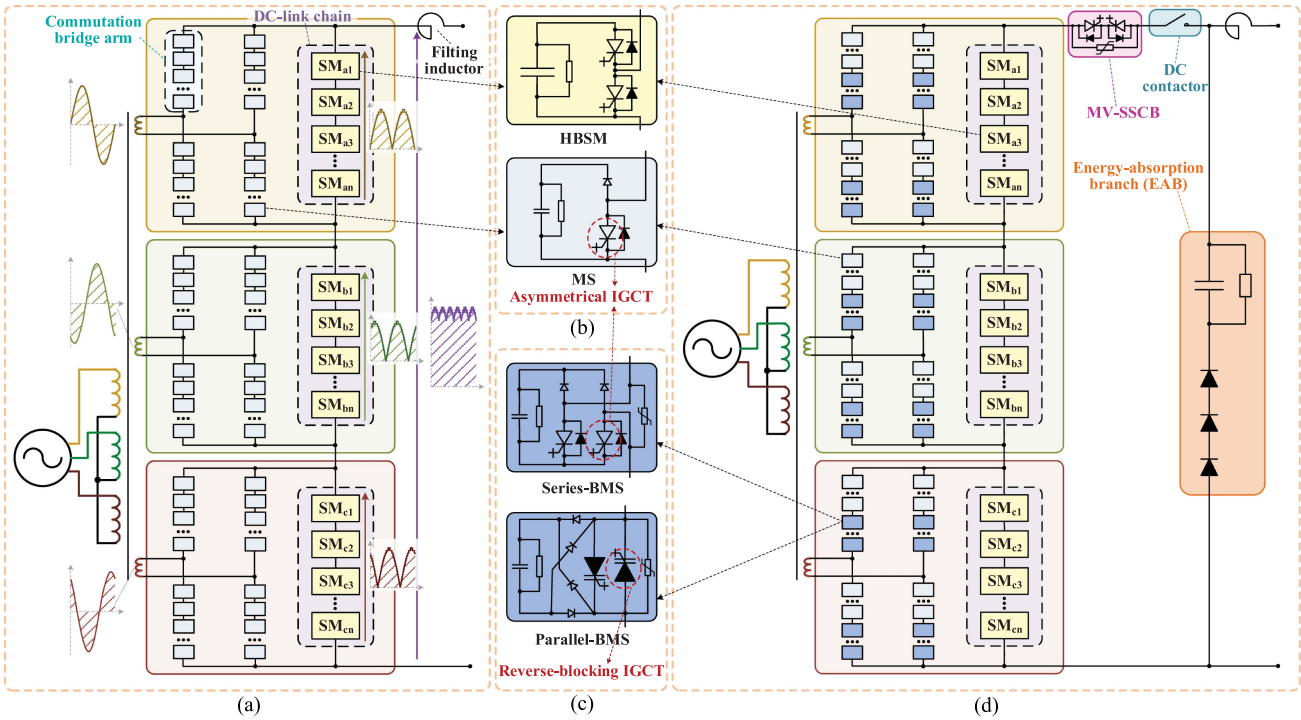

Fig. 1. (a) Topology of a conventional MCC. (b) Half-bridge submodules (HBSM) and modular switches (MS) in the MCC. (c) Bidirectional-blocking MSs (BMS) with RC-IGCTs and RB-IGCTs. (d) Topology of the proposed H-MCC.

devices, resulting in higher energy losses. A high-voltage dc circuit breaker (DCCB) can also interrupt the dc fault current. Nevertheless, a solid state DCCB causes high conduction power loss, while a hybrid DCCB has a huge size. Moreover, both types of DCCBs involve considerable capital cost [19], [20], [21].

To address the aforementioned challenges, this article proposes a hybrid-MCC (H-MCC). It employs bidirectional modular switches (BMSs) capable of rapidly blocking the uncontrolled rectification effect, and incorporates both a hybrid dc switch and a dedicated energy-absorption branch (EAB) in the main circuit to handle DC faults [22]. In this way, the proposal achieves DC-FRT capability while maintaining favorable techno-economic performance.

The remainder of this article is organized as follows: Section II proposes the topology of H-MCC, as well as an enhanced parallel-bidirectional modular switch. Section III analyzes the operation principle of the proposal during DC-FRT in detail, focusing on its control sequence and commutation process. Then, in Section IV, the parameter-design method of H-MCC is demonstrated, and a design example is provided. Section V characterizes the H-MCC and quantitatively presents its performance. Section VI verifies the DC-FRT capability of the proposal by both simulation and experiment. Finally, Section VII concludes this article.

II. Topology of the H-MCC

A. Topology of the Conventional MCC

The topology of a conventional MCC is shown in Fig. 1(a) [7]. In each phase, several series-connected HBSM form a dc-link chain and generate rectified sinusoid voltage. Each of the four commutation bridge arms is composed of reverse-conducting fully-controlled devices in series. They alternately switch at the fundamental frequency to flip the rectified sinusoid in half of each cycle into an ac voltage.

The dc-link chains of the three phases connect in series directly to form a public dc port, which outputs a pulsed dc voltage. The dc port then connects to the dc system through a filter inductor. At the ac side, a converter transformer realizes interphase electrical isolation and grid connection.

The commutation bridges only switch at the zero-crossings of the sinusoid voltage. Therefore, the devices in the commutation bridges exhibit excellent zero-voltage switching (ZVS) characteristics, where switching losses are negligible and conduction losses dominate total power loss. IGCTs are well-suited for efficiency optimization due to their low on-state voltage. Applying modular switches (MSs) instead of monolithic IGCTs will further benefit the voltage sharing and floating supply, as in Fig. 1(b) [8].

B. Proposed H-MCC

Building on the conventional MCC, the proposed H-MCC topology is illustrated in Fig. 1(d). Half of the MSs in each commutation bridge arm are replaced with BMSs, which can bidirectionally conduct and block to temporarily isolate the ac- and dc-side during the DC-FRT and avoid the uncontrolled rectification effect.

A BMS can be composed of two reverse-conducting IGCTs (RC-IGCTs, each equivalent to an asymmetrical IGCT in

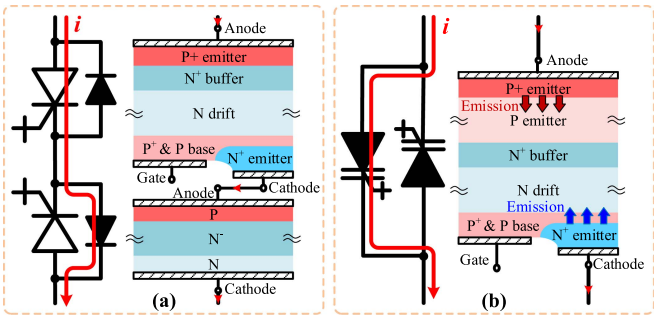

Fig. 2. Conduction path in BMSs. (a) Series-BMS. (b) Parallel-BMS.

parallel with a free-wheeling diode) connected in anti-series, together with some auxiliary components. This configuration is referred to as "series-BMS," as shown in Fig. 1(c). Each BMS also contains a metal-oxide varistor (MOV) to dissipate the energy stored in the ac-side inductors when the arm blocks.

A hybrid dc switch consisting a medium-voltage solid-state current breaker (MV-SSCB) and a fast dc contactor is set between the dc port of MCC and the filter inductor. The MV-SSCB quickly breaks the fault current once it is detected, after which the contactor opens immediately to isolate the faulted dc lines from the converter. An EAB, which consists of a capacitor, a resistor and a series of diodes, is used to absorb and dissipate the energy stored in the filter inductor and the dc lines. They also constitute an LC second-order circuit, which accelerates the arc-quenching of the fault point.

C. Enhanced Parallel-BMS

In a series-BMSs, the conducted current flows through not only an IGCT, but also a diode, which inevitably introduces additional conduction loss, as illustrated in Fig. 2(a). To further improve efficiency, an enhanced parallel-BMS is proposed, as shown in Fig. 1(c). It consists of two reverse-blocking IGCTs (RB-IGCTs) connected in anti-parallel.

In an RB-IGCT, a low-doped deep p-emitter layer is added beneath the high-doped shallow one at the anode side to withstand a high reverse-bias voltage of the anode [see Fig. 2(b)] [23]. Benefiting from the bidirectional conductance modulation effect, the carrier concentration of the additional layer is high in the conduction mode since both the anode emitter and the cathode emitter emit plenty of carriers to the body. Therefore, the conduction voltage drop of the RB-IGCT is only little increased than a common asymmetrical IGCT, and thus the H-MCC based on the parallel-BMS will be able to operate with higher efficiency, similar to a conventional MCC.

D. Operation of the H-MCC Under Normal Conditions

Under normal operating conditions, the additional reverse-blocking or reverse-conducting devices in all BMSs are kept turned ON, making the switching behavior and control strategy of the BMS identical to those of a conventional MS. Besides, the hybrid dc switch remains closed under normal conditions, functioning equivalently as a conductor and thus having no impact on the MCC operation.

Therefore, the proposed H-MCC shares the same operating principle and control strategy as a conventional MCC during normal operation.

III. Operation Principle of the H-MCC During DC-FRT

A. Overview of the DC-FRT Sequences

The whole DC-FRT process of the proposed converter is shown in Fig. 3. When a dc short-circuit fault is detected by a criterion of over-current, under-voltage, or derivate of dc-line current [24], all the submodules in the dc-link chains are switched out (by turning OFF the upper transistor and turning ON the lower transistor) to output zero voltage, and all the BMSs in the commutation bridges are blocked. Then, the MV-SSCB breaks, after which the dc contactor opens to physically isolate the converter from the faulty transmission line.

Once the contactor has been fully opened and established dielectric strength, the MCC can be deblocked to resume the operation toward the ac grid as a STATCOM. Meanwhile, the distributed inductor of the dc transmission line and the filter inductor charge the capacitor of the EAB, forming a second-order circuit and accelerating the decay of the fault current until a zero-crossing to quench the fault arc.

After plenty of fault-point deionization time, the dc transmission line is able to withstand the voltage again. The contactor is then closed and the MCC is controlled to recover the active-power transmission. Thus, a DC-FRT is achieved.

In the rectifier mode, the dc fault current has the same direction as the dc load current, for which the dc inductor stores more energy and thus makes the DC-FRT harder. Therefore, the following analyses are based on this mode.

B. Converter Blocking

Once a dc short-circuit fault occurs, all the HBSMs of the dc-link chain are switched out to output a zero voltage and provide a soft breaking condition for the MV-SSCB. Meanwhile, the commutation bridges are bidirectionally blocked by turning off the IGCTs in the BMSs to prevent a worse fault current injection from the ac grid. Because of the delay of the control link, these two actions cannot be taken concurrently. Here we discuss the influence of their sequence. One phase unit is taken as an example to simplify the analysis.

Assuming that H_1 and H_3 arms are in conduction mode, as in Fig. 4(a), in which L_{AC} is the equivalent ac inductance and L_{sH} is the stray inductance. The switching devices in the figure are marked in red and black to denote the off-state and on-state, respectively. If all the MSs (both conventional and bidirectional ones) of the commutation arms are blocked, as shown in Fig. 4(b), the current in the conducting BMSs will transfer to the MOVs due to the freewheeling of the stray inductance, resulting in a residual voltage across them. This voltage is superimposed on the voltage of the dc-link chain and collectively applied to the H_2 and H_4 arms, which will cause the asymmetrical MSs to break down.

On the other hand, if only the BMSs are blocked first, the current will also transfer to their paralleled MOVs [see Fig. 4(c)].

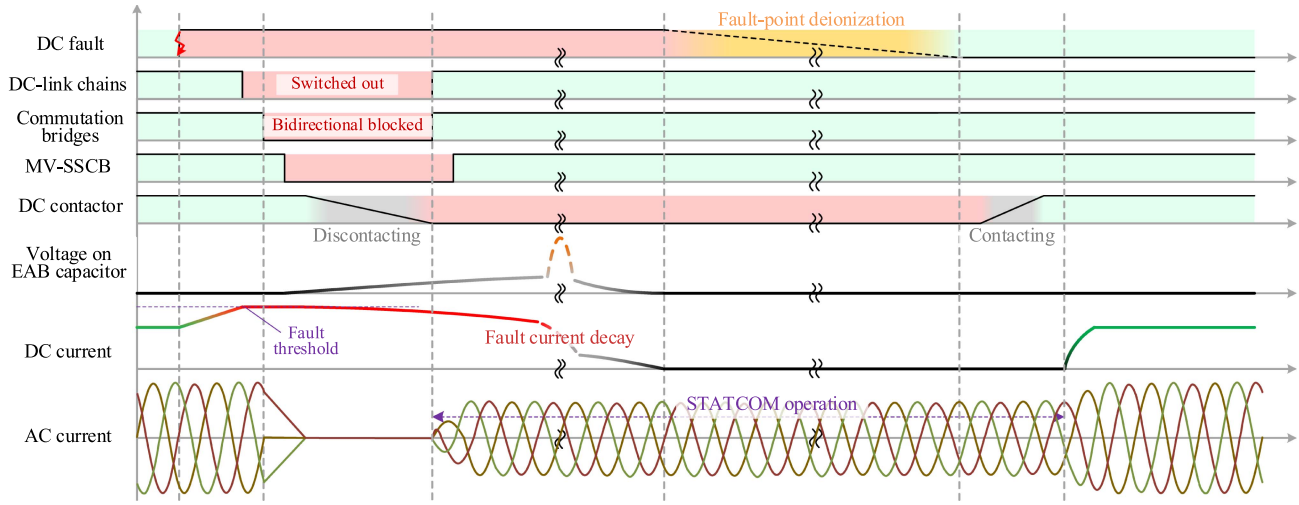

Fig. 3. DC-FRT process of the proposed MCC.

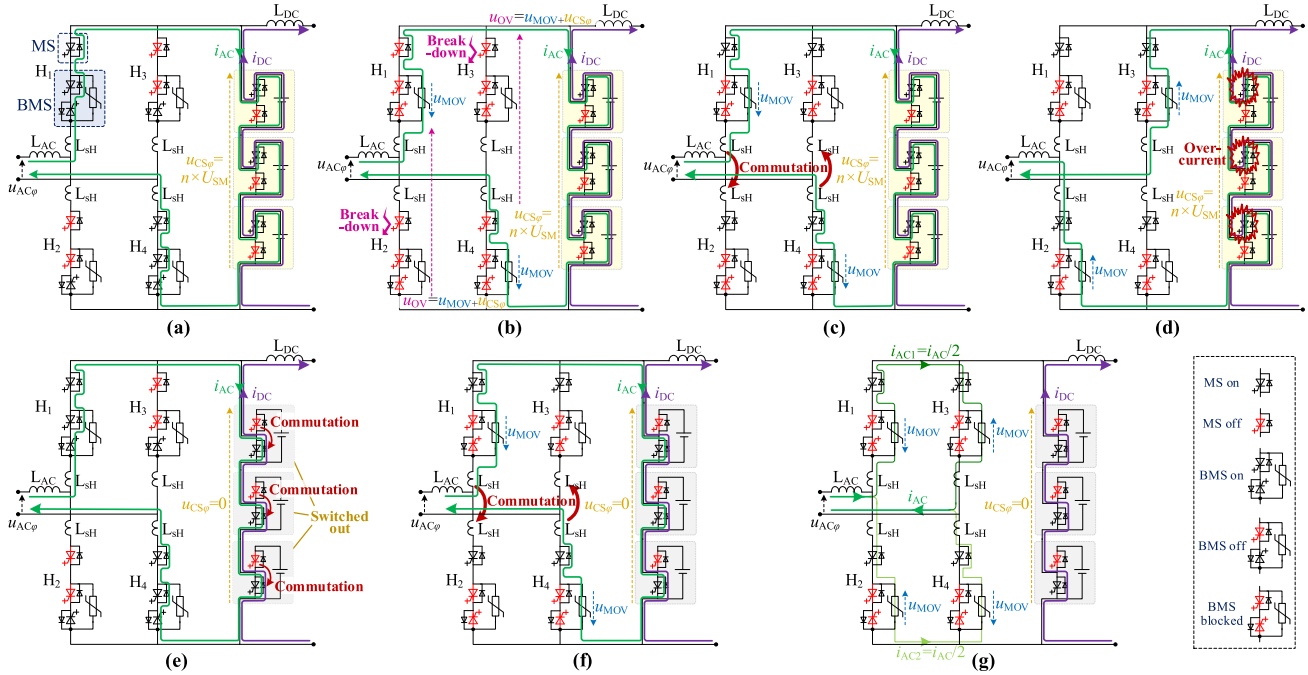

Fig. 4. Analysis of converter-blocking process. (a) Initial state. (b) Blocking all the MSs in the commutation arms causes a breakdown. (c) Only the BMSs are blocked. (d) Reversed AC-current component causes an overcurrent on the DC-link chain. (e) Switching out the HBSMs of the DC-link chain. (f) Commutation bridge arms are bidirectionally blocked under zero bus voltage. (g) Balanced current distribution among the four commutation bridge arms.

Noting the stray inductance L_{sH} is very low, the current then rapidly commutates to the opposite H_2 and H_4 arms under the coupling of the dc-link-chain voltage. From the view of the dc-link chain, it means its ac-component current is reversed, as in Fig. 4(d). The process above leads to two problems. First, the energy stored in the ac inductance will be concentratedly dissipated on the MOVs of H_2 and H_4 arms, which brings them high transient thermal stress. Second, the dc-component current and reversed ac-component current are superimposed, which is too high for the switching devices in the HBSMs to turn OFF.

Otherwise, if the HBSMs of the dc-link chain are switched out first, they will output a zero voltage [see Fig. 4(e)]. Then when the commutation bridges are bidirectionally blocked, the voltage on MOVs causes an inter-arm commutation until reaching a balanced current distribution between the two pairs of commutation bridge arms, as in Fig. 4(f) and (g). The energy of the ac inductance is dissipated evenly on the MOVs of the four commutation bridge arms till the ac current decays to zero.

The latter scheme has obvious advantage. Therefore, the HBSMs of dc-link chain should be switched out before the commutation bridge blocks. It is also worth noting that the commutation bridge arms located diagonally always share the ac voltage, which is equivalent to a series connection. Hence, it

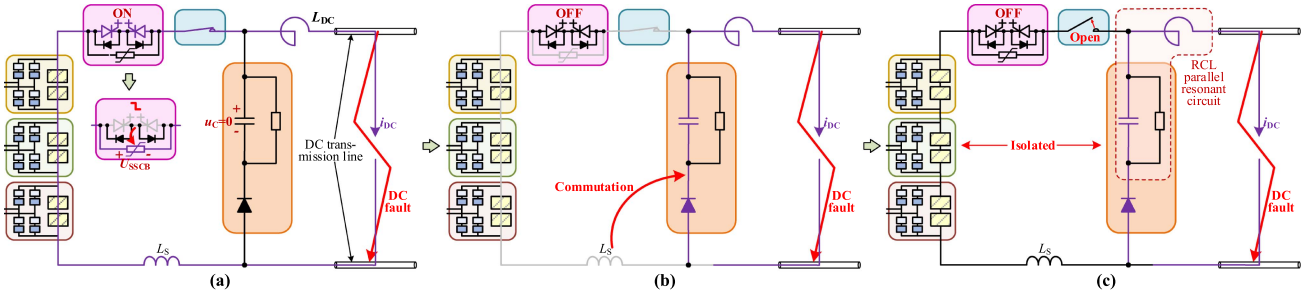

Fig. 5. DC-breaking process. (a) MV-SSCB breaks in zero voltage and its current transfers to the snubber. (b) The voltage on MV-SSCB causes a commutation towards the EAB. (c) DC contactor opens with zero current to isolate the converter from the fault part.

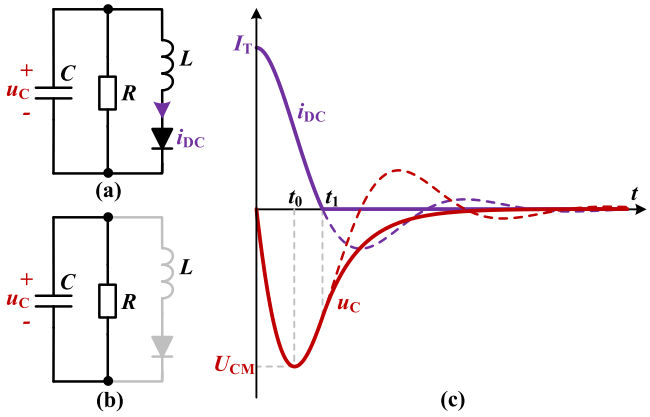

Fig. 6. Equivalent circuit of EAB and DC-side inductor. (a) Before the diode cuts off. (b) After the diode cuts off. (c) Diagram of the electrical quantities. The dotted lines show the situation without the diode.

is enough for fault blocking only to replace half of the MSs with BMSs in each arm.

C. DC Breaking

The MV-SSCB consist of bidirectional power-semiconductor devices and snubbers (such as RC circuit or MOVs) in paralleled connection. When the power-semiconductor devices turn OFF, their current transfers to the snubbers, as in Fig. 5(a). Since the voltages of dc-link chain output and the EAB capacitor are both zero, the MV-SSCB is zero-voltage breaking, for which the voltage on the snubbers (U_{SSCB}) is applied to the stray inductance (L_{S} in Fig. 5) and forces its current to transfer to the EAB [see Fig. 5(b)] with the rapid speed of [25]

$$\frac{di_{\mathrm{DC}}}{dt} = \frac{U_{\mathrm{SSCB}}}{L_S}. \tag{1}$$

The dc contactor does not open until the commutating is finished. It means the contactor is zero-current opened and brings two benefits. On one hand, the contactor will not need to quench the dc arc, avoiding the technical bottleneck of dc-current breaking and significantly saving its cost and size [26]. On the other hand, it will be easy to realize a fast opening within 2 μs by forming this high-voltage contactor with a series connection of several mechanical contacts, each of which has a lower gap, without worrying of their dynamic voltage sharing [27], [28].

When the contactor is fully opened and establishes dielectric strength, it realizes a physical isolation between the fault dc line (including the EAB) and the MCC, as in Fig. 5(c). The present voltage of the EAB capacitor will be the maximum voltage on MV-SSCB, as in (8). the MCC is permitted to deblock, which then operates in STATCOM mode to inject reactive power to the ac grid.

From an energy perspective, the energy stored in the stray inductance of the loop comprising the cascaded module chain, the capacitor and diode of the EAB, and the hybrid dc switch will be dissipated in the snubber of the MV-SSCB during the dc breaking process. Therefore, the physical length and enclosed area of this loop should be minimized in structural design to reduce stray inductance and consequently lower the snubber requirements of the MV-SSCB.

D. Fault Current Decay and Fault Point Recovery

Fig. 5(c) indicates that the distributed inductor of the dc transmission line and the filter inductor (L) form an RCL parallel resonant circuit with the capacitor (C) and resistor (R) of the EAB, as in Fig. 6(a). Its analytic expression is as follows:

$$\begin{cases} -i_{\mathrm{DC}} - \frac{u_{\mathrm{C}}}{R} = C\frac{\mathrm{d}u_{\mathrm{C}}}{\mathrm{d}t} \\ u_{\mathrm{C}} = L\frac{\mathrm{d}i_{\mathrm{DC}}}{\mathrm{d}t} \end{cases} \tag{2}$$

which can be simplified as follows:

$$LC\frac{d^2 i_{\mathrm{DC}}}{dt^2} + \frac{L}{R}\frac{di_{\mathrm{DC}}}{dt} + i_{\mathrm{DC}} = 0. \tag{3}$$

The circuit ought to be designed to be underdamped to accelerate the decay of the fault current

$$R > \frac{1}{2}\sqrt{\frac{L}{C}}. \tag{4}$$

According to the initial conditions

$$\begin{cases} i_{\mathrm{DC}}(0) = I_{\mathrm{T}} \\ u_{\mathrm{C}}(0) = 0 \end{cases} \tag{5}$$

where I_{T} refers to the overcurrent threshold of the dc side, the solution to (3) is

$$\begin{cases} i_{\mathrm{DC}} = \frac{I_{\mathrm{T}}}{\sqrt{LC}\omega} e^{-\frac{t}{2RC}} \sin(\omega t + \theta) \\ u_{\mathrm{C}} = \sqrt{\frac{L}{C}}\frac{I_{\mathrm{T}}}{\omega} e^{-\frac{t}{2RC}} \left[\omega\cos(\omega t + \theta) - \frac{1}{2RC}\sin(\omega t + \theta)\right] \end{cases}, \tag{6}$$

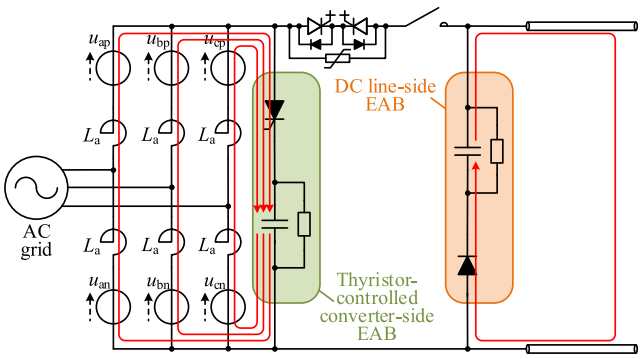

Fig. 7. Configuration of EABs in an MMC for DC-FRT.

in which ω and θ are as follows:

$$\begin{cases} \omega = \sqrt{\frac{1}{LC} - \frac{1}{4R^2C^2}} \\ \theta = \arccos\left(\frac{1}{2R}\sqrt{\frac{L}{C}}\right) \end{cases}. \tag{7}$$

Denoting the opening time as t_{OP}, the maximum voltage on MV-SSCB is as follows:

$$U_{\mathrm{SSCBM}} = u_C\left(t_{\mathrm{OP}}\right). \tag{8}$$

Then the capacitor reaches its maximum voltage (U_{CM}) at t_0 when its current is zero, as are expressed in the following:

$$U_{\mathrm{CM}} = u_{\mathrm{C}}\left(t_0\right), \tag{9}$$

$$i_{\mathrm{DC}}\left(t_0\right) + u_{\mathrm{C}}\left(t_0\right)/R = 0 \tag{10}$$

and the maximum energy storage of the capacitor follows:

$$E_{C\max} = C{U_{\mathrm{CM}}}^2/2. \tag{11}$$

According to (6), the time when the fault current decays to zero (t_1) satisfies that the value within the sin function is equal to π

$$t_1 = \frac{\pi - \theta}{\omega}. \tag{12}$$

At this moment, the EAB diode cuts off, after which the capacitor discharges to the resistor as a first-order circuit with the time constant of τ [see Fig. 6(b)

$$\tau = RC. \tag{13}$$

Meanwhile, the fault arc quenches, and the fault point will recover after the deionization time of hundreds of milliseconds. Then, the dc contactor can be reclosed and the transmission of active power can be resumed.

In the whole process, the energy dissipated on the resistor can be expresses as follows:

$$E_R = \int_0^{t_1+5\tau} \frac{u_C^2\left(t\right)}{R} dt. \tag{14}$$

E. Particularity of the Proposal in MCC

Arm inductors exist inside the MMCs, and their current contains both ac and dc component. It leads to the necessity of an extra thyristor-controlled EAB (see Fig. 7) at the converter side, which increases the complexity and the cost. Conversely, inside the MCC there are only low stray inductors, the current of which decays rapidly during the dc-breaking.

Besides, unlike the MCC using BMSs to block the AC side during the fault, MMC either adopts FBSMs in place of half of the HBSMs to output negative voltage, or uses bypass thyristors to short-circuit the AC grid in order to decouple the AC grid and the converter during the DC-FRT [29]. The former leads to extra cost and power loss due to the additional IGBTs, while the latter causes a violent impulse to the ac grid. Considering these factors, the proposal has particular technological benefits in the application of MCC topology.

IV. Parameter Design Guidelines for H-MCC

A. Considerations in Parameter Design

The following factors need to be considered in parameter design of H-MCC.

1) U_{SSCBM} shown in (8) determines the rated voltage of MV-SSCB. Since the main branch of MV-SSCB consists of series-connected power-semiconductor devices, a lower U_{SSCBM} value of contributes to reduce the cost as well as the conduction loss.
2) As U_{CM} in (9) is directly applied between the positive and negative poles of the dc system, its value should be limited to no more than the rated dc bus voltage to prevent insulation damage to the system. Besides, the maximum voltage on dc contactor is the sum of U_{CM} and rated dc voltage (since the converter operates in STATCOM mode), so a lower U_{CM} leads to lower specification of dc contactor.
3) The fall time of fault current [t_1 in (12)] should be short, in order to accelerate the recovery of faults. However, considering the deionization of fault point takes hundreds of milliseconds, there is no need to be overly restrictive about the recovery time.
4) The discharge time of EAB capacitor [t_1 plus five times τ in (13)] should be approximately equal to the deionization time to enable the DC-FRT process once again if the fault remains in reclose.
5) The maximum energy storage of EAB capacitor [E_{Cmax} in (11)] and the total energy dissipation on resistor [E_{R} in (14)] should both be as low as possible to reduce the size and cost of both these two devices.

According to the analysis in Section III, the factors above are implicitly affected by the rated parameters of the system, inductance of dc line, as well as the resistance and capacitance of EAB. Therefore, the optimal design of R and C parameters can be obtained by numerical solution, considering the performance demand of system and marginal costs of the components in specific applications.

B. Sensitivity Analysis of EAB Parameters

Parameters of the proposal are designed on the basis of a ±500 kV/3000 MW VSC-HVDC system shown in Table I. As the extrema and zero-crossing points of a second-order differential equation are difficult to obtain in analytical form, the effects

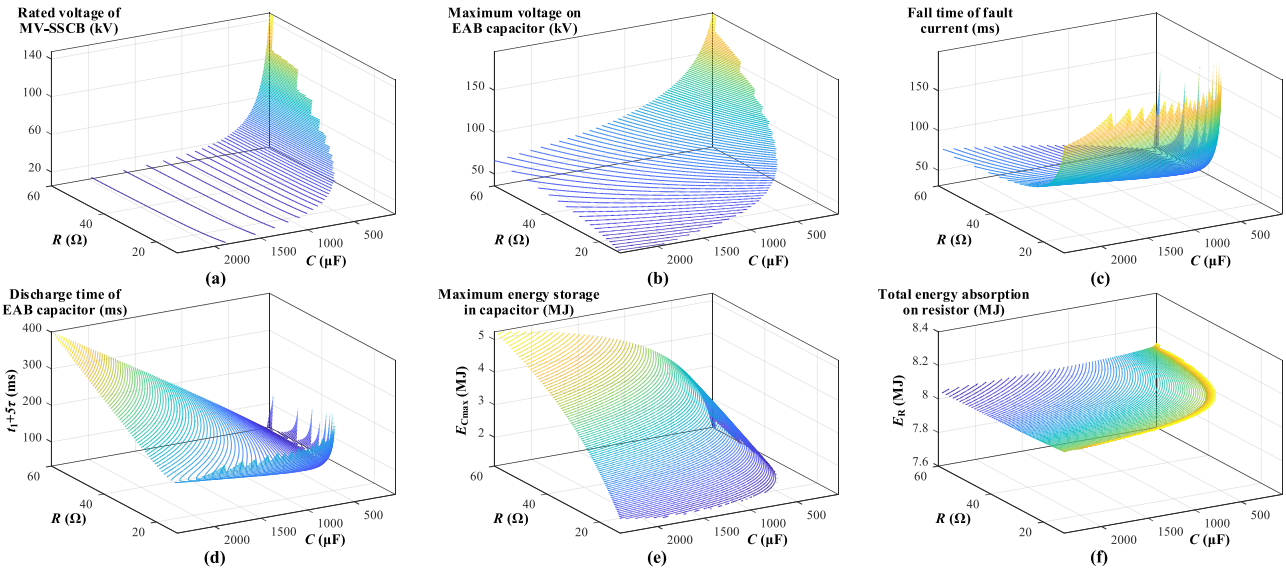

Fig. 8. Sensitivity analysis of key parameters in H-MCC to the R and C value. (a) Rated voltage of MV-SSCB. (b) Maximum voltage on EAB capacitor. (c) Fall time of fault current. (d) Discharge time of EAB capacitor. (e) Maximum energy storage in capacitor. (f) Total energy dissipation on resistor.

TABLE I
PARAMETERS OF THE VSC-HVDC SYSTEM FOR DESIGNING

Item	Parameter
Rated dc voltage	±500 kV
Rated ac voltage	580 kV
Rated active power	3000 MW
Rated power factor angle	9.5°
Ac link inductance	0.15pu (53 mH)
Dc filter inductance	150 mH
Dc line inductance	650 mH
Dc over-current threshold	1.5pu (4500 A)

TABLE II
DESIGN RESULT AND KEY CHARACTERISTICS OF THE H-MCC EXAMPLE

Item	Parameter
EAB resistor (R)	50 Ω
EAB capacitor (C)	450 μF
Rated voltage of MV-SSCB (U_{SSCBM})	27.9 kV
Maximum voltage on EAB capacitor (U_{CM})	111.9 kV
Rated voltage of dc contactor	1111.9 kV
Fall time of fault current (t_1)	42.0 ms
Discharge time of EAB capacitor (t_1+5τ)	84.7 ms
Maximum energy storage in capacitor (E_{Cmax})	2.878 MJ
Total energy dissipation on resistor (E_{R})	8.072 MJ

of R and C values of EAB on key parameters of H-MCC are evaluated through a parameter sweep, as illustrated in Fig. 8.

The resistor dissipates little energy before the dc contactor opens since the open time is very short, so the rated voltage of MV-SSCB is almost exclusively affected by C and decreases with its rising. U_{CM}, on the other hand, increases with the rise of R and the fall of C, while it is always far lower than the rated dc voltage, for which it is not considered a tight constraint.

The times of fault-current falling and EAB-capacitor discharging are also affected by both R and C. The former is determined by the damping coefficient of the second-order circuit, while the latter depends on the time constant of the first-order circuit. The maximum energy storage of capacitor increases with both R and C, but the total energy dissipation on resistor is little varied since it is approximately equal to the energy in dc inductor.

C. Design Example

The parameters are optimally designed by weighing all the abovementioned restrictions. The detailed results are shown in Table II.

V. PERFORMANCE ANALYSIS OF H-MCC

A. Valve

The performance of the proposed H-MCC valve is theoretically analyzed and compared with that of hybrid MMC scheme (60% of full-bridge submodules), as in Fig. 9, in which the characteristics of conventional MMC and MCC are also shown (in gray) as references.

The power-electronic devices of 4500 V are adopted in all these schemes, with the applied voltage of 2200 V. In power-loss analysis, the submodules of MMC and the dc-link chain modules of MCC adopt the IGBT device "5SNA-3000K452300," while the conventional MSs of the commutation bridges in MCC adopt the IGCT device "5SHY-65L4521" with the FRD "D3900U45X172." RB-IGCTs are used in the BMSs with the characteristics inferred from studies [30] and [31]. The submodule switching frequencies are set to 100 Hz for the MMC arms and 150 Hz for the MCC dc-link chain. The device quantity of the H-MCC is increased compared with conventional MCC, yet it is 30% less than that of a hybrid MMC. Besides, it inherits the advantage of conventional MCCs in smaller supporting capacitors, which benefits in power density. The power loss of H-MCC in rated operation is only slightly increased than a conventional MCC since RB-IGCT-based BMSs do not add extra devices to the conduction path. The total power loss of H-MCC is only 56% of a hybrid MMC during rated operation.

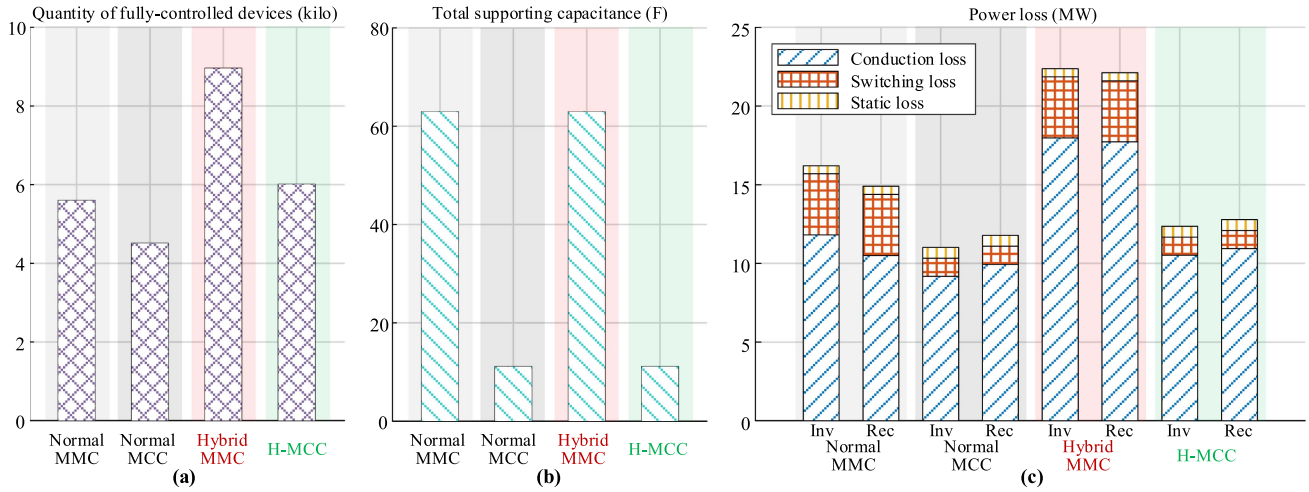

Fig. 9. Performance of the H-MCC and comprehensive comparison. (a) Quantity of fully-controlled devices. (b) Total supporting capacitance. (c) Power loss under rated operation ("inv" and "rec" refers to inverter and rectifier mode, respectively).

Furthermore, the loss analysis results for the conventional and hybrid MMCs in this work are qualitatively consistent with those in [32], confirming the credibility of the loss evaluation method.

In summary, the proposed H-MCC achieves significant improvements in both cost and efficiency compared with the hybrid MMC, demonstrating its clear techno-economic advantages.

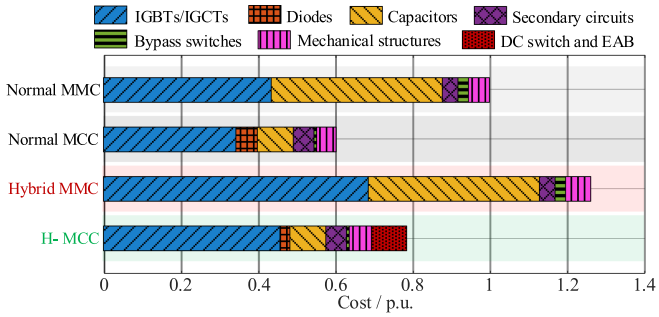

Fig. 10. Cost evaluation of different converters.

B. DC Switch

A fully solid-state dc switch typically requires a large number of series-connected power electronic devices to break the dc load current under the stress of the rated dc bus voltage. This not only results in high equipment cost, but also introduces additional resistance in the dc current conduction path, thereby increasing the operational losses of the system. On the other hand, since the dc current has no natural zero-crossing, a mechanical switch cannot extinguish the arc and thus cannot achieve dc current breaking.

Compared with such conventional solutions, the proposed H-MCC achieves quasi–soft turn-OFF under zero-voltage conditions for the dc switch during the dc fault current breaking stage by bypassing all cascaded modules. Consequently, only a MV-SSCB is required to break the fault current. Subsequently, a fast mechanical dc contactor isolates the faulted dc circuit from the MCC valve, enabling immediate unblocking and STATCOM operation. The contactor does not need to break the dc current and is only used to withstand the dc bus voltage. In this way, the tasks of "dc fault current breaking" and "dc bus voltage withstanding" are decoupled, being handled separately by the MV-SSCB and the contactor.

In the design example, the rated voltages of MV-SSCB and dc contactor are only 2.79% and 111.19% of the rated dc voltage, respectively. As the dc contactor provides a metallic conduction path when closed, its equivalent resistance is low, resulting in power dissipation far lower than that of a fully solid-state dc switch with the same rated voltage. Therefore, compared with a fully solid-state switch scheme, this approach significantly reduces equipment cost and operational losses, thereby improving techno-economic performance of the proposal. In addition, the dc contactor can also function as the dc-side disconnector of the dc transmission system, thus further improving the cost-effectiveness of the system.

C. EAB Components

According to the design in Table II, the maximum energy stored in the EAB capacitor is only 11.3% of the average total energy stored in all submodules of the dc-link chains. Since the EAB capacitor is energized only for a short duration during the DC-FRT process, its short-term overvoltage capability can be utilized to reduce its rated specifications.

The energy dissipated in the EAB resistor during the DC-FRT process is only 2.878 MJ, which is merely one-thousandth of the single-event energy handled by typical dc braking resistors used in similar systems [33], indicating good implementability. The diode in the EAB is realized by a series connection of conventional rectifier diodes, and since it only carries surge current for a very short period, its rated current specification can also be selected at a lower level. Overall, the EAB circuit has a negligible impact on the overall size and cost of the H-MCC.

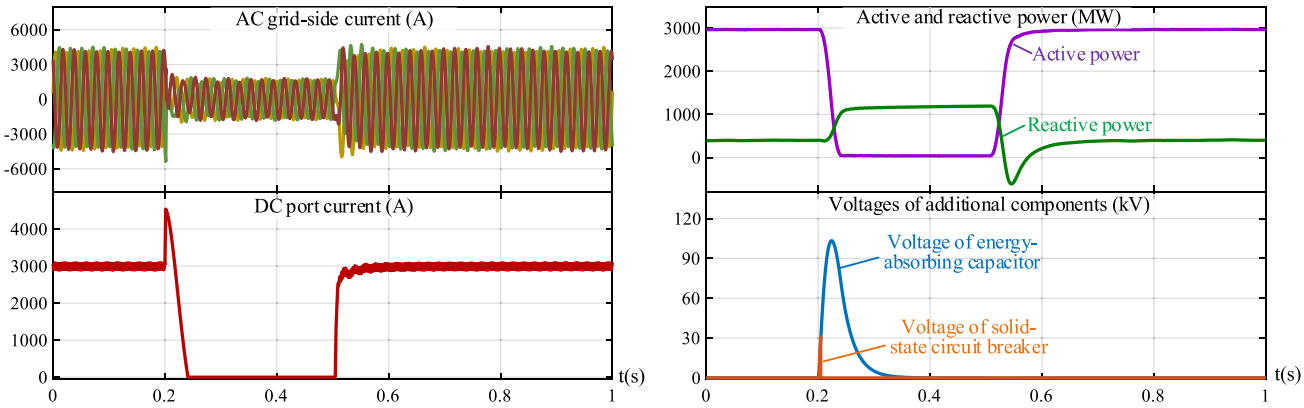

Fig. 11. Simulation waveform of H-MCC during DC-FRT process in ±500 kV/3000 MW VSC-HVDC system.

D. Cost

Fig. 10 presents the hardware cost of different converter schemes with the same voltage and capacity, with all data normalized to that of a normal MMC. Without the DC-FRT requirement, an MCC costs about 40% less than an MMC, mainly due to the substantial reduction in supporting capacitance and a slight decrease in the number of fully controlled devices. The hybrid MMC costs about 25% more than a normal MMC because it requires over 50% additional fully controlled devices.

For the proposed H-MCC, although its cost is about 30% higher than that of a normal MCC owing to the additional fully controlled devices, the hybrid dc switch, and the EAB, it remains over 20% lower than that of a normal MMC and up to 50% lower than that of a hybrid MMC with the same DC-FRT capability. Considering further savings in structural components and land use from the reduced converter footprint [8], as well as the lower life-cycle operating cost from improved efficiency, the techno-economic advantage of the H-MCC becomes more prominent.

E. Controllability of the AC System and DC Fault Recovery

In terms of controllability of the ac system following a dc short-circuit fault, a conventional MMC or MCC suffers from the uncontrolled rectification effect throughout the tens of milliseconds before the ac circuit breaker opens, which causes severe current surges to the ac grid. Besides, it remains disconnected from the ac system until the dc fault is cleared. In contrast, H-MCC can rapidly reduce the ac current by blocking the commutation bridges. Once the dc contactor is quickly opened within 2 ms, H-MCC can immediately unblock and provide reactive power support to the ac grid, similar to a hybrid MMC. With the high-overload design [9], H-MCC can generate a reactive power higher than its rated capacity, thereby achieving better grid robustness than hybrid MMC.

Regarding dc fault recovery, the fault clearance rate of a hybrid MMC depends on the proportion of full-bridge submodules, whereas in the H-MCC it is determined by the parameters of the EAB, as illustrated in Fig. 8(c). In the design example presented in Table II, the fall time of the fault current is 42.0 ms, which is equivalent to that of a hybrid MMC with 60% full-bridge submodules. The discharge time of the EAB capacitor is 87.7 ms, so the next possible DC-FRT will not be affected.

VI. Simulation and Experimental Verifying

A. Simulation Verification

Simulation model is built in Simulink platform with the parameters shown in Tables I and II. The number of cascaded half-bridge submodules in the dc-link chain of each phase is decreased to 16 to accelerate the simulation. Fig. 11 shows the simulation results.

The converter operates under rated capacity at rectifier mode. At 0.2 s, a dc short-circuit fault occurs and the dc current rises rapidly to the protection threshold of 1.5 p.u. Then the DC-FRT process begins, reducing the dc current and charging the EAB capacitor. After that, the MCC operates in STATCOM mode till the fault point is deionized. In the end, the dc contactor closes and the MCC resumes rated operation.

The simulation waveforms accord with the theoretical analysis. The key simulation results, such as the fault current decay time and the withstand voltages of the MV-SSCB and the dc contactor in the hybrid dc switch, are generally consistent with the design values given in Table II. Therefore, the analytic models of DC-FRT process and the method of parameter design are proved to be reliable.

B. Experiment Platform

An experiment platform is built based on a principal prototype of MCC to further verify the feasibility of the proposal. The ac side of MCC is connected to a programmable three-phase grid emulator via a three-phase link inductor of 26 mH and a 95 V/128 V isolated transformer. Each of the dc-link chains in three phases consists of 16 MOSFET-based HBSMs with the rated voltage of 8 V, while each of the commutation bridge arm adopts two MOSFETs in opposing-series connection. The dc side of MCC is connected to a bidirectional dc voltage source with 70 mH dc filter inductor and 140 mH equivalent line inductor. The rated capacity of the prototype is 400 VA.

The settings to the platform such as switching of contactors and given power instruction are input to a PC interface, and

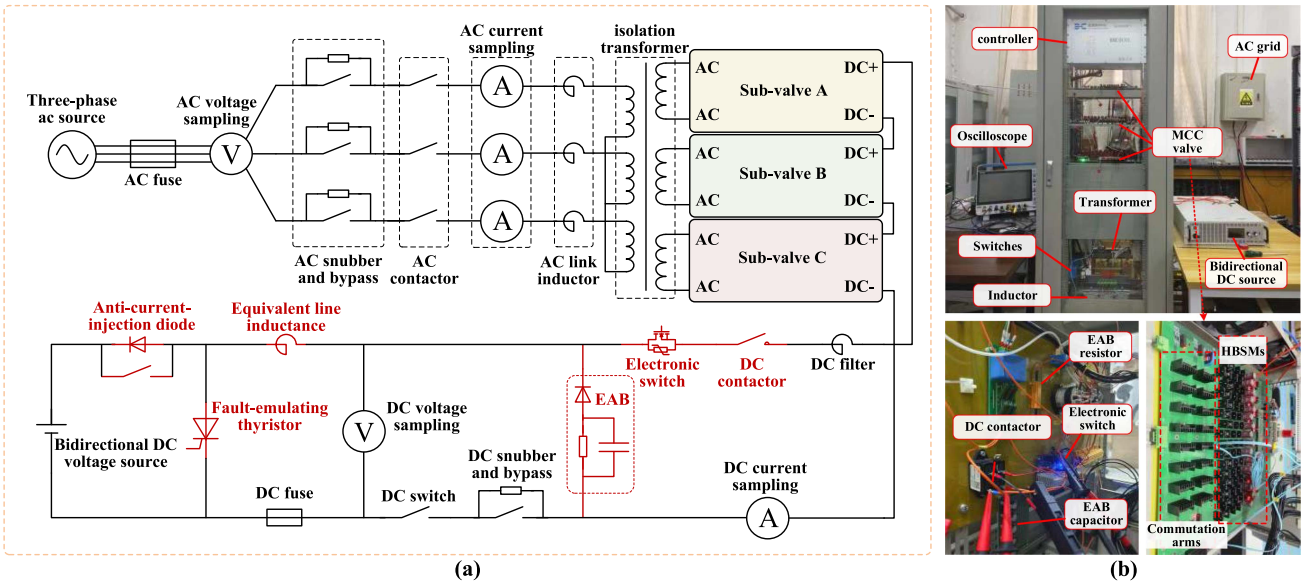

Fig. 12. Experiment platform of MCC with DC-FRT capability. (a) Circuit diagram. The components marked in red are added for the DC-FRT test. (b) Photograph.

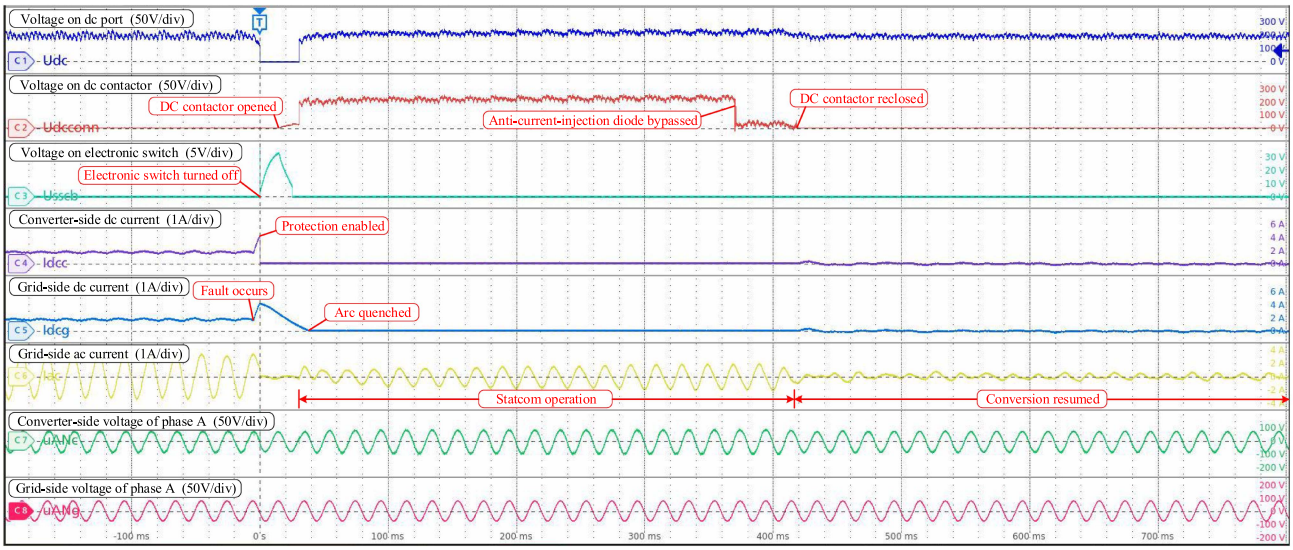

Fig. 13. Test waveform of H-MCC during DC-FRT process.

then transmitted to a DSP-based controller, which controls the MCC by PI controlling and nearest-level modulation. Then the information is given to local FPGAs on phase PCBs for pulse generation to control the MOSFETs.

In order to test the proposed DC-FRT function, an electronic switch (to emulate the MV-SSCB), a dc contactor, and an EAB are added to the dc side of the prototype. The capacitor and resistor of EAB is 1 mF and 24 Ω, respectively. A thyristor is connected in parallel at the dc port of the system to emulate the short-circuit fault and are-quenching characteristic. A diode with a bypass contactor is also set before the dc source to prevent a continuous current injection when the thyristor turns on. The circuit diagram and photograph of the platform are shown in Fig. 12(a) and (b), separately.

C. Experiment Results

The outputs of ac and dc sources are turned on to charge the prototype. The MCC is then started and its given power instruction is gradually increased to the rated value (400 W rectifier). After opening the bypass contactor of the anti-current-injection diode, a pulse is generated by an external circuit to trigger the thyristor. When the DSP detects the overcurrent, it enables the DC-FRT process shown in Fig. 3. Finally, when the fault is ridden through, the MCC resumes power conversion. The test waveforms are shown in Fig. 13.

Once the DC-FRT control is enabled, the commutation bridges are blocked, effectively suppressing the uncontrolled rectification effect on the ac side. Meanwhile, the electronic

switch in the hybrid dc switch rapidly breaks the dc valve-side fault current and withstands the gradually rising voltage of the EAB capacitor (up to 34 V). Subsequently, the dc contactor opens, taking over from the electronic switch to withstand the further rising EAB capacitor voltage and continuously block the dc bus voltage after the converter is unblocked. This sequence demonstrates the decoupling of the "current breaking" and "voltage blocking" functions within the hybrid dc switch, confirming the feasibility of its hardware principle. Once the dc interruption is completed, the converter is unblocked in STATCOM mode and later resumes active power transmission after the fault is cleared.

The experimental results are consistent with the theoretical analysis of dc fault self-clearing shown in Fig. 3. Although the experimental parameters differ from those used in the simulations for an actual overhead-line-based VSC-HVDC system, the test waveforms agree well with the qualitative characteristics of the simulated waveforms in Fig. 12, effectively validating the key physical processes of commutation bridge blocking, hybrid dc switch breaking, fault current decay, and power recovery in H-MCC during DC-FRT. It should be noted that the dc contactor in the experimental prototype is a commercially available low-voltage product with a 10 ms opening time, resulting in a longer interval between fault breaking and converter re-unblocking compared to the theoretical analysis and simulation results. In addition, to ensure stable operation of the experimental system, a conservative design was adopted for the PI parameters of the prototype controller, leading to slower reactive current rising rate in STATCOM mode and slower active current recovery after fault clearance compared to the simulation.

Overall, the experimental results verify the hardware and software capability of MCC to achieve dc fault self-clearing, maintain STATCOM operation during fault clearance, and resume normal operation, thus demonstrating the practical feasibility of the proposed H-MCC scheme for application in overhead-line-based VSC-HVDC systems.

VII. Conclusion

The proposed H-MCC achieves DC-FRT capability through a coordinated strategy combining ac-grid isolation, arc-quenching acceleration, ac-side STATCOM operation during the FRT process, and rapid conversion resumption. Its topology, control sequence, and analytical parameter-design method have been validated through both simulation and experimental results.

Compared with the hybrid MMC, H-MCC not only retains the inherent advantages of conventional MCCs, but also achieves DC-FRT with fewer additional components. This leads to notable reductions in device count and supporting capacitance, along with improved operational efficiency, thereby enhancing techno-economic performance in both footprint and cost. These features make H-MCC a competitive and practical option for overhead-line-based VSC-HVDC applications.

Future research could focus on scaling up the H-MCC to high-voltage, high-power prototypes with full engineering considerations such as thermal management, insulation design, and EMC mitigation, while further optimizing control strategies to enhance dynamic performance and grid support capability during the DC-FRT process. In addition, long-term reliability and lifecycle assessments of key components, including the EAB and hybrid dc switch, under realistic operating conditions would provide valuable insights for practical deployment.

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Ruihang Bai (Graduate Student Member, IEEE) was born in Xi'an, China in 1998. He received the B.S. degree in electrical engineering in 2020 from Tsinghua University, Beijing, China, where he is currently working toward the Ph.D. degree in electrical engineering. Mr Bai was a visiting Ph.D. student at KTH Royal Institute of Technology, Stockholm, Sweden, from July 2024 to January 2025. He has been serving as a Special Intern at Hitachi Energy Research China, Beijing, China, since August 2025.

His current research interests include high power converter, high power semiconductor device, and VSC-HVDC system.

Biao Zhao (Senior Member, IEEE) was born in Hubei, China, in 1987. He received the B.S. degree from the Dalian University of Technology, Dalian, China, in 2009, and the Ph.D. degree from Tsinghua University, Beijing, China, in 2014, both in electrical engineering.

He is currently a Tenured Associate Professor with the Department of Electrical Engineering, Tsinghua University. His current research interests include high power converter, high power semiconductor device, and flexible dc transmission and distribution system.

Xueyin Zhang was born in Sichuan, China, in 1992. He received the B.S. and Ph.D. degrees from the Department of Electrical and Electronic Engineering, North China Electric Power University, Beijing, China, in 2015 and 2020, respectively, both in electrical engineering.

He is currently the Deputy Chief Engineer of DC Research Center, Tsinghua Sichuan Energy Internet Research Institute, Chengdu, China. His current research interests include high power converter, high power semiconductor device, and flexible dc transmission and distribution system. Dr. Zhang was a visiting scholar of FREEDM System Center, North Carolina University, North Carolina, USA, from 2018 to 2019.

Lin Wang (Graduate Student Member, IEEE) was born in Henan, China, in 2001. He received the B.S. degree in electrical engineering from the Department of Electrical Engineering, Huazhong University of Science and Technology, Wuhan, China, in 2023. He is currently working toward the Ph.D. degree in electrical engineering with the Department of Electrical Engineering, Tsinghua University, Beijing, China.

His research interests include high power converter and VSC-HVDC system.

Zhanqing Yu (Member, IEEE) was born in Inner Mongolia, China, in 1981. He received the B.Sc. and Ph.D. degrees from Tsinghua University, Beijing, China, in 2003 and 2008, respectively, both in electrical engineering.

In July 2008, he became a Postdoctor with the Department of Electrical Engineering, Tsinghua University, where he became a Lecturer in 2010 and an Associate Professor in December 2012. His research interests include dc grid, dc breaker, electromagnetic environment and electromagnetic compatibility, and lightning protection.

Qiang Song (Senior Member, IEEE) was born in Changchun, China, in 1975. He received the B.E.E. and Ph.D. degrees from Tsinghua University, Beijing, China, in 1998 and 2003, respectively, both in electrical engineering.

From 2003 to 2008, he was a Lecturer with the Department of Electrical Engineering, Tsinghua University. Since 2008, he has been an Associate Professor with the Department of Electrical Engineering, Tsinghua University. His research interests include high-power electronic interfaces for utility system, flexible ac transmission system, VSC-HVDC system, and custom power quality.

Rong Zeng (Senior Member, IEEE) was born in Shaanxi, China, in 1971. He received the B.Eng., M.Eng., and Ph.D. degrees from the Department of Electrical Engineering, Tsinghua University, Beijing, China, in 1995, 1997, and 1999, respectively, all in electrical engineering.

In 1999, he was a Lecturer with the Department of Electrical Engineering, Tsinghua University, where he became an Associate Professor in 2002 and a Professor in 2007. His research interests include the fields of airgap discharge, lightning protection, and electromagnetic compatibility in power systems, electric and magnetic field measurement by integrated electro-optical sensors, power semiconductor, HVDC system, and dc circuit breaker.