A Fault-Tolerant Method of Submodule Fault Diagnosis and Redundant Cooperative Control for Subsea ISOP-Type DC Converters

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***Abstract*—The subsea direct current (dc) converter is prone to component failures, particularly in switching devices and input capacitors, primarily due to its installation within a tightly sealed, small-volume metal enclosure, which significantly impairs heat dissipation. To enhance the reliability of subsea input-series output-parallel (ISOP) dc converters, this article proposes a multilevel synergistic fault-tolerant strategy that takes into account the challenges of large input voltage fluctuations and limited electrical monitoring. Unlike conventional fixed-threshold methods, the proposed scheme leverages the dynamic voltage–current time-domain signatures of submodules during incipient faults for real-time monitoring and fault localization, thereby maintaining robustness against input voltage variations. Furthermore, a redundant bypass circuit based on current-limiting resistor multiplexing is incorporated to improve the traditional topology. When combined with a smooth redundancy switching mechanism, this approach effectively mitigates transient electrical stresses on healthy modules during fault transitions. These enhancements collectively ensure the operational safety of both the subsea converter and associated high-precision deep-sea equipment. Finally, a comprehensive fault-tolerant control scheme is developed to guarantee the reliable operation of the subsea dc power supply system following fault occurrences.**

***Index Terms*—Fault diagnosis, fault-tolerant, redundancy, subsea direct current (dc) converter.**

I. Introduction

CURRENTLY, the development and utilization of marine resources have led to the expansion of the coverage area of subsea scientific observation networks [1]. This expansion has extended the observation range from shallow coastal waters to deep and remote ocean regions, increasing the cable-laying distance from several tens of kilometers to several hundreds of kilometers. Furthermore, the laying depth has increased from several tens of meters to several thousands of meters. Consequently, the energy demand has surged from a few kilowatts to several hundreds of kilowatts [2], [3]. The configuration of a standard subsea direct current (dc) power supply system is illustrated in Fig. 1. This system comprises a shore station, subsea optoelectronic composite cable, main junction box, secondary junction box, scientific observation instruments, and defense equipment [4]. The shore station generates dc voltages of tens of kilovolts, which are converted to low-voltage dc (e.g., 375 VDC) by a medium-voltage dc converter deployed in the main junction box. The secondary junction box further steps down the voltage to several tens of volts, thereby supplying power to various scientific instruments and defense equipment.

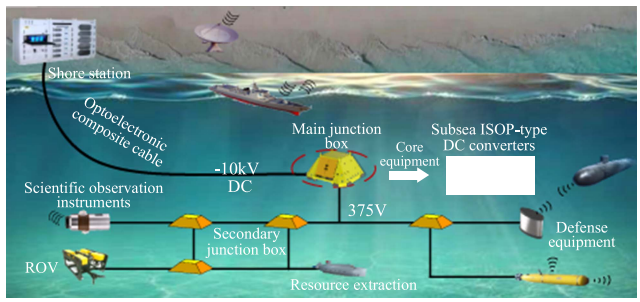

Fig. 1. Configuration of a standard subsea DC power supply system.

The subsea medium-voltage dc converter, which connects medium-voltage and low-voltage subsea cables, serves as the central power supply component of the subsea observation network and directly influences the safety and reliability of the entire system. It demands exceptional service life, high reliability, and significant operational value [5]. If the subsea dc converter fails, the output voltage may drop significantly, which can cause malfunctions in scientific observation instruments and defense equipment, thereby jeopardizing deep-sea exploration missions. In the worst-case scenario, severe damage to the subsea dc converter can result in the complete failure of the entire power supply system. Due to the high pressure and

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severe corrosiveness of the deep-sea environment at depths of several kilometers, subsea dc converters are typically enclosed within compact, highly sealed, corrosion-resistant titanium alloy cylindrical chambers. However, these chambers pose significant challenges, including poor heat dissipation and uneven temperature distribution, which lead to substantially higher failure rates of high-frequency switching devices and capacitors compared to land-based systems [6]. Furthermore, the cost, duration, and complexity of repairing deep-sea electrical equipment are considerably greater than those for land-based systems.

To enhance the continuous and reliable power supply capability of subsea dc converters, the implementation of fault-tolerant strategies is a promising approach. Existing medium-voltage dc converter topologies often incorporate redundant submodules to improve reliability [7]. However, research on fault diagnosis and coordinated redundant control strategies specifically tailored for subsea converter fault-tolerant operation remains limited, whereas fault-tolerant schemes for land-based modular cascaded dc converters have been more extensively investigated [8], [9], [10]. The traditional hot-standby redundancy method is adopted in [11], [12], [13], and [14] ensuring the stability of the converter output by rapidly isolating faulty modules or components using configured switches, thereby maintaining the normal operation of the remaining healthy components. However, this type of method requires redundant modules to be operational in the normal mode and subjects the system to significant electrical stress during the isolation of faulty modules. Wang et al. [15], [16] propose a universal fault-tolerant method for modular series-parallel dc converters, which enables fast and seamless hot swapping through dedicated control algorithms, thereby minimizing the impact on healthy modules. Nevertheless, this method requires additional windings in the inductive core to obtain diagnostic variables. To limit the discharge current of capacitors during the bypassing of a faulty module, Fang et al. [17] propose the use of series current-limiting resistors in the bypass branch to isolate the faulty module. However, once the fault is isolated, the current-limiting resistors remain in the power circuit, which increases converter losses. In addition, the thermal dissipation of these resistors further exacerbates the heat dissipation challenges of subsea converters. To address the increased losses caused by current-limiting resistors, Ting et al. [18] suggest adding a bypass switch in parallel with the series resistor in the bypass branch. This switch is closed after the input capacitor discharges, thereby isolating the faulty module without introducing additional losses. However, this method does not consider the current-limited charging requirements of the input capacitors.

To avoid introducing additional bypass switch branches, Ting et al. [19] propose the use of IGBTs in the module bridge arm to implement the bypass function. However, this approach necessitates a complex digital control and drive circuit, and becomes ineffective if the IGBT itself fails. Zhu et al. [20] and Choi et al. [21] propose fault-tolerant operation strategies for solid-state transformers based on the input-series output-parallel (ISOP) configuration. These methods dynamically adjust the modulation of cascaded modules to reduce the output power of the faulty module relative to other modules, thereby ensuring continuous system operation. However, their effectiveness is limited in the case of severe module faults. Single-fault-tolerant strategies for cascaded H-bridge (CHB) multilevel converters are proposed in [22], [23], [24], [25], and [26]. These strategies maintain normal output by bypassing the fault point to reconfigure the topology, combined with modulation signal adjustments. However, such methods are not adaptable to multiple faults and can only tolerate a limited range of fault types. Many fault-tolerant methods proposed in the literature lack integration with fault diagnosis, as most existing strategies primarily emphasize redundancy control with limited coordination between diagnostic and fault-tolerant process. Furthermore, these approaches often require additional sensors and complex diagnostic and redundancy control circuitry, constraining their applicability in compact subsea converters.

Table I summarizes the existing fault-tolerant methods, which are primarily designed for onshore converters. Considering the extreme conditions in subsea environments, these existing fault-tolerant methods cannot be directly applied to subsea due to the following major challenges: 1) The harsh conditions of deep-sea environments, such as high pressure and corrosion, impose strict constraints on the deployment of dc converters. The extremely limited space within subsea converter enclosures makes it challenging to install additional electrical sensors for fault diagnosis. 2) High-sensitivity, high-precision scientific instruments and defense equipment in subsea are highly susceptible to transient electrical stresses. These cannot withstand excessive transient current or voltage shocks in existing fault-tolerance processes. Under the dual requirements of operating with minimal sensors and avoiding electrical stress impacts, existing fault-tolerant methods often fall short of meeting the demands of subsea applications.

To address the aforementioned challenges and improve the safety and reliability of subsea power supply systems, this article proposes a multilevel coordinated fault-tolerant operation scheme for subsea ISOP dc converters. The main contributions of this work are summarized as follows.

1) A real-time fault diagnosis method is developed, which replaces traditional fixed-threshold approaches by monitoring time-domain variations of voltage and current parameters in submodules during fault initiation. This strategy mitigates misdiagnosis caused by input voltage fluctuations and utilizes existing control variables as diagnostic indicators, thereby eliminating the need for additional sensors, reducing system complexity and cost.
2) The proposed fault-tolerant topology for subsea ISOP converters improves upon conventional designs by integrating a bypass-based redundant circuit incorporating charge/discharge current-limiting resistors. Through coordinated control of dual switches and resistors, discharge and charging currents are effectively limited, and a smooth redundancy switching strategy is implemented to suppress transient electrical stresses, thereby ensuring safe operation of both the subsea converter and sensitive equipment.
3) The proposed scheme integrates diagnostic, power, and fault-tolerant circuits, enabling seamless fault diagnosis, isolation of faulty submodules, and activation of redundant

TABLE I
COMPARISON TABLE FOR FAULT TOLERANT METHODS

Ref.	Topology	Additional electrical sensor	Fault tolerant scheme	Cost	Electrical stress	Control complexity
[11], [14]	Modular dc converter	Not mentioned	Directly bypass the faulty module	Low	Large	Simple
[12]	Cascaded dc/dc converter	Exist	Bypass the faulty module and activate the redundant module	High	Medium	Medium
[13]	Interleaved boost converter	Exist	Directly bypass the faulty module	Medium	Large	Simple
[15], [16] [18], [19]	Modular dc converter	Exist	Bypass the faulty module and activate the redundant module	High	Medium	Medium
[17]	ISOP converter	Not mentioned	Bypass the faulty module and activate the redundant module	Medium	small	Medium
[20], [21] [24], [25], [26]	Cascaded H-bridge	Exist	Adjust the modulation strategy	Low	Large	Complex
[22], [23]	Cascaded H-bridge	Exist	Bypass the faulty module, activate the redundant module and adjust the modulation strategy	High	Medium	Complex

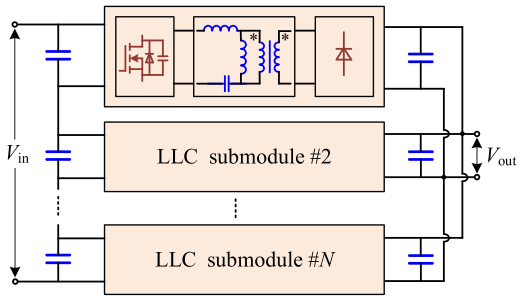

Fig. 2. Typical topology of the *LLC*-ISOP subsea DC converter.

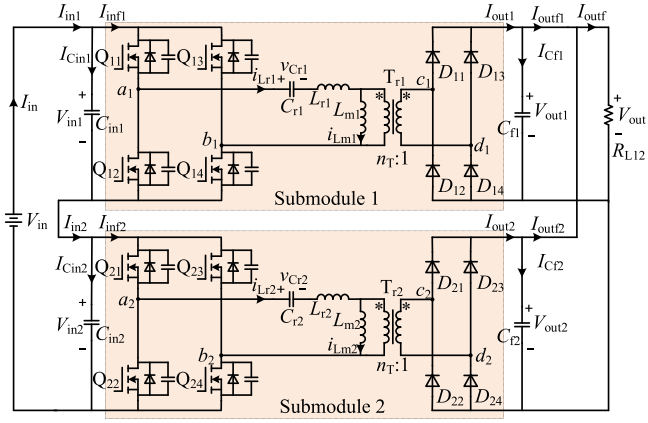

Fig. 3. ISOP converter topology based on two *LLC* submodules.

submodules. In conjunction with coordinated timing control, this approach ensures reliable fault-tolerant operation of ISOP converters, thereby significantly enhancing the reliability and operational capability of subsea dc power supply systems.

The rest of the article is organized as follows. Section II analyzes submodule fault characteristics and develops a diagnostic strategy. A fault-tolerant topology and scheme for coordinated control of fault diagnosis and redundancy switching are proposed in Section III. Then, Section IV carries out experimental verification. Finally, Section V concludes this article.

II. FAULT DIAGNOSIS METHOD FOR CONVERTER SUBMODULES

The subsea medium-voltage dc converters are typically housed within compact, hermetically sealed titanium alloy enclosures to achieve a high degree of compactness. In addition, these converters operate under demanding voltage conditions, with input voltages up to 10 kV and output voltages as low as 375 V. To meet the stringent requirements for wide gain, high voltage conversion ratio, and high-power density, the ISOP-type dc converter topology based on *LLC* resonant modules is considered an optimal solution for medium-voltage to low-voltage energy conversion in subsea applications, as illustrated in Fig. 2 [27], [28].

The subsea dc converters integrate numerous internal components, among which primary-side power switching devices exhibit a high likelihood of failure. Input capacitors are also susceptible to accelerated aging and failure due to high-frequency operation and thermal stress. Given the complexity of fault coupling and propagation within each submodule, as well as the challenges associated with real-time monitoring and sensor deployment, this section presents a submodule-level analysis. Specifically, it investigates the transient voltage and current characteristics at the submodule ports during the initial stages of switching device and input capacitor faults. An online diagnostic procedure is subsequently developed based on this analysis.

A. Submodule Port Characteristics at the Beginning of Power Switching Tube Open Circuit Fault

Due to the inherent characteristics of switching devices and the widespread implementation of integrated short-circuit protection in switching drivers, a short-circuit fault in a switching device is ultimately manifested as an open-circuit fault. Taking two *LLC* resonant submodules configured in an ISOP arrangement as an example, the analysis is illustrated in Fig. 3. Here, $V_{\rm in}$ and $I_{\rm in}$ represent the input voltage and current of the ISOP dc converter, while $V_{\rm out}$ and $I_{\rm out}$ denote the output voltage and current, respectively. For submodules 1 and 2, $V_{\rm in1}$

and V_{in2} are denote the input voltages. I_{Cin1} and I_{Cin2} are the currents flowing into the input filter capacitors. I_{inf1} and I_{inf2} represent the currents entering the switching full-bridge circuits. I_{out1} and I_{out2} are the currents exiting the uncontrolled rectifier bridges. I_{Cf1} and I_{Cf2} are the currents flowing into the output filter capacitors. I_{outf1} and I_{outf2} denote the output currents. The relationships among these variables are defined as follows:

$$\begin{cases} V_{\text{in}} = V_{\text{in1}} + V_{\text{in2}} \\ I_{\text{in}} = I_{\text{Cin1}} + I_{\text{inf1}} = I_{\text{Cin2}} + I_{\text{inf2}} \end{cases} \tag{1}$$

$$\begin{cases} V_{\text{out}} = V_{\text{out1}} = V_{\text{out2}} \\ I_{\text{out}f} = I_{\text{out}f1} + I_{\text{out}f2} \\ I_{\text{out}f1} = I_{\text{out1}} - I_{\text{Cf1}} \\ I_{\text{out}f2} = I_{\text{out2}} - I_{\text{Cf2}} \end{cases}. \tag{2}$$

Consider an open-circuit fault occurring in the switching device Q_{11} of submodule 1. At the onset of the fault, the disconnection of the Q_{11} branch leads to a reduction in the current I_{inf} flowing into the primary-side full-bridge circuit, which in turn causes a decrease in the input current I_{in}. According to (1), when the rate of change of I_{in} is less than that of I_{inf1}, the current flowing through the input filter capacitor increases, thereby charging the input filter capacitor C_{in1} of submodule 1. As a result, the input voltage V_{in1} rises.

Simultaneously, given that the dc bus voltage V_{in} remains constant, the input voltage V_{in2} of submodule 2 decreases. According to (1), this reduction causes the input filter capacitor C_{in2} of submodule 2 to discharge and increases the primary-side full-bridge current I_{inf2} flowing into submodule 2. On the output side, the decrease in I_{inf1} leads to a reduction in the output current I_{outf1} of submodule 1, while the increase in I_{inf2} results in a corresponding rise in the output current I_{outf2} of submodule 2. However, due to the increase in V_{in1} and the decrease in V_{in2}, the control system loses its regulation capability, resulting in a decrease in the output voltage V_{out}.

Following a brief fault transient in the ISOP dc converter system, an input voltage imbalance develops between submodule 1 and submodule 2, with V_{in1} stabilizing at a higher value than V_{in2}. As a result, the ISOP dc converter enters an abnormal steady-state operating condition. Neglecting the currents flowing through the input filter capacitors, I_{Cin1} and I_{Cin2}, the input current I_{inf1} and I_{inf2} become approximately equal due to the series connection at the input. Consequently, the input power P_{in1} of submodule 1 exceeds that of P_{in2}. Assuming minimal efficiency variation between the two submodules, the parallel outputs will no longer supply equal output currents; specifically, the output current of submodule 1 will be greater than that of submodule 2.

Extending this analysis to a multisubmodule ISOP cascaded dc converter system, when an open-circuit fault occurs in the switching device of any *LLC* submodule, the input voltage of the faulty submodule initially increases and stabilizes at a higher level, while its input current experiences a rapid decrease, subsequently recovering to near-normal levels. For the nonfaulty submodules, the input voltage decreases and stabilizes at a lower value, and their input current exhibits a rapid increase followed by a decline, eventually returning to near-normal levels. Simultaneously, both the output voltage and current of the ISOP converter system exhibit a downward trend, ultimately stabilizing at reduced levels.

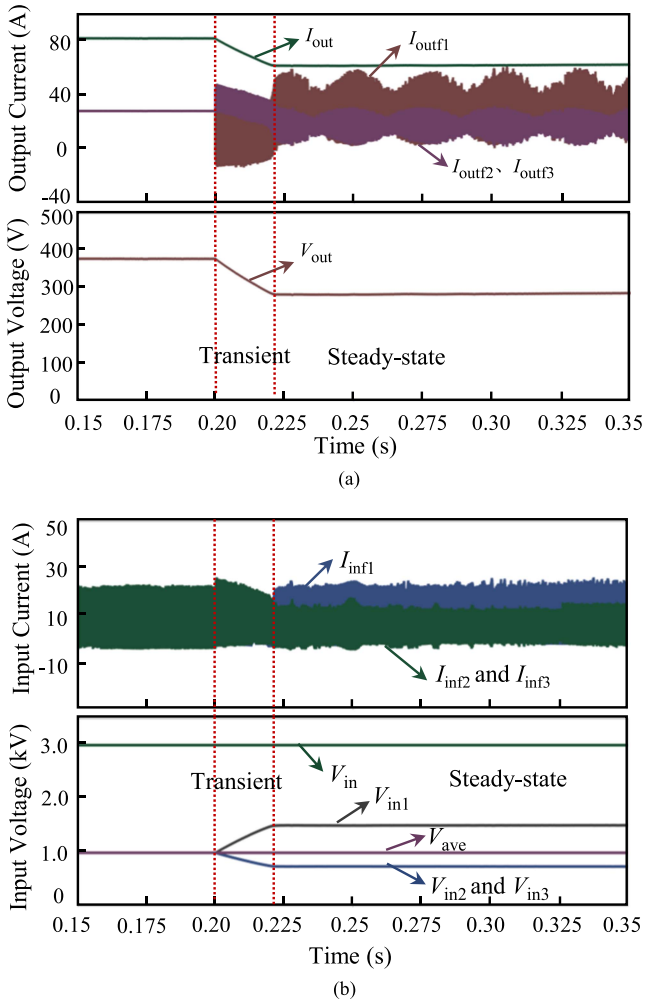

Fig. 4. ISOP converter port critical waveforms after submodule 1 switching tube failure. (a) Output waveforms. (b) Input waveforms.

Fig. 4 presents the port voltage and current waveforms of a subsea ISOP dc converter during a simulated open-circuit fault in the switching device of submodule 1. As depicted in Fig. 4(a), the transient fault induces input voltage fluctuations that disrupt the control system, leading to a temporary drop in both output voltage and output current. The variations in output current among the submodules correspond to the changes in their respective input currents. After a period of transient adjustment, the input voltages of the submodules are redistributed and stabilize, resulting in the output voltage and current converging to constant values.

As shown in Fig. 4(b), at 0.2 s, the drive signal of a switch in submodule 1 is disabled, initiating the open-circuit fault transient. During this process, the current I_{inf1} flowing into submodule 1 decreases, charging its input capacitor and thereby increasing the input voltage V_{in1}. With the total input voltage held constant and identical parameters for all submodules, the

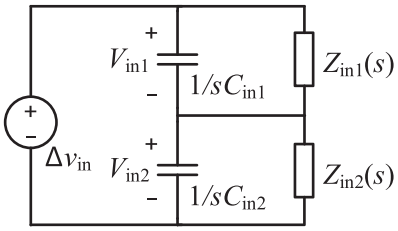

Fig. 5. Simplified equivalent model of a two-module cascade converter.

input voltages V_{in2} and V_{in3} of the healthy submodules 2 and 3 decrease and remain equal, causing their input capacitors to discharge and their input currents I_{inf2} and I_{inf3} to increase. Around 0.22 s, the system transitions to the fault steady-state phase, where the input voltages of all submodules stabilize, with the V_{in1} of the faulty submodule exceeding V_{in2} and V_{in3} of the healthy submodules. Consequently, the input current I_{inf1} of submodule 1 increases to a stable value due to its higher input voltage, while the input currents I_{inf2} and I_{inf3} of the healthy submodules gradually decrease to stable values as their input voltages drop. These results are in close agreement with the theoretical analysis of open-circuit fault behavior in switching devices.

B. Submodule Port Characteristics at the Beginning of Input Capacitor Failure

Metalized film capacitors are widely adopted as input filter capacitors in subsea converters due to their superior frequency response and extended service life. However, prolonged operation in confined, thermally inefficient, and humid environments leads to a gradual temperature rise in both internal and external insulation layers, thereby accelerating the thermal degradation of the insulation film and hastening capacitor failure. Typical failure characteristics are manifested by a decrease in capacitance (C) and an increase in equivalent series resistance (ESR). The elevated ESR exacerbates power loss within the capacitor, resulting in further temperature rise and accelerated aging. Under standard operating conditions, a metalized film capacitor is generally considered failed if its capacitance decreases by more than 20% or its ESR increases to more than twice its initial value, at which point it is unsuitable for continued circuit operation.

Taking as an example a cascaded configuration with two *LLC* resonant submodules connected in series at the input and in parallel at the output, the port characteristics under input capacitor failure are analyzed, as illustrated in Fig. 3. Assume that the input capacitor C_{in1} of submodule 1 has undergone significant aging, resulting in a 20% reduction in capacitance and a twofold increase in its ESR (ESR_1), while all other parameters and control strategies of the submodules remain identical. Neglecting the effects of input capacitors, the input impedances $Z_{in1}(s)$ and $Z_{in2}(s)$ of submodule 1 and 2, respectively, can be considered equal. Consequently, the two-module cascaded converter can be equivalently represented by a model combining the input capacitors and input impedances, as depicted in Fig. 5. Based on Kirchhoff's voltage law and Kirchhoff's current law, the corresponding expressions for the input voltage distribution can thus be derived

$$\begin{cases} V_{in1} = \frac{\Delta v_{in} Z_1(s)}{Z_1(s)+Z_2(s)} \\ V_{in2} = \frac{\Delta v_{in} Z_2(s)}{Z_1(s)+Z_2(s)} \end{cases} \tag{3}$$

where $Z_1(s) = 1/sC_{in1}||Z_{in1}(s)$, $Z_2(s) = 1/sC_{in2}||Z_{in2}(s)$, and $Z_{in1}(s) = Z_{in2}(s)$.

According to (3), the difference in the input voltage variations, Δv_{in}, between the two submodules in response to an input disturbance voltage Δv_{in12} can be expressed as follows:

$$\frac{\Delta v_{in12}}{\Delta v_{in}} = \frac{Z_1(s) - Z_2(s)}{Z_1(s) + Z_2(s)} = \frac{C_{in2} - C_{in1}}{C_{in2} + C_{in1} + \frac{2}{sZ_{in1}(s)}}. \tag{4}$$

For a step disturbance signal, at the initial instant, the following expression can be obtained:

$$\lim_{s\to 0} \frac{\Delta v_{in12}}{\Delta v_{in}} = \frac{C_{in2} - C_{in1}}{C_{in2} + C_{in1}}. \tag{5}$$

Similarly, under steady-state conditions, the following expression can be derived:

$$\lim_{s\to +\infty} \frac{\Delta v_{in12}}{\Delta v_{in}} = 0. \tag{6}$$

According to (3) and (4), it can be observed that when a disturbance occurs in the input voltage, the voltages across the input capacitors of each submodule change. This variation is inversely related to the capacitance value; a smaller capacitance results in larger and faster voltage transitions. Owing to the presence of the voltage balancing control loop, the system eventually stabilizes at a new voltage value. The impact of ESR is neglected here, as it remains small and the step disturbance signal is of high frequency. Specifically, for submodules with failed input capacitors, following a disturbance in the converter input voltage, both the rate of rise and the peak value of the capacitor voltage rapidly reach a maximum before decreasing to a new steady-state value. In contrast, for healthy submodules, the capacitor voltage also increases, but both the rate of rise and the peak value are lower than those of the faulty submodule, and they ultimately stabilize at the same voltage as the faulty unit. Consequently, the entire ISOP dc converter achieves a new voltage balancing reference. Furthermore, according to (1), the rate of rise and the peak value of the input current in the faulty submodule are also higher than those in the nonfaulty submodules. Similarly, these currents eventually decrease and settle at new steady-state values.

Fig. 6 shows the input voltage and current waveforms of the ISOP dc converter when the input capacitor of submodule 1 fails. At 0.2 s, the capacitance of submodule 1 decreases from 220 to 176 μF, and its ESR increases from 0.375 to 1.05 Ω. During this period, with no input voltage disturbance, there are no significant changes in the input voltages or currents of the modules. At 0.3 s, a 5% step disturbance is injected into the converter input voltage (3 kV), causing the input voltage of each submodule to increase rapidly. Notably, the rise rate and the peak value of the input voltage V_{in1} are greater than those of the healthy modules.

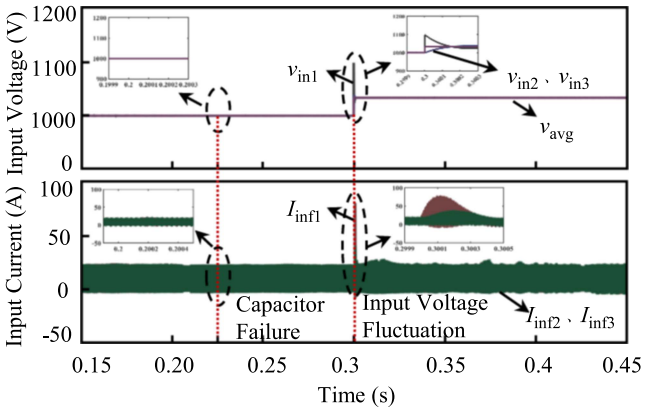

Fig. 6. DC converter input critical waveforms for input capacitor failure.

After reaching the peak value, due to the action of the voltage balancing loop, the input voltages gradually stabilize at 1050 V and remain balanced. Similarly, the input currents of all submodules increase, with the rate of rise and peak value of the input current I_{inf1} of submodule 1 exceeding those of the healthy modules. Ultimately, the output currents of all submodules stabilize and balance. These simulation results are consistent with the theoretical analysis.

C. Submodule Online Fault Diagnosis Process

Taking into account the key characteristics of subsea ISOP-type dc converters, including significant input voltage fluctuations, limited electrical monitoring, and constrained deployment space, a submodule diagnostic method is proposed. This method leverages the time-domain analysis of voltage and current waveforms at the submodule level during the early stages of faults, such as power switch open-circuit failures and input capacitor degradation. Unlike conventional fixed-threshold diagnostic approaches, the proposed method utilizes the differences in the magnitude and rate of change of electrical quantities among submodules to enable online fault detection and localization. As a result, it mitigates the risk of misdiagnosis caused by substantial input voltage fluctuations and eliminates the need for additional sensors. The overall module-level fault diagnosis process is illustrated in Fig. 7, with detailed steps outlined as follows.

1) The control system's monitoring variables are directly utilized: the input capacitor voltage $V_{\mathrm{in}\,i}$, input current $I_{\mathrm{inf}i}$, output voltage V_{out}, and output current I_{out}. In the early stages of a power switch open-circuit fault or severe input capacitor aging, the converter's output voltage or current may exhibit abnormal changes. However, by design, the output voltage remains stable during ordinary input voltage fluctuations.

To account for normal operational variations and potential output drops following a fault, the diagnostic thresholds are defined as upper limits V_{oth1} and I_{oth1}, and lower limits V_{oth2} and I_{oth2}, set at $\pm 20\%$ of the rated values. When the measured output voltage and current satisfy the following criteria, the subsea ISOP dc converter system is considered to be in a fault condition, thereby triggering the fault diagnosis function. Otherwise, continuous monitoring is maintained

$$\begin{cases} V_{\mathrm{out}} > V_{\mathrm{oth1}} \text{ or } V_{\mathrm{out}} < V_{\mathrm{oth2}} \\ I_{\mathrm{out}} > I_{\mathrm{oth1}} \text{ or } I_{\mathrm{out}} < I_{\mathrm{oth2}} \end{cases}. \tag{7}$$

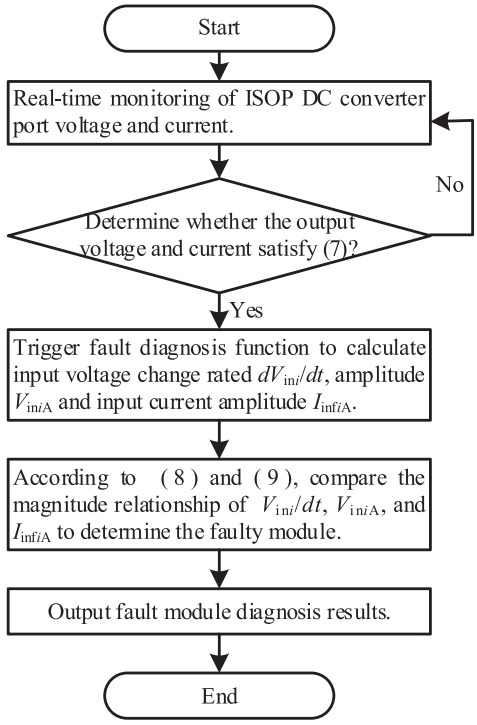

Fig. 7. Proposed module-level fault diagnosis flowchart.

2) Once a fault is detected in the subsea ISOP dc converter system, the rate of change of the input capacitor voltage $dV_{\mathrm{in}\,i}/dt$ for each submodule is calculated, as expressed in (8). Simultaneously, the amplitude of the input voltage $V_{\mathrm{in}\,i\mathrm{A}}$ and input current $I_{\mathrm{inf}\,i\mathrm{A}}$ for each submodule are also determined

$$\frac{dV_{\mathrm{in}i}}{dt} = \frac{V_{\mathrm{in}i}(k+1) - V_{\mathrm{in}i}(k)}{T} \tag{8}$$

where $V_{\mathrm{in}\,i}(k+1)$ and $V_{\mathrm{in}\,i}(k)$ represent the input voltage values at two consecutive sampling intervals, and T denotes the sampling period. The change rate is calculated as the slope of the input voltage curve. A positive slope indicates an increase, while a negative slope signifies a decrease.

3) Based on the results of the fault transient analysis, the fault submodule can be located by comparing the rate of change of the input capacitor voltage $dV_{\mathrm{in}\,i}/dt$, as well as the amplitudes of the input voltage $V_{\mathrm{in}\,i\mathrm{A}}$ and input current $I_{\mathrm{inf}\,i\mathrm{A}}$, among all submodules. Specifically, if a power switch open-circuit fault occurs in a submodule, submodule j is identified as faulty when condition (9) is satisfied. Similarly, if an input capacitor failure is present, submodule j is identified as the faulty module when all

conditions in (10) are satisfied

$$\begin{cases} \frac{dV_{\text{in}j}}{dt} > 0 \text{ and } \frac{dV_{\text{in}i}}{dt} < 0 \\ V_{\text{in}j\,\text{A}} > V_{\text{in}i\,\text{A}} \\ I_{\text{inf}\,iA} > I_{\text{inf}\,jA} \end{cases} \quad (i = 1, 2, \ldots, n \text{ and } i \neq j) \tag{9}$$

$$\begin{cases} \frac{dV_{\text{in}j}}{dt} > \frac{dV_{\text{in}i}}{dt} \\ V_{\text{in}j\,\text{A}} > V_{\text{in}i\,\text{A}} \\ I_{\text{inf}\,jA} > I_{\text{inf}\,iA} \end{cases} \quad (i = 1, 2, \ldots, n \text{ and } i \neq j). \tag{10}$$

4) The identified faulty submodule is determined using the module-level fault diagnosis circuit, and this information is transmitted to the main controller.

III. Fault Diagnosis and Redundant Coordinated Control for Fault-Tolerant Operation

Considering the sensitivity of deep-sea high-precision and high-precision scientific instruments and defense equipment to transient electrical stress during switching operations, existing fault-tolerant strategies for subsea systems face two critical challenges. First, the transient effects associated with redundancy switching remain insufficiently addressed, particularly the electrical stress imposed on both functional modules and loads due to capacitor charging and discharging. Second, current fault-tolerant control schemes lack comprehensive coordination between fault diagnosis and redundancy switching, resulting in limited system robustness. To overcome these limitations, this section develops a fast and smooth redundancy switching method specifically tailored for subsea environments. By integrating the proposed fault diagnosis method, a robust fault-tolerant operational strategy for the subsea ISOP converter is established.

A. Fault-Tolerant Topology Design for ISOP DC Converter

In most existing redundant structures, bypass switches are directly connected to the input side, which inevitably results in voltage overshoots due to capacitor charging and discharging during switching operations. To mitigate this issue, a bypass-based redundant structure employing a reusable current-limiting resistor is proposed. This topology utilizes the coordinated operation of dual switches and a current-limiting resistor to limit both the discharge current of the faulty module's capacitor and the charging current of the redundant module's capacitor, as illustrated in Fig. 8. Specifically, the proposed scheme enhances the basic ISOP dc converter by incorporating a redundant switching structure (highlighted in green) and a redundant submodule *R*e. The redundant switching structure primarily consists of a dc contactor S_{n1} for current limiting during charging and discharging, a bypass dc contactor S_{n2}, and a current-limiting resistor $R_{\text{lin}\,n}$. The redundant submodule *R*e is designed to be identical to the standard *LLC* resonant converter submodules, thereby ensuring seamless integration and operational consistency.

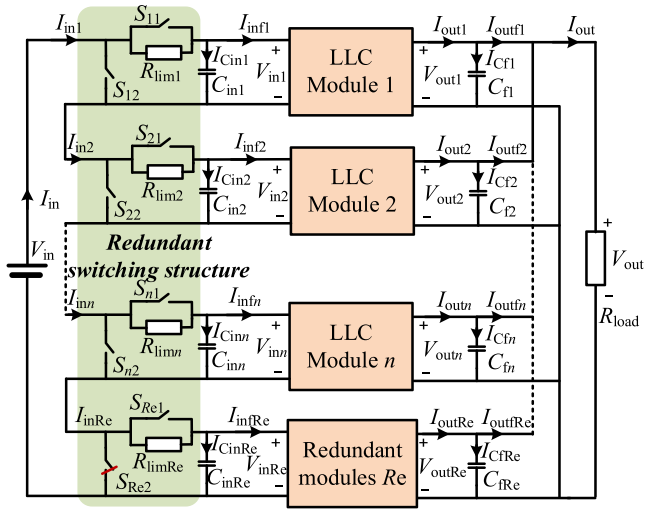

Fig. 8. Topology of the bypass-based subsea ISOP DC converters with current-limiting capability.

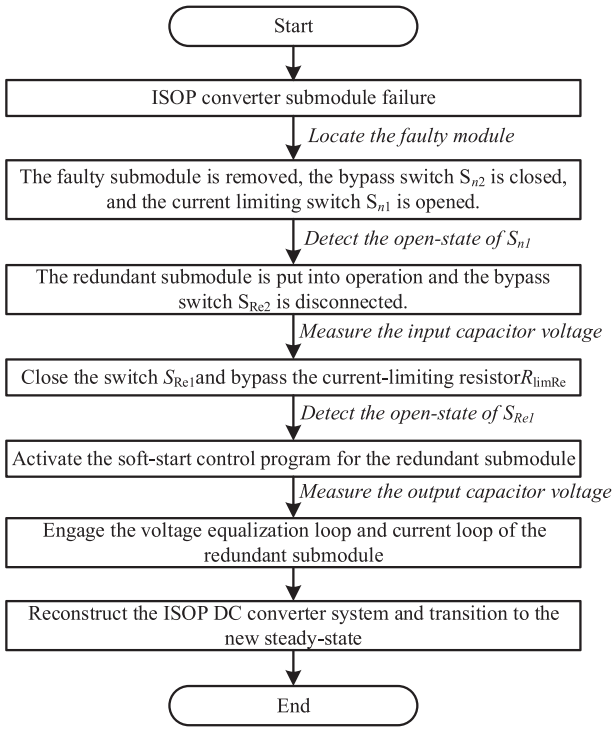

Fig. 9. Smooth redundancy switching control flowchart.

B. Smooth Redundancy Switching Process for Submodules

A fast redundancy switching control method is proposed based on the topology illustrated in Fig. 8, enabling the reconstruction of a converter system identical to the prefault configuration. This approach ensures the fault-tolerant operation of subsea dc systems. The proposed redundancy switching control process is depicted in Fig. 9 and its operation is analyzed as follows.

1) Normal Operation: During the normal operation of the subsea ISOP converter, switches S_{n2} remain open, while

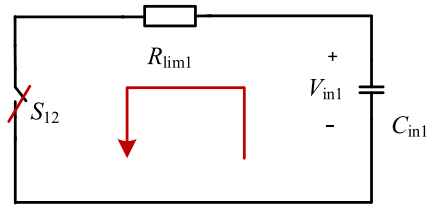

Fig. 10. Equivalent circuit diagram of the input capacitor discharge process during the bypass of submodule 1.

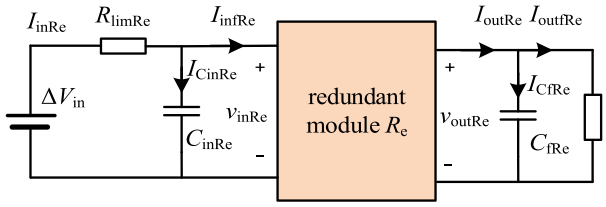

Fig. 11. Equivalent circuit diagram of the redundant submodule during the startup phase.

switches S_{n1} are closed, ensuring that all active submodules are integrated into the system. In this state, the redundant submodule operates in bypass mode, with its switch $S_{\mathrm{Re}2}$ closed and $S_{\mathrm{Re}1}$ open. As a result, the redundant submodule is electrically isolated from the main power flow, while the remaining submodules participate fully in the operation of the subsea ISOP converter, thereby maintaining stable and efficient system functionality.

2) Fault Isolation and Capacitor Discharge: Upon detecting a fault in submodule 1, the primary objective is to ensure sub-module safety. All switching devices within the faulty module are immediately locked to prevent further damage. Subsequently, switch S_{12} is closed and S_{11} is opened, thereby establishing a discharge path for the input filter capacitor of the faulty module. A current-limiting resistor $R_{\mathrm{lim}1}$ is introduced into the discharge circuit to limit the discharge current and dissipate the stored energy in the capacitor. This strategy ensures the safety and reliability of both S_{11} and S_{12} during the fault isolation.

The discharge process of the input capacitor in the faulty submodule is illustrated by the equivalent circuit shown in Fig. 10. The voltage across the input capacitor $C_{\mathrm{in}1}$ of submodule 1 forms *RC* discharge loop through the current-limiting resistor.

Assuming an initial capacitor voltage is $V_{\mathrm{in}1}$, the residual voltage v_{C1} across the capacitor can be expressed accordingly

$$v_{C1} = V_{\mathrm{in}1} \cdot e^{-\frac{t}{R_{\mathrm{lim}1} C_{\mathrm{in}1}}}. \tag{11}$$

After a discharge period of $\Delta t = 4R_{\mathrm{lim}1}C_{\mathrm{in}1}$, the input capacitor voltage of submodule 1 drops to below 2% of its initial value, indicating that the vast majority of the stored energy has been safely dissipated. The maximum discharge current is denoted as $I_{\max}$. Based on the actual operating conditions, appropriate current-limiting resistors and dc contactors can be selected to ensure safe and reliable operation during fault isolation

$$I_{\max} = \frac{4V_{\mathrm{in}1}C_{\mathrm{in}1}}{\Delta t}. \tag{12}$$

3) Redundant Submodule Activation: When a faulty submodule is detected and bypassed, the redundant submodule R_e is subsequently activated. By default, all switching devices in the redundant submodule remain locked prior to activation. First, the bypass switch $S_{\mathrm{Re}2}$ of the redundant submodule is opened. Since the input capacitor of the redundant submodule changes from zero, a buffer resistor R_{limRe} is introduced into the charging path to limit the inrush current, thereby mitigating current surges. Next, as the voltage across the capacitor v_{inRe} reaches the predetermined startup threshold, the redundant submodule is soft-started by adjusting the control loop parameters. During this phase, both the switching frequency and duty cycle are regulated to further suppress inrush currents in the resonant tank and switching devices. Once the redundant submodule achieves a stable operational state, the switch $S_{\mathrm{Re}1}$ is closed, bypassing the buffer resistor R_{limRe} to minimize power loss during steady-state operation. Through this process, the system topology is reconfigured to restore fault-tolerant operation, while current surges are effectively suppressed throughout the entire transition. The startup control phase for the redundant submodule is illustrated by the equivalent circuit shown in Fig. 11.

In the initial phase of startup, all switching devices within the *LLC* converter redundant submodule remain locked. As illustrated in the equivalent circuit diagram in Fig. 11, the transient response for charging the input capacitor on the left side of the submodule can be described as follows:

$$\Delta V_{\mathrm{in}} = R_{\mathrm{lim\,Re}} C_{\mathrm{inRe}} \frac{dv_{\mathrm{inRe}}}{dt} + v_{\mathrm{inRe}} \tag{13}$$

where ΔV_{in} denotes the voltage portion of the bus voltage V_{in} allocated across the redundant submodule. Given that all submodule input capacitors are identical, ΔV_{in} will eventually approach V_{in}/n, where n is the total number of submodules. According on (13), the relationship between the voltage v_{inRe} across the input capacitor C_{inRe} and the current i_{CinRe} flowing through it can is given by

$$v_{\mathrm{inRe}} = \Delta V_{\mathrm{in}} \left(1 - e^{-\frac{t}{\tau}}\right) \tag{14}$$

$$i_{\mathrm{CinRe}} = C_{\mathrm{inRe}} \frac{dv_{\mathrm{inRe}}}{dt} = \frac{\Delta V_{\mathrm{in}}}{R_{\mathrm{lim\,Re}}} e^{-\frac{t}{\tau}} \tag{15}$$

where $\tau = R_{\mathrm{limRe}}\, C_{\mathrm{inRe}}$.

From (14) and (15), it can be deduced that the time required for the voltage across the input capacitor C_{inRe} to reach the predetermined startup value can be regulated by adjusting the current-limiting resistor. The maximum charging current is given by $I_{\mathrm{CinRe\_max}} = \Delta V_{\mathrm{in}}/R_{\mathrm{limRe}}$. Therefore, in the design of the buffer current-limiting resistor, it is crucial to ensure that the maximum current withstand for the devices such as dc contactors, denoted as $I_{\max}$, does not exceed the peak charging current, that is, $I_{\max} < I_{\mathrm{CinRe\_max}}$, to guarantee equipment safety.

In the second phase of startup, when the voltage across the input capacitor of the redundant submodule reaches the preset soft-start threshold, the redundant *LLC* converter submodule commences operation and begins charging the output filter capacitor. To mitigate current stress on the output capacitor, the startup sequence initially employs a high switching frequency

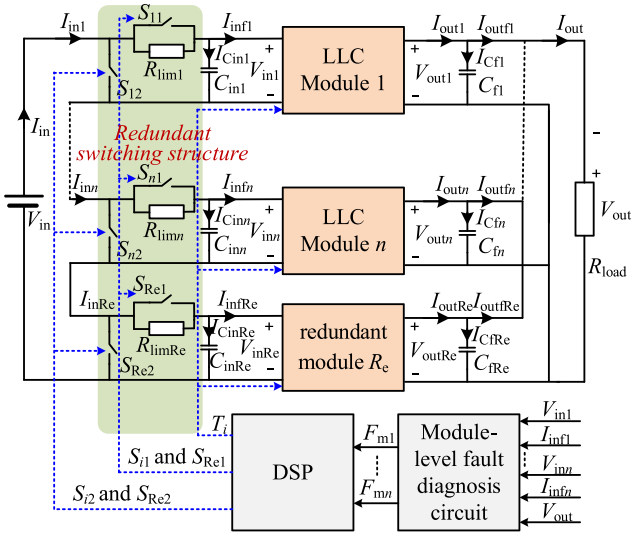

Fig. 12. Schematic diagram of the fault-tolerant topology for a subsea ISOP-type DC converter.

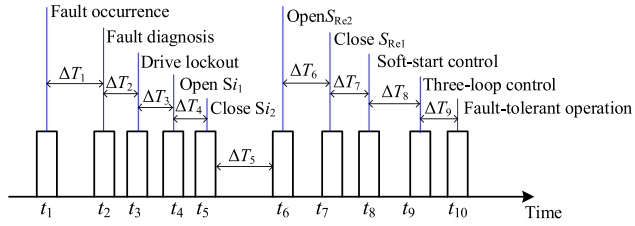

Fig. 13. Timing diagram for fault-tolerant control of subsea ISOP-type dc converter system.

and a small duty cycle. Subsequently, the switching frequency is gradually reduced to the resonant frequency, while the duty cycle is increased to its rated value. This allows the output capacitor to be charged smoothly to the rated output voltage. As depicted in Fig. 11, the transient equation at the output side during the soft-start process can be expressed as follows:

$$R_{\mathrm{CfRe}}C_{\mathrm{fRe}}\frac{dv_{\mathrm{CfRe}}}{dt}+v_{\mathrm{CfRe}}=v_{\mathrm{cd}} \tag{16}$$

$$v_{\mathrm{CfRe}}=v_{\mathrm{cd}}\left(1-e^{-\frac{t}{R_{\mathrm{CfRe}}C_{\mathrm{fRe}}}}\right) \tag{17}$$

where v_{cd} denotes the voltage on the secondary side of the high-frequency isolation transformer. By appropriately controlling the duty cycle and switching frequency, the output voltage can be gradually increased. This approach reduces the current impact on the output circuit and ensures the safety of the secondary-side uncontrolled rectifier diodes as well as the output filter capacitor.

C. Fault-Tolerant Operation Method and Timing Design

Based on the previously analyzed fault characteristics and diagnostic methods, and in conjunction with the fast and smooth redundancy switching control strategy tailored for subsea ISOP converters, an integrated fault-tolerant operation scheme is developed. The schematic diagram of the fault-tolerant topology for a subsea ISOP-type dc converter is presented in Fig. 12. This topology primarily consists of the ISOP converter power circuit, redundancy switching circuit, module-level fault diagnosis circuit, and a DSP control circuit.

The module-level fault diagnosis circuit is implemented according to the proposed fault characteristics and diagnostic principles of the submodules, and is utilized for the detection and localization of faulty modules. The DSP controller, which is a microcontroller widely used for digital signal processing, is responsible for executing the main control functions. In addition to routine control tasks, it also manages fault redundancy switching control. The fault-tolerant operation control scheme acquires the input voltage, input current, and output voltage of each submodule for module-level fault diagnosis, and subsequently transmits the diagnostic results to the DSP. Based on these results, the main controller executes redundancy switching control by isolating the faulty modules and activating the redundant modules. The reconfigured topology is then operated under closed-loop control to restore normal operation.

Fig. 13 presents the timing diagram for fault-tolerant operation control of the subsea ISOP dc converter system. Suppose that at t_1, a fault occurs in submodule i. After a detection delay of ΔT_1, at t_2, the fault diagnosis module is activated. By utilizing sensors to monitor the submodule input voltage and current $V_{\mathrm{in}n}$, $I_{\mathrm{inf}n}$ and output voltage V_{out}, the fault diagnosis principle described in Section II is employed to accurately identify the location of the faulty module. The internal module-level fault diagnosis is completed within ΔT_2.

After the faulty module is identified at t_3, the DSP main controller sends a gate-blocking signal T_i to the subcontroller of the faulted module. Within ΔT_3, the gate signals of the power switches in the faulty module are blocked, thereby preventing further damage to the ISOP converter caused by the fault. Once gate blocking is complete at t_4, the DSP main controller transmits a bypass switch disconnection command for the current-limiting resistor to the subcontroller of the faulty module, prompting switch S_{i1} to open within ΔT_4. Since nonfully controllable switching devices such as dc contactors are utilized to minimize conduction losses, ΔT_4 is typically on the order of milliseconds. This operation is intended to insert the current-limiting buffer resistor $R_{\mathrm{lim}i}$ in preparation for the subsequent step, thereby limiting the discharge current of the input capacitor and preventing component damage due to inrush current.

Following the disconnection of switch S_{i1} at t_5, the DSP main controller sends a submodule bypass switch closure signal to the subcontroller of the faulty module, driving switch S_{i2} to close. At this stage, the input terminals of the faulty submodule are bypassed by switch S_{i2}, ensuring that energy is no longer transferred to the faulty submodule. The input current is redirected to flow through switch S_{i2}, circulating among the normal modules. Upon closure, switch S_{i2} forms a discharge path with the current-limiting resistor $R_{\mathrm{lim}i}$ and the input capacitor, as previously analyzed. The entire process is completed within ΔT_5.

Once the energy stored in the input capacitor of the faulty submodule is fully discharged, the system proceeds to activate the redundant module. At t_6, the DSP main controller sends a command to the subcontroller of the redundant module to disconnect the bypass switch $S_{\mathrm{Re}2}$, thereby opening switch S_{Re}.

TABLE II
KEY PARAMETERS OF THE ISOP-TYPE SUBSEA DC CONVERTER

Parameters	Value
Number of modules	3
Input voltage V_{in}	1500–3000 V
Output voltage V_{out}	375 V
load	4.6875 Ω
Switching frequency f	100 kHz
Number of redundant modules	1
resonant inductance L_r	52 μH
resonant inductance L_m	364 μH
resonant capacitance C_r	43.9 nF

At this stage, the switch of the redundant module is unblocked, and the bus voltage charges the input capacitor C_{inRe} through the buffer current-limiting resistor R_{limRe} until the input capacitor voltage V_{inRe} reaches the preset soft-start threshold. This process is completed within ΔT_6.

Once the input capacitor voltage reaches the pre-set voltage at t_7, the DSP sends a signal to the subcontroller of the redundant module to close the bypass switch for the current-limiting resistor, thereby closing switch S_{Re1}within ΔT_7, thereby reducing power losses during subsequent normal operation.

After confirming that switch S_{Re1} is closed at t_8, the DSP main controller sends a soft-start control signal to the subcontroller of the redundant module. In the initial stage of soft-start, the switching frequency is set to 1.5 times the rated frequency, and the duty cycle is set to 10%. Subsequently, the switching frequency is linearly decreased to the rated value, while the duty cycle is gradually increased to its nominal value. This approach limits the output voltage slew rate and prevents component damage from inrush current stress during startup. The entire soft-start process is completed within ΔT_8.

After the soft-start process of the redundant module is completed at t_9, the DSP controller transitions from the soft-start control program to the three-loop control scheme. The sampled input voltage and output current of the redundant module are utilized in the voltage equalization loop and the inner control loop of the output circuit. The program transition and control adjustment are accomplished within ΔT_9.

This sequence completes topology reconfiguration and control adjustment processes. At t_{10}, the entire subsea ISOP converter system resumes stable operation, thereby successfully realizing fault-tolerant operation following the occurrence of a fault.

IV. EXPERIMENT AND RESULTS

To evaluate the effectiveness of the proposed fault-tolerant strategy for subsea dc converters, fault-tolerant simulation experiments were performed. The key parameters are summarized in Table II, and the results for the proposed method are illustrated in Fig. 14(a).

For comparison, additional simulations were performed under the identical conditions using two conventional fault-tolerant methods: direct isolation of the faulty module and isolation combined with activation of a redundant submodule. The corresponding results are shown in Fig. 14(b) and (c), respectively. In Fig. 14, the upper traces represent the input voltage of each submodule, while the lower trace displays the output voltage.

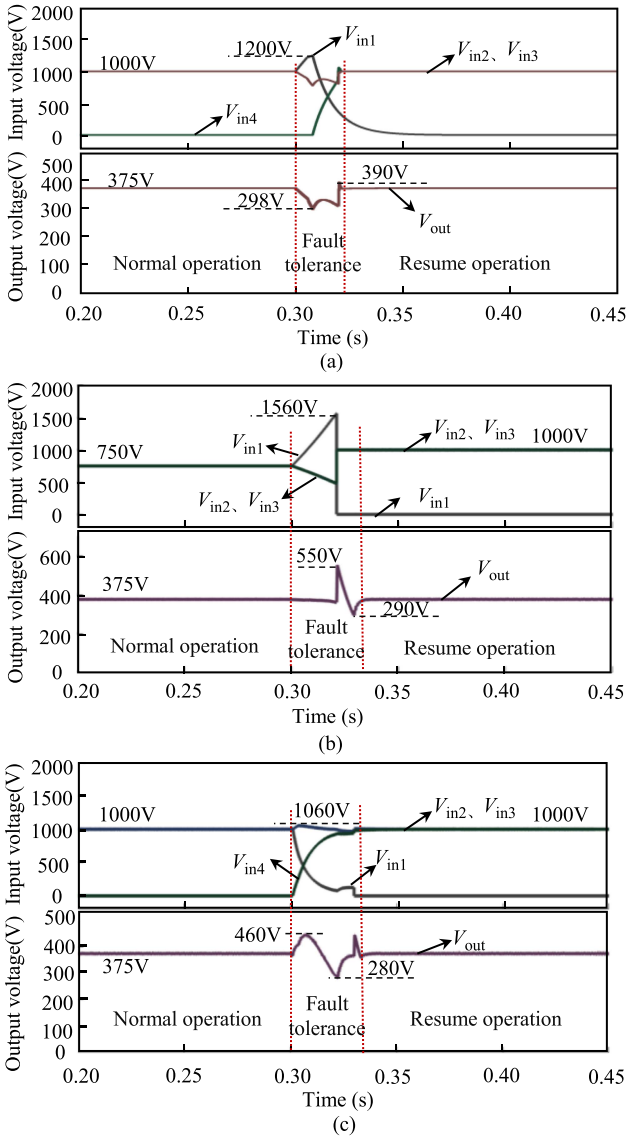

Fig. 14. Fault-tolerant simulation results of the proposed and conventional methods. (a) Fault-tolerant process using the proposed method. (b) Fault-tolerant process with direct isolation of the faulty module. (c) Fault-tolerant process utilizing traditional redundancy switching.

Fig. 14(a) illustrates the simulation results of the proposed fault-tolerant method applied to a 3+1 ISOP dc converter (three functional submodules and one redundant submodule). At 0.3 s, an open-circuit fault occurs in submodule 1. After fault detection, localization, isolation of the faulty submodule, and activation of the redundant module, the converter successfully restores normal operation. Throughout the entire fault-tolerant process, the maximum input voltage of the submodule reaches 1200 V. The output voltage exhibits a maximum transient drop to 298 V (−20.5%) and a maximum overshoot to 390 V (+4%).

TABLE III
COMPREHENSIVE COMPARISON RESULTS BETWEEN THE PROPOSED METHOD AND EXISTING METHODS

	Proposed method	Method of direct isolation of the faulty module, such as [14]	Method utilizing traditional redundancy switching, such as [17]
Maximum input voltage overshoot of submodules	1200 V	1560 V	1060 V
Maximum output voltage overshoot of the system	390 V (4% ↑)	550 V (46.7% ↑)	460 V (22.7% ↑)
Maximum output voltage drop of the system	298 V (20.5% ↓)	290 V (22.7% ↓)	280 V (25.3% ↓)
Number of additional components	Small	Small	Medium
Complexity	Medium	Simple	Medium

Fig. 14(b) illustrates the simulation results of the direct isolation method applied to a 4+0 ISOP dc converter (four functional submodules, no redundancy). As this method does not utilize redundant modules, the converter is designed to maintain normal operation following the isolation of the faulty submodule. Throughout the process, the maximum input voltage of the submodule reaches 1560 V. The output voltage exhibits a maximum transient drop to 290 V (−22.7%) and a maximum overshoot to 550 V (+46.7%).

Fig. 14(c) illustrates the simulation results of the traditional direct fault redundancy switching method applied to a 3+1 ISOP dc converter (three functional submodules and one redundant). Throughout the process, the maximum input voltage of the submodule reaches 1060 V. The output voltage exhibits a maximum transient drop to 280 V (−25.3%) and a maximum overshoot to 460 V (+22.7%).

The comprehensive comparison between the proposed fault-tolerant method and the existing method is presented in Table III.

The proposed method achieves slightly reduced fluctuations in submodule input voltage during the fault-tolerant process. More importantly, it substantially lowers the maximum output voltage drop to only 20.5%, and limits the output voltage overshoot to 4%, the smallest among the evaluated methods. By effectively mitigating output voltage and current stress on the ISOP dc converter, the proposed fault-tolerant method enhances power supply reliability for high-precision and high-sensitivity subsea loads.

To further validate the effectiveness of the proposed module-level fault-tolerant method for the subsea ISOP converters, a 2+1 cascaded ISOP-type subsea dc converter prototype was developed, as illustrated in Fig. 15. The key parameters are provided in Table II. Relevant experiments were conducted on a 2000-V laboratory testing platform.

Fig. 16 presents the module-level redundancy-switching experiment for an ISOP-type dc converter under an open-circuit fault in the power switching tube of submodule 1. The input was

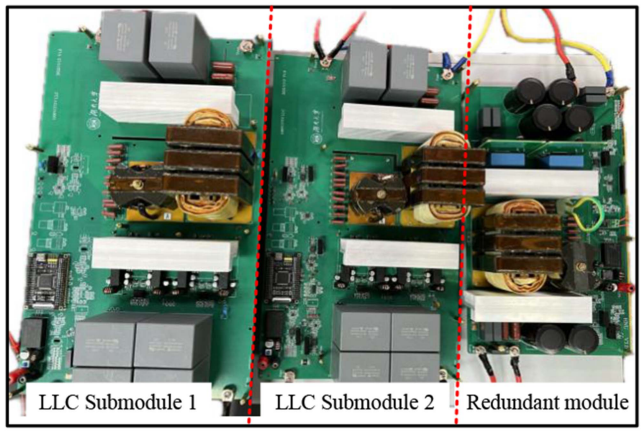

Fig. 15. Prototype of the ISOP-type subsea DC converter.

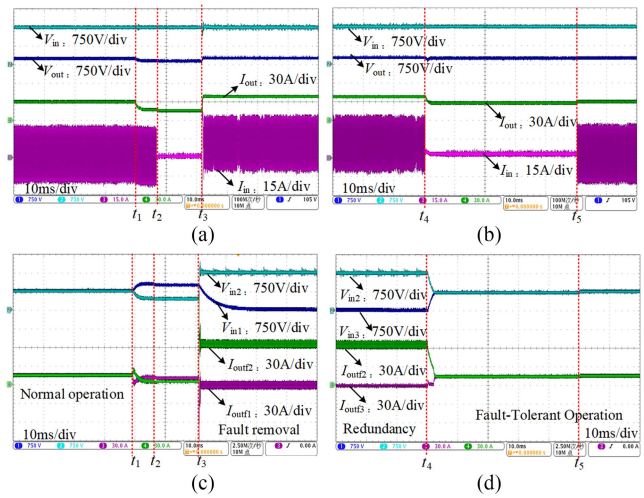

Fig. 16. Fault-tolerant operation waveforms of the ISOP-Type DC converter. (a) Port waveforms of the converter during faulty-module isolation. (b) Port waveforms of the converter during redundant-module activation. (c) Port waveforms of the submodule during faulty-module isolation. (d) Port waveforms of the submodule during redundant-module activation.

set to 1500 V to emulate source fluctuation. Fig. 16 shows the input voltage V_{in} and current I_{in}, output voltage V_{out} and current I_{out} of the converter system, input voltage V_{in1}, V_{in2} and output current I_{outf1}, I_{outf2} of the healthy submodules, input voltage V_{in3} and output current I_{outf3} of the redundant submodule. Owing to oscilloscope channel limitations, the sequence was captured in two steps: faulty-module isolation in Fig. 16(a) and (c), and redundant-module activation in Fig. 16(b) and (d).

The fault-tolerant operation process can be delineated into six distinct stages. As shown in Fig. 16(a) and (c), the ISOP converter operates under normal conditions until t_1, when an open-circuit fault occurs in the power switching tube of submodule 1. At this instant, the input voltage of the converter remains constant at 1500 V, while the input current exhibits a slight decrease. Owing to the open-circuit fault in submodule 1, its input voltage V_{in1} increases, whereas the input voltage of the healthy submodule 2 decreases, eventually stabilizing in the fault steady-state phase. Simultaneously, the output current

I_{outf1} of the faulty submodule 1, exhibits a sharp initial decrease, followed by a gradual return to steady-state. In contrast, the output current I_{outf2} of the healthy submodule 2 shows a sharp initial increase and then gradually decreases to a steady-state value. Consequently, the output voltage V_{out} of the converter drops to nearly half its nominal value, and the output current I_{out} is similarly reduced by approximately half. The extent of this reduction is inversely proportional to the number of cascaded modules. That is, with more modules, the voltage and current drop is less pronounced. The experimental results closely align with the analytical predictions for submodule faults.

After approximately 7 ms, at t_2, the bypass switch S_{11} is turned OFF. Owing to the use of a dc contactor, the switching action occurs on the millisecond timescale. With the current-limiting resistor engaged, the input current is restricted, resulting in a decrease in the output current while exerting minimal impact on other electrical quantities. Approximately 15 ms later, at t_3, the bypass switch S_{12} of submodule 1 is closed, thereby isolating and isolating the faulty submodule from the system. The input capacitor of the faulty submodule discharges through the current-limiting resistor, causing its input voltage to decay exponentially. Simultaneously, the input voltage of the healthy submodule increases as it assumes the voltage previously supported by the faulty module. Consequently, the output current of the healthy submodule increases, while that of the faulty submodule approaches zero. As the input voltage of the healthy module increases, its output voltage also exhibits a slight increase. With a greater number of submodules, the redistribution of the faulty module's voltage facilitates rapid stabilization of the system output voltage. Throughout this process, the input voltage of the converter remains constant, and the input current exhibits a slight increase. After about 50 ms, the faulty module is fully isolated.

According to Fig. 16(b) and (d), at t_4, the bypass switch S_{Re2} of the redundant module is turned OFF. The input capacitor of the redundant submodule begins charging through the current-limiting resistor, while the healthy submodule simultaneously discharges, resulting in a faster voltage increase across the redundant module compared to the discharge rate of the capacitor of the faulty submodule.

During this process, the control of the redundant module is activated, regulating the input voltages V_{in2} and V_{in3} of submodules 2 and 3 to approximately 750 V. Correspondingly, the output currents I_{outf2} and I_{outf3} also stabilize at balanced values, thereby restoring the system output voltage to its nominal level. Due to the current-limiting resistor, the input current of the converter decreases, resulting in the output current and the output currents of the submodule that are temporarily lower than their normal values. After 50 ms of reconfiguration, the ISOP converter closes the bypass switch S_{Re1}, and at t_5, the converter system resumes normal operation. The entire process is completed in approximately 122 ms.

The experimental results demonstrate that the proposed fault-tolerant operation method enable module-level redundancy switching for the subsea ISOP dc converter without inducing significant current surges. It effectively restores normal operation following a fault, thereby ensuring stable output of the system.

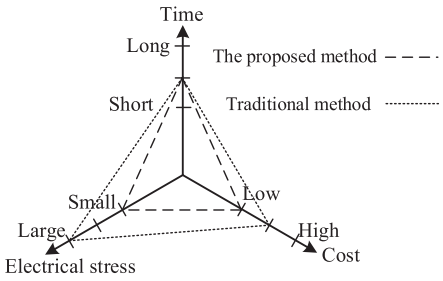

Fig. 17. Comparison between the proposed fault-tolerant method and conventional methods.

Fig. 17 presents a comprehensive comparison between the fault-tolerant method proposed in this work and conventional methods focusing electrical stress, cost, and time consumption. Traditional methods typically perform the isolation of the faulty module and activation of the redundant module as separate steps, or only isolate the faulty module without redundancy activation, as described in [14]. While these methods can achieve fault-tolerant control, they often overlook the electrical stress imposed during module isolation and switching. Combined approaches, such as that described in [17], integrate fault isolation with redundancy activation to reduce the total fault-tolerant response time. However, in these methods, the charging and discharging of capacitors during the isolation and activation processes are highly coupled, leading to uncontrolled current stress particularly problematic in subsea applications, where capacitor charging and discharging currents cannot be effectively limited.

In contrast, the method proposed in this article continues the practice of performing module isolation and redundancy activation sequentially. Although this method does not offer a significant advantage in terms of total operation time, it incorporates the reuse of current-limiting resistors throughout the fault-tolerant process. This innovation effectively restricts the capacitor charging and discharging currents, thereby minimizing voltage and current overshoots during both the isolation of the faulty module and the activation of redundancy. Furthermore, as the current-limiting resistors are reused and no additional sensors are required for fault diagnosis, the proposed method results in relatively low implementation cost. Finally, by closely integrating the fault-tolerant process with fault diagnosis, the proposed method provides a comprehensive and robust solution for medium-voltage subsea dc converter applications.

V. Conclusion

This article proposes a multilevel collaborative fault-tolerant operation method for subsea ISOP-type dc converters, specifically addressing the dual challenges of fault tolerance and high transient electrical stress under limited electrical quantity monitoring and wide input voltage fluctuations. The main conclusions are as follows.

1) The proposed fault diagnosis method abandons the traditional fixed threshold approach and instead exploits the differences in both amplitude and rate of change of voltage, and current time-domain characteristics among submodules during the early stages of a fault. This enables

online monitoring and precise localization of the faulty submodule, while exhibiting low sensitivity to input-voltage fluctuations.

2) The proposed smooth redundancy switching strategy effectively mitigates the transient electrical stress, such as capacitor charging and discharging, that can affect healthy modules during switching events in conventional methods. This method enables millisecond-level fault-tolerant operation following a fault, thereby significantly enhancing the reliability and operational robustness of subsea dc power supply systems.

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