A DHTOL Test-Based Methodology to Investigate the Switching Reliability of GaN HEMTs Under Repeated Drain Voltage Ringing

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***Abstract*—The dynamic high-temperature operating lifetime (DHTOL) test is used to validate the product level robustness of a device in interaction with other system components and various product operating modes. This article presents a DHTOL-based test methodology for investigating the switching reliability of gallium nitride high electron mobility transistors in applications involving large drain-to-source voltage ringing. To conduct this study, a highly scalable, modular and reconfigurable test bench architecture is presented that can simultaneously test multiple devices under realistic stress conditions. The test vehicles are designed to replicate the switching stress typical of a quasi-resonant flyback converter while optimizing overall power consumption. In addition, the setup includes features for inline dynamic $R_{DS,\mathrm{ON}}$ monitoring, enabling user-friendly tracking of the changes of this key parameter throughout the test duration. This real-time monitoring capability is highly beneficial for understanding and gaining valuable insights into the evolution of the devices' $R_{DS,\mathrm{ON}}$ under continuous stress conditions. Using a prototype of the proposed test bench, multiple samples from three different device vendors are stressed under two distinct test conditions each. All tests are conducted over an intended duration of 1000 h and a detailed description of the results observed is also presented in this article.**

***Index Terms*—Dynamic high-temperature operating lifetime (DHTOL), gallium nitride (GaN) high electron mobility transistors (HEMTs), quasi-resonant (QR) flyback converter, reliability.**

I. Introduction

GALLIUM nitride (GaN)-based semiconductor devices exhibit superior electron mobility and higher electron saturation velocity, making them highly suitable for high-frequency applications. GaN also has a very high breakdown electric field, thus enabling the fabrication of devices with lower specific ON-state resistance. Presently, commercially available GaN devices are limited to lateral structure-based devices, commonly known as GaN high electron mobility transistors (HEMTs) [1], [2], [3], [4]. In GaN HEMTs, a 2-D electron gas formed between an AlGaN/GaN heterostructure acts as the conduction channel. This mechanism distinguishes GaN HEMTs from traditional silicon-based MOSFETs and IGBTs at a fundamental level. This unique structure comes with certain advantages, such as the absence of a PN junction, which eliminates the reverse recovery effect as well as the avalanche voltage limit commonly present in Si MOSFETs. However, this uniqueness also presents its own set of challenges in terms of design specifications and device reliability, for which traditional evaluation techniques may not be adequate [5], [6], [7]. One such issue is regarding the transient voltage withstand capability of GaN HEMTs. For a conventional Si MOSFET, its maximum operational voltage specified in the datasheet is typically its avalanche limit; once this limit is crossed, the device no longer blocks voltage. The voltage it can withstand beyond this limit and the frequency of such events depend on its thermal limit. A well-established method, unclamped inductive switching (UIS), is generally used to evaluate the avalanche ruggedness of these devices. In contrast, GaN HEMTs do not experience avalanche, and manufacturers often specify a value significantly lower than the breakdown limit due to various reliability concerns, such as time dependent dielectric breakdown and others [8]. However, GaN HEMTs can safely withstand transient voltages of short duration exceeding these specified limits. Recognizing this, many commercial vendors have begun specifying a separate transient voltage limit in addition to the static blocking voltage limit. A jedec-joint electron device engineering council (jedec) guideline, JEP 186, for specifying a transient OFF-state withstand voltage has also been published [9]. Despite this, a standardized testing methodology for determining the peak transient voltage limit of these devices remains undeveloped.

The most popular range of GaN HEMTs available in the market is of the voltage ratings 600–650 V. These are particularly well-suited for low-power applications in consumer electronics. Among power levels ranging from 60 to 120 W, the quasi-resonant (QR) flyback topology reigns supreme due to its

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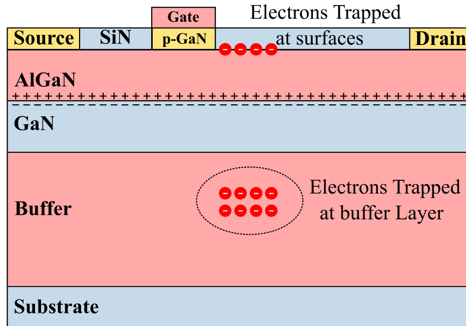


Fig. 1. Charge trapping in GaN HEMTs.

lower component count and straightforward compensation techniques. In a QR flyback setup, the interaction between the magnetizing inductance of the flyback transformer and the parasitic capacitance of the switch facilitates turning on the device under near-zero voltage conditions. Typically, a QR flyback converter incorporates an resistor, capacitor (RCD) clamp circuit to dissipate excess energy stored in the transformer's leakage inductance, protecting the primary switching device from significant voltage spikes during turn-OFF. However, this measure leads to decreased overall converter efficiency, particularly as clamping requirements become more stringent. For silicon-based devices, it is standard practice to limit ringing voltages to less than 80% of the device's rated voltage to avoid avalanche breakdown during normal operation. In contrast, GaN HEMTs are designed with breakdown voltages significantly higher than their rated voltages, allowing them to tolerate substantial transient overvoltages without avalanching. Consequently, utilizing GaN switches in these applications can enhance efficiency by reducing clamping voltage requirements. This transient withstand capability of GaN switches could also be leveraged to improve efficiency in other similar isolated topologies, such as regular flyback and forward converter. Nonetheless, repeated exposure to high-voltage transients may adversely impact the device's performance and reliability. Hence, it is crucial to comprehensively investigate the impact of these repeated transients on device performance under realistic test conditions.

One of the most significant concerns associated with GaN HEMTs is its switching reliability [10] or parametric stability as defined in some manuscripts [5], [11] under actual use conditions of power electronics products. Due to their lateral conduction channel and often being grown on a foreign substrate, typically Si, GaN HEMTs are increasingly susceptible to carrier trapping effect in buffer and near interface regions, as shown in Fig. 1. The presence of charge trapping induces a phenomenon known as dynamic ON-state resistance ($d.R_{DS,\mathrm{ON}}$) in these devices. This results in an increased resistance above its dc value immediately upon being turned ON after a high blocking stress. Extensive research has been conducted on and, focusing on its physical origins, relationship with operational parameters, and mitigation strategies [12], [13], [14], [15], [16]. These studies highlight several sources that affect trapping, e.g., the charges resulting from leakage currents induced by high blocking voltage [17], [18] and hot carriers injected (HCI) during a hard transient event [19], [20]. Furthermore, the impact of $d.R_{DS,\mathrm{ON}}$ is strongly influenced by factors, such as the magnitude of the breakdown voltage, junction temperature, and the duration of relaxation allowed, after high voltage switching events [21], [22], [23]. Hence, it is necessary to consider the specific application requirements when evaluating the reliability of GaN devices. To address this need, JEDEC has established guidelines for GaN transient reliability in the JEP 180 publication [24]. JEP 180 guides on the implementation of dynamic high-temperature operating lifetime (DHTOL) testing at the application level. This involves subjecting the devices to varied dynamic conditions at elevated junction temperatures. Unlike typical accelerated lifetime tests (ALTs) that aim to induce a specific mode of failure, DHTOL is designed to ensure system-level reliability. While the publication offers guidelines, there is currently no fixed procedure for executing the test. However, in all cases, the test necessitates the use of a product test vehicle capable of replicating the stress profile of the targeted application for the device. Compared to typical test vehicles used in ALTs, product vehicles entail more complex application-oriented circuits and often require in-situ measurement capabilities. This can create a lot of issues while performing the DHTOL test on a large number of samples. For instance, $d.R_{DS,\mathrm{ON}}$, a widely used parameter for indicating switching stability in GaN HEMTs, necessitates a high-speed sensing circuit, typically within 1 μs from turn-ON. In addition, testing numerous converter-based product vehicles often requires substantial input power and high output power dissipation capabilities. Furthermore, when applying thermal stress to the device under test (DUT), it is crucial to prevent the aging of peripheral components within the test vehicle, as this could mask DUT-related failures by causing failures in weaker non-GaN components.

TABLE I
SUMMARY OF SYSTEM LEVEL QUALIFICATION TESTS DONE BY SOME KEY GAN MANUFACTURERS

Ref.	Test vehicle	Power consumption
[25]	Boost converter	High
[26]	Boost converter	High
[27]	DPT with RL load	Medium
[28]	DPT with L load	Low
[29]	H-bridge with RC load	Low
[30]	H-bridge with LC load	Low

To ensure the switching reliability of GaN HEMTs, most commercial vendors now publish DHTOL data, sometimes labeled as just extended reliability tests conducted over 1000 h or more, using their own product vehicles. Table I summarizes the test strategies employed by various vendors to qualify their devices. The authors in [25] and [26] used a boost converter as the test topology to induce hard switching stress on the DUT. Smith et al. [25] monitored efficiency drop as the failure parameter, while Wong et al. [26] tracked the increase in $d.R_{DS,\mathrm{ON}}$. koshi et al. [27] employed a double pulse tester-based circuit with an RL load, which uses less power compared to an actual power converter. Bahl et al. [28] further reduced power consumption by using a DPTDouble Pulse Testing (DPT) with an L load, improving scalability in terms of sample testing. However, both methods achieve lower power consumption by limiting the duty

cycle and frequency, thus reducing flexibility. Lin et al. [29] introduced a modified half-bridge test vehicle with an *RC* load, offering lower power consumption and greater flexibility in acceleration parameters. Fichtenbaum et al. [30] used a half-bridge circuit with an *RL* load to stress two DUTs simultaneously, one under hard switching and the other under soft-switching conditions. In addition, Tayyab et al. [31] presented a methodology for designing and performing DHTOL tests by incorporating parasitic elements and thermal modeling of the test board. All these tests aim to explore and validate the switching reliability of GaN HEMTs under hard turn-ON or third-quadrant soft turn-ON conditions. Few approaches have assessed device performance in applications with significant drain node voltage ringing. Although the authors in [26] and [30] and leveraged similarities between their test vehicle stress profiles and a QR flyback waveform for qualification, they do not account for the effects of ringing spikes. This is particularly important, as such voltage profiles are common in single-switch isolated power converter topologies, which are increasingly used in low-power offline applications like laptop adapters and chargers—key markets for GaN HEMTs.

Most studies available in the literature regarding the transient voltage withstand capability of GaN HEMTs focus on the dynamic breakdown limit or the point at which the device experiences irreversible failure [32], [33], [34], which are typically around twice the datasheet limit. These studies help define the safe transient voltage a DUT can withstand during nonrepetitive events, such as line surges or start-up transients. However, they do not explore the safe transient voltage limit GaN HEMTs can endure at high frequency continuous switching without impacting their parametric stability. To address this, Zhang et al. [35] presented a study characterizing device parametric stability through in-situ monitoring of $d.R_{DS,\mathrm{ON}}$ while subjected to repetitive overvoltage up to 150% of the device's rated voltage using an UIS setup. Similarly, Zhang et al. [36] used the same circuit to propose a drain overvoltage specification based on characterized $d.R_{DS,\mathrm{ON}}$ shifts. However, these studies apply stress in the form of periodic overvoltage surges with zero voltage blocking periods in between, which do not fully represent the actual stress profiles experienced by devices in converter applications. Moreover, it is also essential to address the scalability of the test methodology execution when used as a qualification procedure with multiple device samples needing to be tested.

This article presents a methodology for assessing the switching reliability of GaN HEMTs in applications with significant drain-to-source voltage ringing, most often caused by leakage inductance from the isolation element in the power loop. The approach involves conducting DHTOL using a specialized application-specific test vehicle while monitoring shifts in $d.R_{DS,\mathrm{ON}}$ through an in-line measurement circuit. To support this methodology, the authors introduce a highly scalable, modular, and reconfigurable test bench designed to accommodate diverse testing conditions. The test bench integrates multiple product test vehicles, each dedicated to a single DUT, ensuring independent stress application and scalability. These test vehicles are specifically designed to replicate the operational stress experienced by a primary switch in a QR converter, making it highly representative of real-world applications. In addition, the test vehicle offers flexibility in accelerating test conditions, including temperature, frequency, and voltage. The proposed system primarily addresses two key issues associated with performing system-level stress testing on a large number of device samples.

1) For GaN HEMTs, the dynamic ON-state parameter is a clear indicator of charge trapping. Hence, it is beneficial to monitor their $d.R_{DS,\mathrm{ON}}$ throughout the DHTOL test duration. A common practice involves shutting down the test at specific intervals to use in-situ or external measurement setups for characterizing $d.R_{DS,\mathrm{ON}}$. However, this approach does not account for the cumulative effects of charge trapping in a continuous stress environment and disrupts the continuity of the DHTOL test. Therefore, it is more effective to use inline measurement features to monitor $d.R_{DS,\mathrm{ON}}$ while the test is running. Obtaining the sensed inline data for the end user can be a complex process. When testing a large sample size, using a digital oscilloscope increases the cost and adds more postprocessing burden on the user, thus affecting the scalability of the test bench. The presented architecture incorporates an analog-to-digital converter (ADC) + digital-to-analog converter (DAC)-based scheme to sample and streamline the data for $d.R_{DS,\mathrm{ON}}$ estimation throughout the test duration in a more user-friendly manner.
2) DHTOL requires a product test vehicle based on the converter topology for which the application demands. These converter-based test vehicles often necessitate an external load bank to dissipate the output power. Testing a large batch of devices can lead to significant power wastage and an increased load bank size requirement. In addition, using resistive loads for continuous power dissipation throughout the test duration might raise the room temperature. Therefore, it is crucial to manage the power flow in and out of each test vehicle in an optimized and efficient manner. The presented test bench features a novel test vehicle power circuit that subjects the DUTs to a stress profile similar to that of a primary FET in a QR flyback converter, while recirculating power within itself to reduce power consumption.

The rest of this article is organized as follows. Section II provides an overview of the proposed test bench architecture. Section III offers a detailed account of the test bench system implementation. Section IV details the results observed when multiple device samples from three different vendors were subjected to DHTOL tests using the developed prototype under two different test conditions. Finally, Section V concludes this article with final remarks and considerations for future research.

II. Large Scale Dynamic HTOL Test Bench Architecture

To facilitate simultaneous stress testing of multiple devices, a highly scalable dynamic high-temperature operating life (DHTOL) test bench architecture has been introduced. This

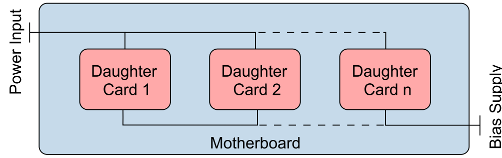


Fig. 2. High-level block diagram of the proposed test bench: The "power input" provides the DC-link voltage across each daughter card, which applies the electrical stress. The bias supply delivers the auxiliary power needed to bias the control and measurement ICs, as well as the heating resistor within each daughter card. In this setup, the power input to each daughter card is designed to recycle within itself, eliminating the need for external load banks.

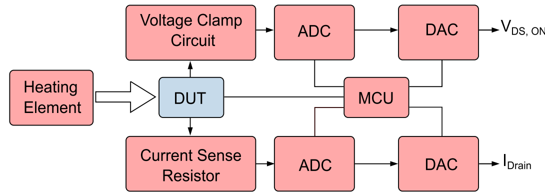
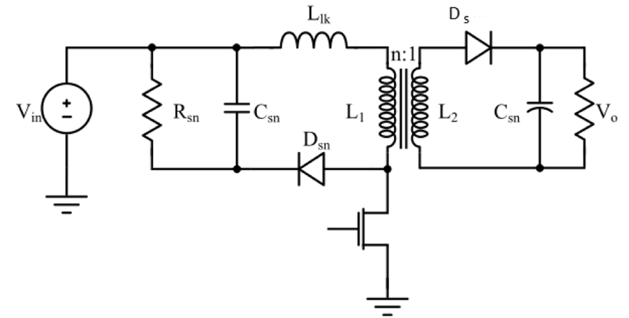
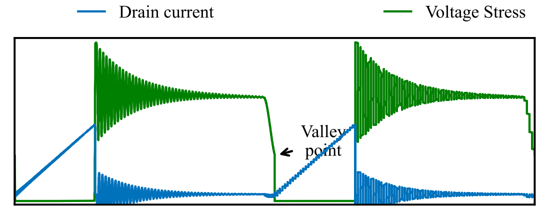


Fig. 3. High-level overview of the product test vehicle.



(a)



(b)

Fig. 4. (a) Schematics of a typical QR-flyback converter. (b) Typical QR flyback voltage and current waveforms.

architecture is designed to efficiently handle a large number of devices, ensuring each one undergoes rigorous testing under high-temperature conditions. As shown in Fig. 2, the test bench consists of a main motherboard that houses several daughter cards. Each daughter card acts as a test vehicle, holding DUT and providing the necessary connections for testing. The motherboard serves as a common interface to inject high voltage input, subjecting the DUTs in each daughter card to stress conditions. It also supplies the bias power required for the control and measurement ICs within each test vehicle. In addition, the motherboard provides mechanical support for each of the product test vehicles. The modular nature of the design allows for easy addition or removal of daughter cards as needed, providing flexibility in the testing process.

A. Overview of the Developed Product Test Vehicle

Fig. 3 provides a high-level overview of the proposed product test vehicle. Each test vehicle is equipped with a separate microcontroller dedicated for control and measurement tasks. To accurately estimate the dynamic on-state resistance, our approach utilizes discrete high-speed ADCs to independently sample current and voltage across the DUT in a synchronous manner in sequence with the turn-on event. The captured data from the ADCs is then transmitted to discrete DACs within the card for conversion back into analog values. These analog voltage and current values can be easily captured by an external data acquisition system throughout the entire test duration. The obtained data enables monitoring of the relative shift in the dynamic resistance value, facilitating reliability studies. In addition, each daughter card incorporates features for providing localized heating to the DUTs. The design also includes provisions for closed-loop control of the DUT temperature. For detailed explanation, each product vehicle can be divided into three stages: a power stage, a sensing stage, and a localized heating system, each serving distinct functions as discussed below.

1) Power Stage: The power stage of the daughter card is based on a QR flyback converter. As mentioned in the previous sections, not only is QR flyback the most popular choice of power supply for the targeted power level, but also a topology in which the unique transient withstand capability of GaN HEMT could be leveraged. Fig. 4 illustrates the schematics and waveform of a typical QR flyback converter with a passive RCD clamp [37]. Similar to a normal DCM flyback converter, when the switch turns OFF, the energy stored in the leakage inductance of the flyback transformer resonates with the parasitic capacitance—primarily from the primary switch—resulting in a ringing effect, as shown in Fig. 4. The frequency and duration of this ringing depend on the parasitic elements in the circuit, while the peak ringing voltage is controlled by designing the clamp circuit appropriately to protect the device. In addition, when all the energy is transferred from the inductor to the output capacitor, another resonance occurs between the magnetizing inductance of the transformer and the device's parasitic capacitance. During this resonant subinterval, the voltage across the switch reaches its minimum value, known as the valley point, given by $V_{\text{in}} - nV_o$. The controller monitors the switch voltage and aims to turn on the device at this valley point to minimize turn-ON switching losses. The extent to which zero-voltage switching is achieved depends on both the output voltage and the transformer's turns ratio.

The circuit diagram of the proposed test vehicle power stage is illustrated in Fig. 5(a). Here, the output of the converter is fed back to its input while replicating the same electrical stress on the DUT as in a normal QR flyback converter. Through careful selection of the turns ratio and duty cycle, energy is efficiently recycled between the input capacitor and the flyback inductor. Consequently, the input source is only required to compensate

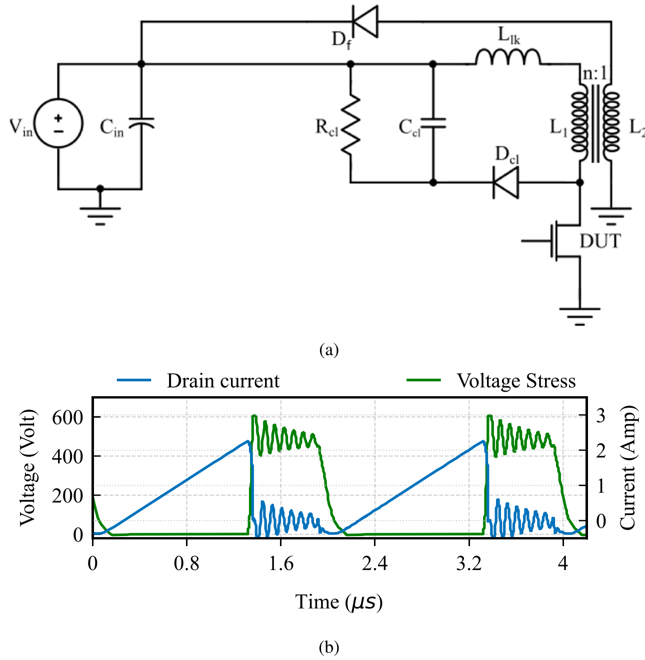


Fig. 5. (a) Schematics of the power circuit of the test vehicle. (b) Simulated result of the voltage and current stress applied to the DUT.

for the power loss occurring within the test vehicle. This approach not only minimizes power wastage but also obviates the necessity for large load dump systems when testing multiple devices. Thus, scalability is achieved in terms of efficiency, size, and cost.

To enable power recycling, it is crucial to allow sufficient off time for the inductor to discharge completely. This ensures that the magnetic field within the inductor resets before the next cycle begins. The OFF time required can be determined by analyzing the circuit presented in Fig. 5(a)

$$L_1\frac{\Delta i_{L1}}{T_1} = L_2\frac{\Delta i_{L2}}{T_2}. \tag{1}$$

Here, $L_1 = n^2 L_2$ and $\Delta i_{L2} = n\Delta i_{L1}$, where n is the turns ratio.

On substituting this in (1), we get $T_2 = T_1/n$, hence to prevent saturation and to maintain effective energy recycling, the system should satisfy the condition

$$T_{\text{off}} \geq \frac{T_{\text{on}}}{n}. \tag{2}$$

Also, the reflected plateau voltage appearing across the DUT can be expressed as

$$V_{DS} = (n+1)V_{\text{in}}. \tag{3}$$

In addition, the peak ringing voltage across the DUT($V_{DS,\text{max}}$) can be controlled by adjusting the value of the clamp resistor R_s, as follows [38]:

$$R_s = \frac{2V_{DS,\text{max}}(V_{DS,\text{max}} - V_{DS})}{L_{\text{leakage}} I_{L,\text{peak}}}. \tag{4}$$

TABLE II
PARAMETER DETAILS USED IN THE SIMULATION OF THE TEST VEHICLE

Parameter	Specification
DC link Voltage	160 V
Turns Ratio ($n_1 : n_2$)	2:1
Primary Mag: Inductance	72 μH
Leakage Inductance	2 μH
Snubber Resistance(R_{sn})	62 $k\Omega$
Switching Frequency	500 kHz
DUT on duration (T_{on})	1.2 μs
Snubber Capacitance (R_{sn})	10 nF
DC link Capacitance	50 μF

In an actual QR flyback converter, generally the controller IC tracks the voltage across the main switch and varies the frequency to make the device turn ON at the valley point at varying conditions of load and input variation. In the presented circuit, however, as long as the dc link is supplied by a fixed voltage source, the valley point remains unchanged, allowing operation at a fixed frequency. Any changes induced by the degradation of devices can also be neglected by selecting the frequency and the primary inductance values such that, $2\pi f L >> R_p$, where R_p is the sum of device ON state resistance and other parasitic resistance elements in the loop. Consequently, the valley point remains nearly constant throughout the test duration, requiring only a one-time calibration at the start to set the duty cycle and ensure consistent valley switching, eliminating the need for additional sensing schemes. In addition, in the presented circuit, pure zero voltage is achieved at the valley point since, $V_o = V_{\text{in}}$. This would help eliminate the charge trapping due to HCI and the effect of the transient voltage can be more clearly assessed. Nevertheless, if hard switching is desired, the turn on instant can be adjusted to achieve the same.

To validate the presented circuit, a simulation study is conducted in Ltspice. The simulation model is configured to generate a plateau voltage stress of 480 V and a peak current of 2.5 A, with the peak ringing voltage set at 600 V. The parameters utilized in the simulation to achieve the desired stress profile have been selected as per (1)–(4) and are summarized in Table II. Fig. 5(b) presents the simulation results, illustrating the voltage stress and drain current waveform, which closely resembles the QR flyback waveform shown in Fig. 4(b).

2) Sensing Stage: The presented test bench is designed to produce the quantized values of the drain current and the onstage voltage, sampled simultaneously throughout the test duration. High-speed ADCs with minimal aperture delays are utilized for the sampling of the required waveforms. While obtaining the current waveform only requires a sense resistor connected in series with the DUT, acquiring the ON-state voltage poses a greater challenge due to the need to clamp out the high OFF-state blocking voltage. Numerous voltage clamping circuits have been documented in the literature to aid in estimating the ON-state drop of power semiconductor switches [21], [39], [40], [41], [42]. Each circuit has its own advantages and disadvantages concerning factors, such as sensing delay, measurement accuracy, sensing range, complexity, and component count. In this test bench, the clamping circuit utilized is the one introduced in [21] due to its fast sensing speed and simpler configuration. The

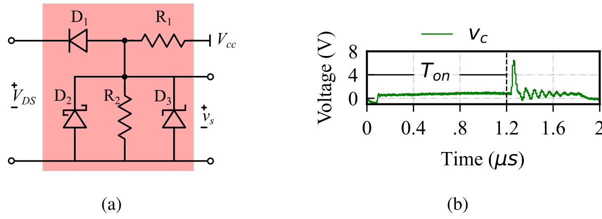


Fig. 6. (a) Clamp circuit for estimating DUT on-state drop. (b) Experimental waveform across the clamp circuit output in a QR flyback converter(V_c). Here, the voltage spike caused by DUT turn OFF at t $= 1.2$ μs is limited to 6 V.

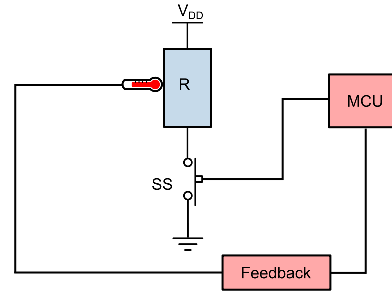


Fig. 7. Block diagram representing an overview of the heating subsystem.

schematic of this circuit is depicted in Fig. 6(a). When the DUT is turned OFF, diode D_1 becomes reverse-biased, preventing the high drain-source voltage from affecting the clamp circuit sensing node (V_c). However, when the DUT is turned on, the sensing node reflects the sum of the DUT's ON-state drop and the forward drop of D_1. D_2 is employed to hasten the discharge of D_1's output capacitance during turn-ON, thereby enhancing the sensing speed. With this circuit, it becomes feasible to sense the dynamic resistance as quickly as within 100 ns from the turn-ON instant. Fig. 6(b) shows the experimental waveform representing the output of the clamp circuit when used with the primary switch of a flyback converter. The ADCs are triggered simultaneously to capture the voltage and current values at the same instant for $d.R_{DS,\mathrm{ON}}$ estimation. DACs connected in series with the respective ADCs then convert the digital words generated by ADC back to analog values. In this way live equivalent values of the sampled voltage and current parameters can be obtained from each test vehicle using simple voltage measuring equipment.

3) Localized Heating System: HTOL testing requires the device junction temperature (T_j) to ideally approach the maximum limit specified in the datasheet. However, directly measuring T_j for control presents a significant challenge. Although various techniques exist for estimating T_j by monitoring temperature sensitive electrical parameters, integrating them into a continuously operating system environment is somewhat complicated. Therefore, in this study, the case temperature (T_c) of the device is monitored instead, which could easily be obtained using an external low-cost sensor. The assumption is that T_j typically resides approximately 5 °C–10 °C above T_c, based on the targeted application's minimal power loss due to its soft-switching nature and their generally lower junction-to-case thermal resistance.

A power resistor affixed to the casing of the DUT serves as the heating element to elevate the device junction temperature to the desired level. The developed test vehicle incorporates features enabling closed-loop temperature control throughout the test duration. Fig. 7 illustrates the block diagram of the temperature control scheme. Power dissipation across the resistor is regulated by toggling a relay switch connected in series between the resistor and a dc supply. The temperature of the DUT-power resistor is monitored using a transducer and transmitted to the main MCU via an appropriate feedback system. The controller implemented within the microcontroller then adjusts the relay duty cycle to maintain the temperature within the desired setpoint.

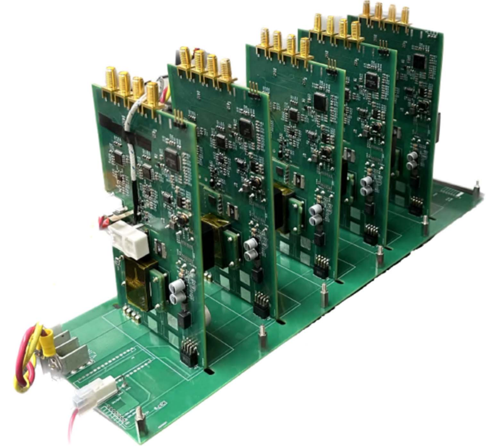


Fig. 8. Developed DHTOL test bench.

III. System Implementation

A prototype of the proposed test bench, featuring five daughter cards or test vehicles, has been developed in the laboratory, as illustrated in Fig. 8. A more detailed view of the individual test vehicles is provided in Fig. 9. Each test vehicle is designed to apply both electrical and thermal stress on a single DUT. These test vehicles are capable of circulating power internally and are equipped with features to sense the DUT's ON-state voltage drop and drain current in an inline, synchronous manner to accurately measure the device's $d.R_{DS,\mathrm{ON}}$.

The power stage is designed with a transformer turns ratio of 2:1, ensuring that the DUT would endure a plateau voltage stress of three times the dc-link voltage applied (3). The flyback transformers are devised to have a primary inductance of 110 μH and a leakage inductance close to 4 μH. The planar structure of the transformer developed enhances the power density and also minimizes the inductance mismatch between test vehicles, often attributable to differences in winding geometry in traditional designs. In addition, the plug-in nature of the planar transformer adds more flexibility to the test vehicle, as it increases the ease of replacement for achieving different stress levels. A pair of 33 μF electrolytic capacitors are used in parallel to create a dc-link capacitance of 66 μF. The MCU employed is F280039 from the TI C2000 series, which would provide the pulsewidth modulation (PWM) signal for controlling the DUT. The switching frequency of the converter operation is chosen to be 500 kHz. As pe (2), a turn-ON time of slightly above 1 μs would yield the

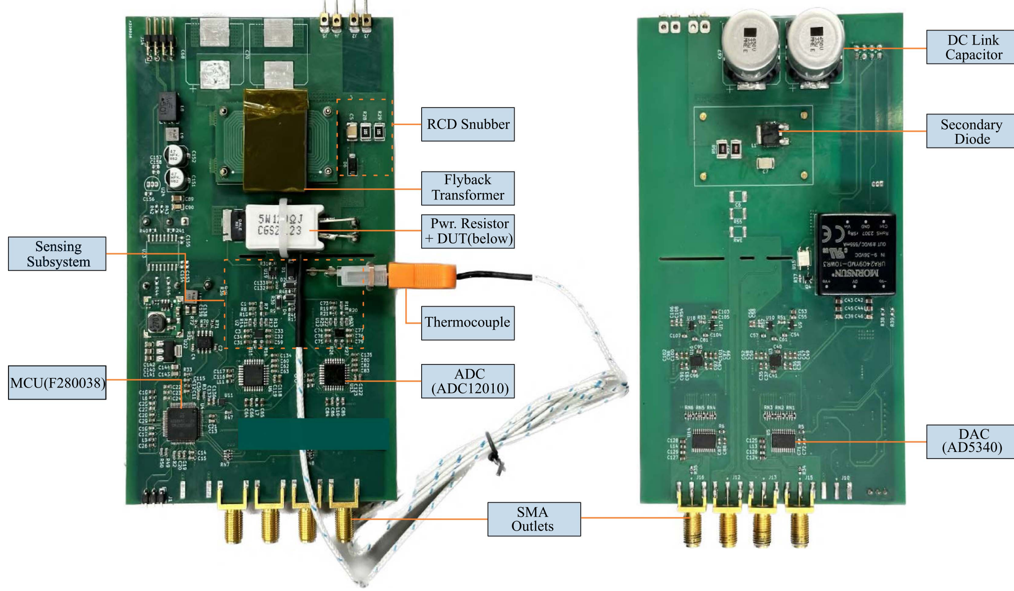


Fig. 9. Developed test vehicle based on QR flyback converter application (a) top side and (b) bottom side.

TABLE III
PARAMETER DETAILS OF THE DEVELOPED TEST VEHICLE

Parameter	Specification
Turns Ratio ($n_1 : n_2$)	2:1
Primary Mag: Inductance	110 μH
Leakage Inductance	4 μH
Snubber Resistance(R_s)	500 $k\Omega$
Switching Frequency	500 kHz
DUT on duration (T_{on})	1.16 μs
DC Link Capacitor	66μF

desired QR operation. The clamp circuit, as per (4) is selected to achieve a peak ringing stress of approximately 130 V above the plateau voltage. The design parameters of the power stage of the implemented test vehicles are summarised in Table III. Fig. 11 depicts the waveform showing the blocking voltage stress experienced by the DUT when subjected to a dc-link voltage of 173 V.

Fig. 10 illustrates the detailed schematic of the developed sensing circuit. The output signals from the clamp circuit (V_c) and the current sense resistor ($i_d R_s$) are fed into the ADC through a fully differential amplifier stage. This configuration helps attenuate the common-mode noise from the power stage entering the sensing subsystem. A high-temperature tolerant 50 mΩ resistor is chosen as the sense resistor (R_s), and the amplifier used is the LMH6553 from Texas Instruments. The selected amplifier exhibits an exceptional bandwidth of 900 MHz and provides precise accuracy, making it a good choice for our application. In addition, the clamping features present in the amplifier protect the ADC from any input signal overdrives. Fig. 11 represents the experimental waveform showing the output of the clamp circuit stage (V_c) and the device drain current (i_d) following the turn-ON event. The input impedance offered by the amplifier stage can be obtained from the circuit represented

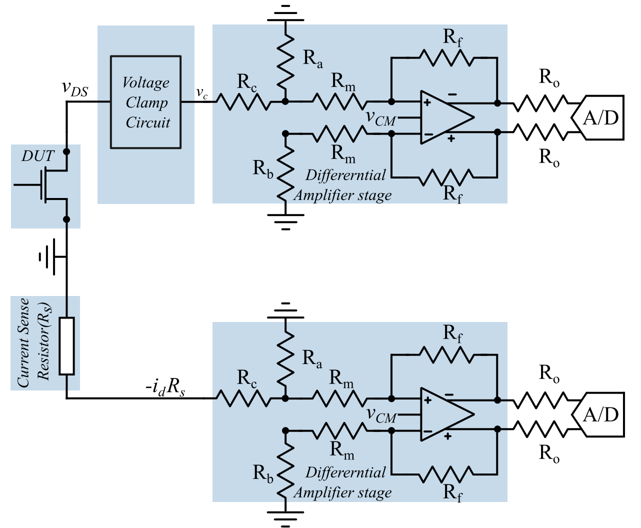


Fig. 10. Schematic of the voltage and current sensing circuit.

in Fig. 10 as

$$R_{\text{in}} = R_c + R_a || R_{\text{in,amp}} \tag{5}$$

where $R_{\text{in,amp}}$ is the input impedance of the differential amplifier, which could be obtained from the datasheet [43] as

$$R_{\text{in,amp}} = \frac{2R_m + R_b(1 - \beta_1)}{1 + \beta_1} \tag{6}$$

where $\beta_1 = \frac{R_b + R_m}{R_b + R_m + R_f}$

The steady-state output voltage of the clamp circuit can be expressed as

$$V_c = \begin{cases} v_{cc}\frac{(R_2||R_{in})}{(R_2||R_{in})+R_1}, & \text{when the DUT is OFF} \\ v_{ds} + v_{D1}, & \text{when the DUT is ON.} \end{cases} \tag{7}$$

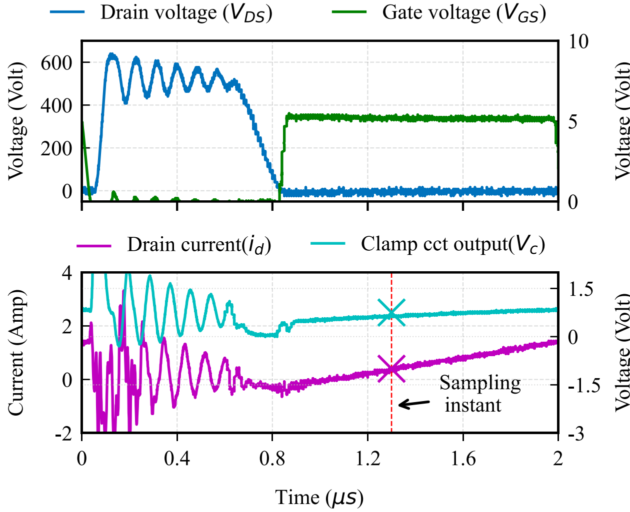


Fig. 11. Experimental waveform representing the drain to source voltage stress across the DUT as well as the drain current and clamp circuit output waveforms, clamp circuit output and the DUT drain current. Here the DUT is turned on at the instant 0.9 us and the marked points at 1.4 us indicate the instant of sampling.

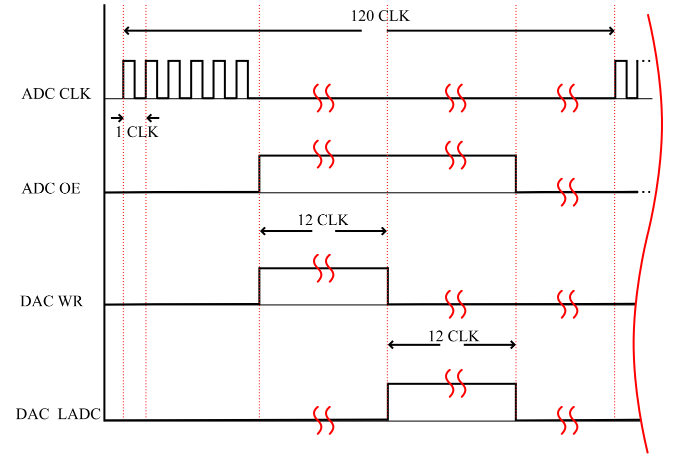


Fig. 12. Data acquisition sequence.

When the device is switched ON, the positive and negative input to the ADC tasked with voltage sensing would be

$$V_{\text{ADC},+} = \frac{\alpha v_s(1-\beta_2) + 2\beta_2 v_{CM}}{\beta_1 + \beta_2} \quad (8)$$

$$V_{\text{ADC},-} = \frac{-\alpha v_s(1-\beta_2) + 2\beta_1 v_{CM}}{\beta_1 + \beta_2} \quad (9)$$

where

$$\alpha = \frac{(R_{\text{in,amp}}||R_a)}{R_c + (R_{\text{in,amp}}||R_a)}$$

$$\beta_2 = \frac{R_m}{R_m + R_f}.$$

Similarly for the current sensing ADC

$$V_{\text{ADC},+} = \frac{\alpha(-i_d * R_s)(1-\beta_2) + 2\beta_2 v_{CM}}{\beta_1 + \beta_2} \quad (10)$$

$$V_{\text{ADC},-} = \frac{-\alpha(-i_d * R_s)(1-\beta_2) + 2\beta_1 v_{CM}}{\beta_1 + \beta_2}. \quad (11)$$

For estimation of the ON-state resistance, simultaneous sampling of voltage and current at the same instant is necessary. To accomplish this, the fast sampling capabilities of two high-speed ADCs are utilized, specifically the ADC12010 from TI [44], which has a very good aperture delay of 1ns and produces the digital output in the form of a 12-bit parallel word. A single PWM pulse generated from the MCU is provided as the clock signal for both ADCs through a clock buffer IC for the instantaneous sampling of both voltage and current. The ADC is of pipeline architecture, controlled by an external clock signal. The digital output is generated after a latency period of six clock cycles from the rising edge of the first clock pulse. To ensure synchronous acquisition of current and voltage data, identical PWM signals, generated by the MCU and facilitated by a clock buffer, are applied to both ADCs. The digital word generated is provided to two discrete DACs, which would convert it back to analog values, thus making it easier to access the end data. The DACs used are AD5340BRUZ [45] from analog devices, devised to produce analog output from 12-bit parallel input data. The selected DAC has a double-buffered interface consisting of one input register and another DAC register. It has one write input pin (WR) to enable/disable the latching of the digital data to the input register, and an LDAC pin governs the data transfer from the input register to the DAC register. In the developed test vehicle, control signals for both these pins are managed by the microcontroller chip.

Fig. 12 illustrates the employed sequence of data acquisition. The clock signal frequency is set the same as the converter frequency. The time delay between the rising edge of the two pulses is set according to the desired instant of $R_{DS,\text{ON}}$ sense. For example, if the desired instant for measuring the resistance is 500 ns after the device turns ON as illustrated in Fig. 10, the phase shift between the PWM pulse and the ADC clock pulse is set to 500 ns. The clock signal is set to trigger the ADC with six successive clock pulses every 120 PWM period. At the end of the sixth pulse, the digital data would be ready for processing. At this instant, the output of the ADC is enabled (OE), as well as the WR pin of the DAC is made high, enabling the digital data to be written into the internal input register of the DAC. In the next step, the WR pin is made low stopping the reading of input data, and the LDAC pin is made high setting up the transfer of data from the input register to the DAC register. At this point, the analog output of the DAC is updated. After another delay of 12 PWM period both the LDAC and OE pin are made low, halting the data acquisition process until the start of the next cycle.

The heating element employed in the test vehicle is a wire-wound resistor. The resistor is attached to the top side of the DUT through a thermal pad. The power is delivered to the heating resistor by a 24 V dc supply, controlled by a solid-state relay connected in series. A thermocouple junction inserted between the DUT casing and the power resistor is employed for sensing the device temperature, with the assumption that the ambient room temperature is a constant 25 °C. The thermocouple's voltage output, which is proportional to the temperature, is then

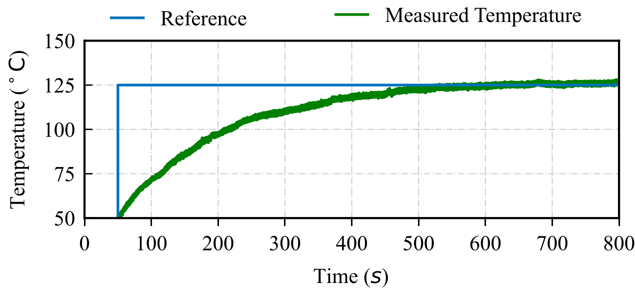


Fig. 13. Temperature control of the heating resistor.

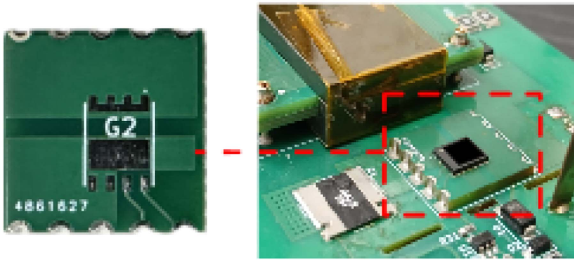


Fig. 14. FET cards employed for placing the DUTs in test vehicles.

amplified and conditioned before being fed to the microcontroller unit (MCU). This amplification process is carried out using an instrumentation amplifier, specifically the INA826 part number, which is configured to provide a gain of 250. With a K-type thermocouple that has a sensitivity of 41 μV/°C, this results in a total system gain of 0.01025 V/°C. Consequently, even at elevated temperatures, such as 250 °C, the input to the ADC remains well within its operating limits, which is capped at 3.3 V. The temperature control system's behavior is regulated by a digital controller embedded in the MCU, which adjusts the solid-state relay's duty cycle to precisely control the power delivered to the heating resistor, thus modulating the heat level to maintain the desired temperature. The performance of this temperature control system is demonstrated in Fig. 13, where the measured temperature closely follows the reference set point of 125 °C.

Furthermore, rather than directly soldering the device onto the test vehicle, a discrete FET card is employed to position the DUT, as depicted in Fig. 14. Subsequently, the FET card is linked to the test vehicle. This method offers scalability, enabling the utilization of the same vehicle to test devices from different vendors with diverse PCB footprints. It also provides the added advantage of reducing the potential for undesirable heat transfer from the DUT to the sensing portion of the daughter card, ensuring more accurate measurements and preventing damage to sensitive components. In addition, for using this test vehicle for highly accelerated tests, it is important to have short circuit protection features to achieve modularity. This can be achieved by introducing fuses into the input of each test vehicle. The ratings of the fuses can be determined by the maximum current rating allowed for the dc input supply. In the event of a short circuit failure of a device, after the reaction time, the fuse will disconnect the faulty test vehicle from the rest, enabling the healthy test vehicles to resume normal operation.

TABLE IV
SUMMARY OF THE STRESS CONDITIONS APPLIED TO DUTs

Parameter	JEDEC recc: test	Accelerated test
Drain-Source plateau voltage	520 V	570V
Peak transient voltage	650V	700V
Peak drain current	1.75A	1.9A
Gate-source voltage	5V	5V

IV. PERFORMING DHTOL TESTS ON GAN DEVICES

This section details the demonstration of the proposed test methodology using the developed DHTOL test bench prototype. For this, power semiconductor device samples from three different vendors, A, B, and C are selected. Devices from all three vendors are rated for 650 V. Devices from all vendors have a datasheet specified nominal on-state resistance close to 200 mΩ. DHTOL tests were performed on the GaN device samples under two different test conditions. First, the tests were conducted under stress conditions recommended for best practice by JEP 180, published by JEDEC. Subsequently, to further accelerate the device degradation within the intended test duration, the DHTOL test is then performed under slightly elevated transient voltage spikes.

A. Under JEDEC Recommended DHTOL Conditions

Four samples each from both vendors are chosen and subjected to the testing conditions recommended for best practice by JEDEC JEP 180 standard [24], as illustrated in Table IV. The plateau voltage was set at 80% of the data sheet specified maximum device rating, which corresponds to 520 V. For achieving the required plateau voltage, a dc link supply of 173 was applied as per the designed test vehicle specification. The 110 μH primary inductance of the transformer would yield a peak current close to 1.75 A for the turn-ON time employed of 1.16 μs. The peak ringing voltage is set approximately to 650 V, aligning with the maximum device rating. The power dissipation in the heating resistor is adjusted to keep the device case temperature at 125 °C while the test is running. Data acquisition was carried out using an NI USB 6351 system, which captured analog output values from DACs representing the voltage and current from each daughter card at a regular interval of 20 h throughout the testing period. The collected data was subsequently processed offline using MATLAB to evaluate the shift in $d.R_{DS,\mathrm{ON}}$ for each of the samples under test.

The primary objective of this study is to monitor the normalized shift in $d.R_{DS,\mathrm{ON}}$ values from their initial state throughout the test. This approach is taken due to the difficulty in precisely determining the absolute $d.R_{DS,\mathrm{ON}}$ value, largely because accurately measuring the voltage drop across the clamping diode D_1 during operation is nearly impossible. Fig. 15 illustrates the observed shift in this parameter over the 1000-h test period for samples from the selected vendors, respectively. For Vendor A, the shift in the $d.R_{DS,\mathrm{ON}}$ value for all tested samples remained within 1.1 times their original values, which means within 10%.

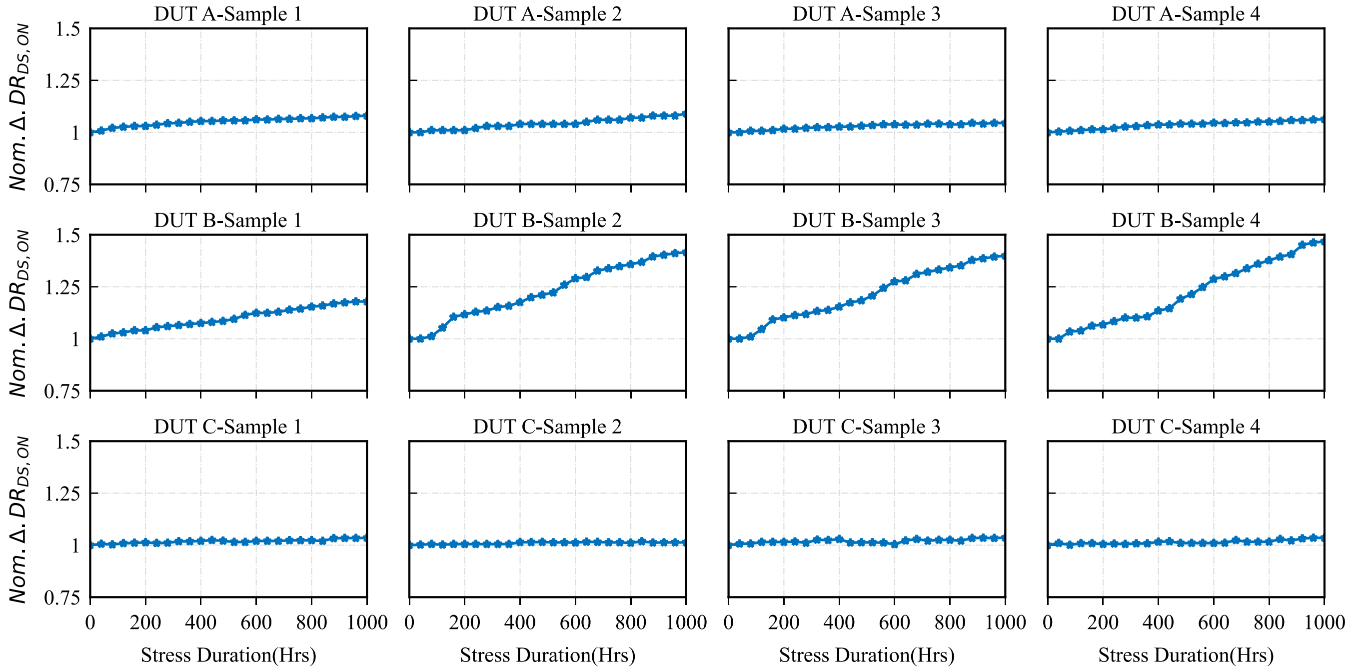


Fig. 15. Relative shift in $d.R_{DS,\mathrm{ON}}$ for the tested samples from the three vendors under JEDEC recommended DHTOL test conditions.

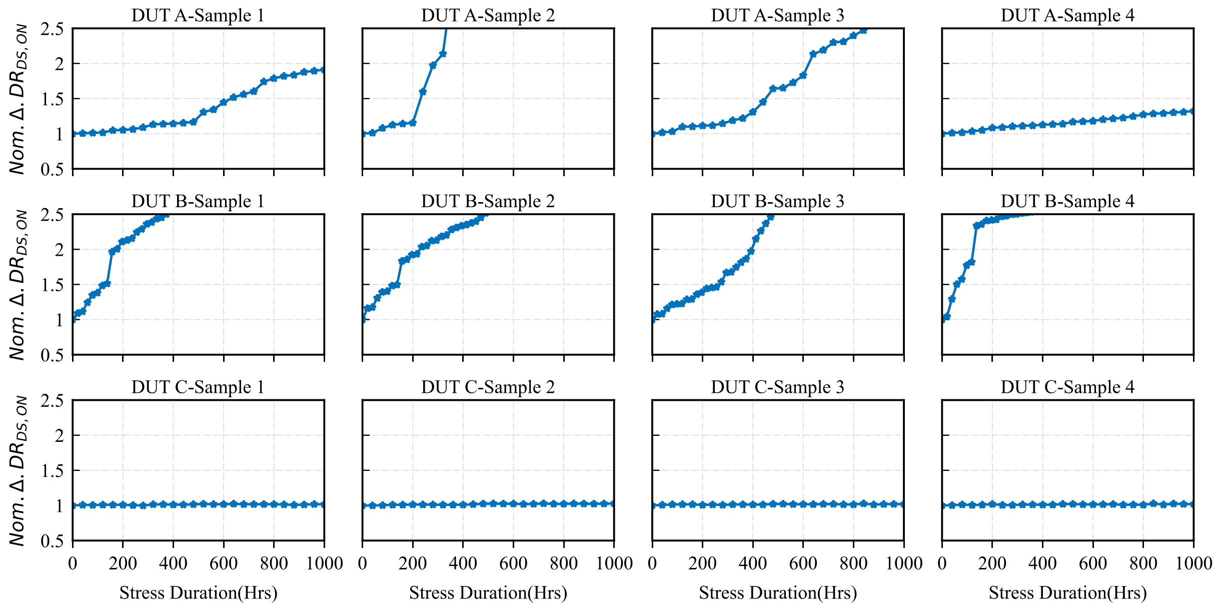


Fig. 16. Relative shift in $d.R_{DS,\mathrm{ON}}$ for the tested samples from the three vendors under accelerated DHTOL test conditions.

In contrast, the tested samples from Vendor B exhibited greater device-to-device variability, with observed shifts of 18%, 42%, 40%, and 47% for samples 1 through 4, respectively. In addition, for samples from Vendor C, all tested samples exhibited a negligible shift in their $d.R_{DS,\mathrm{ON}}$ values, within 5% of their original value.

B. Under Accelerated DHTOL Conditions

To further intensify charge-trapping, the DHTOL is performed at a slightly higher voltage level. The new plateau voltage was selected to be 570 V, with the peak ringing voltage to be 700 V, which is 50 V above the datasheet-specified limits of both devices. To achieve this, a dc-link voltage of 190 V is applied, which would yield a peak current close to 1.9 A. Based on the peak capacity of the sensing circuit employed, a device was considered to have failed once its $d.R_{DS,\mathrm{ON}}$ value reaches 2.5 times its initial value. The case temperature of the tested samples was kept at 125 °C and the same approach was used for data acquisition.

Fig. 16 illustrates the observed shift in the $d.R_{DS,\mathrm{ON}}$ for the tested samples from all selected vendors. For Vendor A,

one sample reaches the failure point of $d.R_{DS,\mathrm{ON}}$ being 2.5 times the initial value at approximately the 350-h mark. Of the remaining samples, one reaches the end of life after 850 h, while the other two survive the entire 1000-h test period. In contrast, for DUT B, all tested samples reach their end of life before 500 h of test time, with the earliest failure occurring around 300 h from the start of the test. For all samples tested from Vendor C, a negligible shift in $d.R_{DS,\mathrm{ON}}$ values is observed once again. Based on these results, Vendor C's samples demonstrate the highest stability under repeated voltage transients, followed by Vendor A, with Vendor B showing the least stability.

V. Conclusion

This article presents a test methodology for analyzing the robustness of GaN HEMTs for applications involving large transient voltage ringing spikes. To aid this, a modular test bench architecture enables continuous dynamic high-temperature operating lifetime (DHTOL) tests on multiple GaN devices simultaneously in an application-relevant manner is presented. The inline resistance estimation features of the test bench allow for user-friendly monitoring of shifts in $d.R_{DS,\mathrm{ON}}$. The test vehicles used for stressing the DUTs are based on flyback converter topology, capable of recycling power within themselves, thereby reducing power wastage and improving scalability. Moreover, the proposed test bench includes provisions for inducing localized thermal stress on the DUTs with closed-loop control features.

The proposed test methodology is experimentally demonstrated using a developed prototype of the DHTOL test bench. For this purpose, four samples of GaN HEMTs from three different vendors with nearly identical parameters were selected. Initially, these samples undergo a 1000-h DHTOL test under stress conditions recommended by JEDEC. In addition, fresh samples of the three commercial devices are subjected to further accelerated stress conditions. Based on the observed data regarding the shift in ON-state resistance, the samples from one device exhibited better stability compared to the other two. However, it is important to note that this article does not outright claim one device is superior to the other in terms of transient reliability, as a much larger batch of samples would be required to draw such a conclusion. Further, there are also other considerations for transient reliability, for example, the time dependent breakdown failure mechanism [46]. The primary aim of this testing is to demonstrate the proposed test methodology rather than to compare the two devices.

The presented DHTOL test methodology is valuable for studying the impact of repeated transient withstand capability on the long-term performance of GaN HEMTs in a realistic test environment. Work like this is important in developing the next set of standards for determining the safe transient voltage ratings of GaN devices. Furthermore, the proposed method could be extended to investigate similar reliability issues in other converter applications, such as buck or boost converters, by simply replacing the power stage of the test bench with the appropriate topology.

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Dr. Bahl played a key role in the GaN industry standardization effort, which led to the formation of the JEDEC JC70 committee and the increasing market adoption of GaN. He serves as Co-Chair of the JC70 GaN reliability task group and led the first JEDEC GaN reliability guideline, JEP180. He Co-Founded TI's GaN product line and coinvented TI's direct-drive GaN architecture. He is a distinguished Member of technical staff at TI.

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