A Combined PWM and Phase-Shift Control Method With Adaptive ZVS Boundary Regulation for Bridge-Arm Reused FSBB-*LLC* Converter

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***Abstract*—The four-switch buck-boost (FSBB) converter cascaded with *LLC* resonant converter can achieve zero-voltage switching (ZVS) of power switches and wide-range voltage regulation. To improve the power density and reduce the costs, the bridge arms in the two converters can be reused, thereby forming the bridge-arm reused FSBB-*LLC* converter. However, the reuse of bridge arms reduces the degrees of control freedom, which is detrimental to the realization of ZVS. In this article, a combined PWM and phase-shift control method with adaptive ZVS boundary regulation for FSBB-*LLC* converter is proposed, which realizes ZVS of power switches while maximizes the reduction on inductor current ripple in the full range (full voltage and load range). First, the ZVS conditions of power switches along with the selection principle of the inductor are revealed. Then, the basic idea of the adaptive ZVS boundary regulation and its design method are proposed. Based on that, a combined PWM and phase-shift control method and its implementation for the FSBB-*LLC* converter are proposed, which not only realizes full-range ZVS but also maximizes the reduction on inductor current ripple. Finally, a prototype of a 500-W FSBB-*LLC* converter is built and tested in the lab. The experimental results are provided to verify the effectiveness of the proposed control method.**

***Index Terms*—Bridge-arm reuse, combined pulsewidth modulation (PWM) and phase-shift control, four-switch buck-boost *LLC* (FSBB-*LLC*) converter, inductor current ripple, zero-voltage switching (ZVS).**

I. Introduction

In the applications with wide input voltage range, such as the distributed power system, electric vehicle charging system, and energy storage system, power electronic converters are required not only to provide galvanic isolation but also to achieve wide voltage regulation, high efficiency, and high power density. The *LLC* resonant converter can achieve zero-voltage switching (ZVS) for the primary-side power switches and zero-current switching (ZCS) for the secondary-side rectifiers, thus improving the efficiency, which has been widely adopted [1], [2], [3]. However, traditional frequency control makes it difficult to optimize the magnetic components over a wide voltage range. To extend the voltage regulation range, the magnetizing inductance of transformer could be reduced, which increases the circulating current losses and degrades the efficiency in the full voltage range [4], [5].

Considering both the wide-range voltage regulation and full-range high efficiency, the two-stage converter based on the *LLC* resonant converter has been proposed [6], [7], [8], [9], such as the preregulator+*LLC* converter. In the two-stage converter, the *LLC* resonant converter functions as a dc transformer (DCX), which achieves galvanic isolation and voltage matching, allowing it to be designed at the optimal condition. The preregulator is used to achieve wide-range voltage regulation, and the nonisolated dc−dc converters can be employed. To improve the efficiency, ZVS for the preregulator is also necessary. For the buck, boost and buck-boost converters, ZVS can be achieved either by auxiliary components [10], [11], which increases the complexity and reduces power density, or by enlarging the inductor current ripple swing negative, which however raises the conduction losses at light load. Besides, the buck converter can only step-down voltage, the boost converter can only step-up voltage, while the buck-boost converter outputs a negative voltage. Compared with them, the four-switch buck-boost (FSBB) converter can both step-up and step-down voltage flexibly with positive polarity. By appropriately controlling the three degrees of control freedom (DoFs), ZVS for all the power switches is realized with fixed switching frequency and the current ripple is reduced as the load decreases, making it an optimal choice for preregulator [12], [13], [14], [15], [16]. The two-stage configuration effectively balances high-efficiency galvanic isolation and wide voltage regulation range, enabling high efficiency in the full range (full voltage and load range), whereas it suffers from increased components number, high costs, and reduced power density.

To reduce the number of devices and improve the power density, the bridge-arm reuse technique, which shares the power switches on both sides of the intermediate bus capacitor, can be adopted. In [17] and [18], the two bridge arms in the interleaved boost converter are reused with the primary-side bridge arms

Received 17 March 2025; revised 7 June 2025 and 5 August 2025; accepted 5 September 2025. Date of publication 10 September 2025; date of current version 13 November 2025. This work was supported in part by the National Natural Science Foundation of China under Grant 52407209 and Grant 52237009, in part by the Delta Power Electronics Science and Education Development Program of Delta Group under Grant DREG2024003, and in part by China Postdoctoral Science Foundation under Grant 2023M741673. Recommended for publication by Associate Editor D. Lu. *(Corresponding author: Xinbo Ruan.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3608727.

Digital Object Identifier 10.1109/TPEL.2025.3608727

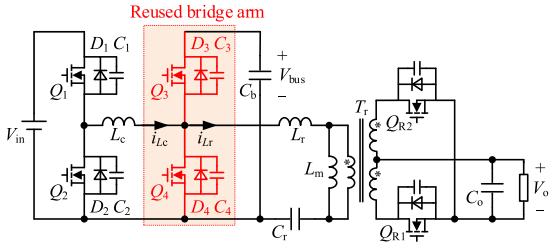

Fig. 1. Topology of the FSBB-*LLC* converter.

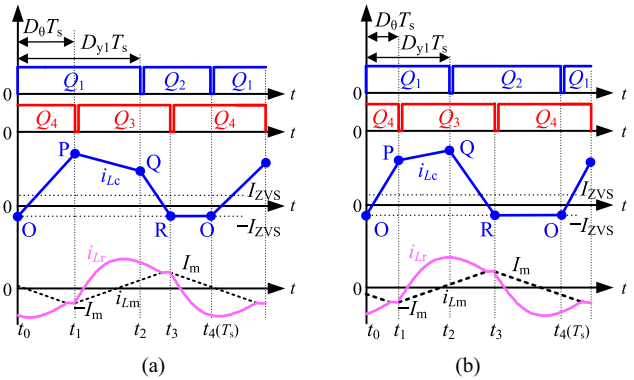

Fig. 2. Key waveforms of the FSBB-*LLC* converter. (a) $V_{\rm in} \le V_{\rm bus}$. (b) $V_{\rm in} > V_{\rm bus}$.

in the full-bridge *LLC* resonant converter, thereby saving four power switches, whereas it makes the *LLC* resonant converter be operated with PWM control and thus the efficiency is reduced. The buck-boost converter is employed as the preregulator and its bridge arm is shared with the half-bridge *LLC* resonant converter in [19]. However, the buck-boost converter exhibits the negative output-voltage polarity and suffers from high voltage stress on power switches. As mentioned, the FSBB converter offers full-range ZVS and minimized inductor current ripple with flexible DoFs. By reusing the bridge arms in the two converters, the bridge-arm reused FSBB-*LLC* converter is formed [20], [21], [22], [23], [24], as shown in Fig. 1, which is hereafter referred to as the FSBB-*LLC* converter for brevity.

In the FSBB-*LLC* converter, the *LLC* resonant converter is operated in DCX mode, where the duty cycle of power switches in the reused bridge arm is fixed at 50% . As a result, one of the DoFs in the FSBB converter is lost, imposing great challenge on the realization of ZVS and minimization of inductor current ripple.

Several control methods have been proposed for the FSBB-*LLC* converter. The simplest method is the PWM control with unipolar inductor current [20]. This method is easy to implement, whereas the power switches in the nonreused bridge arm are operated under hard-switching condition. A dual-frequency control method is introduced in [21], where the switching frequency of the reused bridge arm is increased to three times that of the nonreused bridge arm, thus the power density is increased. However, the power switches in the nonreused bridge arm are still operated with hard-switching. By incorporating the phase-shift control into the PWM control, a bipolar inductor current with quadrilateral shape can be realized, thus the power switches in the nonreused bridge arm can realize ZVS, and this is the combined PWM and phase-shift control method. Based on that, six switching modes were derived in [22] according to the ZVS conditions. However, the inductor current is excessively negative in some redundant modes, leading to increased current ripple and high conduction losses. Additionally, the phase-shift duty cycle is changed abruptly during load transients, resulting in poor dynamic performance. In [23], the switching modes are further optimized to four types, and a numerical fitting method is employed to select the optimal phase-shift cycle, thus expanding the ZVS range and reducing the conduction loss, whereas the inductor ripple is not maximally reduced, indicating that the inductor loss could be further reduced.

This article proposes a combined PWM and phase-shift control method with adaptive ZVS boundary regulation, which realizes ZVS for all the power switches while maximizes the reduction on inductor current ripple in the full range. The contribution of this article includes the following:

1) The ZVS conditions and inductor design principle considering the constraints on ZVS current and phase-shift duty cycle are revealed.
2) The basic idea of the adaptive ZVS boundary regulation and its design method are proposed.
3) The combined PWM and phase-shift control method with adaptive ZVS boundary regulation and its implementation are proposed for realizing full-range ZVS and maximally reducing the inductor ripple.

The rest of this article is organized as follows. In Section II, the ZVS conditions for the FSBB-*LLC* converter is revealed and the design principle of the inductor is proposed. Then, the basic idea of the adaptive ZVS boundary regulation and its design method are proposed in Section III. Based on that, the combined PWM and phase-shift control method for the FSBB-*LLC* converter is proposed in Section IV. Experimental validation of the proposed control method is provided in Section V. Finally, Section VI concludes this article.

II. ZVS Conditions for the FSBB-*LLC* Converter

A. Operating Principle of the FSBB-LLC Converter

The topology of the FSBB-*LLC* converter has been shown in Fig. 1, where, $Q_1 \sim Q_4$ are the power switches, $D_1 \sim D_4$ and $C_1 \sim C_4$ are the body diodes and junction capacitance of $Q_1 \sim Q_4$, respectively, $Q_{\rm R1}$ and $Q_{\rm R2}$ are the output rectifier, $L_{\rm c}$ is the connection inductor, $L_{\rm r}$, is the resonant inductor, $C_{\rm r}$, is the resonant capacitor, and $L_{\rm m}$ is the magnetizing inductor, $C_{\rm b}$ is the intermediate bus capacitor, and $C_{\rm o}$ is the output filter capacitor. $V_{\rm in}$, $V_{\rm bus}$ and $V_{\rm o}$ represent the input voltage, intermediate bus voltage, and output voltage, respectively.

Fig. 2 illustrates the key waveforms of the FSBB-*LLC* converter. Since the duty cycle of Q_3 and Q_4 is fixed at 50%, there are two DoFs left, namely, the duty cycle of the power switch Q_1, $D_{\rm y1}$, and the phase-shift duty cycle, D_θ, which corresponds to the delay time between the turn-ON instants of Q_3 and Q_1. There are four switching modes in the FSBB-*LLC* converter, which are presented as follows.

Mode 1: Q_1 and Q_4 are conducting, $V_{\rm in}$ is applied on $L_{\rm c}$, forcing i_{Lc} to increase linearly. $L_{\rm r}$ resonates with $C_{\rm r}$, and when i_{Lr} equals to i_{Lm}, $Q_{\rm R2}$ is turned OFF with ZCS. Subsequently, $L_{\rm r}$, $C_{\rm r}$, and $L_{\rm m}$ resonate together.

Mode 2: Q_1 and Q_3 are conducting, $V_{\rm in}-V_{\rm bus}$ is applied on $L_{\rm c}$, making i_{Lc} increase ($V_{\rm in} > V_{\rm bus}$) or decrease ($V_{\rm in} < V_{\rm bus}$) linearly. $L_{\rm r}$ resonates with $C_{\rm r}$, and i_{Lm} increases linearly.

Mode 3: Q_2 and Q_3 are conducting, $-V_{\rm bus}$ is applied on $L_{\rm c}$, forcing i_{Lc} to decrease linearly. $L_{\rm r}$ continues to resonate with $C_{\rm r}$, and when i_{Lr} equals to i_{Lm}, $Q_{\rm R1}$ is turned OFF with ZCS. Subsequently, $L_{\rm r}$, $C_{\rm r}$, and $L_{\rm m}$ resonate together.

Mode 4: Q_2 and Q_4 are conducting, and the voltage across $L_{\rm c}$ is 0, maintaining i_{Lc} constant. $L_{\rm r}$ resonates with $C_{\rm r}$, and i_{Lm} decreases linearly.

Since the duty cycle of the reused bridge arm is fixed at 50%, the voltage gain of the FSBB converter is

$$\frac{V_{\rm bus}}{V_{\rm in}} = \frac{D_{\rm y1}}{1-0.5} = 2D_{\rm y1}. \tag{1}$$

The *LLC* resonant converter operates in DCX mode, and its voltage gain could be expressed as [25]

$$\frac{V_{\rm o}}{V_{\rm bus}} = \frac{1}{2N} \tag{2}$$

where N is the primary-to-secondary turns ratio of transformer.

Combining (1) and (2), the voltage gain of the FSBB-*LLC* converter is expressed as

$$\frac{V_{\rm o}}{V_{\rm in}} = \frac{V_{\rm bus}}{V_{\rm in}}\frac{V_{\rm o}}{V_{\rm bus}} = \frac{D_{\rm y1}}{N}. \tag{3}$$

As seen from (3), the output voltage of the FSBB-*LLC* converter can be regulated by $D_{\rm y1}$.

B. ZVS Conditions

1) Constraints on the ZVS Current

Before the analysis, it is defined that the minimum current required to achieve ZVS of power switches is $I_{\rm ZVS}$, and the current through $L_{\rm c}$ at points O, P, Q, and R are $I_{\rm O}$, $I_{\rm P}$, $I_{\rm Q}$, and $I_{\rm R}$, respectively. Since all the power switches are identical, we have $C_1 = C_2 = C_3 = C_4 = C_{\rm oss}$.

For the nonreused bridge arm, during the dead time of Q_1 and Q_2, i_{Lc} charges/discharges the junction capacitance for providing the ZVS condition. Specifically, when Q_1 is turned OFF, $I_{\rm Q}$ charges C_1 and discharges C_2. Once the voltage of C_2 decays to zero, Q_2 can be turned ON with zero voltage. When Q_2 is turned OFF, $I_{\rm O}$ charges C_2 and discharges C_1. Once the voltage of C_1 decays to zero, Q_1 can be turned ON with zero voltage. To complete the charging/discharging process within the dead time, the required minimum ZVS current is

$$I_{\rm ZVS} = 2C_{\rm oss}V_{\rm in}/t_{\rm d} \tag{4}$$

where $t_{\rm d}$ is the dead time, and $C_{\rm oss}$ is the output capacitor of the MOSFETs, which is nonlinear and could be considered as a constant and obtained from the datasheet of MOSFETs [26].

Therefore, to turn ON Q_2 with zero-voltage, $I_{\rm Q} \geq I_{\rm ZVS}$ must be satisfied, and to turn ON Q_1 with zero-voltage, $I_{\rm O} \leq -I_{\rm ZVS}$ must be met.

For the reused bridge arm, during the dead time of Q_3 and Q_4, the inductor current i_{Lc} and the magnetizing current i_{Lm} (i.e., $I_{\rm P} + I_{\rm m}$ and $I_{\rm R} - I_{\rm m}$) jointly charge/discharge the junction capacitance for providing the ZVS. This means that, even if $I_{\rm m}$ is zero, ZVS can be still realized by i_{Lc} in the FSBB converter. This in turn, allows to design the magnetizing inductance to be infinitely large, resulting in zero magnetizing current and thus reducing the turn-OFF losses in the reused bridge arm, which is another benefit brought by bridge-arm reuse.

Assuming that the magnetizing inductor is infinite, we have $I_{\rm m} = 0$. When Q_3 is turned OFF, $I_{\rm R}$ charges C_3 and discharges C_4. When the voltage of C_4 decays to zero, Q_4 can be turned ON with zero-voltage. When Q_4 is turned OFF, $I_{\rm P}$ charges C_4 and discharges C_3. Once the voltage of C_3 decays to zero, Q_3 can be turned ON with zero-voltage. To complete the charging/discharging process within the dead time, the required minimum ZVS current is

$$I_{\rm ZVS} = 2C_{\rm oss}V_{\rm bus}/t_{\rm d} = 4C_{\rm oss}NV_{\rm o}/t_{\rm d}. \tag{5}$$

Therefore, to turn ON Q_4 with zero-voltage, $I_{\rm P} \geq I_{\rm ZVS}$ must be satisfied, and to turn ON Q_3 with zero-voltage, $I_{\rm R} \leq -I_{\rm ZVS}$ must be met.

Based on (4) and (5), to achieve ZVS for all power switches in the entire input and output voltage range, $I_{\rm ZVS}$ must satisfy

$$I_{\rm ZVS} = 2C_{\rm oss}\max\{V_{\rm in\_max}, 2NV_{\rm o\_max}\}/t_{\rm d} \tag{6}$$

where $V_{\rm in\_max}$ is the maximum input voltage, and $V_{\rm o\_max}$ is the maximum output voltage.

2) Constraints on the Phase-Shift Duty Cycle

According to the operating principle, to realize full-range ZVS for all the power switches, the optimal switching sequence of the FSBB-*LLC* converter should remain consistent with that of the FSBB converter. Specifically, Q_1 should be turned OFF before Q_3, Q_3 should be turned OFF before Q_2, and Q_2 should be turned OFF before Q_4 [12], [13], [14], [15], [16].

As can be observed from (1), when $V_{\rm in} \leq V_{\rm bus}$, $D_{\rm y1} \geq 0.5$. Referring to Fig. 2(a), to ensure that Q_1 is turned OFF before Q_3, D_θ should be larger than $D_{\rm y1}-0.5$. Additionally, to ensure that Q_3 is turned OFF before Q_2, D_θ should be smaller than 0.5. Conversely, when $V_{\rm in} > V_{\rm bus}$, $D_{\rm y1} < 0.5$. Referring to Fig. 2(b), to ensure that Q_2 is turned OFF before Q_4, D_θ should be larger than 0. Additionally, to ensure that Q_1 is turned OFF before Q_3, D_θ should be smaller than $D_{\rm y1}$. Therefore, the constraints for D_θ satisfying the optimal switching sequence can be obtained as

$$\begin{cases} \frac{V_{\rm bus}}{2V_{\rm in}} - 0.5 < D_\theta < 0.5 & (V_{\rm in} \leq V_{\rm bus}) \\ 0 < D_\theta < \frac{V_{\rm bus}}{2V_{\rm in}} & (V_{\rm in} > V_{\rm bus}) \end{cases}. \tag{7}$$

In summary, to achieve full-range ZVS for the FSBB-*LLC* converter, the two constraints are required: the absolute value of the ZVS current for any power switch should be no less than $I_{\rm ZVS}$ in (6); and the phase-shift duty cycle should satisfy the constraints in (7) considering the optimal switching sequence.

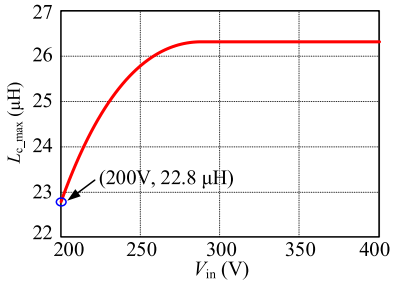

Fig. 3. The curve of the maximum inductor value.

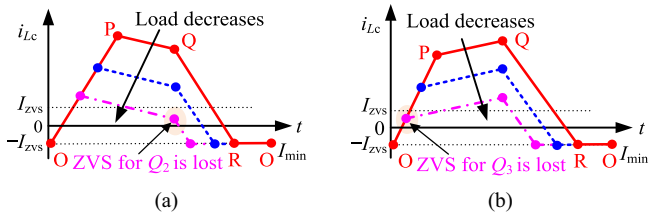

Fig. 4. Inductor current waveforms when the load decreases. (a) $V_{in} \le V_{bus}$. (b) $V_{in} > V_{bus}$.

C. Design Principle of the Inductor

In the FSBB-*LLC* converter, the inductor is not only closely related to ZVS range, but also affect its current ripple.

According to Fig. 2, the average current of Q_1 is

$$I_{Q1} = \frac{(I_P + I_{min})\, D_\theta}{2} + \frac{(I_P + I_Q)\,(D_{y1} - D_\theta)}{2} \tag{8}$$

where I_{min} is the minimum inductor current, and $I_R = I_O = I_{min}$. I_P and I_Q can be expressed as

$$I_P = I_{min} + \frac{V_{in}}{L_c} D_\theta T_s \tag{9}$$

$$I_Q = I_{min} + \frac{V_{bus}}{L_c}\,(0.5 - D_{y1} + D_\theta)\, T_s. \tag{10}$$

Substituting (9) and (10) into (8), we have

$$I_{Q1} = \frac{V_{in} D_{y1}^2 T_s}{2L_c} - \frac{V_{bus}(D_{y1} - D_\theta)^2 T_s}{2L_c} + I_{min} D_{y1}. \tag{11}$$

Based on (11), the input power can be expressed as

$$P_{in} = V_{in} I_{Q1} = \frac{V_{in}^2 D_{y1}^2 T_s}{2L_c} - \frac{V_{in} V_{bus}(D_{y1} - D_\theta)^2 T_s}{2L_c} + V_{in} I_{min} D_{y1}. \tag{12}$$

Assuming the efficiency is 100% [27], we have $P_{in} = P_o$. Then, according to (12), I_{min} can be derived as

$$I_{min} = -\frac{V_{in} D_{y1} T_s}{2L_c} + \frac{P_o}{V_{in} D_{y1}} + \frac{V_{bus}(D_{y1} - D_\theta)^2 T_s}{2L_c D_{y1}}. \tag{13}$$

To achieve full-range ZVS, $I_{min} \le -I_{ZVS}$ is required. Then, combining with (13), the inductor can be derived as

$$L_c \le L_{c\_max} = \frac{\left[V_{in} V_{bus} - (V_{bus} - 2V_{in} D_\theta)^2\right] V_{bus} T_s}{4V_{in}\,(V_{bus} I_{ZVS} + 2P_o)}. \tag{14}$$

According to (7), D_θ is always smaller than $V_{bus}/(2V_{in})$ in the full range. Therefore, L_{c_max} increases as D_θ rises. Substituting the maximum value of D_θ into (14), we have

$$L_{c\_max} = \begin{cases} \frac{\left[V_{in} V_{bus} - (V_{bus} - V_{in})^2\right] V_{bus} T_s}{4V_{in}(V_{bus} I_{ZVS} + 2P_o)} & (V_{in} \le V_{bus}) \\ \frac{T_s V_{bus}^2}{4(V_{bus} I_{ZVS} + 2P_o)} & (V_{in} > V_{bus}) \end{cases}. \tag{15}$$

Based on (15), the curve of L_{c_max} can be plotted, as shown in Fig. 3, where the parameters are given in Table II in Section V.

As seen, L_{c_max} increases as the input voltage rises. To achieve full-range ZVS for all the switches, L_c should be selected at the minimum input voltage. Considering the losses and the parameter deviations in practical circuit, L_c is selected to be slightly lower than L_{c_max}.

III. Basic Idea and Design Method of the Proposed Adaptive ZVS Boundary Regulation

A. Basic Idea of the Adaptive ZVS Boundary Regulation

The inductor current ripple is expressed as

$$\Delta I_{Lc} = \begin{cases} I_P - I_{min} = \frac{V_{in}}{L_c} D_\theta T_s & (V_{in} \le V_{bus}) \\ I_Q - I_{min} = \frac{V_{bus}}{L_c}\,(0.5 - D_{y1} + D_\theta)\, T_s & (V_{in} > V_{bus}) \end{cases}. \tag{16}$$

As seen from (16), when the load is unchanged, the inductor current ripple reduces as D_θ decreases. However, the decrease of D_θ also shifts I_R and I_O upward, making it more challenging to realize ZVS. Conversely, as D_θ increases, the inductor current ripple increases, which also shifts I_R and I_O downward, facilitating the realization of ZVS but increasing the conduction losses. Therefore, there is a tradeoff between the inductor current ripple and ZVS, that is, to minimize the inductor current ripple while ensuring the ZVS condition, D_θ should be controlled to guarantee that I_{min} is exactly equal to $-I_{ZVS}$.

Fig. 4 shows the inductor current waveforms when the load changes. As seen, as the load decreases, D_θ that corresponds to the interval from O to P decreases, and I_Q ($V_{in} \le V_{bus}$) or I_P ($V_{in} > V_{bus}$) also decreases, thus inductor current ripple is reduced. When the load continues to decrease, if D_θ is further decreased, I_P or I_Q will fall below I_{ZVS}, as shown with the dash-dot line in Fig. 4, resulting in the loss of ZVS for Q_2 ($V_{in} \le V_{bus}$) and Q_3 ($V_{in} > V_{bus}$) at light load.

To address this issue, when the load decreases to the point when I_Q ($V_{in} \le V_{bus}$) or I_P ($V_{in} > V_{bus}$) equals to I_{ZVS}, D_θ should be limited for ensuring that I_Q or I_P remains constant at I_{ZVS}, as illustrated in Fig. 5. As a result, D_θ is controlled for maintaining the minimum inductor current (I_R and I_O) at $-I_{ZVS}$ at heavy load and is limited for ensuring I_Q or I_P at I_{ZVS} at light load. This is the basic idea of adaptive ZVS boundary regulation. It is worth noting that the minimum inductor current may be slightly lower than $-I_{ZVS}$ at light load.

Fig. 6 shows the implementation of the adaptive ZVS boundary regulation. At heavy load, the minimum inductor current is compared with $-I_{ZVS}$, and then a phase-shift closed-loop

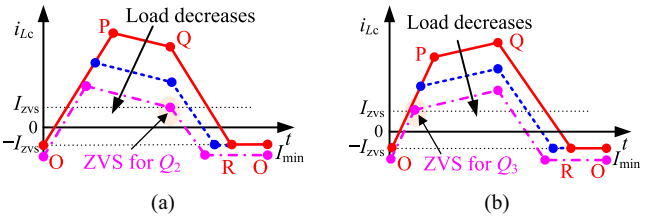

Fig. 5. Inductor current waveforms with adaptive ZVS boundary regulation when the load decreases. (a) $V_{in} \le V_{bus}$. (b) $V_{in} > V_{bus}$.

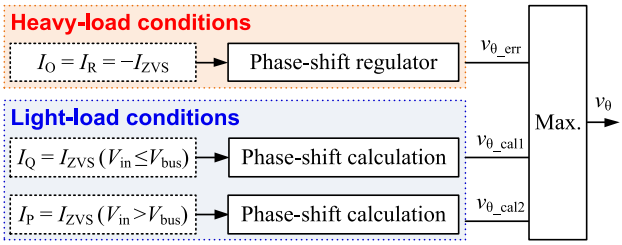

Fig. 6. Implementation of adaptive ZVS boundary control.

control is employed to adjust D_θ, thus regulating the minimum inductor current at $-I_{ZVS}$. At light load, the phase-shift regulator is saturated, and D_θ is determined through calculation to regulate I_Q ($V_{in} \le V_{bus}$) or I_P ($V_{in} > V_{bus}$) to I_{ZVS}. At the power boundary point, where $I_Q = I_{ZVS}$ ($V_{in} \le V_{bus}$) or $I_P = I_{ZVS}$ ($V_{in} > V_{bus}$) and $I_R = I_O = -I_{ZVS}$, D_θ generated by the phase-shift closed-loop precisely aligns with the phase-shift calculation, enabling smooth transitions between different load conditions.

B. Design Method of the Adaptive ZVS Boundary Regulation

1) Calculation Method for D_θ at Light Load: When $V_{in} \le V_{bus}$, to realize ZVS for Q_2, $I_Q \ge I_{ZVS}$ is required. Combining it with (11), we have

$$D_\theta \ge (I_{ZVS} - I_{min}) \frac{L_c}{V_{bus} T_s} + D_{y1} - 0.5. \quad (17)$$

D_θ is obtained by comparing the phase-shift signal V_θ with a sawtooth waveform, satisfying $D_\theta = V_\theta / V_M$, where V_M is the amplitude of the sawtooth waveform. Therefore, the phase-shift signal V_{θ_cal1} can be expressed as

$$V_{\theta\_cal1} = (I_{ZVS} - I_{min}) \frac{L_c V_M}{V_{bus} T_s} + D_{y1} V_M - 0.5 V_M. \quad (18)$$

When $V_{in} > V_{bus}$, to realize ZVS for Q_3, $I_P \ge I_{ZVS}$ is required. Combining it with (10), we have

$$D_\theta \ge (I_{ZVS} - I_{min}) \frac{L_c}{V_{in} T_s}. \quad (19)$$

Therefore, the phase-shift signal V_{θ_cal2} can be expressed as

$$V_{\theta\_cal2} = (I_{ZVS} - I_{min}) \frac{L_c V_M}{V_{in} T_s}. \quad (20)$$

Based on (18) and (20), the value of D_θ at light load when $V_{in} \le V_{bus}$ and $V_{in} > V_{bus}$ could be calculated, respectively.

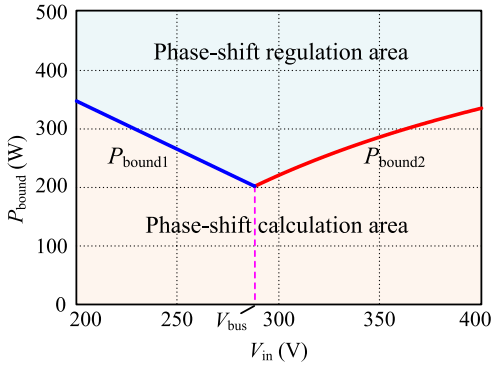

Fig. 7. Boundary power curve in the FSBB-*LLC* converter.

2) Selection of the Boundary Power: Based on (13), D_θ can be derived as

$$D_\theta = D_{y1} - \sqrt{\left(\frac{D_{y1}}{2} + \frac{L_c I_{min}}{V_{in} T_s} - \frac{2 L_c P_o}{V_{in} V_{bus} T_s}\right)}. \quad (21)$$

When $V_{in} \le V_{bus}$, $I_Q = I_{ZVS}$ and $I_{min} = -I_{ZVS}$ are satisfied at the boundary between light and heavy loads. Combining (11) and (21), the boundary power when $V_{in} \le V_{bus}$ can be derived as

$$P_{bound1} = V_{bus}\left[I_{ZVS}\left(\frac{V_{in}}{V_{bus}} - \frac{1}{2}\right) + \frac{T_s (V_{bus} - V_{in})}{8 L_c} - \frac{2 L_c V_{in} I_{ZVS}^2}{T_s V_{bus}^2}\right]. \quad (22)$$

Similarly, when $V_{in} > V_{bus}$, $I_P = I_{ZVS}$ and $I_{min} = -I_{ZVS}$ are satisfied at the boundary between light and heavy loads. Combining (10) and (21), the boundary power when $V_{in} > V_{bus}$ can be derived as

$$P_{bound2} = V_{bus}\left[I_{ZVS}\left(\frac{V_{bus}}{V_{in}} - \frac{1}{2}\right) + \frac{T_s V_{bus} (V_{in} - V_{bus})}{8 L_c V_{in}} - \frac{2 L_c I_{ZVS}^2}{T_s V_{in}}\right]. \quad (23)$$

Based on (22) and (23), the curve of the boundary power versus input voltage is plotted, as shown in Fig. 7, where the parameters are provided in Table II. As seen, at heavy load (see the blue region), D_θ is obtained through the phase-shift regulator, while at light load (see the yellow region), D_θ is calculated through (18) and (20). When the operating region shifts due to power change, the phase-shift duty cycle transits smoothly. Therefore, the power boundary changes adaptively with the input voltage, and thus D_θ regulates adaptively with the input voltage and output power, thus ensuring ZVS while maximally reducing the inductor current ripple.

With the adaptive ZVS boundary regulation, the full-range operating waveform of the FSBB-*LLC* converter is shown in Fig. 8. As seen, ZVS for all the power switches is realized in the full voltage and load range, and the inductor current ripple is maximally reduced as load decreases, thus high efficiency could be achieved.

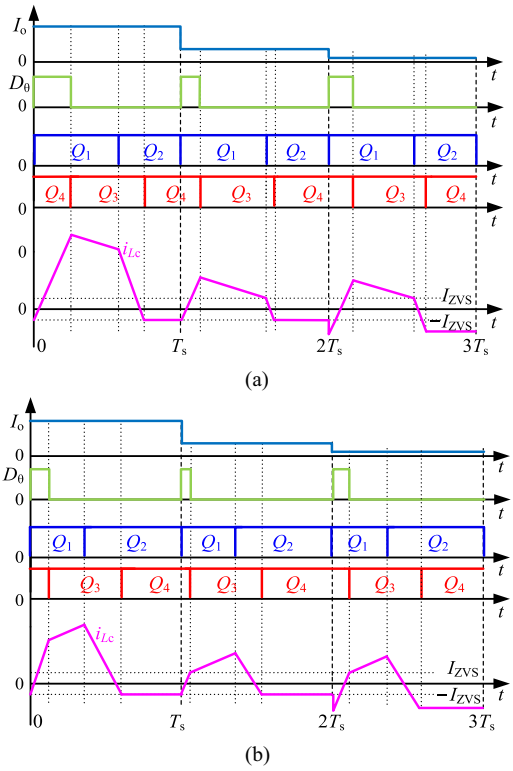

Fig. 8. Operational waveforms of the FSBB-*LLC* converter in the full load range. (a) $V_{\rm in} \le V_{\rm bus}$. (b) $V_{\rm in} > V_{\rm bus}$.

IV. Combined PWM and Phase-Shift Control Scheme With Adaptive ZVS Boundary Regulation

A. Proposed Control Scheme of the FSBB-LLC Converter

With the adaptive ZVS boundary regulation, a combined PWM and phase-shift control method is proposed for the FSBB-*LLC* converter, which is described as follows.

1) The output voltage of the FSBB-*LLC* converter depends only on $D_{\rm y1}$, so the PWM control is used to generate the duty cycle of Q_1 and Q_2 and thus to regulate the output voltage.
2) The phase-shift regulation part including the phase-shift closed-loop control and phase-shift calculation is employed to realize the adaptive ZVS boundary regulation.

The specific control block diagram is shown in Fig. 9, which consists of the output voltage control unit, the phase-shift closed-loop control unit, and the phase-shift calculation unit.

Part A is the output voltage control unit and generate $D_{\rm y1}$. The output voltage is sensed and compared with the voltage reference $V_{\rm oref}$, and the error is sent to the voltage regulator, producing the output voltage control signal $v_{\rm err}$, which is used to generate the duty cycle signal $D_{\rm y1}$.

Part B is the phase-shift closed-loop control unit, which is used to generate the phase-shift duty cycle at heavy-load conditions and maintain the minimum inductor current at $-I_{\rm ZVS}$. The minimum inductor current is sampled through valley detection circuit and then compared with the current reference of $-I_{\rm ZVS}$. The error signal is fed into a phase-shift regulator to generate the phase-shift duty cycle control signal $v_{\theta\_\rm err}$ at heavy-load conditions.

Part C is the phase-shift calculation unit, which is used to control the minimum phase-shift duty cycle at light load, ensuring that the ZVS currents $I_{\rm Q}$ for Q_2 ($V_{\rm in} \le V_{\rm bus}$) and $I_{\rm P}$ for Q_3 ($V_{\rm in} > V_{\rm bus}$) are maintained at $I_{\rm ZVS}$. Taking $I_{\rm min}$ and $v_{\rm err}$ as the input for (18), and $I_{\rm min}$ and $v_{\rm in}$ as the input for (20), the phase-shift signals of $v_{\theta\_\rm cal1}$ ($V_{\rm in} \le V_{\rm bus}$) and $v_{\theta\_\rm cal2}$ ($V_{\rm in} > V_{\rm bus}$) under light-load conditions are calculated, respectively. Finally, the output signals from the phase-shift closed-loop control unit and the phase-shift calculation unit, $v_{\theta\_\rm err}$, $v_{\theta\_\rm cal1}$, and $v_{\theta\_\rm cal2}$, are compared to obtain their maximum value v_θ. This signal, along with the output signal from the output voltage control unit, $v_{\rm err}$, are fed into the PWM generator to collectively generating the driving signals for power switches Q_1~Q_4.

B. Comparison and Discussion

Table I gives the comparison between the proposed control method and other control methods for the FSBB-*LLC* converter. When the PWM control is employed, the inductor current is usually modulated as unipolar shape for reducing its ripple, whereas the power switches in the nonreused bridge arm are operated with hard switching. By employing the combined PWM and phase-shift control, the inductor current could be modulated as bipolar shape, enabling ZVS for the power switches. However, the inductor current ripple in the existing control methods is not maximally reduced, and the inductor loss could be further reduced. The proposed method in this article introduces the adaptive ZVS boundary regulation to the traditional combined PWM and phase-shift control method, which realizes full-range ZVS while maximally reducing the inductor current ripple, thus improving the efficiency over the entire range.

V. Experimental Verifications

To verify the effectiveness of the proposed control method, a prototype of a 500-W FSBB-*LLC* converter is built and tested in the lab, as shown in Fig. 10. The specific parameters of the prototype are given in Table II. In this prototype, the digital control method is adopted, which is realized in the DSP (TMS320F28335) from TI. The primary-side power switches adopt the GaN MOSFET (NV6128) from Navitas, and the output rectifiers employ the MOSFET (BSC117N08NS) from Infineon. Thanks to the realization of soft-switching, the switching frequency is selected as 500 kHz for increasing the power density. As for the FSBB-*LLC* converter, the bus voltage is typically set at the midpoint of the input voltage range to maximize efficiency [15]. Considering the convenience of selecting an integer number of turns for the transformer, the intermediate bus voltage is designed to be 288 V ($24 \times 6 \times 2 = 288$ V) here.

Figs. 11–13 show the steady-state experimental waveforms of the FSBB-*LLC* converter under no-load, half-load, and full-load conditions when the input voltage is 200, 300, and 400 V, respectively, where, $v_{\rm gs\cdot Q2}$ and $v_{\rm ds\cdot Q2}$ represent the gate driving signal and drain-source voltage of power switch Q_2, $v_{\rm gs\cdot Q4}$ and $v_{\rm ds\cdot Q4}$ represent the gate driving signal and drain-source voltage of power switch Q_4, and i_{Lc} is the inductor current. As can be

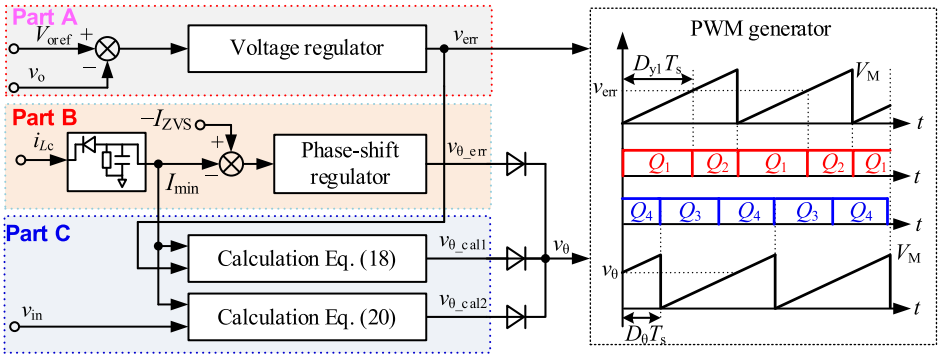

Fig. 9. The combined PWM and phase-shift control block diagram for the FSBB-*LLC* converter.

TABLE I
COMPARISON OF THE PROPOSED CONTROL METHOD WITH OTHER CONTROL METHODS

Reference	Modulation method	Current polarity	Switching mode	Implementation	ZVS condition	Inductor current ripple	Peak efficiency
Li and Ruan [20]	PWM	Unipolar	2	/	Hard switching	Small	95%
Sun et al. [21]	PWM (dual frequency)	Unipolar	4	Closed-loop control	Hard switching	Small	92%
Sun et al. [22]	PWM and phase-shift	Bipolar	6	Lookup table	Full-range ZVS	Large	90.5%
Liu et al. [23]	PWM and phase-shift	Bipolar	4	Lookup table	Full-range ZVS	Slightly large	96.4%
This article	PWM and phase-shift with ZVS boundary regulation	Bipolar	4	Closed-loop control and real-time calculation	Full-range ZVS	Medium	97.2%

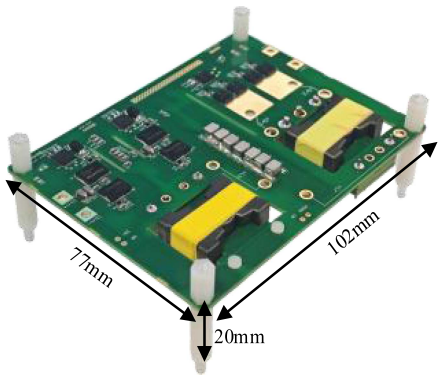

Fig. 10. Photograph of the prototype.

TABLE II
SPECIFICATIONS AND PARAMETERS OF THE FSBB-*LLC* CONVERTER

Parameter	Value	Parameter	Value
Input voltage / V_{in}	200–400 V	Inductor / L_c	21.5 μH
Output voltage / V_o	24 V	Bus capacitor / C_b	6 μF
Bus voltage / V_{bus}	288 V	Magnetizing inductor / L_m	90 μH
Output power / P_o	500 W	Resonant inductor / L_r	1.7 μH
Switching frequency / f_s	500 kHz	Resonant capacitor / C_r	58 nF
Turns ratio / N	12 : 2 : 2	Output capacitor / C_o	100 μF

observed, the drain-source voltage of Q_2 and Q_4 have already decayed to zero before they are turned on, thereby realizing zero-voltage turn-ON. In fact, Q_1 and Q_3 also achieve ZVS, where the waveforms are omitted for brevity. The experimental results demonstrate that full-range ZVS is realized for all the power switches with the proposed control method. Additionally, it can be also seen that under heavy- load conditions, the minimum inductor current is maintained constant at $-I_{\rm ZVS}$, and the inductor current ripple is gradually reduced as the load decreases, thus maximally reduced the current ripple while ensuring ZVS. When the load decreased below the power boundary, the ZVS current for Q_2 ($V_{\rm in} \le V_{\rm bus}$) or Q_3 ($V_{\rm in} > V_{\rm bus}$) is limited at $I_{\rm ZVS}$, and the $I_{\rm min}$ is slightly lower than $-I_{\rm ZVS}$. The experimental results agree well with the theoretical analysis in Section IV, validating the effectiveness of the proposed combined PWM and phase-shift control method with adaptive ZVS boundary regulation.

Fig. 14 shows the dynamic experimental waveforms of the FSBB-*LLC* converter. The dynamic waveforms when the load is step changed between no load and full load at rated input voltage (300 V) is shown in Fig. 14(a), where $i_{\rm o}$ is the load current, $v_{\rm o}$ is the output voltage, i_{Lc} is the inductor current, and i_{Lr} is the resonant current. As seen, the overshoot and undershoot on the output voltage during the load transients is only 1.6 and 3.2 V, and the recovery time is short, indicating that good dynamic performance is realized with the proposed control method. More importantly, with the proposed adaptive ZVS boundary regulation, the phase-shift signals for light-load and heavy-load conditions are generated through the phase-shift calculation unit and the phase-shift closed-loop control unit, respectively. Clearly, the transition of the phase-shift duty cycle is smooth during load transients. Fig. 14(b) shows the dynamic waveforms when the input voltage $v_{\rm in}$ is step changed between 200 and 400 V at full-load condition. As can be seen, the output voltage also exhibits small overshoot and undershoot, indicating that the control method exhibits good dynamic performance.

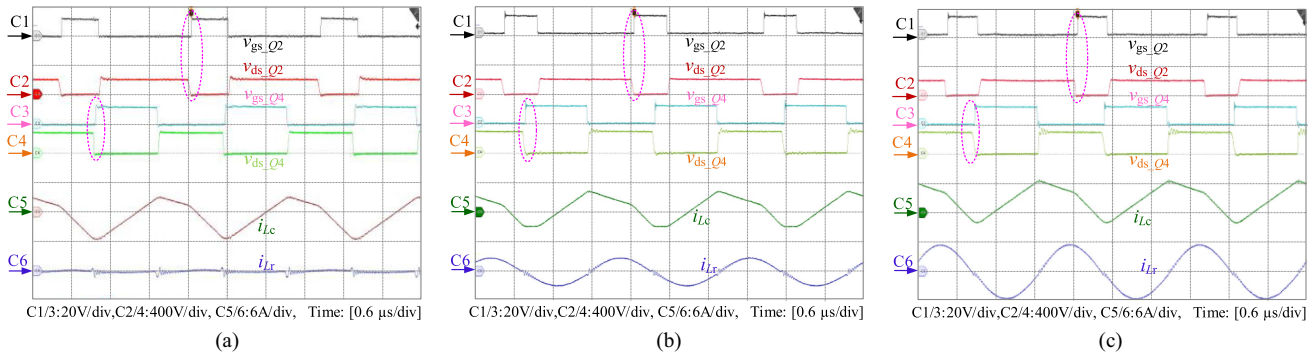

Fig. 11. Steady state waveforms of the FSBB-*LLC* converter when $V_{\text{in}} = 200$ V. (a) No load. (b) Half load. (c) Full load.

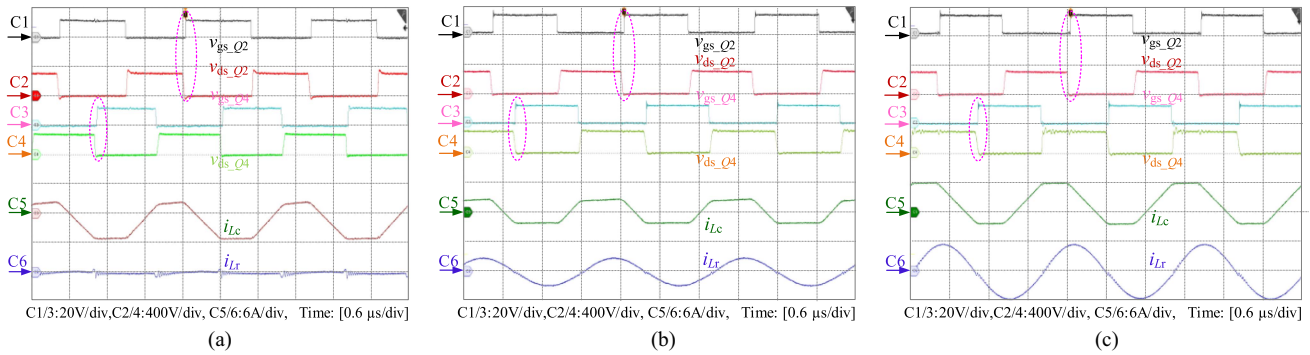

Fig. 12. Steady state waveforms of the FSBB-*LLC* converter when $V_{\text{in}} = 300$ V. (a) No load. (b) Half load. (c) Full load.

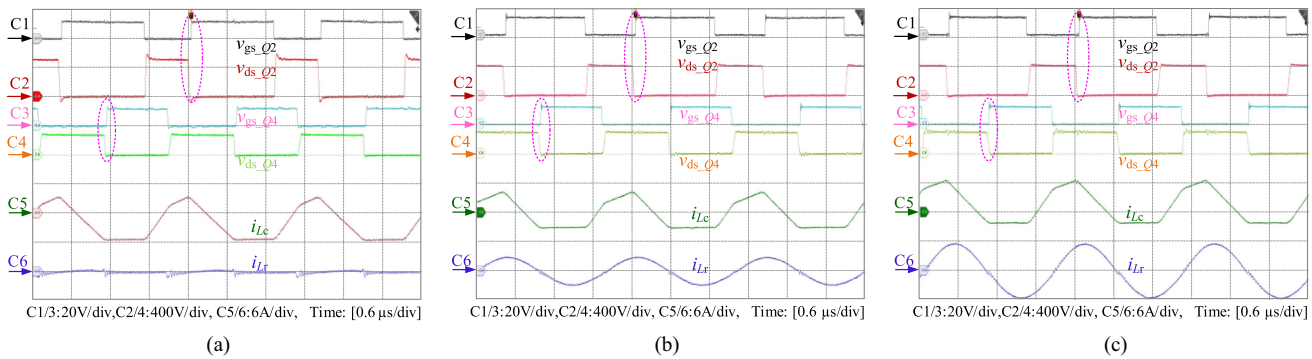

Fig. 13. Steady state waveforms of the FSBB-*LLC* converter when $V_{\text{in}} = 400$ V. (a) No load. (b) Half load. (c) Full load.

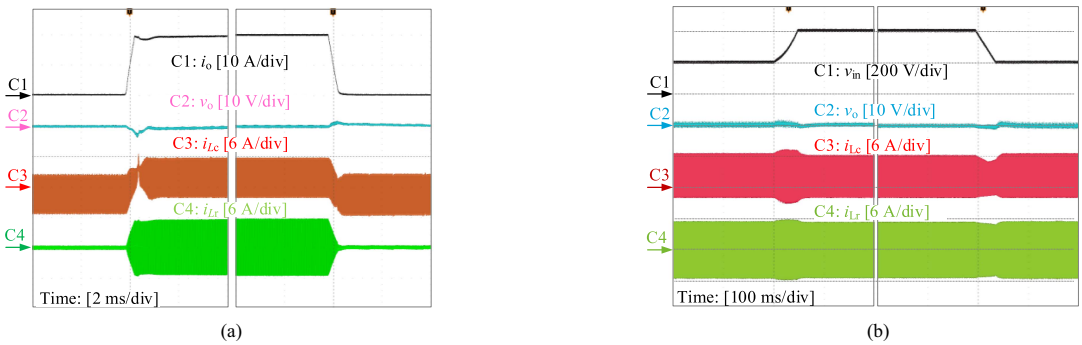

Fig. 14. Dynamic waveforms of the FSBB-*LLC* converter. (a) Load step change between no load and full load when $V_{\text{in}} = 300$ V. (b) Input voltage step change between 200 V and 400 V at full-load condition.

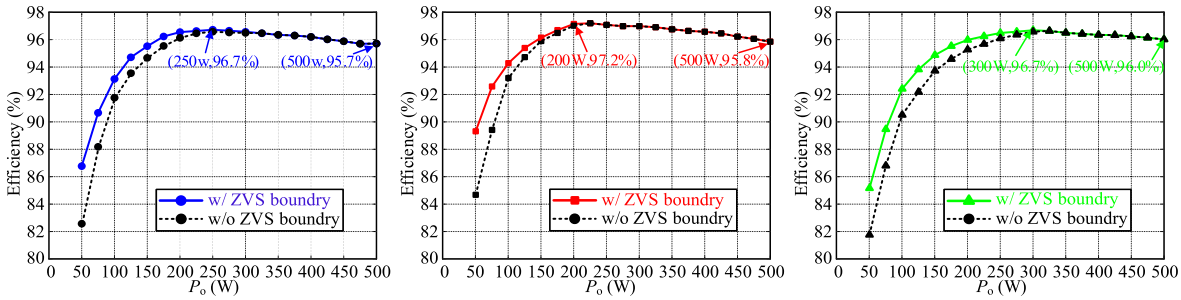

Fig. 15. Measured efficiencies of the FSBB-*LLC* converter in the full range. (a) $V_{\rm in} = 200$ V. (b) $V_{\rm in} = 300$ V. (c) $V_{\rm in} = 400$ V.

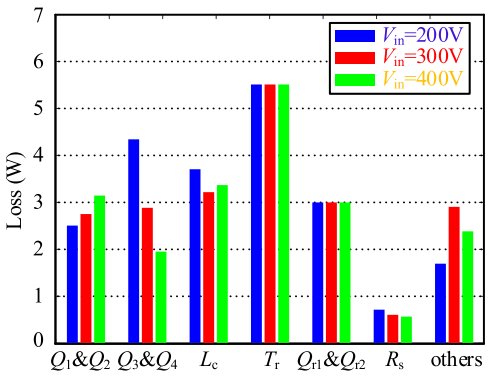

Fig. 16. Loss breakdown of the FSBB-*LLC* converter.

Fig. 15 presents the measured efficiencies of the FSBB-*LLC* converter in the full load range, both with and without the ZVS boundary control, when the input voltages is 200, 300, and 400 V, respectively. As seen, the peak efficiency reaches 97.2% when $V_{\rm in} = 300$ V and $P_{\rm o} = 225$ W. Furthermore, with the incorporation of the proposed adaptive ZVS boundary regulation, a notable efficiency improvement is achieved under light-load conditions when the power is lower than the boundary power. Therefore, high efficiencies are realized in the full range with the proposed control scheme.

Fig. 16 shows the calculated loss breakdown of the FSBB-*LLC* converter at the rated output power, where $R_{\rm s}$ is the sensing resistor for the inductor current. Since all the power switches realize ZVS, the switching losses are negligible. Consequently, the majority of the losses in power switches are conduction losses. As seen, the losses in the nonreused bridge arm (Q_1 and Q_2) increase with the rise of the input voltage, while the current flowing through the reused bridge arm (Q_3 and Q_4) is $i_{Lc}-i_{Lr}$, and the current cancellation effect is enhanced as input voltage increases. Thus, the losses in Q_3 and Q_4 decrease with the rise of the input voltage. For the transformer and secondary rectifier devices, since the bus voltage is regulated to a constant value, the *LLC* stage works in the same situation across the full input voltage range and results in the same transformer loss and secondary devices loss at different input voltages. The efficiency over the entire voltage range is the result of the sum of several parts, and in this prototype, the highest full-load efficiency is obtained at an input voltage of 400 V, which is 96.0% . Obviously, the loss breakdown is well in agreement with the measured efficiencies shown in Fig. 15.

VI. Conclusion

The bridge-arm reused FSBB-*LLC* converter can achieve wide-range voltage regulation and high-efficiency galvanic isolation with reduced number of devices. In this article, a combined PWM and phase-shift control method with adaptive ZVS boundary regulation is proposed, which realizes ZVS of power switches while maximally reduces the inductor current ripple in the full range. First, ZVS conditions considering the constrains on ZVS current and phase-shift duty cycle are revealed, and the design principle of the inductor considering ZVS range and maximized reduction on inductor current ripple is proposed. Then, the basic idea and design method of the adaptive ZVS boundary regulation is proposed. By adjusting the phase-shift duty cycle to control the inductor current adaptively, ZVS is ensured while the inductor current ripple is maximally reduced. Based on that, a combined PWM and phase-shift control method and its implementation for the FSBB-*LLC* converter are proposed and compared. Finally, a prototype of a 500-W FSBB-*LLC* converter is built and tested in the lab. The experimental results verified the effectiveness of the proposed control method.

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