Reliability-Oriented Routing of Internal Current Stress in the Two-Stage SST Submodule

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***Abstract*—Power routing has emerged as a promising technique for balancing the remaining useful lifetime of modular converters, e.g., solid-state transformers (SSTs). However, this approach does not address the internal stress distribution within the individual two-stage submodules. In this article, a method to balance the internal stress by redistributing the second harmonic current between the dc-link capacitors and the devices in dc/dc stage is presented. This method introduces an adjustable ripple to the basic phase-shift modulation, directing a portion of the second harmonic current to the rear-end dc/dc stage in accordance with the lifetime differences within submodules. It requires minimal control effort and provides sufficient thermal balance capability within the submodule. Notably, it focuses exclusively on the second harmonic current, with negligible impact on the output power. Experimental results demonstrate its effectiveness in achieving thermal regulation and lifetime balance within the submodules.**

***Index Terms*—Harmonic current, lifetime balance, power routing, reliability, solid-state transformer (SST).**

I. Introduction

SOLID-STATE transformers (SSTs) are potential solution for the future power distribution, which is formed by the serial or parallel connection of the power units [1], [2]. A typical modular SST consisting of cascaded H-bridge (CHB) cell and isolated dc/dc converter is shown in Fig. 1. However, its reliability remains a significant concern, particularly regarding the fragility of capacitors and power devices [3], [4]. High-margin designs are employed to ensure the required useful lifetime, leading to a significant increase in manufacturing costs. Moreover, mismatches in the remaining useful lifetime (RUL) among power electronics components result in frequent maintenance. This issue is especially significant in remote or offshore environments, where the energy yield loss from frequent maintenance often far exceeds the direct operation and maintenance costs of the equipment [5]. Thereby, it is essential to investigate viable solutions that ensuring a longer failure-free operation time.

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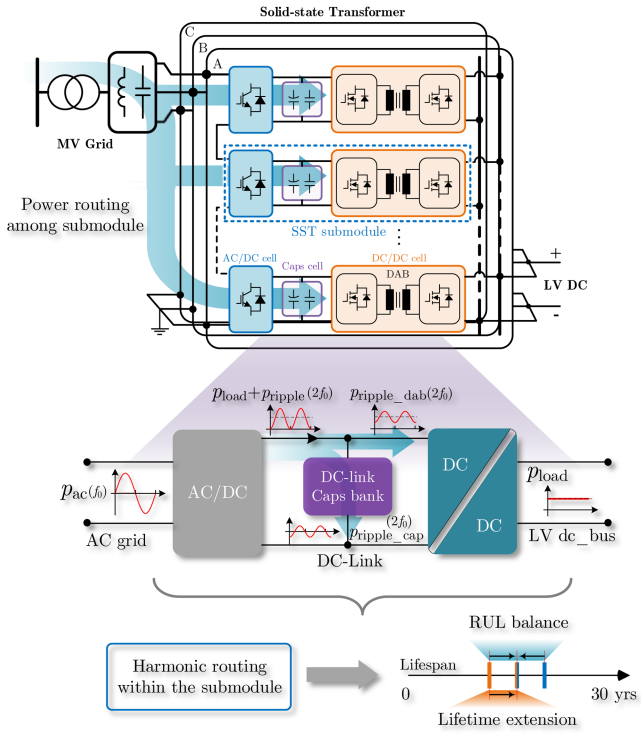

Fig. 1. Structure of the modular SST and illustration of the power routing concept. The power distribution between submodules is shown in the upper part, while the energy distribution within the submodule proposed in this article is illustrated in the lower part.

Power routing, as illustrated in the bottom of Fig. 1, is considered an effective software-based solution for achieving lifetime balance without incurring additional fabricating costs [6]. It maximizes the overall useful lifetime of the system by actively coordinating energy allocation while preserving the required external characteristics [7]. The power routing approach leverages recent advancements in aging mechanism research, condition monitoring techniques, and RUL estimation for capacitors and power devices [3], [8], [13]. These theories enable informed decision-making for proactive equipment control during operation.

Preliminary studies have demonstrated the effectiveness of power routing, particularly in modular power electronic converters. Marquez et al. [15] propose a control scheme which implement the power routing concept in a modular dc/dc converter, extending the overall lifetime by thermal balance. Leon et al. [16], Ko et al. [17], and Ko et al. [18] control the electrical

stress across multiple submodules using pure sinusoidal modulation, multifrequency modulation, and discontinuous modulation strategies, respectively, to align the RUL of different submodules. Moreover, the active thermal control has been implemented to extend the lifetime of submodules [20], delaying the 10% failure rate by 11 months [21]. However, while existing power routing strategies have achieved balancing across multiple submodules, they are limited in the ability to achieve balance within the submodules. The issue of reliability imbalance within the submodule still needs to be addressed.

Inside the submodule, the second harmonic current is generated by the front-end ac/dc stage and distributes across the dc-link capacitors and the rear-end dc/dc stage. By redistributing the harmonic current in the early design phase, the lifetime of the dc-link capacitors and DAB devices can be balanced [22]. This article primarily investigates the active control methods for harmonic distribution. Liu et al. [25] and Zhang and Ruan [26] suppress the second harmonic current from the perspective of output impedance in a single phase two-stage converter, the reduced demand for capacitance leads to fewer number of capacitors, which in turn reduces potential risks in capacitor bank. Xue et al. [27] actively introduces the second harmonic current to the dc/dc converter, thereby reducing the ripple current stress on the capacitor and reducing the demand for capacitance. Whereas, the second harmonic has a negative impact on the lifetime of the rear-end dc/dc converter.

Therefore, the correct distribution of harmonics within submodules is crucial, and this can be managed during the design phase by selecting appropriate dc-link capacitors [9]. However, even if the lifetime is balanced in the design phase, this balance may be disrupted during operation due to parameter drifts and environment variations [6].

This article aims to achieve a balanced lifetime for the dc-link capacitor and the devices of rear dc/dc stage by actively manipulate the sharing of harmonic during operation. Based on the condition monitoring and lifetime estimation results, the proposed method utilizes the feedback of the dc-bus voltage with a band pass filter to actively distributes the harmonic distribution, allowing cells that are aging severely to bear less ripple current stress. The novelty of proposed approach lies primarily in three aspects:

1) The accurate quantification of second-order harmonic distribution in the CHB topology.
2) Quantitative evaluation of harmonics on temperature and losses.
3) Lifetime-aware energy routing across heterogeneous components.

The effectiveness of this method was verified in a 3.8 kW SST submodule, where it was demonstrated that the distribution of harmonic energy can be readily controlled in an adequate range.

II. Aging Mechanisms and Driven Factors of the Key Components

The submodule contains multiple capacitors and power devices that are critical to its reliability. Understanding the mechanisms and driving factors behind their degradation is essential for identifying effective routing targets and solutions.

A. Aging of Power Semiconductor Devices

The primary factors contributing to thermal-related failure is the bond wire damage and the degradation of die-attach. These failures primarily arise from the average temperature and the temperature swing. According to the lifetime model, the expected number of cycles to failure, N_f, is computed by Coffin–Manson–Arrhenius model [28], [29], [30].

$$N_f = \mathrm{C} \times (\Delta T_j)^{-\alpha} \times \exp\left(\frac{E_a}{k_B \times T_{jm}}\right) \tag{1}$$

where ΔT_j is the junction temperature swing. T_{jm} is the mean junction temperature. C and α represent the aging index factors. The value of activation energy E_a represents the degree to which failure is affected by temperature. k_B is Boltzmann constant.

After computing the cycle-to-failure for a specific mission profile, the annual damage fraction D_{sw} can be obtained by considering the annual power cycling (N_p) and the cycle-to-failure for each operating condition (denoted by "i") as described as

$$D_{\mathrm{sw}}(N_p) = \sum_{i=1}^{n} \frac{N_p(i)}{N_f(i)}. \tag{2}$$

The damage fraction represents the portion of the device's lifespan consumed by exposure to cycles at different stress levels. Generally, when the damage fraction reaches 1, it indicates that the number of failure samples is highest, suggesting that the device has reached the end of its lifespan.

B. Aging of Capacitors

The reliability issues of capacitors are as important as power semiconductors [8]. The lifespan of electrolytic capacitors is determined by three main factors. The ambient temperature and ripple current contribute to the diffusion of electrolyte through the capacitor seal. The applied voltage induces an electrochemical reaction at the dielectric layer. These factors have been given in [16]. Consequently, the lifespan model for electrolytic capacitors can be expressed as follows:

$$L_{\mathrm{ex}} = L_r \cdot K_T \cdot K_R \cdot K_V \tag{3}$$

$$\begin{cases} K_T = 2^{\frac{T_r - T_a}{10}}; & \text{ambient temperature coefficient} \\ K_R = 2^{\left(1-\left(\frac{I_x}{I_r}\right)^2\right)\cdot\frac{\Delta T_0}{n_1}}; & \text{ripple current coefficient} \\ K_V = \left(\frac{V_r}{V_x}\right)^{n_2}; & \text{operating voltage coefficient} \end{cases} \tag{4}$$

where L_{ex} is the operation life of the electrolytic capacitors, L_{r} the rated lifetime, T_r the upper category temperature, T_a the ambient temperature, and ΔT_0 the increase of core temperature. V_x and I_x are the actual operating voltage and ripple current, whilst V_r and I_r are the rated voltage and ripple current respectively. n_1 is the acceleration factor of the temperature rise caused by the ripple, with a value between 5 and 10. n_2 is the electrolytic capacitors acceleration factor caused by operate voltage.

Compared to electrolytic capacitors (E-caps), film capacitors (F-caps) offer superior reliability, featuring self-healing properties and a higher tolerance to ripple current. Under appropriate operating conditions, their service life significantly exceeds that

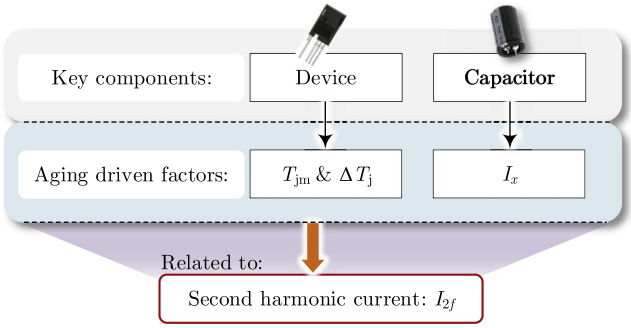

Fig. 2. Aging driven factors of the key components under a given hardware specification and operating environment.

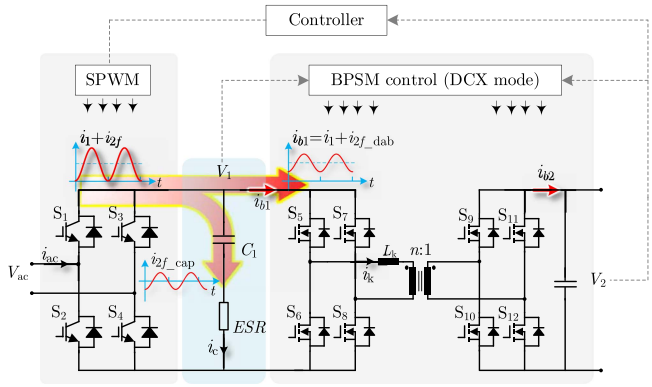

Fig. 3. Control scheme of the SST submodule.

of E-caps. The lifetime of F-caps can be modeled as follows:

$$L_{\mathrm{fx}} = L_r \cdot 2^{\frac{T_r - T_a}{10}} \cdot \left(\frac{V_r}{V_x}\right)^{n_3} \tag{5}$$

where L_{fx} is the operation life of the F-cap and n_3 the factor of acceleration caused by the operating voltage.

To evaluate the reliability in long-term operation, cumulative damage can be converted to capacitance loss [31]

$$\begin{cases} \Delta C_{e-\mathrm{cap}}(t_p) = \sum_{i=1}^{n} \frac{t_p(i)}{L(i)} \cdot 20\% C \\ \Delta C_{f-\mathrm{cap}}(t_p) = \sum_{i=1}^{n} \frac{t_p(i)}{L(i)} \cdot 5\% C \end{cases} \tag{6}$$

where $\Delta C_{e\text{-cap}}$ and $\Delta C_{f\text{-cap}}$ denote the capacitance loss of electrolytic capacitor and film capacitor at operating time instant t_{p}, $L(i)$ represents the expected lifetime under a specific operating condition i. The more the capacitance loss, the higher the unreliability probability [31].

C. Discussion of Aging Driven Factor

The aging of power devices is primarily determined by the average temperature and temperature swing, while the aging of capacitors is mainly influenced by the ripple current. These parameters are both influenced by the second harmonic currents, as illustrated in Fig. 2.

On one hand, the second harmonic current increases the device losses, leading to rises in the average temperature and a temperature fluctuation at secondary frequency. On the other hand, second harmonic current is the main components of the capacitor ripple current, making them the primary causes of capacitor aging.

Given the significant influence of second harmonic current on the reliability of key components, the power routing from the view of second harmonic current is performed to ensure lifetime balance within the submodule.

III. Modeling and Control Scheme of the Second Harmonic Current

Building on the aging mechanism of the power device and capacitor, this section explains how the proposed harmonic routing method balances the stress on dc-link capacitors and dc/dc stage devices in an SST submodule, including the generation mechanism, distribution modeling, and control strategy of harmonic current.

A. Generation of the Harmonic Current

One typical control scheme involves controlling the dc-bus voltage and the LV side dc voltage, where the front-end controls the low side dc voltage, while the rear-end dual active bridge (DAB) operates in DCX mode, offering a fixed voltage ratio [32], as shown in Fig. 3.

The harmonic is inevitably introduced by ac/dc stage, which can be defined as an ac current source at secondary frequency [3]

$$i_{2f} = \frac{P}{V_1} \cos(2\omega_0 t + \theta) \tag{7}$$

where $\omega_0 = 2\pi f$, f is the line frequency (e.g., 50 Hz), θ denotes the phase angle, P represents the transferred power, and V_1 denotes the dc-bus voltage.

B. Modeling of Its Propagation and Distribution

The distribution of i_{2f} depends on the specific impedance between the dc-link and the rear-end DAB stage.

For dc-link, the impedance can be computed by the capacitance and the *ESR*, and the capacitive impedance is dominant at second harmonic frequency

$$\boldsymbol{Z}_{\mathrm{cap}} = \mathrm{ESR} + \frac{1}{\boldsymbol{j}\omega_{2f} C_1} \approx \frac{1}{\boldsymbol{j}\omega_{2f} C_1}. \tag{8}$$

While for the DAB, the equivalent impedance is related to the design parameters and the control strategy. Under convention control scheme as Fig. 3, the impedances of DAB cell are analyzed as Fig. 4.

The double switching frequency $2f_{\mathrm{s}}$ dominates the DAB cell due to the chopping of switches. Focusing only on the double switching frequency, the secondary side is approximately modeled as an ideal voltage source because of multiple capacitors connected in parallel, with extremely very small impedance ($1/\omega C$), while the magnetizing inductance L_m and the core equivalent resistance R_{core} have large impedances and can be ignored.

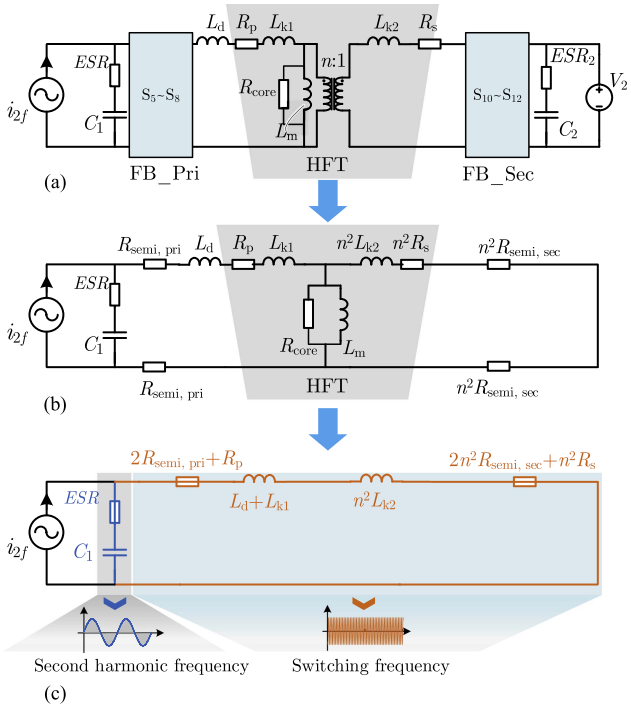

Fig. 4. Equivalent impedance model in view of second harmonic frequency current. (a) Original circuit model. (b) Transformer-equivalent model. (c) High-impedance neglected model.

Therefore, the impedance of the DAB at the $2f_s$ frequency can be derived as:

$$\boldsymbol{Z}_{\text{dab\_2}f_s} = 2R_{\text{semi,pri}} + R_p + 2n^2R_{\text{semi,sec}} + n^2R_s + \boldsymbol{j}\omega_{2f_s}(L_d + L_{k1} + n^2L_{k2}) \approx \boldsymbol{j}\omega_{2f_s}(L_d + L_{k1} + n^2L_{k2}) \tag{9}$$

where the DAB inductance $L_k = L_d + L_{k1}$, L_d represents the additional inductance, and L_{k1} denotes the leakage inductance in the primary side of transformer.

The switching frequency of SiC MOSFET-based DAB, usually in more than hundreds of kilohertz, which is much higher than the second harmonic frequency (e.g., 100 Hz). Different from the impedance model of *CLLC* resonant converter in [22], where the resonant inductance and capacitance impedance can be completely offset, the leakage inductance (L_{k1}, L_{k2}) and the additional inductance (L_d) in DAB cause a quite larger impedance than that of dc-link, and the inductive impedance dominants, as shown in (9). Therefore, most of the second harmonic current flows into the dc-link, inducing a high current stress in capacitors.

C. Illustration of the Proposed Control Strategy

Fig. 3 illustrates the targets second harmonic frequency current will share in dc-link capacitor and the rear-end DAB stage. The proposed strategy aims to control the sharing ratio of the harmonic current, and thereby regulates the thermal stress following the estimated lifetime.

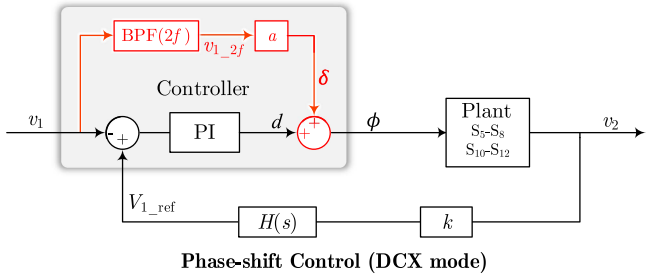

Fig. 5. Basic control scheme and the proposed harmonic current control.

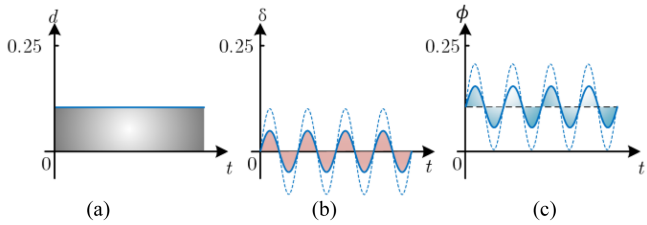

Fig. 6. Phase-shift angle. (a) Basic control. (b) Secondary ripple induced by active control. (c) Active control.

The expression of output current i_{b2} can be established as

$$P_0 = v_1 i_{b1} = v_2 i_{b2} \tag{10}$$

$$i_{b1} = \frac{n\phi(1-2\phi)}{f_s L_k} v_2 = \xi\phi(1-2\phi) \tag{11}$$

$$i_{b2} = \frac{n\phi(1-2\phi)}{f_s L_k} v_1 \tag{12}$$

where the normalized phase shift angle is denoted as ϕ, ranging from 0 to 1. To ensure high efficiency, this value is typically restricted to a maximum of 0.25 [24]. ξ represents a constant value that are constituted by the voltage transfer ratio n, the DAB inductor L_k, the switching frequency f_s and the voltage V_2. It can be expressed as

$$\xi = \frac{nV_2}{f_s L_k}. \tag{13}$$

To manage the harmonic distribution, a phase shift control strategy by incorporating a second harmonic frequency ripple δ into the basic phase-shift ratio d is illustrated as Fig. 5, which actively directs part of the second harmonic current into rear-end dc/dc stage. The coefficient k represents the transfer relationship between v_1 and v_2. By introducing a band-pass filter (BPF) at second harmonic frequency, the DAB phase shift ratio changes from a constant value to a variable encompassing second harmonic frequency, as shown in Fig. 6. The transfer function of BPF and low-pass filter H(s) is as follows:

$$\text{BPF}(s) = \frac{2\pi s}{s^2 + 2\pi s + (2\omega_0)^2} \tag{14}$$

$$H(s) = \frac{\omega_{\text{ref}}}{s + \omega_{\text{ref}}}. \tag{15}$$

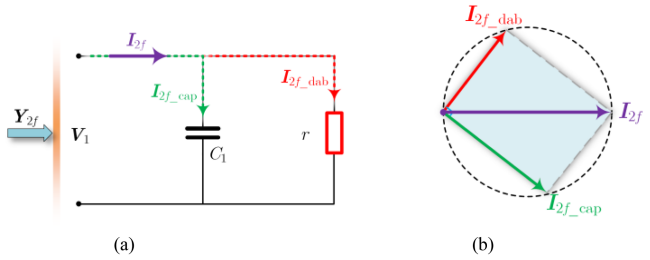

Fig. 7. (a) Impedance distribution corresponding to (18). (b) Second harmonic current sharing law.

Adjusting the value of "*a*," the amplitude of δ can be changed, thereby enabling control over the online distribution of the second harmonic frequency component.

The model can be derived as follows:

$$\phi = d + \delta = d + av_{1\_2f} = d + aV_{1\_2f}\cos(2\omega_0 t + \theta_v) \quad (16)$$

where the $v_{1\cdot 2f}$ represents the second harmonic frequency component (i.e., 100 Hz) of v_1, with amplitude $V_{1\cdot 2f}$ and phase angle θ_v. The value of a should not be too large, as this would cause the amplitude of δ to exceed the fundamental phase shift ratio d, leading to an increase in the overall second harmonic current and consequently introducing additional thermal stress to the system.

Substituting (15) into (10), two components dominate current i_{b1}: The dc component $i_{b1\cdot \mathrm{dc}}$, which indicates the power transmitted between the primary and secondary sides of the DAB; and the second harmonic frequency component $i_{b1\cdot 2f}$, which represents the harmonic current generated by the active control strategy

$$\begin{cases} i_{b1\_\mathrm{dc}} = kd(1-2d) - ka^2 V_{1\_2f} \\ i_{b1\_2f} = ka(1-4d)V_{1\_2f}\cos(2\omega_0 t + \theta_v) \end{cases} \quad (17)$$

where the basic phase shift ratio d is automatically calculated by the PI controller.

According to (16), $i_{b1\cdot 2f}$ and $v_{1\cdot 2f}$ are in phase, and the equivalent model of the DAB is resistive at a frequency of $2f$, and its expression is as follows:

$$\boldsymbol{Z}_{\mathrm{dab}\_2f} = r = \frac{1}{ka(1-4d)}. \quad (18)$$

Replacing the subsequent circuit with the impedance $Z_{\mathrm{dab}\cdot 2f}$, the equivalent circuit model at the 2_f frequency is obtained, as shown in Fig. 7(a), which is a parallel model consisting of a variable resistor r and a dc-Link capacitor C_1. The admittance expression is as follows:

$$\boldsymbol{Y}_{2f} = \frac{\boldsymbol{I}_{2f}}{\boldsymbol{V}_{1\_2f}} = j\omega C_1 + \frac{1}{r}. \quad (19)$$

The vector relationships of their respective impedances and harmonic currents are illustrated in Fig. 7(b) adjusting the additional impedance $Z_{\mathrm{dab}\cdot 2f}$ allows for the regulation of harmonic currents distribution ratio.

According to (18) and the vector relationship in Fig. 7(b), the amplitude relationship of i_{2f}, $i_{2f\cdot \mathrm{dab}}$, and $i_{2f\cdot \mathrm{cap}}$ is obtained as follows:

$$I_{2f\_\mathrm{dab}} = \frac{1}{\sqrt{1+(2\omega_0 rC_1)^2}} I_{2f} \quad (20)$$

$$I_{2f\_\mathrm{cap}} = \frac{2\omega_0 rC_1}{\sqrt{1+(2\omega_0 rC_1)^2}} I_{2f}. \quad (21)$$

Define $R(a)$ as the ratio of $i_{2f\cdot \mathrm{dab}}$ to I_{2f}, and utilize (18)–(20) to determine the effect of a on the second harmonic frequency current, as follows:

$$R(a) = \frac{I_{2f\_\mathrm{dab}}}{I_{2f}} = \left[1 + \left(\frac{2\omega_0 C_1}{ka(1-4d)}\right)^2\right]^{-\frac{1}{2}}. \quad (22)$$

As the value of a increases, the value of $R(a)$ increases and approaches 1. When the double frequency current I_{2f} is the largest and $I_{2f\,\mathrm{dab}}$ is approximately 0, the upper limit of the value of a is determined. Using (19) to (20), the ratio of the two amplitudes is 50, which is approximately equivalent to the above situation, and the following relationship can be obtained:

$$100\omega_0 C = \frac{1}{r} = ka(1-4d). \quad (23)$$

Using the parameters in Table I, the range of variable a can be calculated to be from 0 to 0.1. When $a > 0.1$, the changes in the distribution pattern of harmonic current will no longer be significant.

TABLE I
ELECTRICAL SPECIFICATIONS

Parameters	Value
DC-bus voltage V_1	400 V
DC-link capacitance C	630 μF
Output voltage V_2	300 V
AC voltage V_{ac}	220 Vrms
Transferred power P	3.8 kW
AC/DC switching frequency $f_{\mathrm{ac/dc}}$	10 kHz
DAB switching frequency f_s	100 kHz
DAB inductance L_k	15 μH

IV. Routing Frameworks and Impacts Evaluation

A. Overall Procedures of Harmonic Current Routing

This active power routing strategy uses a variable phase shift angle to intervene in the distribution of harmonic current based on the results of condition monitoring and remaining lifetime assessment. When the remaining life of the dc link capacitor is shorter than that of the rear devices, part of the harmonics is transferred to the downstream stage. Conversely, when the remaining lifetime of the downstream devices is shorter than that of the capacitor, part of the harmonics is transferred to the dc-link capacitor. The goal of the control strategy is to align the lifetime of the dc-link capacitors and the rear dc/dc devices.

The procedures are shown in Fig. 8, which can be explained as follows.

1) Monitoring the health state of dc-link capacitor through the capacitance or ESR [3], [8], [9], and monitoring the

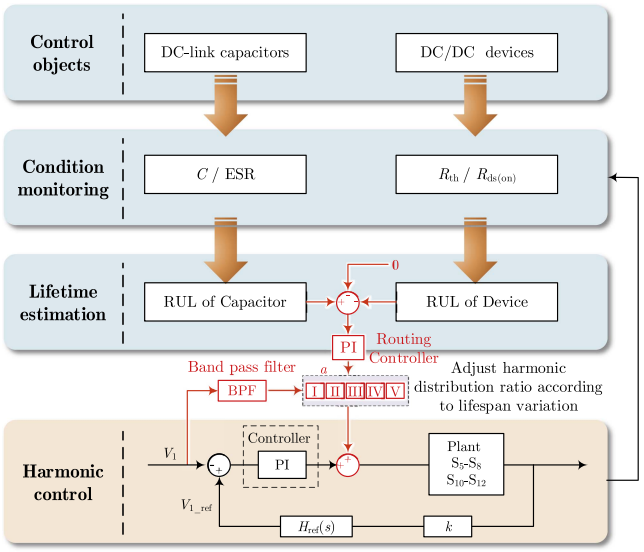

Fig. 8. Methodology of power routing strategy.

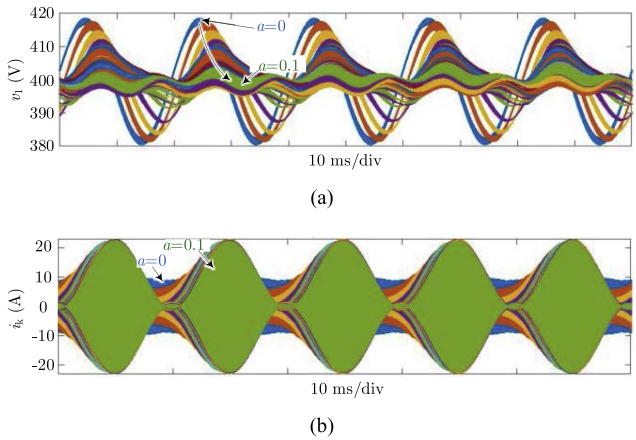

Fig. 9. Electrical stresses vary as "a." (a) DC-bus voltage v_1. (b) DAB inductance current i_k.

health of power semiconductor devices in the DAB via thermal resistance R_{th} or the on-state resistance $R_{ds(on)}$ [10], [11], [12].

2) Based on the condition monitoring results, combined with historical aging data and the life estimation model, the RUL can be calculated [13], [14].
3) Regarding condition monitoring and lifetime assessment of key components, the harmonic distribution level is adjusted through the control strategy outlined in Section III until their lifetimes are balanced.

Due to the long feedback cycle of the entire routing control loop, five control levels are adopted to ensure stable operation of the controller and to minimize potential risks to the system.

B. Impacts on Electrical Stresses

As shown in Fig. 9(a), the 100 Hz component of the dc-bus voltage decreases with an increase in "a". When "a" is zero,

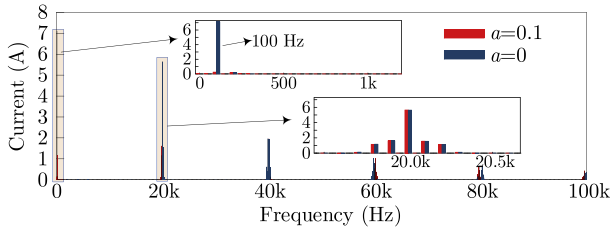

Fig. 10. FFT decomposition of capacitor current.

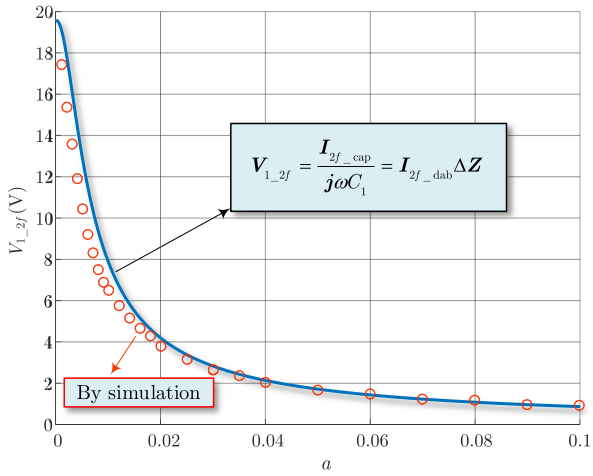

Fig. 11. Second harmonic voltage ripple under active control.

meaning no active control is applied, most of the second harmonic current naturally inject into the dc-link capacitor bank. As "a" increases, more and more second harmonic current flows into the rear-end DAB stage.

When "$a > 0.1$," nearly all harmonics are controlled and directed into the DAB converter, resulting in a significant increase in the ripple current of the DAB inductance, as illustrated in Fig. 9(b).

The second harmonic current I_{2f} is primarily distributed in the capacitor without active control, while it is mostly distributed in the rear-end DAB with strong active control, i.e., a>0.1. Moreover, as shown in the Fourier decomposition results in Fig. 10, the ripple current in the dc-link capacitors remains unaffected by high-frequency (i.e., 20 kHz) components at both $a = 0$ and $a = 0.1$, whereas the secondary harmonic current is redistributed.

In addition, Fig. 11 shows the impact of the variation in the parameter a on voltage fluctuations. It can be observed that the voltage fluctuation amplitudes calculated using the proposed model align well with the simulation results, demonstrating the accuracy of the distribution model. This indicates that the proposed scheme can adjust the distribution of second harmonic currents between the dc-link capacitors and the DAB converter, thereby optimizing the internal electrical stress distribution within the submodules.

C. Impacts on Power Loss

Injecting harmonic current into the DAB stage increases losses in its power devices and high-frequency transformer,

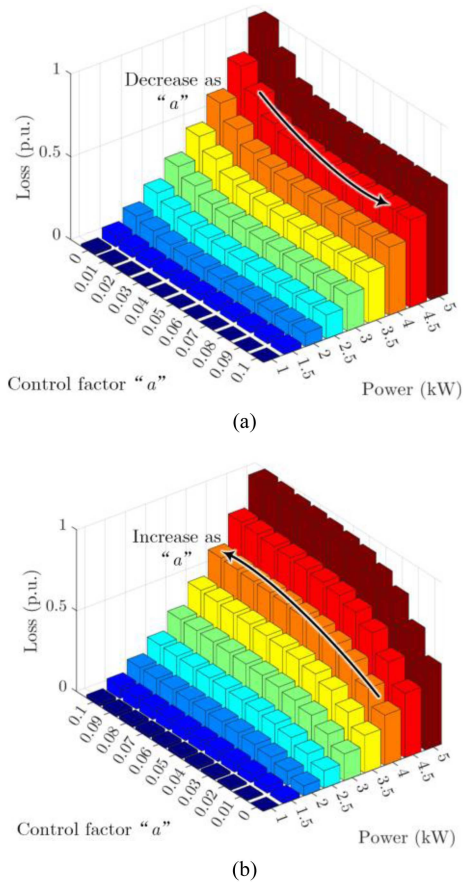

Fig. 12. Power loss vary as "a" and operating power. (a) Loss in DC-link capacitor. (b) Loss in rear-end DAB stage.

while injecting harmonic current into the dc-link capacitor raises the ripple current, leading to additional losses due to ESR. The assessment of loss in the DAB stage and dc-link capacitors can be analyzed through the total effective value of the ripple current [22].

The rms current calculation equation is given as

$$I_x = \sqrt{I_1^2 + I_2^2 + I_3^2 + \ldots + I_n^2} \tag{24}$$

where I_x represents the total effective value of the ripple current, while I_1, I_2,…, I_n represent the effective values of the fundamental, second-order, and n th-order harmonic currents, respectively.

The second harmonic current induces additional power loss in the DAB devices, high-frequency transformer windings, and dc-link capacitors. The loss increase in the DAB converter constitutes the major portion, and the efficiency can decrease by up to approximately 2% [22]. The impact on capacitors primarily involves lifespan degradation due to increased ripple current. The relationship between the active control factor "a" and the losses is presented.

As illustrated in Fig. 12(a), the loss in the dc-link capacitors decrease with the control factor "a," while the loss in the DAB converter increases with "a," as shown in Fig. 12(b). This suggests that not only is the harmonic distribution negatively correlated, but the power losses are also mutually constrained.

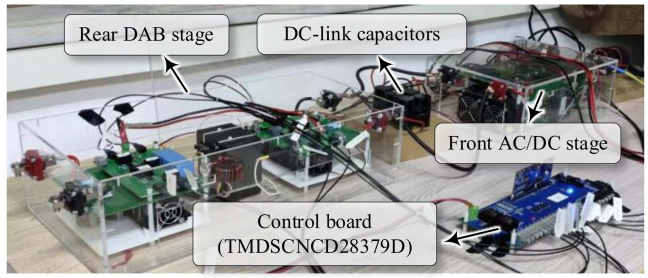

Fig. 13. Hardware setup.

Since the harmonic components in the switching devices of the DAB are relatively fixed and predictable, consisting mainly of the switching frequency and its sideband frequencies. As such, the associated losses and their controllability can be quantitatively analyzed and are largely independent of specific case conditions [3]. The total loss control range for the DAB is approximately 50% .

In contrast, the capacitor current contains a much broader and more complex harmonic spectrum. In addition to the fundamental low-frequency components (e.g., 100 Hz), it also includes significant higher-order harmonics whose magnitudes and frequencies vary depending on the system topology, control method, and operating conditions [22]. In this case, the loss control range for the dc-link capacitors is around 30% to 40% . Given that lifetime balancing is a continuous, long-term process, this control capability is sufficient to meet the requirements for balancing lifetimes.

V. Verifications

A. Prototype Specifications

To validate the accuracy of the harmonic distribution model and the effectiveness of the proposed active lifetime balancing strategy, experiments were conducted on a two-stage SST submodule. This submodule includes a front-end ac/dc converter based on IGBTs and a rear-end DAB converter based on SiC MOSFETs. The hardware specifications are set as Table I and Fig. 13.

B. Performance of Proposed Control Scheme

According to the harmonic distribution model established in Section III, the harmonic distribution control levels shown in Fig. 14 are specially formulated, which correspond to the five angles of 0°, 30°, 45°, 60°, and 90° in the vector diagram.

The current amplitudes of the dc-link capacitor unit and the DAB unit corresponding to the five harmonic distribution levels are given in Table II.

Based on the five adjustable levels of harmonic distribution, the harmonic distribution level can be selectively switched during operation according to the results of condition monitoring and lifetime prediction.

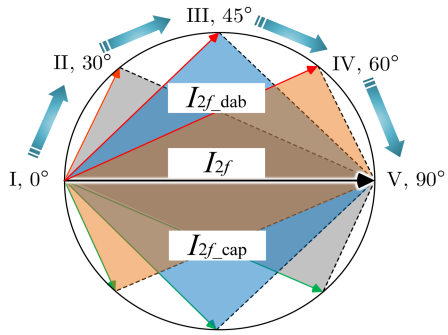

Fig. 14. Five levels of harmonic distribution.

TABLE II
RIPPLE CURRENT AMPLITUDE OF DC-LINK CAPACITOR AND DAB AT FIVE LEVELS

Routing Level	a	$I_{2f\ cap}$	$I_{2f\ dab}$
I	0	I_{2f}	≈ 0
II	0.0025	$\frac{\sqrt{3}}{2} I_{2f}$	$\frac{1}{2} I_{2f}$
III	0.0045	$\frac{\sqrt{2}}{2} I_{2f}$	$\frac{\sqrt{2}}{2} I_{2f}$
IV	0.008	$\frac{1}{2} I_{2f}$	$\frac{\sqrt{3}}{2} I_{2f}$
V	0.1	≈ 0	I_{2f}

Note: The values of a are calculated by Eqn. (21).

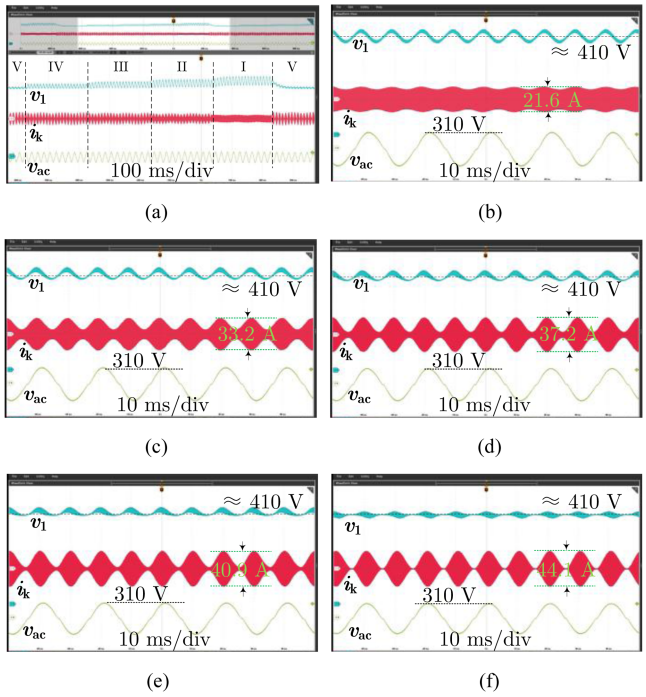

Fig. 15. Second harmonic current under open-loop control experiment. (a) Sweeping from distribution I to V. (b) Distribution I. (c) Distribution II. (d) distribution III. (e) Distribution IV. (f) Distribution V.

To verify the accuracy of the model presented in Section III-C, a set of tests is conducted under open-loop control mode. As shown in Fig. 15, the five distribution levels of harmonic current are swept. Fig. 15(a) illustrates the switching between different distributions, while Fig. 15(b)–(f) correspond to the details of each level, respectively. The results show that the harmonic current in the DAB $I_{2f\mathrm{dab}}$ gradually increases from level I to level V, while the dc-bus voltage is buffered due to the reduction in $I_{2f\mathrm{cap}}$. The relationship between the dc-bus voltage v_1 and the ripple current i_k exhibits a mutually constrained behavior, which aligns with the vector distribution model presented in Section III.

Furthermore, the voltage on the ac side remains unaffected across all five active control levels, indicating that the methods proposed in this article are independent of those in previous literature [6], [17], [18], [19], where power routing is performed by adjusting the voltage. It reveals that these methods can be combined with the proposed control to ensure the lifetime balance within the submodule.

The current distribution under the experiment and the proposed model is compared in Fig. 16. First, based on the analysis of the distribution impedance model in Section III, the DAB in the subsequent stage exhibits a high impedance to the secondary harmonic current. Therefore, at distribution level I, where no active control is applied, the harmonic current is almost entirely absorbed by the capacitance. The experimental results in level I, shown in Fig. 16, also align with this behavior. Additionally, the model and experimental results at other distribution levels correspond well. The results indicate the accuracy of the distribution model under the hardware parameters in this article.

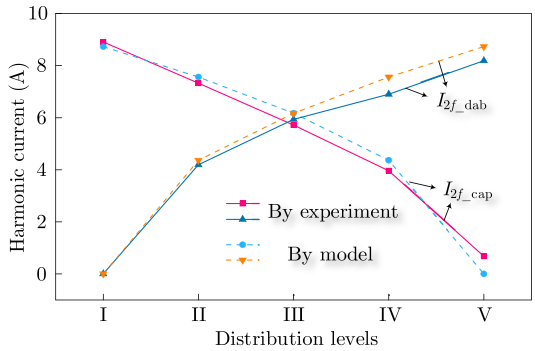

Fig. 16. Comparison between experiment and model in Section III-C.

To evaluate the performance of the control strategy in practical operation, a closed-loop testing approach is used to assess the dynamic response of harmonic redistribution. As shown in Fig. 17, the control system enables smooth transitions between distribution levels I and V, as well as between V and I. Specially, the proposed control targets on the reliability, and the degradation is a very slow process during the entire lifespan, resulting in minimal requirements for response speed.

Besides, as shown in Fig. 18, injecting harmonics into different units results in varying temperature distributions. In Fig. 18(a), since more harmonics are distributed across The dc-link capacitors, the temperature of the capacitors is higher, reaching 47.4 °C, while the external temperature of the DAB device is 46.9 °C. In Fig. 18(b), with more harmonics being injected to the DAB, the temperature of the power devices

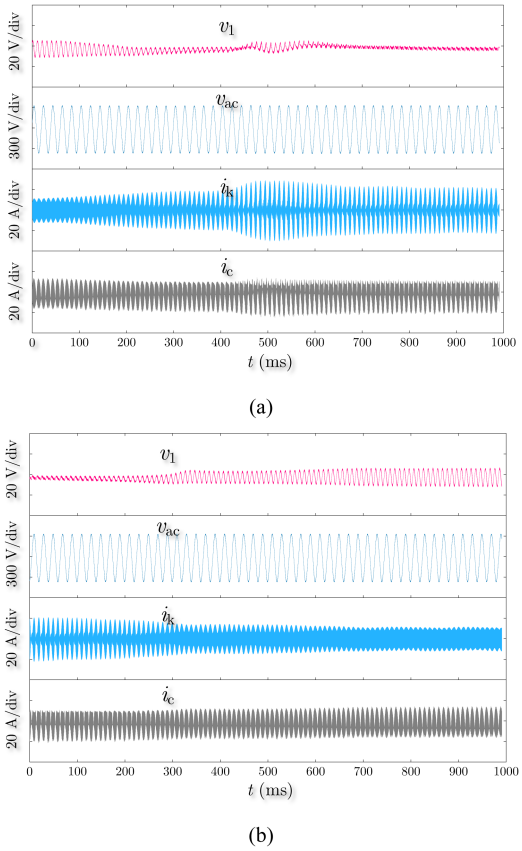

Fig. 17. Dynamic response under close-loop control. (a) I to V. (b) V to I.

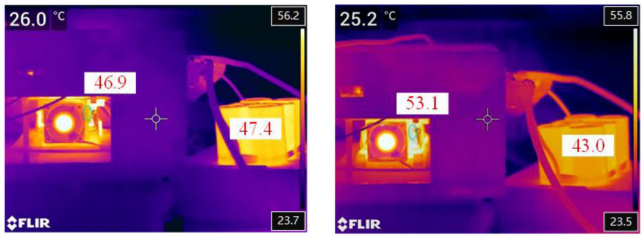

Fig. 18. Temperature distribution. (a) Level I. (b) Level V.

increases to 53.1 °C, while the external temperature of the capacitor drops to 43.0 °C. This temperature regulation range will also expand as the operating power increases.

C. Lifetime Balanced Performance

The goal of the proposed active lifetime balancing method is to prolong the failure-free operating time of the system by actively redistributing the stress among key components or cells. To evaluate the effectiveness of this method, collecting the annual load profile from the SCADA system of a 10 kV distribution transformer operated by state grid, which supplies power to multiple loads [22]. Based on this real-world data, the system's reliability was assessed through lifetime modeling and analysis.

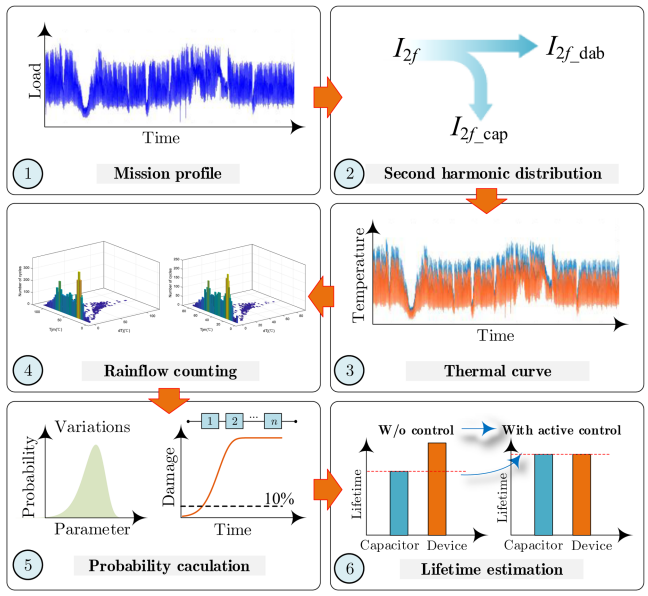

Fig. 19. Procedures of reliability estimation.

According to the model of the second harmonic current and the lifetime model in Section II, the lifetime balance performance can be estimated. The related parameters of lifetime formula are given as [22], and the overall procedures of reliability estimation are illustrated in Fig. 19.

The time-to-failure of samples obeys Weibull distribution

$$f(t) = \frac{\beta}{\eta}\left(\frac{t}{\eta}\right)^{\beta-1} \cdot \exp\left[-\left(\frac{t}{\eta}\right)^{\beta}\right] \tag{25}$$

where η and β represents the scale parameter and shape parameter, respectively.

The cumulative damage function is an integral of probability damage function, which can be written as

$$F(t) = \int f(t)dt = 1 - \exp\left[-\left(\frac{t}{\eta}\right)^{\beta}\right] \tag{26}$$

where the value of $F(t)$ can be seen as the unreliability probability at t operation period, which belongs to $0 \sim 1$.

Considering a system composed of several independent components, each exhibiting a constant hazard (or failure) rate. If the failure of any component will result in failure of the system, the system can be represented by a reliability block diagram [23]. Then, the failure probability of the overall system $F_{\mathrm{All}}(t)$

$$F_{\mathrm{All}}(t) = 1 - \prod_{i=1}^{k}\left(1 - F_{\mathrm{Individual},i}(t)\right) \tag{27}$$

where k denotes the number of components which influence reliability.

In this case, the unreliability probability of system is characterized by

$$F_{\mathrm{All}}(t) = 1 - \prod_{i=1}^{m}\left(1 - F_{\mathrm{cap},i}(t)\right) \cdot \prod_{j=1}^{n}\left(1 - F_{\mathrm{sw},j}(t)\right) \tag{28}$$

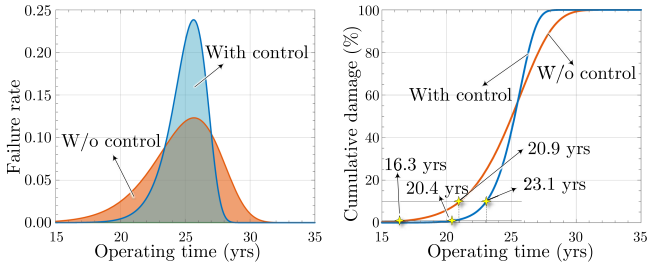

Fig. 20 System reliability evaluation before and after active control. (a) Failure rate. (b) Cumulative damage rate.

$$L_{B10} = T_{F_{\text{All}}==0.1} \tag{29}$$

$$L_{B1} = T_{F_{\text{All}}==0.01} \tag{30}$$

where the $F_{\text{cap},i}(t)$, $F_{\text{sw},i}(t)$ denote the unreliability probabilities of the i capacitors, j semiconductors, respectively. m, n are the numbers of capacitors and semiconductors.

The reliability under with or without active power routing is evaluated, and the results are shown in Fig. 20(a) and (b). It indicates that both the B_{10} and B_1 lifetimes are extended after the implementation of active control. Specifically, the B_{10} lifetime increases from 20.9 years to 23.1 years, while the B_1 lifetime extends from 16.3 years to 20.4 years.

Before the active control was applied, as discussed in Section III-C, the capacitors were subjected to higher levels of second harmonic current, resulting in lower reliability. According to the series reliability model, the failure of any single component leads to system failure. Thus, even though the power devices in the DAB converter own a longer lifetime, maintenance must still be scheduled earlier due to the failure of the capacitors.

With the proposed active harmonic current control method, a part of the second harmonic current is directed into the DAB, thereby reducing the ripple current stress on the dc-link capacitors. As a result, the remaining lifetime of both the dc-link capacitors and the devices in the DAB stage become more uniform, ultimately extending the failure-free operating lifetime of the system.

VI. Conclusion

This article addresses the issue of internal lifetime imbalance in the submodules of SST, proposing a balancing technique based on the regulation of second harmonic current distribution between the dc-link capacitors and the DAB devices. The strategy is low cost, easy to implement, and can be adjusted online. The main conclusions of this chapter are summarized as follows:

1) A distribution model for the second harmonic current in the front-end ac/dc cascaded with rear-end DAB submodules is established. Most of the second harmonic current flows into the capacitors before control, leading to high thermal stress and reduced reliability.
2) A control strategy is proposed that facilitates the redistribution of second harmonic current through a feedforward design of the dc-bus voltage ripple, utilizing only the existing control sampling.
3) With the power routing strategy, the B_{10} lifetime of the SST submodule in this case are extended from 20.9 years to 23.1 years, and the B_1 lifetime extends from 16.3 years to 20.4 years. Additionally, its effectiveness is more pronounced in higher operating power.

In practical applications, this method, which involves power routing within the submodule, can be combined with existing power routing techniques between submodules to ensure a longer lifespan of the SST system. Although this method may slightly compromise the inherent harmonic cancellation on the low-voltage side of the SST, the impact remains acceptable and manageable. Coordinated control among unbalanced harmonic components can be implemented to further mitigate this effect.

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References

[1] X. She, A. Q. Huang, and R. Burgos, "Review of solid-State transformer technologies and their application in power distribution systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 3, pp. 186–198, Sep. 2013.
[2] L. F. Costa, G. De Carne, G. Buticchi, and M. Liserre, "The smart transformer: A solid-state transformer tailored to provide ancillary services to the distribution grid," *IEEE Power Electron. Mag.*, vol. 4, no. 2, pp. 56–67, Jun. 2017.
[3] J. Wei, H. Feng, and L. Ran, "Integrated design for lifetime extension and ESR monitoring of hybrid DC link in solid-State transformer from the perspective of high-frequency ripple current," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 15583–15593, Dec. 2022.
[4] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1441–1451, May/Jun. 2011.
[5] J. F. Unnewehr, H. P. Waldl, T. Pahlke, I. Herráez, and A. Weidlich, "Reducing operational costs of offshore HVDC energy export systems through optimized maintenance," *Energies*, vol. 13, no. 5, May 2020, Art. no. 1146.
[6] M. Liserre et al., "Power routing: A new paradigm for maintenance scheduling," *IEEE Ind. Electron. Mag.*, vol. 14, no. 3, pp. 33–45, Sep. 2020.
[7] S. Zhao, X. Zhao, Y. Wei, Y. Zhao, and H. A. Mantooth, "A review of switching slew rate control for silicon carbide devices using active gate drivers," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4096–4114, Aug. 2021.
[8] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters—An overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sep./Oct. 2014.
[9] Z. Zhao, P. Davari, W. Lu, H. Wang, and F. Blaabjerg, "An overview of condition monitoring techniques for capacitors in DC-link applications," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3692–3716, Apr. 2021.
[10] Sumiti and V. Shrivastava, "Condition monitoring of power electronic devices-A review," in *Proc. 2nd Int. Conf. Adv. Comput. Innov. Technol. Eng.*, 2022, pp. 749–753.
[11] G. Susinni, S. A. Rizzo, and F. Iannuzzo, "Two decades of condition monitoring methods for power devices," *Electronics*, vol. 10, no. 6, pp. 683–711, Sep. 2021.
[12] J. Wei, F. Liang, H. Feng, and L. Ran, "Condition monitoring of discrete power devices: A data-driven approach with stress quantification and mold temperature sensing," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 3, pp. 2569–2579, Jun. 2024.

[13] S. Dusmez, M. Heydarzadeh, M. Nourani, and B. Akin, "Remaining useful lifetime estimation for power MOSFETs under thermal stress with RANSAC outlier removal," *IEEE Trans. Ind. Inform.*, vol. 13, no. 3, pp. 1271–1279, Jun. 2017.
[14] J. Wei, Y. Wang, S. Liu, H. Feng, and L. Ran, "Reliability-oriented design of DC-link considering the second-order harmonic current routing in an SST cell," *CPSS Trans. Power Electron. Appl.*, vol. 8, no. 3, pp. 290–299, Sep. 2023.
[15] A. Marquez, J. I. Leon, S. Vazquez, L. G. Franquelo, G. Buticchi, and M. Liserre, "Power device lifetime extension of dc-dc interleaved converters via Power routing," in *Proc. 44th Annu. Conf. IEEE Ind. Electron. Soc.*, 2018, pp. 5332–5337.
[16] J. I. Leon, S. Kouro, L. G. Franquelo, J. Rodriguez, and B. Wu, "The essential role and the continuous evolution of modulation techniques for voltage-source inverters in the past, present, and future power electronics," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2688–2701, May 2016.
[17] Y. Ko, M. Andresen, G. Buticchi, and M. Liserre, "Power routing for cascaded H-bridge converters," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9435–9446, Dec. 2017.
[18] Y. Ko, V. Raveendran, M. Andresen, and M. Liserre, "Advanced discontinuous modulation for thermally compensated modular smart transformers," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2445–2457, Mar. 2020.
[19] M. Andresen, V. Raveendran, G. Buticchi, and M. Liserre, "Lifetime-based power routing in parallel converters for smart transformer application," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1675–1684, Feb. 2018.
[20] M. Andresen, M. Liserre, and G. Buticchi, "Review of active thermal and lifetime control techniques for power electronic modules," in *Proc. 16th Eur. Conf. Power Electron. Appl.*, 2014, pp. 1–10.
[21] M. Andresen, J. Kuprat, V. Raveendran, J. Falck, and M. Liserre, "Active thermal control for delaying maintenance of power electronics converters," *Chin. J. Elect. Eng.*, vol. 4, no. 3, pp. 13–20, Sep. 2018.
[22] J. Wei, H. Feng, and L. Ran, "Multidimensional design of DC-link for two-stage solid-State transformer cell considering second-order harmonic current distribution," *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 10244–10255, Aug. 2023.
[23] P. D. T. O'Connor and A. Kleyner, *Practical Reliability Engineering*, 5th ed. Hoboken, NJ, USA: Wiley, 2012.
[24] S. Shao et al., "Modeling and advanced control of dual-active-bridge DC–DC converters: A review," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1524–1547, Feb. 2022.
[25] F. Liu, X. Ruan, X. Huang, and Y. Qiu, "Second harmonic current reduction for two-stage inverter with DCX-LLC resonant converter in front-end DC–DC converter: Modeling and control," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4597–4609, Apr. 2021.
[26] L. Zhang and X. Ruan, "Control schemes for reducing second harmonic current in two-stage single-phase converter: An overview from DC-bus port-impedance characteristics," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 10341–10358, Oct. 2019.
[27] L. Xue, Z. Shen, D. Boroyevich, P. Mattavelli, and D. Diaz, "Dual active bridge-based battery charger for plug-in hybrid electric vehicle with charging current containing low frequency ripple," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7299–7307, Dec. 2015.
[28] P. D. Reigosa, H. Wang, Y. Yang, and F. Blaabjerg, "Prediction of bond wire fatigue of IGBTs in a PV inverter under a long-term operation," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7171–7182, Oct. 2016.
[29] A. Testa, S. De Caro, and S. Russo, "A reliability model for power MOSFETs working in avalanche mode based on an experimental temperature distribution analysis," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 3093–3100, Jun. 2012.
[30] L. Ding, R. Song, S. Zhao, J. Wang, and H. A. Mantooth, "Active peltier effect heat sink for power semiconductor device thermal stability enhancement," *IEEE Trans. Power Electron.*, vol. 38, no. 9, pp. 11507–11520, Sep. 2023.
[31] Y. Li, Y. Zhang, R. Cao, X. Liu, C. Lv, and J. Liu, "Redundancy design of modular DC solid-state transformer based on reliability and efficiency evaluation," *CPSS Trans. Power Electron. Appl.*, vol. 6, no. 2, pp. 115–126, Jun. 2021.
[32] R. Ding, F. Wang, N. Zhang, S. Shi, S. Cheng, and F. Zhuo, "A decentralized control strategy with output voltage deviation-correction for input-series-output-parallel DC transformer based on dual-active-bridge," in *Proc. IEEE 9th Int. Power Electron. Motion Control Conf.*, 2020, pp. 2458–2462.

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