Real-Time and High-Speed Talkative Power Converter Based on High-Frequency Harmonic Modulation

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***Abstract*—An efficient isolated dc–dc converter requires an information link between the isolated sides for power regulation and performance optimization. Talkative power converter (TPC) technology offers a cost-effective communication solution. However, the signal in existing technologies is susceptible to power noise. Consequently, the existing TPC method requires several switching cycles to transmit a single signal, and the data rate is constrained by noise, making it challenging to meet the demands of advanced communication. In this article, a faster TPC method is proposed, using *M*-ary modulation based on amplitude-shift keying. The nature of the magnetic tank—consisting of an inductor and the transformer—is similar to the traditional resonant circuit, which is used to select signal frequency. It enables the signal to transmit by a frequency far above the switching frequency, thus improving the antinoise ability. Compared to traditional communication methods, this approach eliminates the additional multipliers, enhancing integration and offering valuable insights for digital signal modulation. Thanks to the high signal strength and antinoise ability, information transmission and demodulation can be completed within a single cycle. This method achieves the highest per-cycle transmission rate among state-of-the-art TPC techniques. The proposed method is validated on a 30-kHz 1-kW 200-V dual-active-bridge prototype, achieving a record bit rate per switching cycle to date (three bits/cycle) and a bit rate of 90 kb/s.**

***Index Terms*—Amplitude-shift keying (ASK), high-frequency carrier, high-speed communication, power conversion.**

I. Introduction

With the development of renewable energy and the transition toward low carbon, dc–dc converters have been widely applied in fields, such as renewable systems and electric vehicles [1]. In these scenarios, isolated dc–dc converters are required to provide galvanic isolation and voltage conversion.

A typical isolated dc–dc converter, shown in Fig. 1, consists of a front-side inverter, a load-side rectifier, and an isolation transformer. The dc voltage at the front side is first converted to ac, then transmitted through the transformer to the load-side ac port, and rectified into dc load. In addition, the load-side conditions, such as voltage and current, need to be transmitted in real time to the front side for control guidance. However, due to the galvanic isolation, the reference voltage on each side cannot be directly connected. Consequently, in high-voltage (HV) applications, fiber-optic or wireless communication is required [2], adding extra cost and increasing the risk of communication failure.

Power line communication (PLC) has been proposed as a method to inject signals into the power flow, requiring only one communication channel [3]. In PLC, dedicated electronic circuits are employed to inject signals into the power bus. Consequently, two separate sets of devices are required to handle power

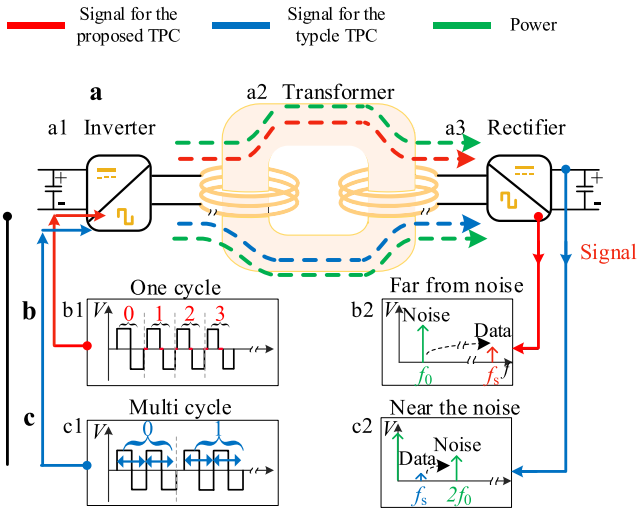

Fig. 1. Schematic of the communication method for the DC–DC system. (a) DC–DC converter, including (a1) an inverter, (a2) a transformer, and (a3) a rectifier. (b) Proposed TPC, where the data are embedded in the switching transient. (c) Traditional TPC technology, where the signal is embedded in the DC voltage of the load. f_0 is the switching frequency, and f_s is the signal-related frequency.

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independently, leading to an increased risk of failure. It is highly desirable that both power and information can be transmitted simultaneously to reduce costs and improve reliability.

In recent years, significant research attention has been directed toward technologies that enable simultaneous power and information transmission, known as a talkative power converter (TPC) [4]. The information-carrying disturbances are introduced for power/signal dual modulation (PSDM). The information injection is achieved by modulating the switching variables. There are three primary digital modulation methods: amplitude-shift keying (ASK), frequency-shift keying (FSK), and phase-shift keying (PSK) [5], [6]. Typically, the frequency or phase of the dc bus voltage ripple is modulated to carry information, enabling FSK or PSK. Since the ripple amplitude directly affects power quality, most TPC studies have focused exclusively on FSK and PSK, with ASK being rarely explored.

The FSK-based method transmits information by introducing additional switching frequencies [4]. Since FSK does not interfere with power transmission in nonresonant converters, it provides simple control and maintains good power quality. In this approach, switching harmonics are filtered and sampled on the dc bus, and the amplitude of the information-related harmonics is sampled for demodulation. It is commonly used in nonisolated low-voltage dc–dc converters [6]. Typically, He et al. [4] and Bertoni et al. [7] used two switching frequencies to represent binary symbols "0" and "1" in nonisolated dc–dc converters. The ripple on the dc bus is extracted using filters and discrete Fourier transformation (DFT) for signal demodulation. In [4], the two frequencies are orthogonal within a bit period and maintained continuous phase, requiring the switching frequencies to be integer multiples of the signal carrier frequency. By using 100 and 83.3 kHz as switching frequencies, a bit rate of 2.78 kb/s was achieved. Similarly, Bertoni et al. [7] utilized orthogonal frequencies of 0.893 and 1.14 MHz with an 80-kHz carrier, achieving the highest reported FSK-based TPC bit rate of 80 kb/s. For isolated converters such as the dual-active-bridge (DAB) converter, TPC schemes have been proposed in [8], [9], and [10], where information is encoded into the switching ripple of the terminal voltage by modulating the switching frequency, thereby altering the ripple frequency. In [11], the coupling between power and signal in FSK-DAB was identified and modeled, revealing the issue of current bias caused by this interaction. However, for isolated ones, the transformer core design sets a lower frequency limit to prevent saturation, while the thermal considerations are based on higher frequency [4]. This results in reduced power density and higher costs. In addition, the switching frequency is proportional to switching losses, resulting in a narrow information bandwidth.

The PSK-based method embeds the signal into the phase of the carrier and has been applied for various types of TPC [12], [13], [14], [19]. As shown in Fig. 1(c), the output ripple is determined by the phase disturbances. However, the frequency of the ripple is close to the power frequency, and the amplitude is much smaller than the power dB amplitude [6], [15], [16]. In addition, a single communication requires multiple cycles. To address these issues, sinusoidal disturbances are introduced as signal carriers in buck converters, with a frequency lower than the power frequency. This approach offers improved noise immunity and reduced interference with power regulation [17]. He et al. [18] proposed a method for wireless power transfer, in which a low-frequency sinusoidal ripple (one-eighth of the switching frequency) is generated by the front-end boost converter and modulated into a high-frequency envelope by a full-bridge inverter. This ensures that both the signal and power frequencies lie within the coil's passband. As the signal carrier frequency is much lower than the switching frequency, the filtering requirements are relaxed, and a high communication rate can be achieved. However, this method relies on a two-stage dc–dc architecture and employs a low-frequency carrier, which requires multiple switching cycles per bit, resulting in limited data rates and increased delay.

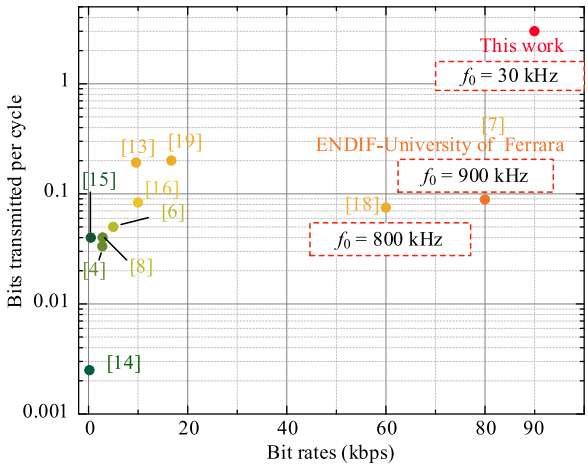


Fig. 2. Parameters of the state-of-the-art TPC. Horizontal coordinate is the bit rate, vertical coordinate is bits transmitted per unit cycle, and f_0 is the switching frequency.

Due to constraints related to noise and power quality, signals are typically embedded in the minor ripple of the dc bus, requiring DFT to extract harmonic content. The sliding window, equaling the period of one bit, generally needs to be at least five times the information frequency [6], [14], [16], [18], [19] resulting in multiple cycles for one communication. Besides, it entails a sampling rate that is an order of magnitude above the switching frequency, increasing the hardware complexity of the implementation [8]. In state-of-the-art TPCs, transmitting one bit requires multiple switching cycles, as shown in Fig. 2. This implies that transmitting the same information requires a significantly higher switching frequency, which not only substantially increases switching losses but also places inherent limits on achievable bit rates. Therefore, the power noise and data rates in TPC for dc–dc converter remain a challenge.

ASK, which transmits information using a fixed-frequency and variable-amplitude signal, is a promising solution to the above issues. In typical dc–dc converters such as the DAB converter, the ac output voltage is a square wave containing wideband high-frequency harmonics. By embedding information signals in the amplitude of these high-frequency harmonics,

robust antinoise high-rate communication can be achieved. Furthermore, the self-resonance characteristics of high-frequency transformers and inductors act as a natural frequency selector, allowing specific high-frequency harmonics to pass through the transformer and be easily detected on the other side. Since only the ac sensing waveform is modulated, the load voltage waveform remains unaffected due to the filtering effect of the large output capacitor. Based on these properties, we propose a novel PSDM, as shown in Fig. 1(b), where the signal is modulated through the waveform of each cycle, with a frequency much higher than the switching noise.

Given this, a novel TPC method is proposed and validated using a DAB converter, a typical isolated converter. The main contributions are listed as follows.

1) The information signals are embedded in the high-frequency harmonics, which are significantly higher than the switching frequency. The power and communication bandwidth are completely separated, resulting in improved anti-interference ability without compromising power quality.
2) The series resonance of the transformer is used to amplify the signal-related harmonics. Unlike traditional TPC methods, which rely on low-intensity injected harmonics, the proposed approach offers higher signal strength and can be adapted to various scenarios.
3) A demodulation method is introduced, where harmonics are sampled and detected at the switching frequency using a built-in analog-to-digital converter (ADC). Compared to the traditional methods that require sampling multiple times the switching frequency to achieve DFT, the proposed approach reduces hardware requirements without sacrificing accuracy.
4) The proposed TPC method is validated by the experiment, achieving the current highest symbol rate of up to three bits per symbol.

The rest of this article is organized as follows. Section II presents the whole process of the proposed TPC method, including the injection, amplification, and demodulation for signal-related harmonics. The experiments are given in Section III. Finally, Section IV concludes this article.

II. Basic Concept of TPC and Harmonic Analysis

A. Concept of the TPC

In dc–dc converters, power transmission includes three steps. First, the reference signal is modulated into the switching frequency by the full-bridge inverter; then, the power transfers through the transformer. Finally, the power is demodulated by the full-bridge rectifier into the waveform required by the load. Similarly, in communication systems, the desired carrier frequency is obtained by a frequency-selective network; then, the baseband signal is modulated on a carrier with another frequency to pass the channel, and finally, it is demodulated into the information [8]. Both processes can be summarized as selecting a frequency of the modulated signal, transmitting it through the channel, and demodulation. As a result, dc–dc converters naturally possess the ability to be talkative.

The spectrum of a square wave varies with the waveform, which can be adjusted flexibly based on modulation strategies through factors, such as voltage changing time and duty cycle. Based on this, the information can be embedded into the amplitude of specific high-frequency harmonics. This process is analogous to using a multiplier to combine a high-frequency carrier and a baseband signal to produce a modulated signal, as shown in Fig. 3(a). The communication channel, consisting of the high-frequency transformer and inductors, inherently functions as a high-order *RLC* network, acting as a frequency-selective oscillator circuit. The modulated signal is amplified and transmitted through the channel to the receiving side, as illustrated in Fig. 3(b). Finally, the signal is demodulated at the receiver, as depicted in Fig. 3(c). The detailed procedure can be divided into three steps.

Step 1: Signal modulation: The ASK method is applied, using a high-frequency sinusoidal carrier with frequency f_s. Thus, the amplitude of the f_s harmonic in the output voltage u_{LV} varies with the information signal, which can be adjusted by modifying the inner phase-shift ratio of the LV side D_3 with the detailed explanation shown in Section II-B. For instance, when transmitting a symbol sequence such as "0"–"3," as shown in Fig. 3(a1), the ASK is used to embed the information into a high-frequency carrier. The resulting signal is a sinusoidal wave at frequency f_s with varying amplitude, as illustrated in Fig. 3(a2). The f_s harmonic is embedded in u_{LV}, and its amplitude is modulated by adjusting the waveform through D_3, as shown in Fig. 3(a3). However, the harmonic amplitude is relatively small and requires amplification for extraction, as shown in Fig. 3(a4).

Step 2: Signal amplification: The series resonance in the magnetic tank, which consists of a transformer and an inductor, is used to amplify the f_s harmonic. It can be equivalated to a circuit, as shown in Fig. 3(b1) [20]. The series resonance is triggered by the interaction of capacitance and leakage inductance. This results in a high-gain band around the resonance frequency shown in Fig. 3(b2), allowing the information signal to be naturally amplified when f_s is selected as the resonance frequency, distinguishing it from nearby noise.

Step 3: Signal demodulation: In the final step, the amplified harmonic generates a high-frequency oscillation with frequency f_s on the receiver side, as shown in Fig. 3(c3) and (c4). The signal is demodulated from the oscillation amplitude. An active filter extracts the signal from the transformer port and converts it to a dc pulse that represents the information. The digital signal processor (DSP) samples the square-wave amplitude each cycle to demodulate the signal.

B. Basic Principle of Signal Modulation

The amplitude of the signal-related harmonic can be adjusted by modifying the waveform of the ac output voltage. A typical waveform of the full-bridge output voltage is shown in Fig. 4, with its fast Fourier transform (FFT) as follows:

$$u_h(f_h) = a_h \sin(\omega_h t) + b_h \cos(\omega_h t)$$

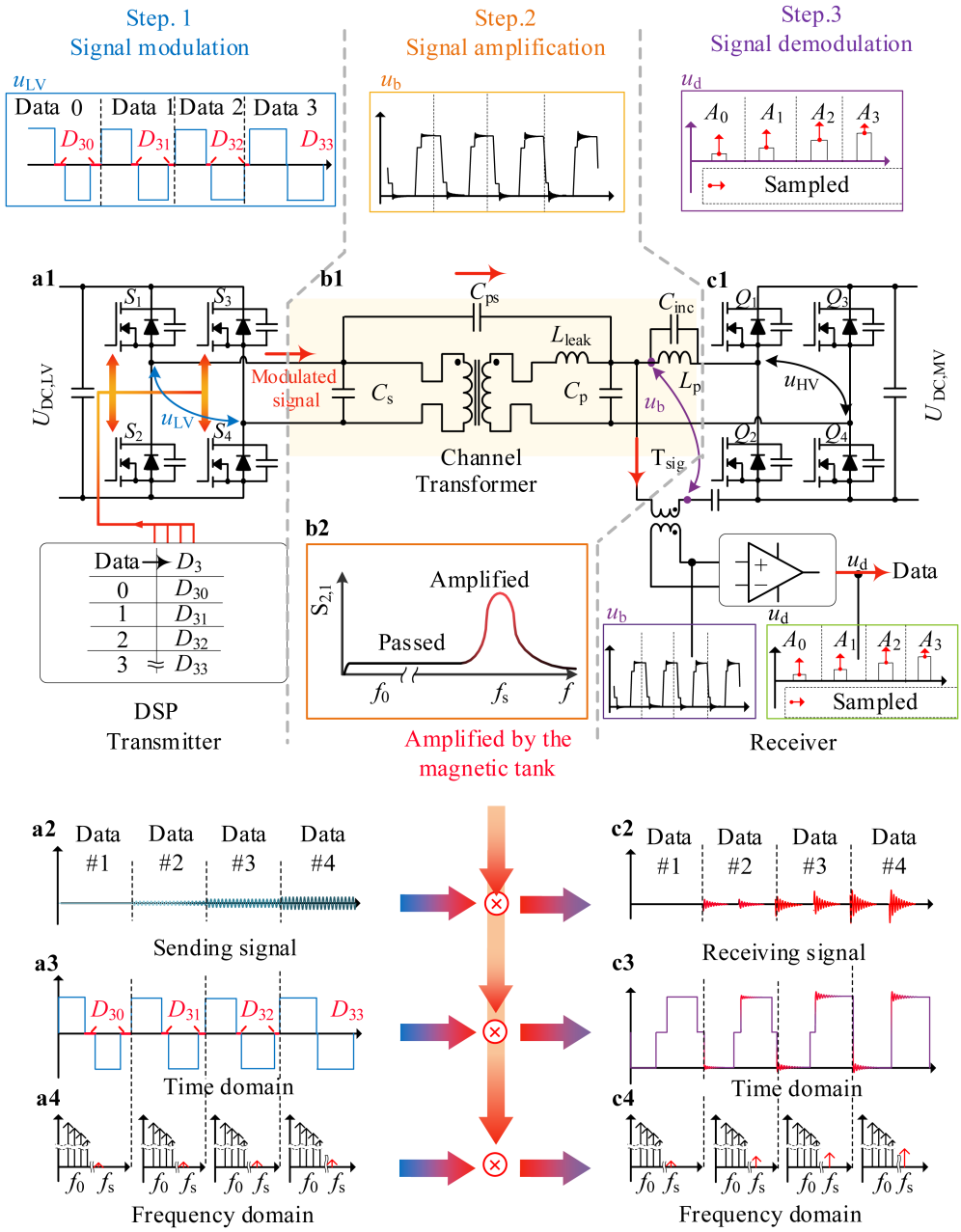


Fig. 3. Schematic of the proposed TPC method. The TPC method consists of three steps: (a1)–(a4) signal is injected by a full-bridge converter; (b1) and (b2) the signal is amplified by the magnetic tank that consists of a transformer and an inductor; (c1)–(c4) the signal is demodulated by the conditioning circuit. $C_{\rm ps}$ is the interwinding capacitance, C_p is the equivalent capacitance of the HV side, C_s is the equivalent capacitance of the LV side, $L_{\rm leak}$ is the leakage inductance of the transformer, and $C_{\rm inc}$ is the equivalent parallel capacitance of the external inductor L_p.

$$a_h = \frac{4U_{\rm DC,LV}}{\pi h^2\omega_0}\left\{\begin{array}{l}\frac{1}{t_{r1}}\sin\left(\frac{h\omega_0}{2}t_{r1}\right)\cos\left[\frac{h\omega_0}{2}\left(t_{\rm ph}+t_{r1}\right)\right]\\ +\frac{1}{t_{r2}}\sin\left(\frac{h\omega_0}{2}t_{r2}\right)\cos\left[\frac{h\omega_0}{2}\left(t_{\rm ph}+t_{r2}\right)\right]\end{array}\right\}$$

$$b_h = \frac{4U_{\rm DC,LV}}{\pi h^2\omega_0}\left\{\begin{array}{l}-\frac{1}{t_{r1}}\sin\left(\frac{h\omega_0}{2}t_{r1}\right)\sin\left[\frac{h\omega_0}{2}\left(t_{\rm ph}+t_{r1}\right)\right]\\ +\frac{1}{t_{r2}}\sin\left(\frac{h\omega_0}{2}t_{r2}\right)\sin\left[\frac{h\omega_0}{2}\left(t_{\rm ph}+t_{r2}\right)\right]\end{array}\right\} \quad (1)$$

where $u_h(f_h)$ is the amplitude of the harmonics at frequency f_h, and $U_{\rm DC,LV}$ is the dc voltage of the LV side. T_{r1} and t_{r2} are the voltage rise time after S_2 and S_3 turned OFF, and $t_{\rm ph}$ is the zero-voltage time. The amplitude of specific harmonics can be adjusted by changing either t_{rj} or $t_{\rm ph}+t_{rj}$ ($j=1$ or 2). However, t_{rj} is determined by the inductor current or load conditions, which are difficult to control. Thus, $t_{\rm ph}+t_{rj}$ can be used to modify the resulting voltage spectrum and transmit signals, as it is only related to the inner phase-shift ratio D_3.

According to (1), $t_{\rm ph}+t_{rj}$ is included in a trigonometric function, so the amplitude of signal-related harmonics $u_h(f_s)$ varies with $t_{\rm ph}+t_{rj}$ with the period $T_s=1/f_s$. Therefore, to achieve a full variation of $u_h(f_s)$ from its minimum to maximum, $t_{\rm ph}+t_{rj}$ only needs to change within half a period T_s. Since f_s

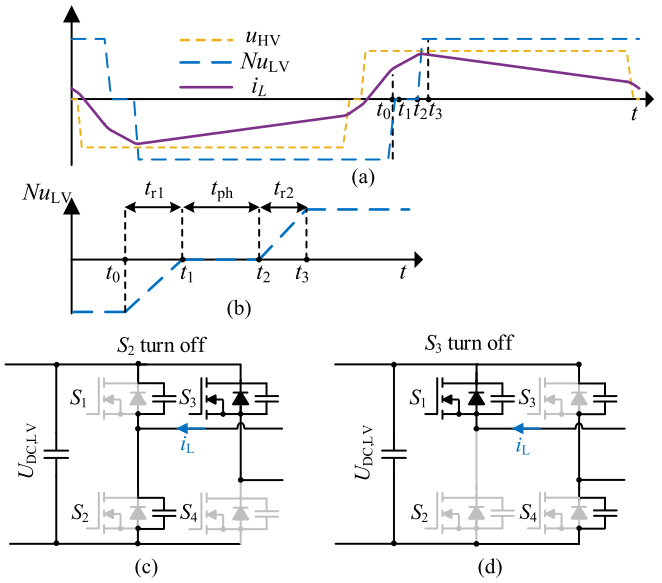


Fig. 4. Schematic waveform of the DAB converter. (a) Typical waveforms of the DAB converter; N is the turns ratio of the transformation. (b) Schematic waveform of NU_s during the switching transient. The equivalent circuits during switching transients with the time interval (c) $[t_0, t_1]$ and (d) $[t_2, t_3]$; $U_{DC,LV}$ is the DC voltage of the LV side.

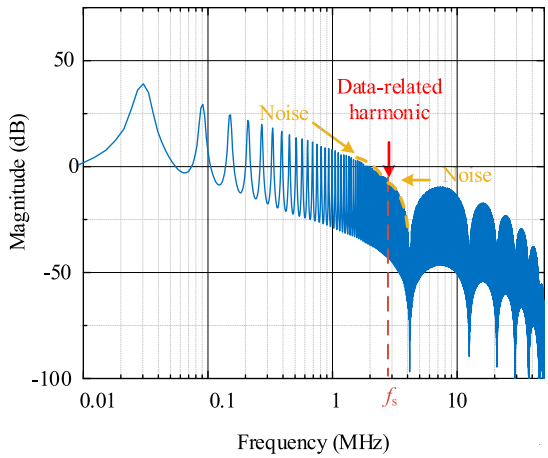


Fig. 5. FFT spectrum of square waves with $t_{rp} = 120$ ns and $U_{DC,LV} = 100$ V.

is much higher than the switching frequency f_0, T_s is relatively small, meaning that the interval between diagonal switches is very short. Then, the inductor currents that determine t_{r1} and t_{r2} are almost the same, and $t_{r1} = t_{r2} = t_r$. Therefore, $t_{rp} = t_r + t_{ph} = D_3/f_0$ can be used to adjust the magnitude of harmonics around f_s.

The spectrum of the output voltage is shown in Fig. 5. The amplitude of harmonics decreases with frequency. Since f_s is much higher than the switching frequency f_0, its amplitude is relatively low and surrounded by broadband noise. Thus, the signal-to-noise ratio (SNR) is too low for reliable signal transmission. To improve the SNR, the signal-related harmonics need to be enhanced. It can be achieved by series resonance in the magnetic tank.

TABLE I
KEY COMPONENTS AND SPECIFICATIONS OF THE DAB CONVERTER

Items	Parameters
Rated HV voltage	200 V
Rated LV voltage	100 V
Rated Power	1 kW
Phase-shift inductor L_{ps}	50 μH
Transformer specification	Turns ratio $N = 2{:}1$ Primary/Secondary: 28/14 turns Litz wire: 0.1 mm×1000 strands Core: nanocrystal, PC0070, A_e=7.8 cm^2, L_e=32.99 cm
Switching frequency	30 kHz
Control board	DSP28335

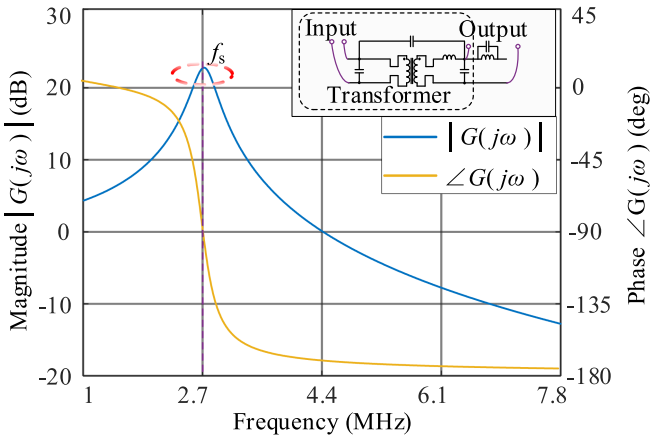


Fig. 6. Magnitude and phase response of the DAB magnetic tank. The signal is injected at the LV port, and the HV port is measured. The parameters of the transformer and inductors are shown in Table I.

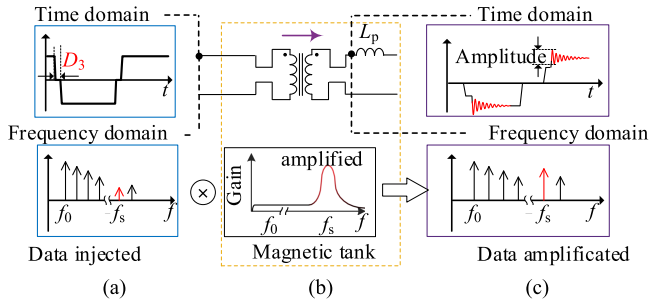


Fig. 7. (a)–(c) Voltage waveforms before and after the information signals are amplified. u_s is the LV-side AC output voltage, and u_{Mp} is the HV-side port voltage.

The amplification effect is analyzed by the magnitude and phase response curve of a DAB sample shown in Table I. Take the upload communication as an example, i.e., the information is transmitted from the LV side to the HV side. The signal is injected at the LV side, and the HV side is measured. As shown in Fig. 6, a series resonance is formed, and the corresponding harmonics are amplified and passed through the transformer. Then, the amplified harmonics are superimposed on the square wave at the HV side port 12 with f_s, as shown in Fig. 7. Therefore,

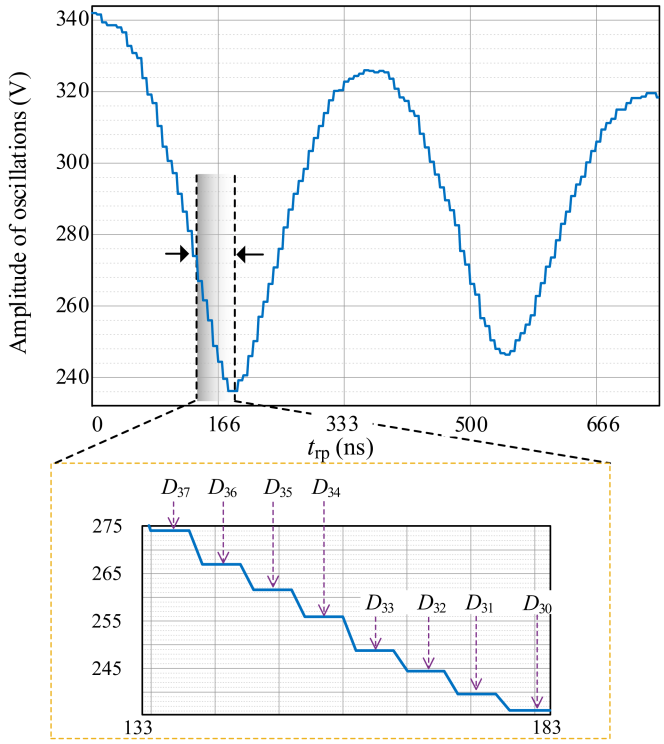


Fig. 8. Relationship between the inner phase-shift ratio and the amplitude of the voltage oscillations in the HV port.

$u_h(f_h)$ on the LV side can be used for signal transmission, which can be adjusted according to (1).

The relationship between t_{rp} and the port voltage oscillation amplitude is shown in Fig. 8. T_{rp} is varied from 0 to 750 ns. Using the DSP28335 with a pulsewidth modulation (PWM) clock frequency of 150 MHz, the adjustment resolution is 6.67 ns. T_s is 377 ns, so the port voltage oscillation undergoes about two complete cycles. It can be observed that the oscillations initially decrease with increasing t_{rp}. This is because the required t_{rp} is relatively small, less than 166 ns, resulting in approximately equal turnOFF currents for S_1 and S_4 (or S_2 and S_3). Assuming $tr_1 = tr_2 = t_r$, the a_h term in (1) dominates over the b_h term. As $(h\omega_0/2) \times t_{rp}$ varies from 0 to $\pi/2$ [i.e., t_{rp} increases from 0 to $1/(2f_s)$], the part $\cos((h\omega_0/2)\cdot t_{rp})$ lies in a decreasing interval. Consequently, u_h decreases as t_{rp} increases.

However, the signal-related oscillation should remain low in amplitude to avoid insulation issues, and the adjustment range of t_{rp} should be minimized to prevent interference with power. As shown in Fig. 8, a part of the curve is selected to transmit the signal, referred to as the signal-related interval.

The oscillation range V_{sig} is limited to 20% of the rated voltage. It is sufficient for demodulation, as the sampled voltage range is often much smaller than the load voltage. Next, the oscillation amplitude within the signal-related interval is proportionally divided into n subintervals. Each subinterval corresponds uniquely to a specific D_3 and a signal value. Thus, the oscillation amplitude of each cycle is used to transmit one symbol, and each symbol can represent n signal values. The symbol rate—the number of bits transmitted per symbol—is $\log2(n)$. For example, to achieve a symbol rate of three bits per symbol, the oscillation amplitude is divided into 2^3 possible levels, each corresponding to specific values D_{30}–D_{37}.

The oscillation amplitude has a wide adjustable range, allowing for a high symbol rate. However, a higher symbol rate means that the subintervals become narrower, which increases the susceptibility to noise and may lead to a higher error rate. When a higher number of n intervals is selected, the bit rate increases, but the decision interval for each symbol narrows and the signal energy decreases, leading to a lower SNR. Moreover, this also requires larger voltage oscillation amplitudes. Therefore, the choice of n and bit rate should be carefully balanced against the measured SNR and insulation requirements.

The signals can, therefore, be embedded in D_3 and demodulated by the amplitude of the voltage oscillations. Since the oscillation frequency is also much higher than the switching frequency, $D_3 \times T_0 = t_{rh}$ is relatively small—shorter than 183 ns—compared to the switching period, which is 33.3 μs. As a result, it has minimal influence on the output voltage and is expected to have high SNRs.

C. Basic Principle of Signal Demodulation

The conditioning circuit consists of a bandpass filter and a peak-hold circuit, as shown in Fig. 9(a) and (b). To avoid affecting the power waveform, an active filter is used. It has a high input impedance to reduce the influence on the power. A second-order multifeedback bandpass filter is used to extract the high-frequency components. The passband is a 300-kHz range centered around the resonance frequency f_s, as shown in Fig. 9(c). It connects to one end of the HV port through an isolated transformer T_{sig}. Due to the high input impedance of the filter, T_{sig} carries minimal current, requiring minimal size and cost. The input is a square wave with HFVOs, as shown in u_b. The output of the active filter is a high-frequency ac voltage, as shown in u_c.

This high-frequency signal is difficult to sample. Since only the amplitude of the oscillation carries the signals, a peak-hold circuit is required. It converts the oscillation amplitude of each cycle into a dc pulse. First, diode D retains the positive component of u_c. Then, it charges capacitor C_q until its voltage u_d plus the voltage of the diode equals the oscillation amplitude. The decay of u_d is minimal, as no discharge resistance is set. After each sampling, C_q is discharged through Q_r to prepare for the next sample. Finally, u_d is sampled by the DSP's ADC and decoded into signals based on a predefined table. Since the signals are transmitted once per switching cycle, only one sample is needed per cycle. Compared to traditional methods using DFT, the proposed approach improves information transmission efficiency and reduces the reliance on hardware such as ADC.

D. Advantages, Limitations, and Prospects for HV Applications

The proposed method offers advantages as follows.

1) By utilizing high-frequency harmonics of the series resonance for information transmission, it effectively avoids noise near the switching frequency.

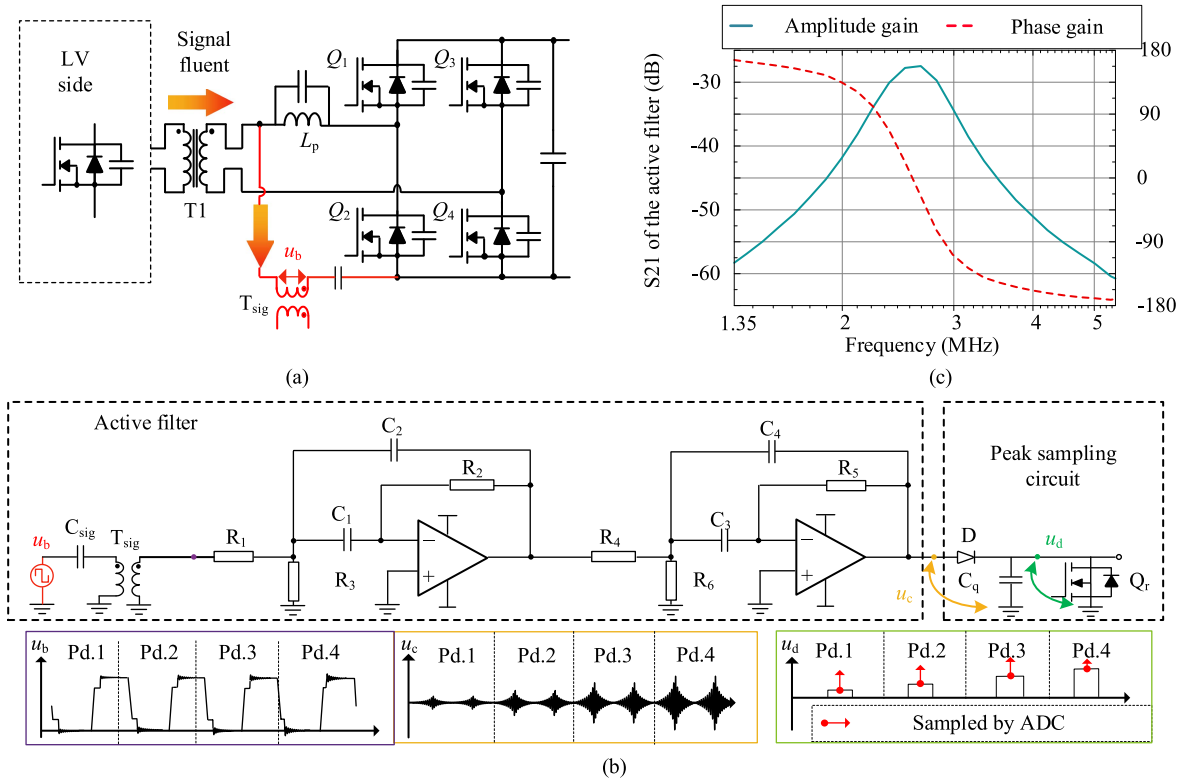


Fig. 9. Schematic of the information demodulation. (a) Signal is obtained by the port of the transformer via a signal transformer T_{sig}. (b) Conditioning circuit consisting of an active rectifier and a peak sampling circuit. (c) Measured bode plot of the active rectifier.

2) Since the signal is modulated onto the ac port waveform, the load capacitance attenuates the corresponding harmonics. As verified in Section III-A, the impact on load voltage ripple is negligible.
3) Information can be extracted once per switching cycle, in contrast to conventional DFT-based approaches that require multiple cycles per bit, improving communication efficiency and reducing controller complexity.

However, the proposed method also has certain limitations as follows.

1) The parasitic capacitance that affects the resonance frequency may drift over time due to aging, requiring calibration. The mapping between the modulated information and the internal phase-shift angle (D_3) can be adaptively adjusted according to the measured output voltage of the conditioning circuit.
2) The conditioning circuit requires an additional I/O pin to control a small MOSFET for resetting the signal capacitor voltage in each switching cycle.
3) The amplitude of high-frequency harmonics of the transformer port is constrained by insulation requirements and should be kept at a low level.

It should be noted that for the reproducibility of TPC technology, the parasitic capacitance of the transformer affects the signal frequency. To obtain an accurate model, parasitic capacitance can refer to [21] and [22], which provide a detailed analysis of high-frequency harmonic amplification and parasitic networks.

For HV applications, the higher *dv/dt* of switching devices may introduce additional electromagnetic interference (EMI) challenges. To mitigate this, common-mode inductors can be added to the input of the conditioning circuit. Besides, the sampling of u_d can be shifted away from switching transient to avoid EMI noise.

From an insulation perspective, a conventional modulation strategy typically does not constrain voltage oscillations during modulation, which can result in more severe oscillations, as shown in Fig. 8. In contrast, the proposed method limits the voltage oscillation at the transformer port to a relatively low range, thus alleviating insulation stress. Nevertheless, the peak transformer port voltage may still exceed the nominal dc voltage due to communication requirements. Therefore, insulation design must consider the actual peak port voltage.

Regarding the magnetic core, the integral of the port voltage is proportional to the magnetic flux density. Since the voltage oscillation decays rapidly within each half-switching cycle, its contribution to the flux density can be considered negligible. As a result, standard core design procedures remain applicable.

III. Modulation Scheme and Experiments

A. TPC Experimental Validation

A 1-kW/30-kHz/200-V DAB prototype is prepared to verify the proposed TPC method, as shown in Fig. 10. The specifications of the prototype are shown in Table I. The built-in

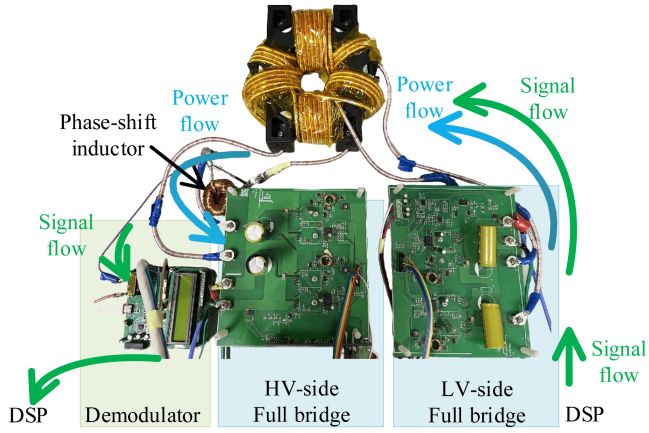


Fig. 10. Graph of the DAB prototype. The demodulator includes a conditioning circuit to demodulate the signal and an LCD screen to verify the method.

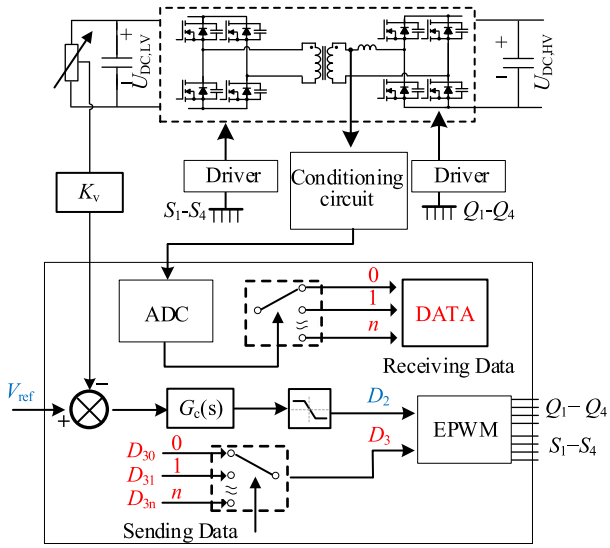


Fig. 11. Control Schematic of proposed TPC method. The power- and signal-related quantities are highlighted as blue and red, respectively.

ADC of DSP28335 is used and triggered once per switching cycle by the enhanced pulse width modulation (EPWM). The sampling frequency must be consistent with the transmitter PWM frequency, and the sampling phase must be aligned with the power phase information. When a single DSP is used for both transmitting/receiving information and power control, the phase-shift information can be directly accessed. If an independent DSP is employed for demodulation, two alternatives are available: 1) increasing the sampling frequency to identify the signal, and 2) using u_d triggered synchronization. These two methods are described in detail in the following sections.

The power and signal modulation is illustrated in Fig. 11. The DAB converter has three control variables: HV-side inner phase-shift ratio D_1, LV-side inner phase-shift ratio D_3, and phase-shift ratio D_2. This modulation method is known as triple phase shift [23]. Transmitting signals from the LV side relies on D_3. Similarly, injecting signals from the HV side depends on D_1. Therefore, D_2 can be used to adjust the power and achieve PSDM. First, D_3 is generated based on the predefined signal. The resulting voltage fluctuation is compensated by D_2. Since no signal transmission is required from the HV side, D_1 is free and defaults to 0.

The proposed TPC method is validated by transmitting two sets of signals, as shown in Figs. 12 and 13. CH1 and CH2 are the full-bridge output voltages of HV and LV sides u_{HV} and u_{LV}, respectively; CH3 is the port-to-ground voltage of HV side u_b; CH4 is the voltage after the active filter u_c that is the high-frequency components of u_b; CH5 is the voltage after peak sampling circuit u_d, which is sampled by the built-in ADC; and CH6 is the output voltage of a digital-to-analog converter (DAC) for a demodulated signal.

First, it is verified by repeatedly sending the signal sequence "0, 1, 2, 3, 4, 5, 6, 7," as shown in Fig. 12. Each signal represents three bits, e.g., "7" represents "111." The inner phase-shift ratio within the LV side is circularly switched from D_{30} to D_{37}. There is a delay of about 1 μs between u_b and the output of the filter u_c due to the group delay of the active filter. It is much shorter than a single switching cycle and, thus, can be neglected. There is minimal delay between the moment information is injected via D_3 on the transmitter side and when it is sampled by the ADC, enabling reliable real-time communication. The demodulated signal is outputted by the DAC, but a delay between the DAC and the demodulated signal is introduced by the 1-MHz serial peripheral interface communication rate and program processing time. Nevertheless, this delay does not affect the performance of the proposed method.

Therefore, a three-bit symbol per cycle, a bit rate of 90 kb/s with low communication delay, is achieved in the proposed TPC. Compared to other methods shown in Fig. 2, this is the first time to achieve single-cycle communication, enabling real-time data transfer and extending the boundaries of communication speed. With a modest increase in a bit rate, the switching frequency can be reduced by orders, as shown in Fig. 2. It is important to note that the three bits/symbol is selected to ease the insulation stress on the transformer. In scenarios with higher insulation margins, additional voltage oscillation segments can be used to achieve an even higher bit rate.

The proposed method is also used to drive an LCD for displaying the string "HELLO WORLD," as shown in Fig. 13. The data frame structure is defined as: one start bit, 33 data bits, one end bit, and one gap. Each American Standard Code for Information Interchange (ASCII) is represented by eight bits, and each cycle can transmit three bits. Therefore, each ASCII character requires three cycles to transmit. The string "HELLO WORLD" includes 11 characters, which takes 33 cycles or data bits. The proposed method can also be applied to other distributed energy systems, such as battery and photovoltaic systems.

The load voltages and their corresponding oscilloscope spectra are shown in Fig. 14. Fig. 14(a) illustrates the case without information transmission, while Fig. 14(b) corresponds to repeated transmission of symbols 0–7. The ripple of $u_{\mathrm{DC,LV}}$ in Fig. 14(b) is approximately 4.64% of the dc voltage, which is only 0.18% higher than that in the no-communication case, showing no significant difference in shape or waveform.

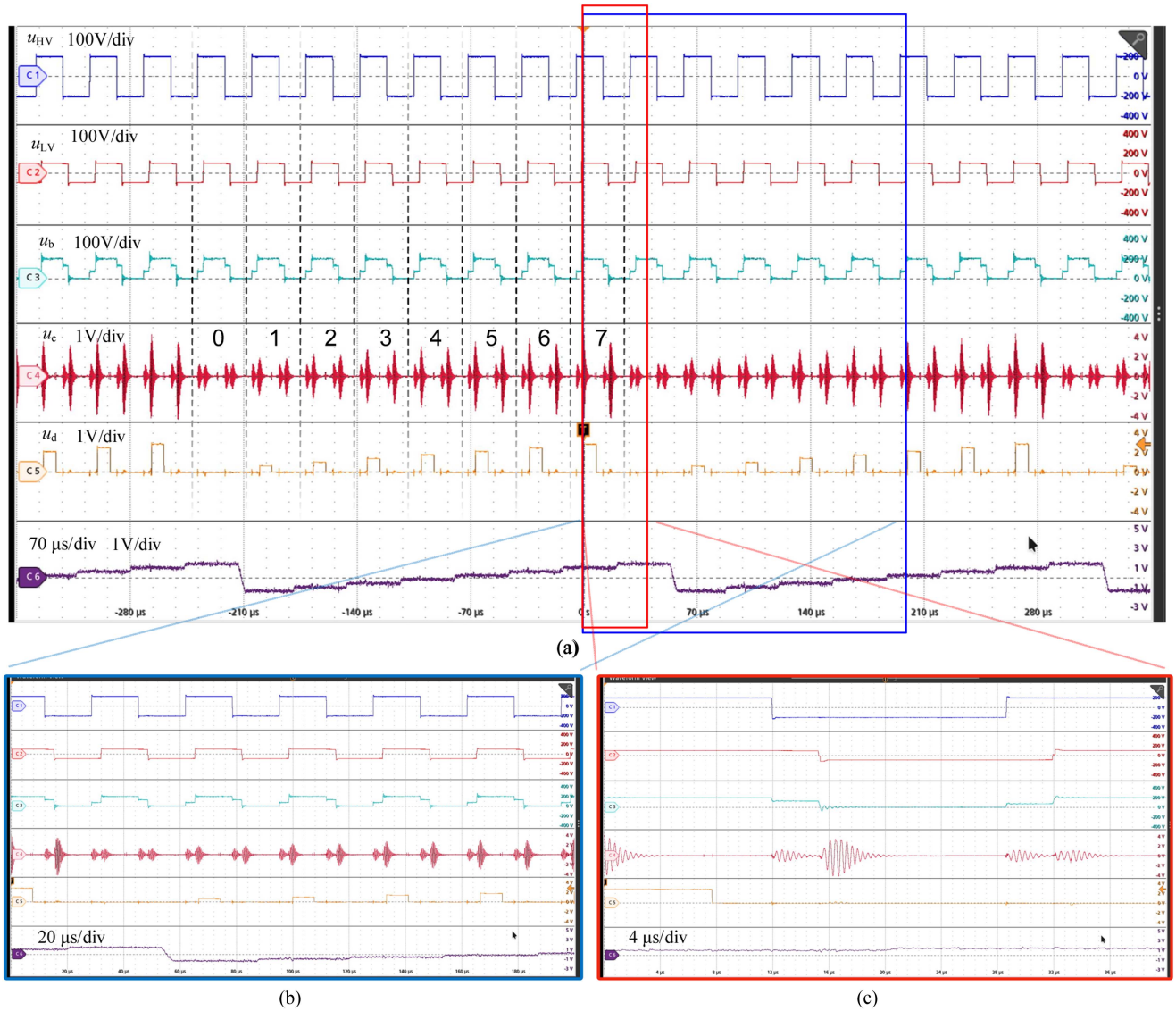


Fig. 12. Waveform of the proposed TPC. (a) HV output voltage u_{HV} CH1, the LV output voltage u_{LV} CH2, the HV port voltage u_b CH3, the output voltage of the rectifier u_c CH4, the sampling voltage u_d CH5, and the DAC output voltage CH6 for transmitting bits "0"−"7." (b) and (c) Zoom-in waveform for transmitting bits "0"−"7."

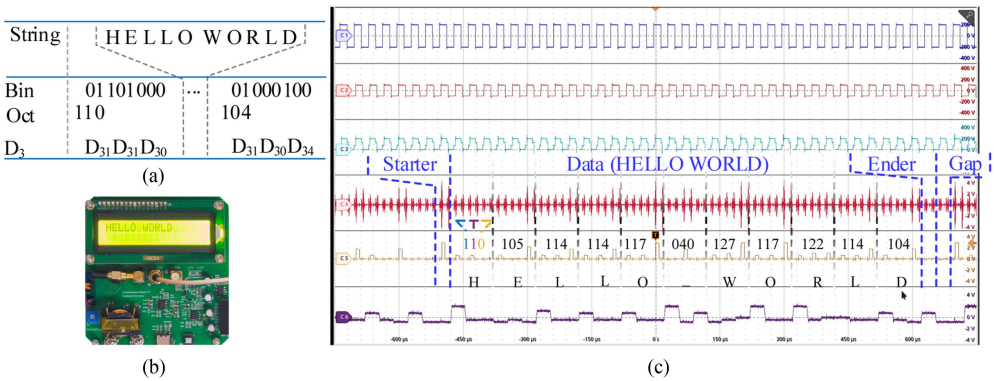
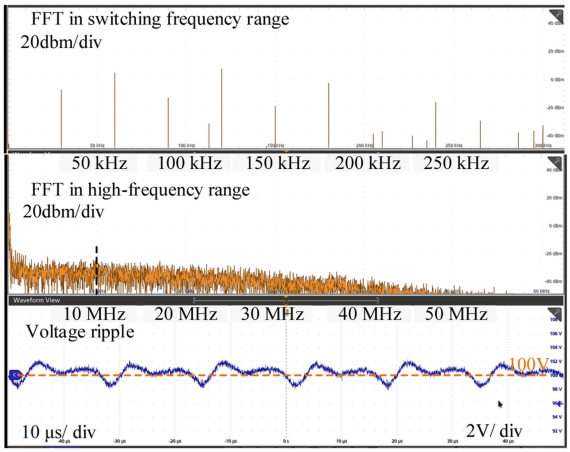
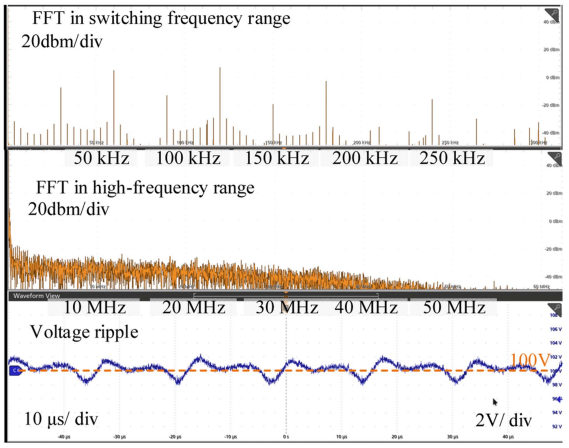


Fig. 13. Graph of the display of the string on LCD1602. (a) Relationship between strings and binary, octal, and phase-shift ratio. (b) Display of the string. (c) HV output voltage CH1, the LV output voltage CH2, the HV port voltage of the transformer CH3, the output voltage of the rectifier CH4, the sampling voltage u_d CH5, and the DAC output voltage CH6 for transmitting string "HELLO WORLD." The data frame structure is defined as: one start bit, 33 data bits, one end bit, and one gap.



(a)



(b)

Fig. 14. Load voltage waveforms and their corresponding spectra. (a) Without communication. (b) With repeated transmission of symbols "0"–"7."

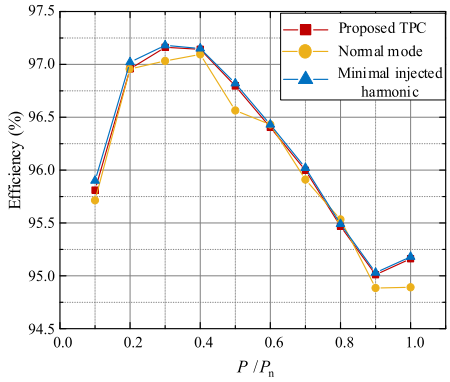


Fig. 15. Efficiency curves with three modes. The efficiency of the TPC method is measured for transmitting string "0"–"7." The normal mode is measured without information transmitted, D_3 is set as 0, and a single DSP controls both sides. The efficiency of the minimal injected harmonic is measured with minimal oscillation amplitude. Optical fiber communication is used between DSPs on both sides; the loss of fiber hardware is not considered.

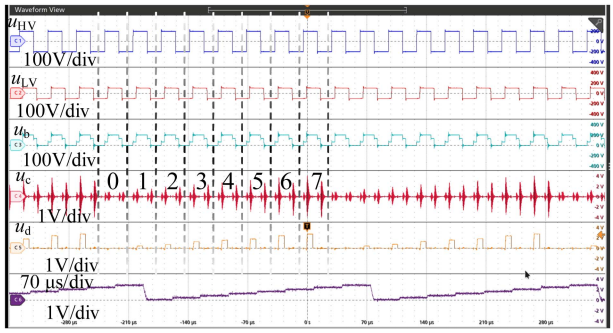


Fig. 16. Waveforms for using independent DSP to demodulate information, which include: CH1, the HV output voltage u_{HV}; CH2, the LV u_{LV}; CH3, the HV port voltage u_b; CH4, the output voltage of the rectifier u_c; CH5, the sampling voltage u_d; and CH6, the DAC output voltage.

The spectral analysis reveals that information transmission introduces additional sideband harmonics near the switching frequency and its lower order harmonics. However, their amplitudes remain small—more than 20 dB lower than those of the dominant switching harmonics. In the high-frequency region, particularly around the signal carrier frequency f_s, there is nearly no difference, indicating that high-frequency harmonics have little direct impact on the load voltage.

Fig. 15 shows the efficiency curves for transmitting symbols "0"–"7," compared with the normal operation mode. The efficiencies in both cases are nearly identical. At some points, a slight improvement in efficiency can be observed. This is attributed to the additional loss caused by voltage oscillations at the inductor and transformer ports, which is observed by the damping effect of the oscillations. Conventional methods do not regulate these oscillations via modulation of D_3. During voltage-matching operation, D_3 is typically set to zero, as shown in Fig. 8, which corresponds to a high-oscillation region. In contrast, the proposed modulation confines the voltage oscillation to a lower range during information transmission, thereby slightly improving efficiency by reducing oscillatory losses.

However, compared to the case with minimal injected harmonic—where D_3 is set for the minimum oscillation shown in Fig. 8 (i.e., equally transmitting symbol "0")—the proposed modulation results in a slight decrease in efficiency.

The proposed method is also compatible with alternative demodulation schemes. For example, to avoid reliance on power information, the signal can be identified by increasing the sampling frequency. The ADC sampling frequency of the DSP is set to 1 MHz, while the effective level of u_d lasts for 6 μs, yielding approximately six samples per cycle. The program determines the signal period by detecting the minimum interval between two rising edges. When three consecutive samples exceed the decision threshold after a rising edge, the level is regarded as valid, and the median value is taken as the signal amplitude. If no valid level is detected within 1.1 times the signal period after the previous cycle, the signal is determined as zero. The experimental waveforms are shown in Fig. 16. As it requires period detection, the signal delay is longer than that of the single-sample-per-cycle method.

B. *Isolated Communication Based on the TPC*

For isolated converters such as DAB, although both sides can be controlled by a single DSP, a common signal ground is required. Thus, the power–signal isolation should be designed according to the higher voltage side, increasing the isolation

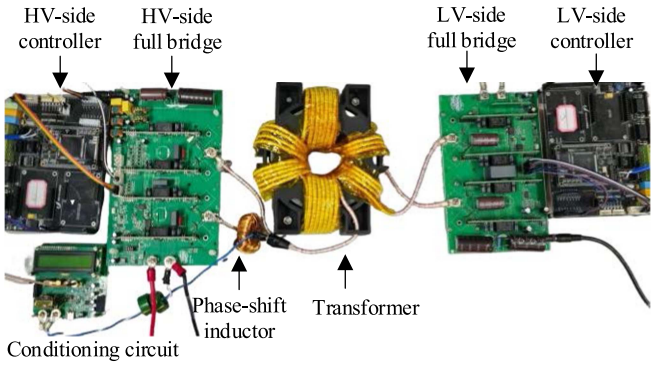


Fig. 17. TPC hardware setup for isolated communication.

requrements of the hardware. Moreover, it introduces additional low-resistance common-mode paths. Therefore, isolated communication is a preferable choice for isolated converters.

Optical fiber is a classic isolated communication solution, but it requires additional fiber cables and hardware, leading to higher costs. It also suffers from environmental fluctuations, such as temperature and atmospheric pressure changes [24], [25]. Hence, implementing isolated communication via the TPC offers a novel and cost-effective alternative.

This section employs a new test platform to validate the practical value of the TPC. The power remains a parameter with 1 kW/200 V/100 V, but the transmitting and receiving sides are each controlled by separate DSPs, as shown in Fig. 17. The two DSPs achieve synchronization and communication using the proposed TPC method.

Isolated communication is validated through a dynamic load step experiment, with waveforms shown in Fig. 18. Fig. 18(b) and (c) shows waveform details at different time intervals during one load step. The complete dynamic process is presented in the top row, while the detailed waveforms at different time intervals are shown in the lower sections of Fig. 18(b) and (c). The transmitter sends load voltage information to the receiver. The transmitter uses the switching signal of S_1 as the synchronization reference, ensuring a nearly constant interval between voltage oscillation events triggered by u_b. The receiver synchronizes using the rising edge of the demodulated u_d oscillation, which resets the PWM counter.

The voltage information sequence follows a defined protocol: the transmitter encodes the load voltage into an octal information sequence. The start bits are $A_0 = 0$ and $A_1 = 7$, followed by three octal digits A_2, A_3, and A_4 that represent the load voltage encoding, as expressed by the following equation:

$$\text{volt} = \frac{A_2 \times 8^2 + A_3 \times 8^1 + A_4 \times 8^0}{512} \cdot 200. \qquad (2)$$

Thus, the load voltage resolution is 0.39 V. The end bit is $A_5 = 0$. The transmitted voltage information is used for closed-loop voltage control.

Since the information receiver samples only once per cycle, it is necessary to ensure both the sampling frequency and phase, so that the sampling instant falls within the valid level of u_d. First, the switching frequency at the signal transmitter side is fixed.

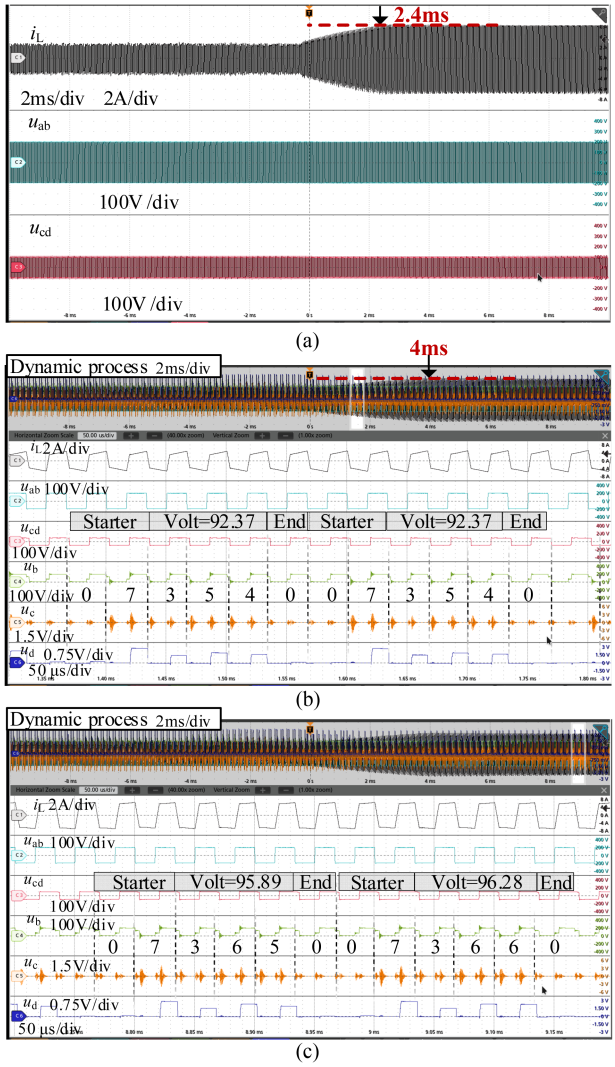


Fig. 18. Dynamic response during load step change. (a) Without communication. (b) and (c) Different time interval of communication.

Therefore, by configuring the signal receiver to use a PWM interrupt with the same switching frequency and performing sampling at the start of each interrupt, the sampling frequency can be guaranteed. The phase information is obtained through a synchronization process. The signal u_d is connected to the receiving DSP through a Schmitt trigger. Each time a rising edge of the information signal exceeds the Schmitt threshold, an synchronization signal is received at SYNCIN pin of the signal–receiver DSP, which forces the PWM counter to zero for synchronization. It occurs at most once every six cycles, since the starter contains synchronization information. Furthermore, each time the PWM counter is forced to zero, an interrupt is triggered, which coincides with the rising edge of u_d, and a typical delay of 2 μs is applied to ensure that sampling time occurs after the rising edge.

The isolated TPC requires six switching cycles to transmit one voltage information symbol; the control bandwidth decreases. For example, the rise time is extended from 2.4 to 4 ms. Nevertheless, the voltage during the dynamic transition can

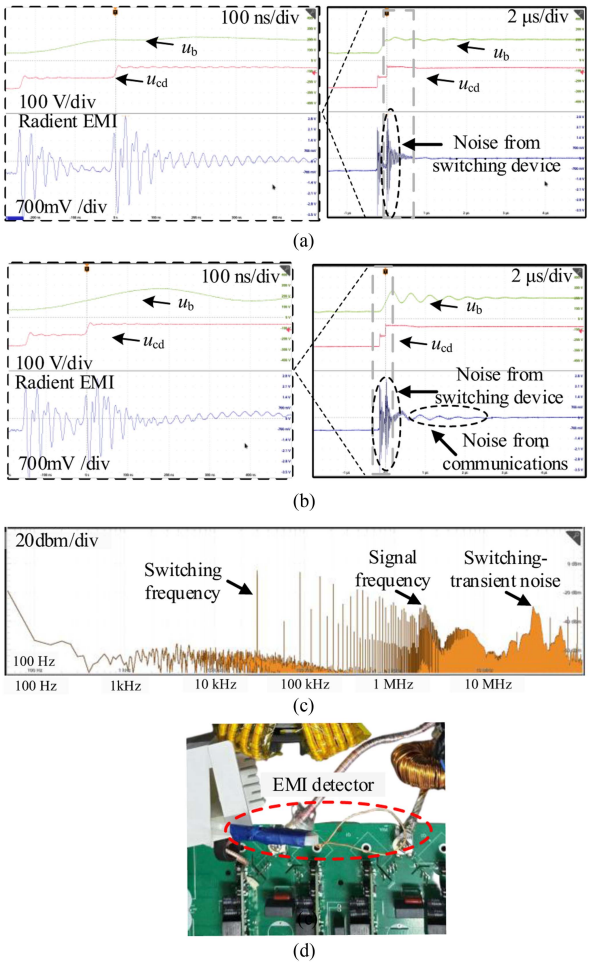


Fig. 19. Radiated EMI waveforms and spectrum (10× amplified). (a) Case with minimum signal amplitude. (b) Case with the maximum signal amplitude, and the corresponding noise spectrum is shown in (c). The EMI detector is shown in (d).

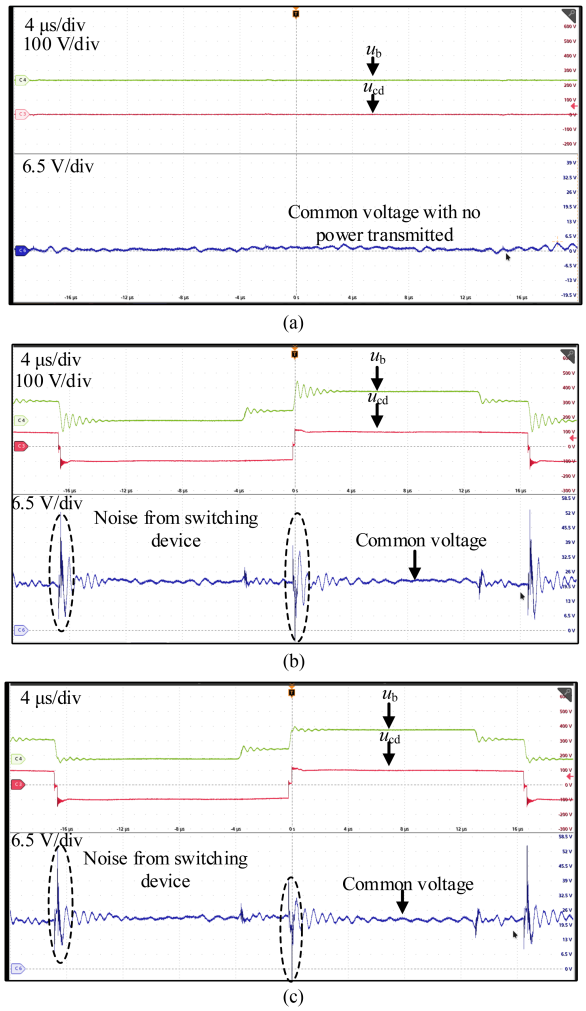


Fig. 20. Common-mode voltage between the power grounds. (a) Common-mode voltage present without power transmission, (b) waveform at maximum signal amplitude, and (c) waveform at minimum signal amplitude.

still be transmitted via TPC and successfully reaches the new steady state. Two stages of the dynamic process are captured in Fig. 18(b) and (c), where the transmitted information accurately reflects the load voltage variations during the transition.

C. EMI Noise

Since the signal frequency of the proposed TPC is significantly higher than that of conventional methods to verify whether transformer voltage oscillations introduce additional EMI issues, measurements were conducted on electromagnetic emissions near the transformer, common-mode voltages between both power sides, and the PWM signals in the HV side.

The radiated EMI is measured using a self-made single-turn coil placed near the transformer port, as shown in Fig. 19(c). The measured voltage waveform is shown in Fig. 19(a) and (b). Although a quantitative magnitude is not accurate, the relative noise levels can be obtained. It can be seen that the dominant EMI source remains the power switching noise at the switching frequency from Fig. 19(c). The proposed modulation amplifies the noise near the resonance frequency; however, its magnitude is still significantly lower than that of the switching power noise.

The common-mode noise on the power grounds of both isolated sides is shown in Fig. 20. Fig. 20(a) shows the noise present when no power is transmitted, i.e., when the devices are inactive. Fig. 20(b) and (c) shows the waveforms without and with information transmission, respectively, exhibiting negligible differences.

The PWM signal on the receiver side is measured, as shown in Fig. 21. It can be observed that common-mode interference occurs at the switching instants, with frequencies much higher than the signal frequency. Therefore, the signal harmonic does not interfere with the PWM signal since its frequencies are significantly lower than the switching-induced noise—which can reach as short as 20 ns, with harmonic bands in the tens of megahertz range.

In summary, the primary sources of EMI are power and switching actions. The noise from the signal harmonic is relatively little.

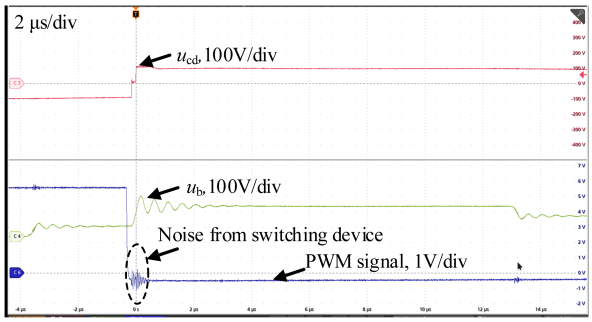


Fig. 21. PWM signal at the receiver side and the noise superimposed on it.

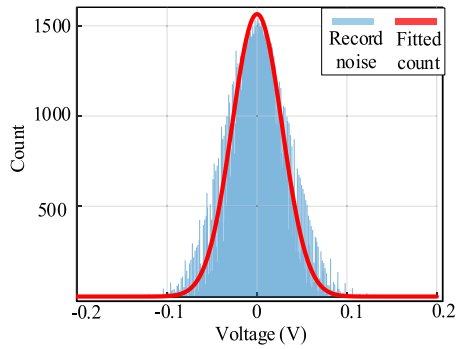


Fig. 22. Noise distribution extracted from received signals during repeated transmission of symbols "0"–"7."

D. Signal-to-Noise Ratio

In the proposed method, both power and information signals share the same transmission channel, and the conditioning circuit inevitably introduces noise. As a result, the received signal is superimposed with noise. To evaluate the transmission quality under different load conditions, it is necessary to quantify the SNR and estimate the corresponding bit error rate (BER).

To this end, symbols "0"–"7" are transmitted with equal probability over about 300 000 counts, under load power ranging from $0.5P_n$ to P_n. The output voltage u_d from the conditioning circuit was recorded. The noise is obtained by subtracting the signal offset from the recorded voltage. The recorded noise approximately follows a Gaussian distribution, as shown in Fig. 22, and can be modeled as

$$v \sim N\left(\mu, \sigma^2\right) \tag{3}$$

where μ is the expected amplitude of the received signal, and $\sigma = 0.0278$ represents the standard deviation, indicating the fluctuation level caused by noise. According to the definition, the SNR can be expressed as

$$\begin{aligned} \mathrm{SNR(dB)} &= 10\log_{10}(P_s/P_n) \\ &= \frac{1}{M\sigma^2}\sum_{i=1}^{M/2}\left[d_i\left(2i-1\right)\right]^2 \end{aligned} \tag{4}$$

where σ^2 denotes the noise power, M represents the modulation order (which is eight in this case), and d_1 is the first decision threshold, set to 0.175 in this work. The calculated SNR is 15.56 dB.

Furthermore, if the absolute noise value $|v| > d$, a symbol error occurs. Thus, the BER can be expressed as

$$\mathrm{BER} = \frac{1}{8}\sum_{i=1}^{8}\left(P\left(v < d_{i-1}\right) + P(v > d_i)\right). \tag{5}$$

The BER can be theoretically calculated as approximately 1.02×10^{-10}. However, in practice, additional disturbances are introduced by the ADC and transmission lines between the conditioning circuit and the DSP. As a result, the actual BER measured by the DSP is 1.2×10^{-9}.

IV. Conclusion

In this article, we explored a novel TPC using the nature of dc–dc converters. The information is intrinsically carried in the waveform of output voltage in the dc–dc converter. And the resonant characteristics of the magnetic tank are similar to those of oscillation circuits in communication systems. Consequently, dc–dc converters inherently support amplitude modulation and frequency selection for the signal transmission, enabling ASK-based high-frequency signal communication. On this basis, we have proposed a high-speed TPC method that uses carriers far exceeding the switching frequency without relying on increased switching frequency. This study also introduces a novel perspective on communication systems by reconsidering the nature of converter output waveforms. The switching output waveform carries rich information. ASK communication can be easily achieved by adjusting the waveform and using frequency-selective networks, without needing multipliers to combine the carrier and data. The proposed method is validated on a DAB converter with the highest communication rate in the state-of-the-art TPC.

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