Physical Modeling of Output Pulse Process in Pulse Generator Based on Drift Step Recovery Diodes

Ziwen Chen, Yuxiao Yang, Zao Yang, Binghui Li, Ruize Sun, Wanjun Chen, and Bo Zhang

***Abstract*—Drift step recovery diodes (DSRDs) are essential components in pulse generators, applicable to a broad spectrum of high-power and high-frequency applications. However, existing models predominantly emphasize device structural parameters while neglecting the critical influence of circuit parameters such as output current and pulsewidth. This study introduces a physical model for pulse generators that integrates drive circuit parameters and device structural parameters through rapid current interruption, thereby enhancing the accuracy of output pulse predictions and improving design efficiency. The proposed model calculates the current interruption phase by analyzing the turn-OFF oscillations of the MOSFET within the drive circuit and incorporates time-dependent current dynamics to generate a temporal variation of the output voltage. Validation through extensive simulations and experimental measurements confirms the accuracy of the model in predicting key output pulse characteristics, including output voltage rise rate, and peak voltage, with relative deviations of less than 10% compared to simulation results and experimental results. Meanwhile, the model is capable of predicting the trend of the prepulse variation. Furthermore, the applicability of the proposed model has been thoroughly discussed, thereby providing a reliable tool for the optimization of DSRDs-based pulse generators. This work significantly contributes to the design of DSRDs-based pulse generators.**

***Index Terms*—4H-SiC, device model, drift step recovery diodes (DSRDs), high-speed electronics, high-voltage (HV) techniques.**

NOMENCLATURE

x_n, x_p	Thickness of the *N-drift* and *P-base* region.
N_D, N_A	Doping of the *N-drift* and *P-base* region.
L_1, L_2	Branches 1 and 2 inductances.
V_{drain}, V_{bias}	Supply voltage.
C_2	External Branches 2 capacitance.
T_{MOS}	Turn-ON time of MOSFET.
J_{ave}	Average forward injection current density.
$i_{\text{branches}-1}(t)$	Current branches 1 during T_{MOS}.
$i_{\text{branches}-2}(t)$	Current branches 2 during T_{MOS}.
$i_{\text{branches}-2}(t)\|_2$	Current branches 2 after T_{MOS}.
J_{PR}	Peak reverse current density.
D	Diffusion coefficient.
a	Slope of the DSRDs current after T_{MOS}.
C_a	Average carrier density in the drift region.
V_{int}	MOSFET voltage at the instant of turn-OFF.
$W_{\text{SCR}}(t)$	Width of the space charge region (SCR).
$\nu_s(t)$	SCR expansion velocity.
$E_m(t)$	Electric field across the PN junction.

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I. INTRODUCTION

THE high-voltage (HV) nanosecond-duration pulses are essential in applications, such as plasma chemistry and reforming: conversion of CH_4/CO_2 and methane to ethylene [1], [2], [3], nitrogen oxides treatment [4], cancer treatments [5], plasma-assisted ignition and combustion [6], [7], [8], [9], plasma actuators and airflow control [10], [11], and ultra-wideband systems [12]. Typical requirements for key component pulse power supplies are amplitudes from kV to tens of kV, repetition rates from kHz to MHz, high efficiency, and low jitter, so the opening switch represented by drift step recovery diodes (DSRDs) have been developed [13]. The DSRDs is a nanosecond timescale opening switch based on the controllable plasma commutation principle, which can be easily assembled in a HV stack, including pump-in and pump-out stages. This has drawn considerable attention to the application of DSRDs in pulse power supplies.

Extensive studies have been conducted on the physical characteristics of DSRDs, pulse discharge circuit topologies, and optimization of these circuits [13], [14], [15]. The simplified model proposed by Benda and Spenke [16] remains the primary physical basis for explaining the operation of DSRDs. Kardo-Sysoev et al. [17] investigated the voltage pulse generation mechanism, identifying key factors affecting the voltage rise rate. In these studies, only the effects of the structure of DSRDs parameters were considered. Kyuregyan [18] derived an approximate analytical formula for evaluating DSRDS characteristics. The circuit model, based on an RLC circuit, does not account for practical application circuits. In addition, the rapid current interruption process is considered by the variation in the nonlinear capacitance of the DSRDS, which necessitated the introduction of assumptions and empirical analysis. Yang [19] investigated the operating mechanism of DSRDs using a simple RLC circuit by coupling circuit equations with the current continuity equation through the Newton method. Fang [20] analyzed

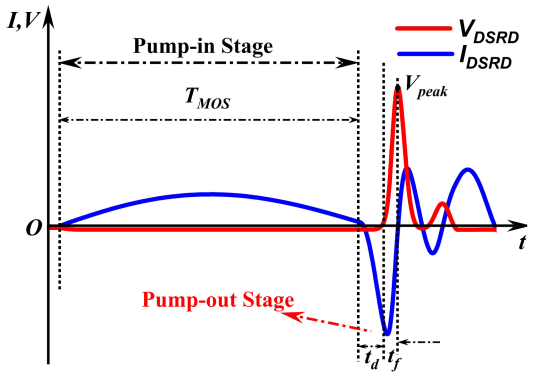

Fig. 1. Typical working principle diagram of the pulse generator based on DSRDs.

practical application drive circuits and determined the impact of circuit parameters on output pulse characteristics. However, the rapid current interruption was obtained empirically. Although the operating principles of DSRDs and the influence of driving circuit parameters have been extensively studied, the absence of a method for calculating the rapid current interruption phase has prevented existing models from being directly applied to pulse generator design. As a result, the design process of the pulse generator still largely depends on extensive simulations and experimental efforts to achieve the desired pulse characteristics.

In this study, a DSRDs pulse generator model for calculating the rapid current interruption phase is proposed by leveraging the voltage variation of the MOSFET during the current interruption phase. This model treats the device and the drive circuit as an integrated system to analyze the output pulse characteristics. By coupling fundamental semiconductor equations with circuit equations, a quantitative description of the rapid current interruption characteristics is provided. Expressions governing the output pulse characteristics of the DSRDs are derived. The accuracy of the model is validated through extensive experimental and simulation data. The primary contributions of this study are threefold.

1) A novel method for modeling the rapid current interruption dynamics of DSRDs was proposed.
2) The interactions between circuit parameters and output pulse characteristics were comprehensively elucidated.
3) A reliable tool for designing DSRDs-based pulse generator circuits in practical applications was developed.

II. Working Principles and Parameters

Fig. 1 illustrates the operating principle of the DSRDs during its output pulse process. The DSRDs operation can be divided into two distinct phases. The first phase is the pump-in phase, in which the switching of the drive circuit is turned ON, thereby injecting forward charge into the DSRDs. The second phase is the pump-out phase, which commences once the switching device is turned OFF. During this phase, a rapid current interruption occurs in the DSRDs current, enabling the realization of nanosecond-level output pulses. This rapid current interruption [28] is crucial for achieving the nanosecond pulse performance of the DSRDs.

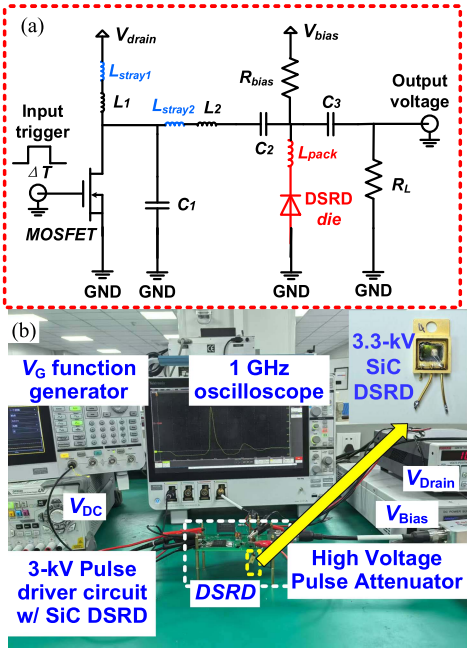

Fig. 2. (a) DSRDs drive circuit diagram. (b) Picture of measurement hardware and the 3-kV pulse generator with SiC DSRDs.

Researchers [13], [14], [15] typically use these pulse characteristic parameters to describe the DSRDs output pulse waveform. The *dV/dt* refers to the slope of the output voltage between 20% and 80% during the pumping-out phase, and the pulse delay (t_d) is defined as the time interval between the MOSFET turn-OFF and the appearance of the output voltage pulse. The pulse peak (V_{peak}) is the maximum value of the output voltage pulse, and the pulse front (t_r) is the time required for the output voltage to rise from 20% to 80%. The prepulse amplitude (V_{pre}) is not depicted in Fig. 1. This parameter corresponds to the voltage at the peak of the second derivative of the output voltage pulse [14].

III. Proposed Modeling Approach

The drive circuit of the DSRDs, as shown in Fig. 2(a), adopts a dual-power DSRDs pulse generator. The DSRDs drive circuit features two main branches that influence the operation of the DSRDs. Branch 1 comprises the power supply V_{drain}, inductor L_1, the stray inductance L_{stray1} associated with this branch, and a MOSFET. Branch 2 includes capacitor C_2, inductor L_2, stray inductance L_{stray2}, a MOSFET, the power supply voltage V_{drain}, the supply voltage V_{bias}, the DSRDs die, and the package inductance L_{pack}. Fig. 2(b) demonstrates the desktop of measurement hardware and the compact pulse generator, where parasitic inductance has been optimized by both layout and cable connections. The hardware includes Tektronix MSO54B oscilloscope, the high voltage pulse attenuator (HVAT-10K20-3.5, HVAT-3K20-5, and DC-6 GHz) from ESDEMC, AFG31252 function generator, DP932A dc power supply, Keithley 248 voltage sources, and MSP6230 voltage sources. The transistor marked as MOSFET is a power MOSFET, DE475-102N21A, produced by IXYS.

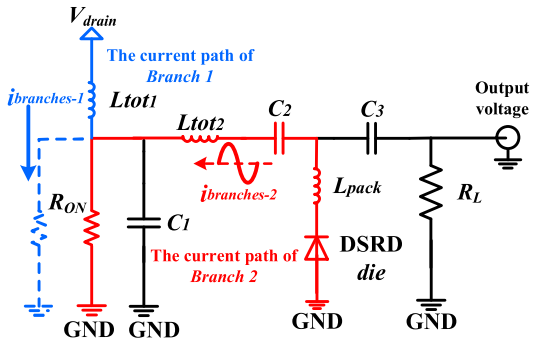

Fig. 3. Equivalent schematic diagram of the DSRDs drive circuit during the pump-in stage.

A. Pump-in Stage

Initially, capacitor C_2 is charged to a voltage of V_{drain}–V_{bias}. The equivalent schematic diagram of the DSRDs drive circuit in the pump-in stage is shown in Fig. 3. L_{tot1} is the sum of L_1 and L_{stray1}, and L_{tot2} is the sum of L_2 and L_{stray2}. The trigger pulse is applied to the MOSFET turn-ON, turning it on and allowing the discharge current of C_2 to provide pumping to the DSRDs through the MOSFET, L_2, L_{stray2}, and C_2 circuits. The width of the trigger pulse determines the turn-ON time of the MOSFET (T_{MOS}). Simultaneously, V_{drain} charges branch 1, and the L_1 inductor stores energy. The forward current amplitudes of branches 1 and 2 are equal to

$$\begin{cases} V_{1L}(t) + V_{R_{\text{on}}}(t) = V_{\text{drain}} \\ V_{C2}(t) + V_{2L}(t) + V_{R_{\text{on}}}(t) + V_{\text{DSRD}}(t) = 0 \end{cases} \tag{1}$$

where

$$\begin{aligned} V_{1L}(t) &= L_{\text{tot1}} \cdot \frac{di_{\text{branches}-1}(t)}{dt} \\ V_{2L}(t) &= (L_{\text{tot2}} + L_{\text{pack}}) \cdot \frac{di_{\text{branches}-2}(t)}{dt} \\ V_{R_{\text{on}}}(t) &= i_{\text{MOSFET}}(t) \cdot R_{\text{on}} \\ V_{\text{DSRD}}(t) &= i_{\text{branches}-2}(t) \cdot R_{\text{DSRD}} \\ V_{C2}(t) &= \frac{1}{C_2} \int i_{\text{branches}-2}(t)dt \\ i_{\text{MOSFET}}(t) &= i_{\text{branches}-1}(t) + i_{\text{branches}-2}(t) + i_{C1}(t) \\ i_{C1}(t) &= \frac{V_{\text{drain}}}{R_{\text{on}}} e^{-\frac{1}{R_{\text{on}}C_1}t} \\ V_{C2}(t)|_{t=0} &= V_{\text{drain}} - V_{\text{bias}} \\ i_{\text{branches}-1}(t)|_{t=0} &= i_{\text{branches}-2}(t)|_{t=0} = 0. \end{aligned} \tag{2}$$

The current of branch 2 governs the charge injected into the DSRDs. Given that the minority carrier lifetime (at least 500 ns) in the DSRDs is significantly longer than the MOSFET turn-ON duration, charge loss can be neglected. The carrier concentration distribution within the DSRDs is derived based on the injection current. Since the minority carrier lifetime exceeds the MOSFET on time, the carrier lifetime is effectively replaced by the T_{MOS} [17]. The following equation then gives the width of the DSRDs diffusion region:

$$W_d = \sqrt{\text{DT}_{\text{MOS}}}. \tag{3}$$

D represents the diffusion coefficient, which can be derived using the Einstein relationship. Since the minority carrier mobility in the *N-drift* region is low, the diffusion width $W_d(N)$ is much smaller than the x_n. The *P-base* region requires further consideration, with two possible scenarios: 1) the diffusion width $W_d(P)$ of the *P-base* region is greater than the x_p of; 2) $W_d(P)$ is less than x_p.

When $W_d(P)$ is greater than x_p. The catenary carrier concentration distribution formula, along with the boundary conditions, can be used to derive the carrier concentration distribution [22]

$$p(x) = \frac{J_{\text{ave}} T_{\text{MOS}}}{2qW_d} \left[\frac{\cosh(x/W_d)}{\sinh(x_p/W_d)} - \frac{B\sinh(x/W_d)}{\cosh(x_p/W_d)} \right] \tag{4}$$

$$\begin{aligned} C_a &= \int_0^{T_{\text{MOS}}} J_{\text{branches}-2}(t)dt/(qx_p) \\ J_{\text{ave}} &= \left(\int_0^{T_{\text{MOS}}} J_{\text{branches}-2}(t)dt \right) / T_{\text{MOS}} \end{aligned} \tag{5}$$

where q is the charge, B is a constant given by $[(\mu_{\text{n}}+\mu_{\text{p}})/(\mu_{\text{n}}-\mu_{\text{p}})]$, and J_{ave} is the average current density in the pumping-in stage. When $W_d(P)$ is less than x_p and in the *N-drift* region, the carrier concentration exhibits an exponential decay within the diffusion region, and a simple approximation is applied to some key parameters

$$C_a = \frac{W_d(P)}{2x_p} \cdot p\left(\frac{x_p}{2}\right) + \frac{N_A}{2x_p} \cdot (2x_p - 3W_d(P)) \tag{6}$$

where C_a represents the average carrier density in the drift region. In the pump-in stage, the primary function of the DSRDs drive circuit is to inject charge into the DSRDs, initiating forward conduction. As noted earlier, the minority carrier lifetime in DSRDs is longer than that of T_{MOS}, meaning that T_{MOS} determines the carrier distribution in DSRDs.

B. Pump-Out Stage

When the MOSFET is turned OFF, the current cannot undergo an abrupt phase reversal due to the influence of inductance. The equivalent schematic diagram of the DSRDs drive circuit in the pump-out stage is shown in Fig. 4, which transfers the energy stored in L_1 to L_2, thereby increasing the speed of current extraction in the DSRDs pump-out stage. During this stage, the magnitude of the reverse current can reach 3–5 times that of the forward current, this value is obtained experimentally and commonly used in previous empirical formula calculations for DSRDs [20]. In this study, a method is proposed to calculate the rapid current interruption phase based on the turn-OFF process of MOSFET, thereby obtaining an accurate value for the maximum reverse current. Using the classic equivalent model, the MOSFET is represented by the capacitance C_{oss} and a parallel on-resistance $R_{\text{ds-on}}$. The expression for the voltage of MOSFET during the turn-OFF stage is [23], [24]

$$\begin{aligned} V_{\text{MOSFET}}(t) = {} & A_1 \cos(\omega_{d1}t - \phi_1) \\ & + A_2 \cos(\omega_{d2}t - \phi_2) + 2V_{\text{drain}} - V_{\text{bias}} \end{aligned} \tag{7}$$

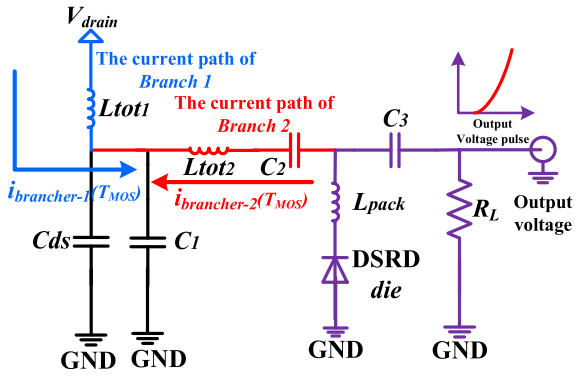

Fig. 4. Equivalent schematic diagram of the DSRD drive circuit during the pump-out stage.

where

$$A_{1(2)} = \sqrt{(V_{\text{init}} - V_{1(2)})^2 + Z_{1(2)} i_{1(2)}^2}$$

$$\phi_{1(2)} = \omega_{1(2)} \frac{T_{\text{MOS}}}{2} + \arctan \left\{ \frac{(V_{\text{init}} - V_{1(2)}) \sin \frac{\omega_{1(2)}}{2} T_{\text{MOS}} + Z_{1(2)} i_{1(2)} \cos \frac{\omega_{1(2)}}{2} T_{\text{MOS}}}{(V_{\text{init}} - V_{1(2)}) \cos \frac{\omega_{1(2)}}{2} T_{\text{MOS}} - Z_{1(2)} i_{1(2)} \sin \frac{\omega_{1(2)}}{2} T_{\text{MOS}}} \right\}$$

$$\omega_{1(2)} = \sqrt{\frac{1}{2L_{\text{tot1(tot2)}}(C_1 + C_{\text{oss}})}}$$

$$V_1 = V_{\text{drain}}$$

$$V_2 = V_{\text{drain}} - V_{\text{bias}}$$

$$Z_{1(2)} = \sqrt{2L_{\text{tot1(tot2)}}/(C_1 + C_{\text{oss}})} \tag{8}$$

where V_{init} is the initial voltage of MOSFET when the MOSFET turn-OFF, i_1 and i_2 denote the current magnitudes of Branch 1 and Branch 2, respectively, evaluated at the moment T_{MOS}, A represents the amplitude of the oscillatory component in the corresponding branch, Z denotes the characteristic impedance corresponding to the two components, and ϕ denotes the initial phase of the component. Due to the fast turn-OFF of the MOSFET, the voltage across capacitor C_2 undergoes only minimal change. For simplicity in calculation, it is assumed to be constant. The current expression for branch 2 can be derived based on the voltage change across inductor L_2 after the MOSFET turn-OFF

$$i_{\text{branches}-2}(t)|_2 = \frac{1}{L_{\text{tot2}}} \int_{T_{\text{MOS}}}^{t} [V_{\text{MOSFET}}(t) - V_{C_2}(T_{\text{MOS}})]dt + G \tag{9}$$

where

$$G = i_{\text{branches}-2}(T_{\text{MOS}}) \tag{10}$$

where G is the current density of branches-2 at the time of T_{MOS}.

Based on the step-recovery process [22], the initial slope of the current of DSRDs during the reverse recovery phase matches the current slope of L_2. parameter "a" can be obtained through linear approximation

$$a = \frac{d\, i_{\text{branches}-2}(t)|_2}{dt}. \tag{11}$$

The significant current passes through the DSRDs resulting in a storage of electric charges Q_1 in a close neighborhood of the diode junction, where the Q_1 charge is [30]

$$Q_1 = \int_0^{T_{\text{MOS}}} J_{\text{branches}-2}(t)dt. \tag{12}$$

Based on the reverse recovery mechanism, the pulse delay time t_1 for the voltage rise of the DSRDs is the time required to remove the minority carriers. This can be expressed as [30]

$$\int_{T_{\text{MOS}}}^{t_1} J_{\text{branches}-2}(t)|_2 dt = Q_1. \tag{13}$$

At $t = t_1$, the DSRDs suddenly become reversed biased. During the phase of the DSRDs turn-OFF process, the reverse current rapidly reduces at approximately a constant rate [22]. The peak reverse recovery current J_{PR}

$$J_{\text{PR}} = G - a(t_1 - T_{\text{MOS}}) = 2qD\frac{C_a}{h} \tag{14}$$

$$h = \frac{2qDC_a}{J_{\text{PR}}}. \tag{15}$$

The parameter "h" represents a dimensional parameter in the theoretical [22]. At $t = t_2$, $V(t)$ becomes maximum when we have $i_{\text{branches-2}} = 0$. This can be equated to the charge left in the drift region at $t = t_1$ if recombination during this time is neglected due to the short duration of this time interval relative to the minority carrier lifetime. The time interval for the reduction of the reverse current is then obtained [22]

$$\Delta t = t_2 - t_1 = \frac{2qC_a}{J_{\text{PR}}}(x_p - W_{\text{SCR}}(t_1) - h). \tag{16}$$

The reverse ramp rate is obtained by dividing the peak reverse recovery current by this time interval

$$\left[\frac{dJ}{dt}\right]_R = \frac{J_{\text{PR}}}{\Delta t} = \frac{J_{\text{PR}}^2}{2qC_a(x_p - W_{\text{SCR}}(t_1) - h)}. \tag{17}$$

During the period from t_1 to t_2, the rate of expansion of the SCR in the *N-drift* region ($\nu_{s\text{-}N}(t)$) is expressed as [17]

$$\nu_{s-N}(t) = \frac{J_{\text{PR}} - [dJ/dt]_R(t - t_1)}{qC_a}. \tag{18}$$

The extent of SCR is expressed as

$$W_{\text{SCR}}(t) = \int_{t1}^{t} \nu_{s-N}(t)dt. \tag{19}$$

The electric field intensity distribution can be derived from the Poisson equation. For the DSRDs, the focus is on the electric field across the PN junction, which is expressed as

$$E_m(t) = \frac{qC_a}{\varepsilon\varepsilon_0} W_{\text{SCR}}(t) \tag{20}$$

where ε_0 is the dielectric constant of vacuum, and ε represents the relative dielectric constant of the material. E_m reaches a maximum value ($E_{m\max}$), given by $3.3\times10^4 N_D{}^{1/8}$ for 4H-SiC

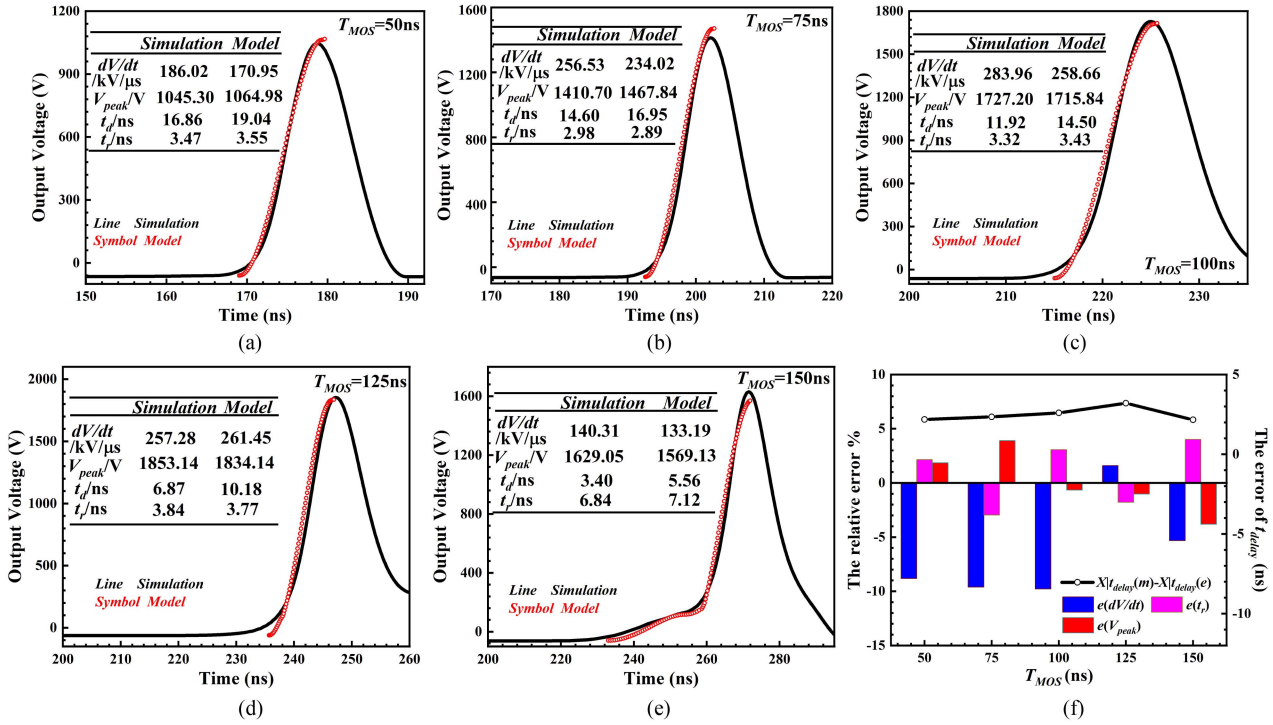

Fig. 5. Simulation curve and model calculated curves with varying the MOSFET turn-ON time (T_{MOS}). (a) $T_{\mathrm{MOS}} = 50$ ns. (b) $T_{\mathrm{MOS}} = 75$ ns. (c) $T_{\mathrm{MOS}} = 100$ ns. (d) $T_{\mathrm{MOS}} = 125$ ns. (e) $T_{\mathrm{MOS}} = 150$ ns. (f) Relative error analysis and the error of t_d extracted from (a)–(e).

and $4010N_D^{1/8}$ for Si. The rate of voltage drops across the SCR in the DSRDs die is given by [17]

$$\frac{dV_{\mathrm{die}}}{dt} = E_m(t)\nu_{s-N}(t) \tag{21}$$

$$V_{\mathrm{die}}(t) = \int_{t_1}^{t_2} E_m(t)\nu_{s-N}(t)dt. \tag{22}$$

Previous studies [25] have suggested that prepulses are primarily influenced by p-region concentration and current density. However, recent research [15] indicates that package inductance also plays a significant role in the formation of prepulses. Since the detailed mechanism behind prepulse formation is not the focus of this study, both factors will be considered in the model. The calculation method [15] for the prepulse induced by package inductance is shown below

$$V_{\mathrm{DSRD}} = L_{\mathrm{pack}} \frac{di_{\mathrm{branches}-2}(t)}{dt} + V_{\mathrm{die}}. \tag{23}$$

Based on the above-mentioned derivation, the DSRDs pulse output curve can be obtained by inputting the structure and drive circuit parameters. Both drive circuit parameters and device structural parameters were jointly incorporated into the model, enabling the calculation of drive circuit parameters through the proposed approach. This integration significantly enhances the efficiency of drive circuit design and facilitates the application of pulse generators based on DSRDs. It is worth noting that the proposed model is only applicable to single-switch pulse generators whose operation principles resemble that illustrated in Fig. 2. Specifically, the model is valid for circuits where the forward injection loop consists of an *RLC* network and the reverse extraction relies on the rapid turn-OFF of the switching device.

IV. Verification the Proposed Model

In this section, the feasibility of the proposed model is validated using simulation and experimental results.

A. Simulation Verification

Synopsys Sentaurus Technology Computer-Aided Design software [26] was employed as the DSRD simulator, employed in mixed mode configuration to cosimulate the pulse generator. The simulation addressed the coupled Poisson and current continuity equations in conjunction with the SPICE model. These include the doping dependence Masetti model, Carrier-carrier scattering Conwell-Weisskopf model, and carrier velocity saturation in high field Canali model. Shockley-Read-Hall recombination included its doping dependence and Auger. The Van Overstraeten-de Man model was used for avalanche generation, and the Slotboom model for the band-gap narrowing effect and incomplete ionization effect. All models were employed using their default values [26].

Fig. 5(a)–(e) compares the simulation results with the model fitting under varying T_{MOS} conditions. In the simulation presented in Fig. 5, the DUT structural and circuit parameters are consistent with those shown in Table I, except that parasitic inductance and package inductance were not considered. An inset table within the figure characterizes the voltage pulse curves by contrasting key parameters, including t_{d}, t_{r}, V_{peak}, and *dV/dt*. To evaluate the accuracy of the model, the relative

TABLE I
PARAMETERS UTILIZED IN THE SIMULATION

Symbol	Meaning	Value
N_A	doping of *P-base*	1.0e17 cm^{-3}
x_p	length of *P-base*	4.0 μm
N_D	doping of *N-drift*	1.0e15 cm^{-3}
x_n	length of *N-drift*	35.0 μm
V_{drain}	voltage of drain	180 V
V_{bias}	voltage of bias	100 V
T_{MOS}	MOSFET turn-on time	100 ns
L_1	inductance	80 nH
L_2	inductance	60 nH
C_1	capacitance	1 nF
C_2	capacitance	45 nF
area	DSRD area	1 cm^2

error e, as defined in (24), is utilized, where X_m represents the model prediction value and X_e represents the experimental

$$e = \frac{(X_m - X_e)}{X_m}. \tag{24}$$

Based on the extraction of the parameters from Fig. 5(a)–(e), the relative error presented in Fig. 5(f) indicates that $e(dV/dt)$, $e(V_{\text{peak}})$, and $e(t_r)$ are below 10%. The errors of t_d with varying T_{MOS} are approximately 2 ns. This indicates that the proposed model achieves high accuracy under ideal conditions.

Notably, Fig. 5(e) demonstrates that the model successfully predicted the occurrence of the prepulse amplitude (V_{pre}). The simulated V_{pre} is 127.01 V, whereas the model-calculated V_{pre} is 120.93 V, with $e(V_{\text{pre}})$ of −5.03%. The results illustrated in Fig. 5 indicate that the mismatch between T_{MOS} and the drive circuit induces plasma extraction during the pump-in phase, thereby contributing to the generation of prepulse. The novel explanation for the occurrence of prepulses is provided by the proposed model, and this explanation is supported by theoretical analysis. The prepulses induced by mismatches in T_{MOS} lead to a reduction in the performance of the output pulses. Consequently, the occurrence of current commutation should be avoided during the design process of DSRD drive circuits.

Previous studies [14], [15], [29] have demonstrated that the formation of prepulses results from the combined effects of multiple factors. In addition to the mismatch between T_{MOS} and the drive circuit proposed herein, the most prevalent influencing factor is the package parasitic inductance [15]. Fig. 6 illustrates the simulation and model-calculated curves for a package inductance of 7 nH. Fig. 6 indicates that the $e(dV/dt)$, $e(V_{\text{peak}})$, and $e(V_{\text{pre}})$ are 2.77%, 1.92%, and −7.05%, respectively. The proposed model is not only capable of calculating the prepulse induced by T_{MOS} mismatch, but it also accurately captures the effects of parasitic package inductance. In summary, the comparison with simulation results confirms that the proposed model can effectively predict the output pulse waveform, indicating its utility in supporting device design.

B. Experimental Verification

To validate the practical significance of the proposed model for device and drive circuit design, experimental verification was

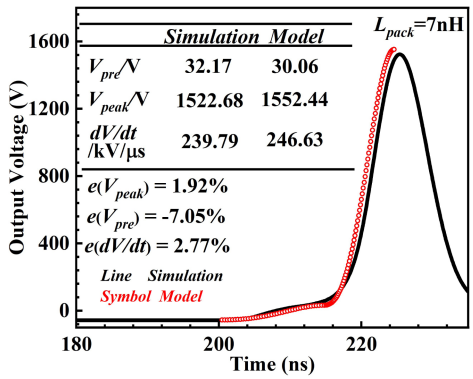

Fig. 6. Simulation curve and model calculated curves for $L_{\text{pack}} = 7$ nH.

TABLE II
PARAMETERS UTILIZED IN THE EXPERIMENTS

Symbol	Meaning	Value
N_A	doping of *P-base*	1.0e17 cm^{-3}
x_p	length of *P-base*	4.0 μm
N_D	doping of *N-drift*	1.0e15 cm^{-3}
x_n	length of *N-drift*	35.0 μm
V_{drain}	voltage of drain	260 V
V_{bias}	voltage of bias	110 V
T_{MOS}	MOSFET turn-on time	50 ns
L_1	inductance	66 nH
L_2	inductance	46 nH
C_1	capacitance	470 pF
C_2	capacitance	15 nF
L_{stray}	stray inductance	4.5 nH
L_{pack}	package inductance	6 nH
area	DSRD area	30 mm^2

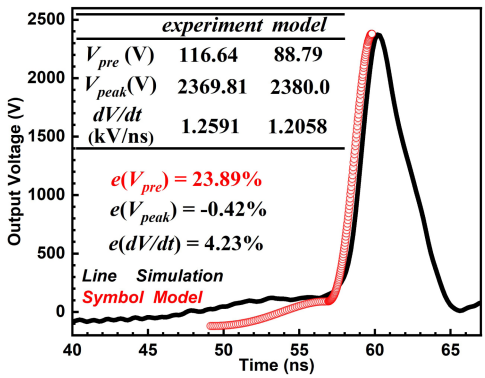

Fig. 7. Experimental and model-calculated curves under benchmark parameters.

conducted under the conditions specified in Table II. Experimental validation was carried out using a custom-designed SiC DSRD device and pulse generator [27]. The parasitic inductance of the SiC DSRDs package and the test board at 100 MHz is extracted using ANSYS.

Under the benchmark parameters outlined in Table II, both the experimental results and the model calculation outcomes are depicted in Fig. 7. The inset table in Fig. 7 presents the key parameters of the pulse curves extracted from the data. The $e(V_{\text{peak}})$ is

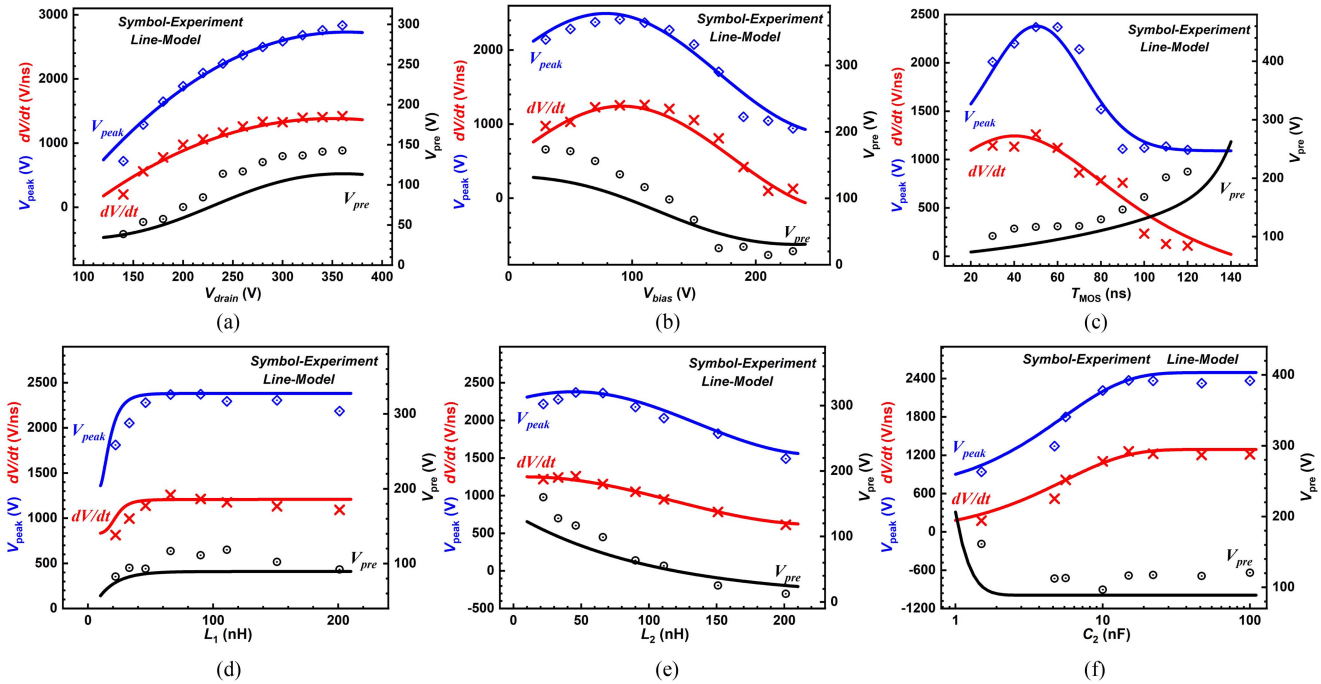

Fig. 8. Trend curves of *dV/dt*, V_{peak}, and V_{pre} extracted from experimental and model output pulse waveforms as functions of (a) V_{drain}, (b) V_{bias}, (c) T_{MOS}, (d) L_1, (e) L_2, and (f) C_2. Black represents V_{pre}, red represents *dV/dt*, and blue represents V_{peak}; symbols denote the experimental data, and lines represent the model calculations.

-0.42%, the $e(dV/dt)$ is 4.23%, and the $e(V_{\mathrm{pre}})$ is 23.89%. Small relative errors of *dV/dt* and V_{peak} are observed, indicating the proposed model has high accuracy. And the significant relative error of V_{pre} was found. Based on the results of Figs. 5 and 6, it is inferred that the relatively high error in the prepulse amplitude between the experimental and model-calculated results in Fig. 7 is likely attributable to parasitic series inductance introduced during the soldering process and the use of vias in the pulse test circuit.

To ensure that the relative error in the prepulse does not adversely affect the practical application of the model, Fig. 8 presents extensive experimental data that illustrate the predicted trends of the output pulse curves. Fig. 8 shows the trend curves of V_{pre}, *dV/dt*, and V_{peak} extracted from experimental and model output pulse waveforms, plotted as functions of (a) V_{drain}, (b) V_{bias}, (c) T_{MOS}, (d) L_1, (e) L_2, and (f) C_2. Fig. 8(a) presents the trend curves of V_{pre}, *dV/dt*, and V_{peak} as functions of V_{drain}. The fitting results in Fig. 8 for the three parameters indicate that *dV/dt*, and V_{peak} exhibit relatively low relative errors across different V_{drain} conditions, demonstrating the high accuracy of the model under varying V_{drain}. Although the relative error of V_{pre} is large, the trend of increasing prepulse amplitude with rising V_{drain} is consistent with the predictions of the model. Fig. 8(b)–(f) presents results consistent with those shown in Fig. 8(a). In all cases, *dV/dt*, and V_{peak} are predicted with high accuracy under varying conditions, while the trend of the prepulse amplitude agrees with the model calculations. These results indicate that, although the proposed model exhibits limited precision in predicting the exact prepulse amplitude in practical applications, it effectively captures the trend of its variation. Furthermore, the model accurately predicts both the voltage rise rate and the peak voltage.

In summary, the proposed model has been experimentally validated and shown to be applicable to pulse generator design. It enables the prediction of *dV/dt* and V_{peak} within a small margin of error and captures the trend of prepulse behavior, thereby supporting the advancement of DSRD-based applications.

V. Comparison and Discussion

In this section, the applicable scope of the proposed model is first discussed. Subsequently, a comparative analysis is conducted between the proposed model and existing models within this scope to evaluate its contributions. Moreover, pulse generator design strategies are advanced based on the proposed model, and its applicability is discussed.

A. Applicability of the Proposed Model to Pulse Generator Circuits

A variety of topologies exist for pulse generator circuits, which can be classified based on the mechanism of fast current interruption into magnetic switch triggered (SO) [34], [35], [36], switch turn-OFF triggered (STF) [20], [27], [31], [33], [37], [38], [39], and switch turn-ON triggered types (STO) [21]. Table III provides a comparison of the three circuit topologies, highlighting their respective advantages and disadvantages, as well as the applicability of the proposed model.

As the proposed model accurately determines the current interruption phase by calculating the voltage oscillations generated during MOSFET turn-OFF under high current conditions, it is, as

TABLE III
COMPARISON OF THREE TYPES CIRCUIT TOPOLOGIES

Category	SO	STF	STO
Origin of the Rapid Current Interruption Phase	Magnetic Switch	Switch Turn-Off	Switch Turn-On
Switch Operation Cycle	Switch always on	Turn-on followed by Turn-off	Two switches turn-on at different times
Advantages	1.Simplified active control; 2. Magnetic compression yields sub-ns rise times; 3. Lower stress on MOSFET	1. Simple passive components; 2. Easier to synchronize with other systems. 3. High repetition	1. Independent control of forward and reverse pulse; 2. Reduce stress per switch;
Disadvantages	1. Relies on magnetic cores and precise *LC* tuning; 2. Reset time of saturable inductors limits repetition rate; 3.Large in volume	1. Fast transistor switching needed; MOSFET endures high voltage spike and *di/dt* stress; 2. Switching losses can be significant	1. More complex: needs two perfectly synchronized switches and dual energy storage loops; 2. Greater risk of timing error
Ref.	[34], [35], [36]	[20], [27], [31], [33], [37], [38], [39]	[21]
Applicability of the proposed model	NO	**YES**	NO

TABLE IV
COMPARISON OF DIFFERENT MODELS BASED ON DSRD

Category	[20], [31]	[17], [19]	[15]	[30]	**Proposed**
Peak voltage variation with external circuit parameters	YES	NO	NO	YES	**YES**
Peak voltage variation with internal device parameters	NO	YES	NO	NO	**YES**
Pre-pulse amplitude trend prediction	NO	NO	YES	NO	**YES**
Rapid current interruption phase calculation	NO	NO	NO	YES	**YES**
Temporal evolution of output voltage	NO	NO	NO	NO	**YES**
Applicable Device Structures	*P-π-v-N*	*P-v-N* [17] *P-π-N* [19]	*P-π-v-N*	*P-v-N*	***P-π-v-N*** ***P-v-N***

indicated in Table III, applicable only to STF-type pulse generator circuits. This circuit offers advantages such as compact size, the capability to operate at high repetition rates, and ease of synchronization with other systems through switch-controlled pulse output. However, as demonstrated in the model derivation, the MOSFET is subjected to HV spikes. Moreover, the significant turn-OFF losses in the MOSFET may adversely affect the energy transfer from L_1 to L_2. Therefore, different circuit parameters have been employed across the studies under investigation.

The proposed model calculates the fast current interruption phase based on the turn-OFF oscillation of the MOSFET, thereby taking into account the turn-OFF loss. More importantly, by accurately determining the current interruption phase, the model establishes a connection between the circuit parameters of the pulse generator and the structural parameters of the DSRD device. This provides a useful reference for the design of STF-type pulse generators.

B. Compared With Other Models Based on DSRD

To further evaluate the advantages of the proposed model, Table IV provides a comparative summary of the key features of six representative DSRD-based modeling approaches [15], [17], [19], [20], [30], [31]. Compared to existing DSRD-based models, the proposed model offers a more comprehensive theoretical foundation for the design of DSRD applications in three key aspects.

1) *Comprehensive Parameter Dependency Modeling*: Unlike prior models that consider either internal or external influences in isolation, the proposed model simultaneously accounts for the effects of both device structural parameters and external driving circuit conditions on pulse characteristics.
2) *Prepulse Amplitude Trend Prediction*: The model introduces a physically grounded explanation for prepulse formation, enabling the prediction of prepulse amplitude trends under varying circuit and device conditions—a feature absent in most existing models.
3) *Temporal Evolution Modeling of the Output Pulse*: The rapid current interruption phase is quantitatively modeled by coupling semiconductor and circuit dynamics, which allows temporal evolution modeling of the output pulse and supports precise circuit parameter design.

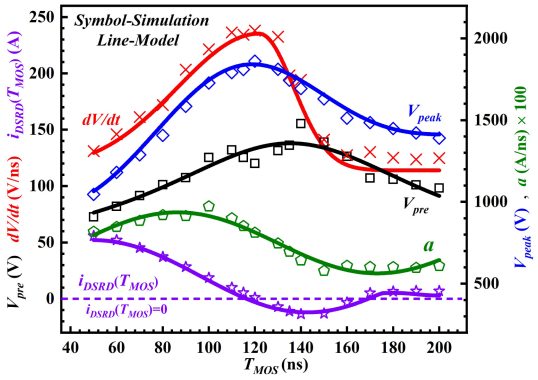

Fig. 9. Trend curves of *dV/dt*, V_{peak}, V_{pre}, a, and i_{DSRD} (T_{MOS}) extracted from simulation and model output pulse waveforms as functions of T_{MOS}. Black represents V_{pre}, red represents *dV/dt*, blue represents V_{peak}, green represents parameter a, and purple represents i_{DSRD} (T_{MOS}). Symbols denote the simulation data, and lines represent the model calculations.

C. Design Guidelines and Analysis

This section examines the key parameters of the pulse generator to guide its design. Based on the proposed model, the establishment of design guidelines for their implementation.

Based on the proposed model, for a given set of pulse generator circuit parameters and DSRD device structural parameters, the value of T_{MOS} can be used to determine whether the pulse generator operates at the condition that yields the maximum achievable output voltage peak. Fig. 9 illustrates the trend curves of V_{pre}, *dV/dt*, V_{peak}, a, and i_{DSRD} (T_{MOS}) extracted from simulation and model output pulse waveforms, plotted as functions of T_{MOS}. The parameter a denotes the characteristic of the rapid current interruption phase, and i_{DSRD} (T_{MOS}) represents the DSRD current at the instant T_{MOS}. In addition, as T_{MOS} increases, the W_d expands. Under conditions where i_{DSRD} (T_{MOS}) assumes positive values, an augmentation of T_{MOS} results in an increased injected charge; conversely, when i_{DSRD} (T_{MOS}) is negative, an increase in T_{MOS} leads to a reduction in injected charge. The peak of parameter a occurs around 100 ns, while i_{DSRD} (T_{MOS}) begins to reverse at 118 ns. During the interval from 112 to 120 ns, *dV/dt* exhibits minimal variation, and the peak of V_{peak} is observed at 120 ns. This indicates that the injected charge is a critical parameter influencing output pulse characteristics. Notably, as parameter a begins to decline, the rate of increase for both *dV/dt* and V_{peak} is attenuated. Based on the analytical and modeling results, a design guideline for DSRD-based pulse generators is proposed: during the pumping-in stage, the outer circuit should be configured such that the switching is turned OFF at an appropriate time, maximizing the amount of forward-injected charge. The turn-ON time that yields the maximum injected charge is defined as T_C.

To validate the effectiveness of the proposed design guideline in practical pulse generator operation, Fig. 10 presents (a) The output voltage pulse curves and (b) DSRD current curves for T_{MOS} values of $T_{\mathrm{MOS}} < T_C$, $T_{\mathrm{MOS}} = T_C$, and $T_{\mathrm{MOS}} > T_C$. When T_{MOS} is less than T_C, the reduction in forward-injected charge leads to a decrease in the reverse peak current and a lower average carrier concentration during the injection process. As a result, *dV/dt* is reduced.

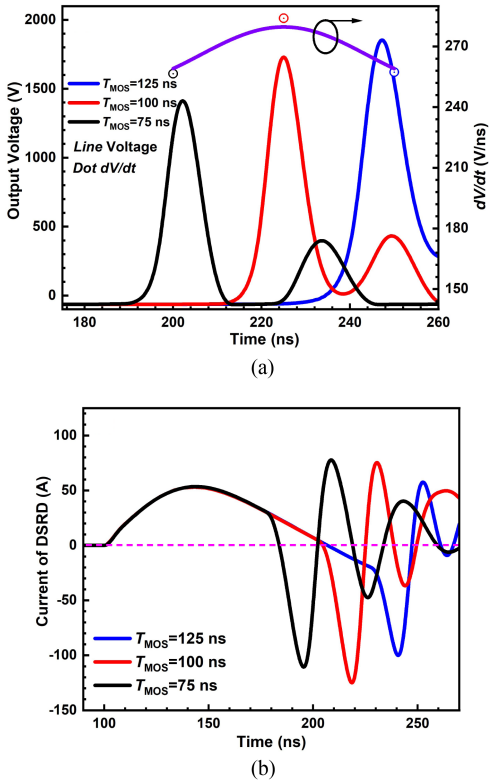

Fig. 10. (a) Output voltage pulse curves and (b) DSRD current curves for T_{MOS} values of $T_{\mathrm{MOS}} < T_C$, $T_{\mathrm{MOS}} = T_C$, and $T_{\mathrm{MOS}} > T_C$.

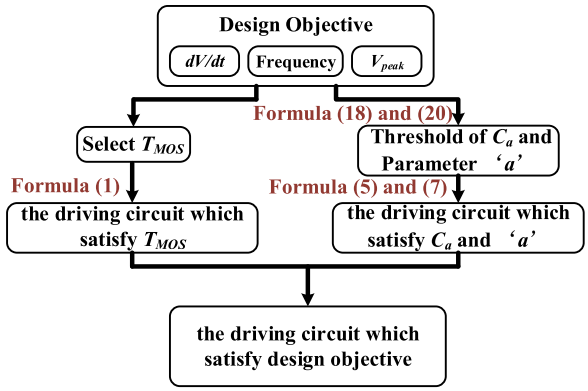

Fig. 11. Design approach for the drive circuit.

When $T_{\mathrm{MOS}} > T_C$, the forward injection remains consistent with the case of $T_{\mathrm{MOS}} = T_C$. However, during the reverse extraction process, a period of slower charge extraction occurs, resulting in a reduced reverse peak current and a decreased *dV/dt*. The lower reverse current peak prolongs the voltage rise time during the pulse generation stage, leading to an increase in the peak voltage. However, when the reverse current peak falls below a certain threshold, the peak voltage correspondingly decreases, as shown in Fig. 5(e). This process is consistent with the conclusions derived from the proposed model and is also observed in the experimental results.

Based on the design guideline, a design methodology for drive circuit parameters is proposed, as depicted in Fig. 11.

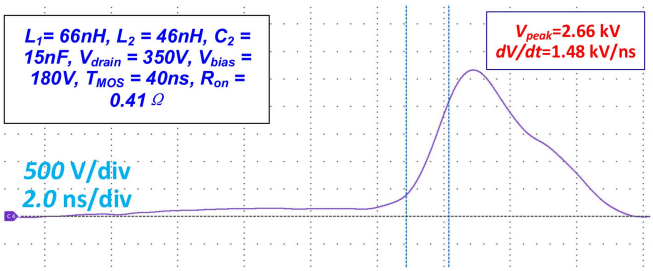

Fig. 12. Experimental results of the pulse output waveform based on circuit parameters designed using the proposed model.

For pulse generators engineered to achieve designated output pulse characteristics, the maximum MOSFET turn-ON time is determined according to frequency and duty cycle requirements and is defined as T_{MOS}. Once T_{MOS} has been established, it is incorporated into the model, thereby yielding a set of circuit parameter relationships. Furthermore, by inputting the target values for V_{peak} and *dV/dt* into the proposed model, an additional set of circuit parameter relationships is derived. The circuit parameters must satisfy both sets of relationships to meet the specified requirements. Thus, the drive circuit parameters that satisfy the design specifications have been computed through the proposed model.

Taking the device structure in this work as an example, a target voltage rise rate of 1.4 kV/ns was set. According to the model calculation, the SCR boundary expansion velocity must reach 3.5×10^6 cm/s, corresponding to a required peak reverse current density of 585.8 A/cm^2. Fig. 12 presents the experimentally measured pulse output waveform based on the circuit parameters designed using the proposed model. The *dV/dt* of 1.5 kV/ns were achieved, meeting the design specifications.

Previous modeling approaches relied on empirical judgment to determine the rapid current interruption phase [20], thereby failing to integrate the output pulse parameters with the driving circuit parameters. In contrast, the proposed model provides the first theoretical framework for calculating the DSRD driving circuit design, thereby enhancing the design efficiency of pulse generators.

D. Discussion on the Proposed Model Applicability

In this section, the applicability of the proposed model is examined, and its scope of validity is systematically analyzed. The previous discussion primarily focused on the accuracy of the model for SiC DSRDs with a *P*-π-ν-*N*-type epitaxial structure under various operating conditions and introduced a method for determining the driving circuit parameters for this structure. As demonstrated in Section III, the proposed model establishes a linkage between semiconductor equations and circuit equations through the rapid current interruption phase, and is therefore expected to apply to all epitaxial DSRD devices, including *P*-ν-*N* structure and *P*-π-*N* structure, operating within the circuit configuration shown in Fig. 2(a).

Fig. 13 presents the output characteristic fitting results for three epitaxial structures: (a) SiC DSRDs with *P*-ν-*N* structure, (b) SiC DSRDs with *P*-π-*N* structure, and (c) Si DSRDs with *P*-π-ν-*N* structure. The relative errors for the three structures are as follows: for the SiC DSRDs with *P*-ν-*N* structure, $e(dV/dt)$ is -8.06% and $e(V_{\mathrm{peak}})$ is 2.96%; for the SiC DSRDs with *P*-π-*N* structure, $e(dV/dt)$ is 6.44% and $e(V_{\mathrm{peak}})$ is 2.25%; for the Si DSRDs with *P*-π-ν-*N* structure, $e(dV/dt)$ is -10.14% and $e(V_{\mathrm{peak}})$ is 0.93%. This indicates that the proposed model is applicable not only to SiC DSRDs with the *P*-ν-*N* structures but also to the Si DSRDs with the *P*-π-ν-*N* structure. It is worth noting that, as shown in Fig. 13(b), a prepulse phenomenon is observed in the SiC DSRD with a *P*-π-*N* structure. This behavior is primarily attributed to the saturation of hole mobility [29].

For a given 10 mm^2 DSRD device, considering the hole saturation velocity of $\nu_{\mathrm{h\text{-}sat}} = 8.37 \times 10^6$ cm/s and an acceptor doping concentration of $N_A = 1.0 \times 10^{14}$ cm^{-3}, the maximum theoretically supported current density is approximately 1340 A/cm^2. Under these conditions, the maximal current density that can be supported in a DSRD is approximately 13.4 A. Therefore, the hole concentration beyond the plasma front can drop below the background doping level [29]. This low base doping limits the rapid extraction process, contributing to the formation of a pronounced pre-pulse. Due to its higher critical electric field of SiC allows for higher doping concentrations in the drift region. This enables the current density to remain within the allowable limits of the base region, thereby resulting in a relatively smaller prepulse amplitude.

A larger device area and higher base doping concentration facilitate the applicability of the proposed model to DSRDs with a P-π-N structure. However, an excessively large device area reduces the stored charge following forward injection, which in turn degrades the pulse performance. Due to the higher critical electric field of SiC, a higher drift region doping concentration is typically employed, which favors the implementation of the proposed model in this structure. Therefore, the model remains applicable to *P*-π-*N* structured SiC DSRDs when the drift region doping concentration is sufficiently high, as illustrated in Fig. 13(b).

In practical applications, series and multileg configurations are often employed to enhance the voltage rise rate of DSRDs [15], [32], [33]. Therefore, to address design considerations, the series and multileg implementations of DSRDs are further analyzed in this work. Fig. 14 indicates that the relationship between the quantity of DSRDs used in series or multileg configurations and the resulting V_{peak} and *dV/dt*. To enhance clarity in Fig. 14, certain results were adjusted for improved visibility. The shifted data points are explicitly annotated in the figure. A linear relationship between the number of DSRDs and both V_{peak} and *dV/dt* confirms the scalability of the model to series and multileg applications. As shown in Fig. 14, in series applications, Si-based DSRDs [33] exhibit a linear voltage scaling relationship of $F(Q) = F(1) \times Q$ (F denotes the value of either *dV/dt* or V_{peak}) when the number of series-connected DSRDs (Q) is fewer than 12. As the number increases further, the incremental voltage gain begins to diminish and eventually saturates, primarily due to the non-negligible resistance of the series-connected DSRDs. For SiC-based DSRDs [32], such ideal scaling is not observed, mainly due to packaging constraints. In

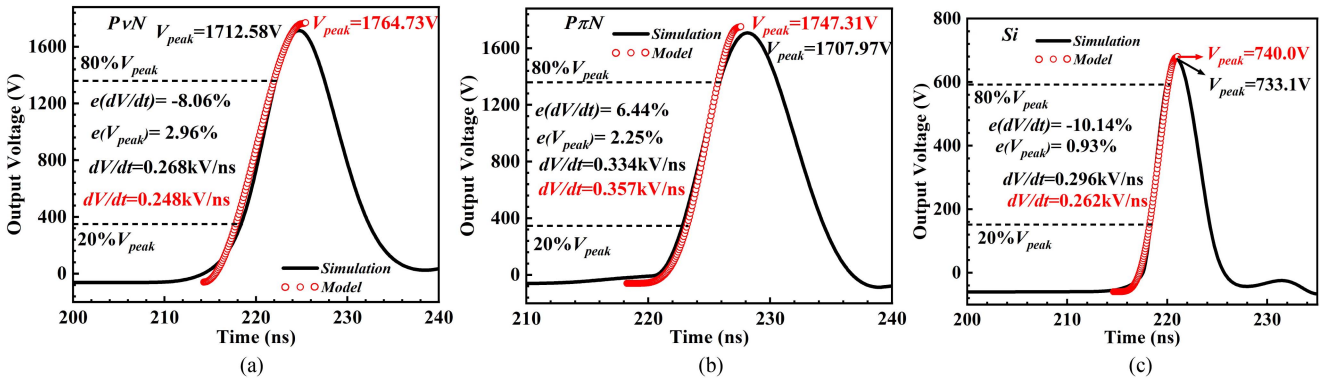

Fig. 13. Simulation curve and model fitting with varying the structure of DSRDs. (a) SiC *P-ν-N*. (b) SiC *P-π-N*. (c) Si *P-π-ν-N*.

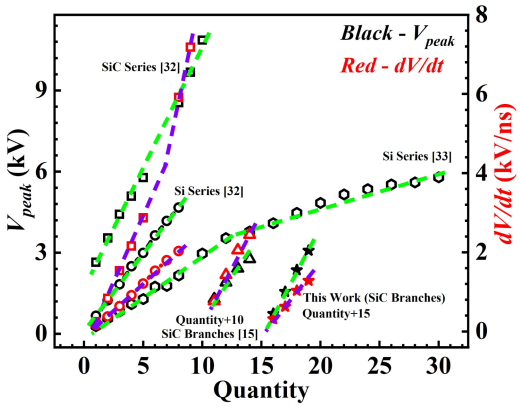

Fig. 14. Relationship between the quantity of DSRDs used in series or multileg configurations and the resulting V_{peak} and *dV/dt*. Black denotes the V_{peak}, and red denotes *dV/dt*. The lines are for visual guidance.

this case, the voltage increment per additional device remains constant, i.e., $F(Q) = F(1) + (Q-1) \times \Delta F$. This linear scaling behavior is consistent with the stacked Si-based DSRD series configuration reported in [32], which demonstrated a near-ideal relationship. This deviation from the ideal linear relationship is likely attributed to the excessive parasitic inductance introduced by the packaging of HV SiC DSRDs. Therefore, the proposed model is applicable to series-connected Si-based DSRDs. Moreover, with further investigation into the influence of packaging inductance in series configurations, the model can be extended to SiC-based DSRD applications.

For multileg applications, Fig. 14 presents the results of two different multileg pulse generator circuits reported in [15] and this work, both of which share the same fundamental operating principle as the single-switch pulse circuit shown in Fig. 2(a). The results indicate that, for pulse generators with a small number of legs (leg < 4), the pulse characteristics exhibit an ideal linear relationship with the number of legs, thereby validating the applicability of the proposed model to multileg configurations with limited branch count. Naturally, as the number of branches increases, the associated rise in parasitic inductance may lead to saturation effects similar to those observed in series-connected applications. Therefore, with further investigation, the model proposed in this work may be extended to fully support the design and analysis of multileg pulse generator systems.

In summary, the proposed model is structurally applicable to SiC DSRDs with *P-ν-N*, *P-π-N*, and *P-π-ν-N* epitaxial structures, as well as to Si DSRDs with *P-ν-N* and *P-π-ν-N* structures. It also supports series-connected applications. From a circuit perspective, the model is applicable to single-switch pulse generator topologies ranging from single-leg to multileg configurations.

VI. Conclusion

Taking the dual-supply DSRDs pulse generator as an example, the rapid current interruption phase was derived by the turn-OFF of the MOSFET within the drive circuit under high-current conditions. Building upon this rapid current interruption phase, a pulse output model was developed that simultaneously incorporates both drive circuit parameters and SiC DSRDs device structural parameters. The proposed model can be utilized for the design of drive circuits, thereby enhancing the design efficiency of pulse generators based on DSRDs.

The parameters of the pulse output curve include pre-pulse amplitude, pulse duration, pulse delay, and maximum voltage rise rate. The proposed model exhibits less than 10% relative error when predicting key output pulse characteristics, such as pulse duration, peak voltage, and *dV/dt*, compared to both experimental and simulation results. However, the relative error for the prepulse amplitude is approximately 35% compared with the experimental result, due to parasitic inductances introduced in the measurement setup. Based on the proposed model, it was deduced that the injected charge is a critical parameter influencing the pulse output characteristics. Building upon this discovery, a rapid method for determining whether the drive circuit operates under optimal conditions was introduced. Furthermore, utilizing the proposed method, a framework for calculating drive circuit parameters was proposed, thereby enhancing the efficiency of drive circuit design. The applicability of the proposed model is discussed. It is suitable for SiC DSRDs with *P-π-ν-N*, *P-π-N*, and *P-ν-N* epitaxial structures, as well as Si DSRDs with *P-π-ν-n* and *P-ν-N* epitaxial structures. Furthermore, the model is

also applicable to series-connected configurations and multileg single-switch pulse generator topologies.

In this article, we present a physical model to compute the performance parameters of DSRDs pulses. The findings provide a broader and deeper understanding of SiC DSRDs applications and reveal the key parameters for drive circuits and DSRDs device design. Importantly, the proposed model is applicable for designing drive circuits tailored to specified target output pulses, thereby enhancing the design efficiency of DSRDs drive circuits and facilitating the application of DSRDs pulse generators.

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