Parameter Design and Predictive Antiwindup of Double Closed-Loop Control for DC Three-Stage Generator in More Electric Aircraft

Chengxiang Zhang, Xinbo Ruan, *Fellow, IEEE*, Yuying He, *Member, IEEE*, Haiying Meng, Donghua Wu, and Yi Wang

***Abstract*—The DC three-stage generator (TSG) has been widely adopted as the main power source in aviation high-voltage dc power systems. With the evolution toward more electric aircraft, it is crucial to regulate the output voltage of the DC-TSG under complex operating conditions with numerous nonlinear loads. This article proposes a step-by-step parameter design method for double closed-loop control of the DC-TSG system. Based on the system model, PI controller characteristics, and dynamic and stability requirements, a feasible region is identified for key parameters, enabling fast and easy tuning while ensuring near-optimal control performance. Moreover, a predictive antiwindup method is proposed to eliminate integrator windup in PI controllers used in double closed-loop control systems. The proposed parameters design method does not require repeated trial-and-error, and the predictive antiwindup method is simple to implement. Finally, the effectiveness and advantages of the proposed methods are verified by simulations and experiments.**

***Index Terms*—Antiwindup, double closed-loop control, integrator windup, more electric aircraft (MEA), three-stage generator (TSG).**

NOMENCLATURE

d	PWM duty cycle signal.
$f_{\rm ci}, f_{\rm cv}$	Cutoff frequency of loop gains for each loop.
$K_{\rm cip}, \omega_{\rm ciz}, K_{\rm cii}$	Proportional gain, corner frequency, and integral gain of the current loop PI controller.
$K_{\rm cvp}, \omega_{\rm cvz}, K_{\rm cvi}$	Proportional gain, corner frequency, and integral gain of the voltage loop PI controller.
$\rm PM_{ci\_req}, PM_{cv\_req}$	Phase margin of the loop gain for each loop.
$T_{\rm cif}, T_{\rm cvf}$	Time constant of the first-order low-pass filter for each loop.
$v_{\rm ef}, i_{\rm ef}$	Regulated field voltage and current of DC-TSG.
$v_{\rm o}, i_{\rm o}$	DC output voltage and current of DC-TSG.
$v_{\rm o\_sp}, i_{\rm ef\_sp}$	Setpoint signal of $v_{\rm o}$ and $i_{\rm o}$.
$V_{\rm dc\_PE}$	Chopper input voltage.
$y_{\rm sp}, y, u_{\rm act}, u$	Setpoint, plant output, plant input, and controller output.
$\omega_{\rm ME}, \omega_{\rm MG}$	Electrical angular frequency of the ME and MG.
$\phi_{\rm cim}, \phi_{\rm cvm}$	Maximal phase of each controller.

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I. INTRODUCTION

OVER the past decades, three-stage generators (TSG) have been widely used as the main power source in aircraft [1], such as the variable frequency AC (VFAC) generation system in Airbus A380 [2] and Boeing 787 [3], and the high-voltage DC (HVDC) generation system in F-35 [4]. Different from that in the VFAC system, the speed and pole pairs of the TSG in HVDC system are not limited by the generation frequency, leading to high power density. Moreover, the HVDC system can easily realize multichannel paralleled power supply, and has no need for reactive power compensation and power factor correction. Therefore, the TSG in HVDC system, which is also termed the DC-TSG [5], [6], has become the research spot.

The output voltage of the DC-TSG is regulated through the generator control unit (GCU). The design of GCU for DC-TSG faces several challenges, mainly including: 1) compared with the traditional synchronous generator (SG), TSG features a three-stage coupling structure with multiple inertia links, and its output has an additional large inertia link such as bridge rectifier with capacitor for HVDC system; 2) compared to constant frequency generation system, the generators in HVDC system operate at wide variable frequency, resulting in significant changes in operating points and dynamics; and 3) with the development of aircraft toward more electric aircraft (MEA), nonlinear loads, such as constant power loads, are increased, which makes the operating conditions more complex and thus leads to increased

risk of system instability [7], [8], [9], [10]. So, it is essential to study the design of the GCU to ensure desired system performance and adequate stability.

In the early stages, the GCU adopted a single voltage loop [11], which is quite simple and easy to implement. However, its dynamic performance and disturbance rejection capability are not satisfactory, especially for the TSG in MEA. Then, double closed-loop control is used for the TSG in VFAC power system [12], [13], [14] and DC-TSG in HVDC power system [15], [16], [17], where the outer loop is responsible for regulating the output voltage and the inner loop is used to control the field current for the exciter. In addition, for the DC-TSG, a feedforward loop is added to compensate for the load disturbance for achieving a better transient response [15], [16], [17]. Moreover, a nonlinear PI controller is employed in the outer voltage loop [17]. The proportional gain varies with the generator speed, ensuring good dynamic performance even under high-speed conditions and during large load unloading. However, the controller parameters in [15], [16], and [17] are designed and tuned using empirical methods, such as the widely adopted Ziegler–Nichols method [18]. While this type of approach is appealing because it does not require a detailed model of the system, it comes at the cost of relying heavily on experimental trial-and-error procedures. As a result, it is often time-consuming and may lead to suboptimal control performance, particularly in complex or highly dynamic systems.

The aforementioned controllers are primarily based on a PI controller. When the system undergoes significant operating condition changes, the PI controller's performance may be adversely affected by actuator saturation, such as the pulsewidth modulation (PWM) duty cycle constraints and the output protection thresholds [19], [20]. As the controller output reaches the actuator's limit, the actuator output remains fixed at the limit, causing the controller to lose its regulating ability. As a result, the error will accumulate continuously through the integrator of the PI controller, causing the integral value to become abnormally large. This phenomenon is known as integrator windup, which leads to significant overshoot, slow regulation, and even system instability [21], [22]. To solve this problem, various antiwindup schemes are proposed, which can be mainly classified into two categories, namely, conditional integration [23], [24] and back-calculation [25], [26]. Generally, these antiwindup schemes are effective for single-loop control. However, in double closed-loop control, integrator windup is caused not only by each individual loop but also by a cascade-type integrator windup, where saturation in the inner loop leads to integrator windup in the outer loop. This cascade-type integrator windup problem is difficult to eliminate by the aforementioned two antiwindup schemes.

In this article, a step-by-step parameter design method of the double closed-loop control for the DC-TSG is proposed based on accurate models, which avoids trial-and-error, simplifies the tuning process, and facilitates achieving optimal control performance. Then, a predictive antiwindup scheme for double closed-loop control is proposed, which can not only eliminate the windup problem caused by each individual loop but also resolve the cascade-type integrator windup problem, and it is simple and easy to implement.

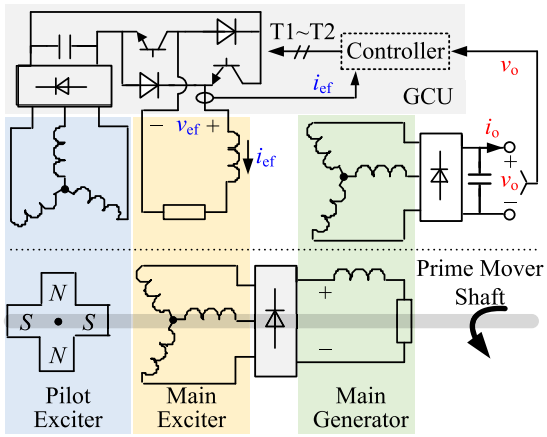

Fig. 1. Structure of the DC-TSG.

The rest of this article is organized as follows. The structure and basic principles of DC-TSG are introduced in Section II. In Section III, the mathematical model of the DC-TSG is presented and its basic characteristics are analyzed, followed by the design of the corresponding control structure. On this basis, a step-by-step parameter design method for the inner and outer loops is provided in Section IV. In Section V, the causes of integrator windup are analyzed, and the principles of traditional antiwindup schemes are discussed, and their limitations in double closed-loop control are pointed out. Then, a predictive antiwindup scheme is proposed. The above-mentioned theoretical analyses are verified by the simulation model and the hardware-in-the-loop (HIL) test in Section VI. Finally, Section VII concludes this article.

II. Structure and Principles of DC-TSG

Fig. 1 shows the configuration of the DC-TSG. Each stage consists of an SG and a diode rectifier. The three SGs, i.e., the pilot exciter (PE), the main exciter (ME), and the main generator (MG), are connected in the same transmission shaft of the engine. The PE is a permanent magnet SG and serves as the power supply for primary excitation. The armature winding of the PE is mounted on the stator and connected to the diode rectifier to feed the two-quadrant dc chopper in the GCU. This chopper delivers the regulated field current i_{ef} to the ME, which is a wound field SG similar to the MG. The armature winding of the ME is mounted on the rotor and supplies the MG's field current through the shaft-mounted diode rectifier (rotating rectifier). Finally, the stator three-phase output power/voltage of the MG is converted to dc output by a diode rectifier.

The GCU regulates the ME's field current i_{ef} by modulating the duty cycle of the switching device in the chopper, and then regulates the MG's field current to maintain the terminal voltage v_o at 270 V and de-energize the dc field of ME during overload and short-circuit faults. The dc voltage v_o and field current i_{ef} are continuously measured and fed back to the controller for closed-loop control.

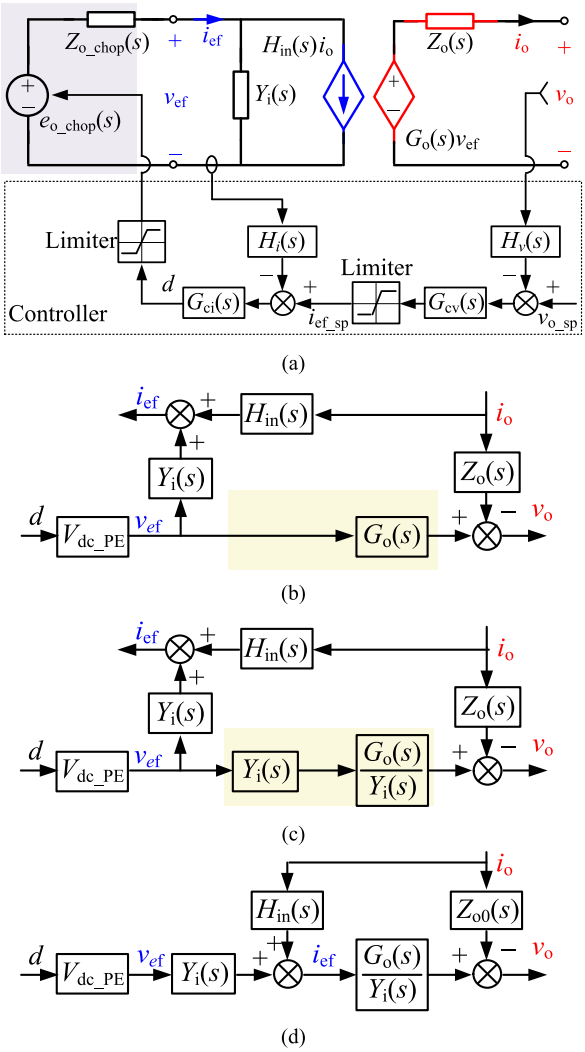

Fig. 2. Equivalent model of DC-TSG. (a) Two-port circuit model with control scheme. (b)–(d) Block diagram model.

It is noted that during normal generator operation, the chopper is controlled such that one switching device remains ON, while the other operates in PWM mode, establishing Buck converter operation. When a rapid reduction in the ME field current is required, both switching devices are turned OFF simultaneously, forcing the field winding current to decay rapidly under the negative chopper input voltage to meet dynamic response requirements.

III. Mathematical Model of the DC-TSG

A modular modeling technique for the DC-TSG is presented in [6], where each component is modeled as a linearized small-signal two-port network, and the overall small-signal model is constructed by integrating the two-port models of individual components. Furthermore, the entire DC-TSG is represented as a singly terminated two-port system, as illustrated in Fig. 2(a).

Fig. 2(a) shows the small-signal two-port network equivalent circuit and the control scheme of DC-TSG. In the equivalent circuit, the ports are the field port of the ME and the dc output port of the MG's rectifier. v_{ef} and i_{ef} are the field port voltage and current, respectively, corresponding to the same quantities labeled in Fig. 1, while v_o and i_o are the voltage and current at the dc output port of the MG's rectifier illustrated in Fig. 1. The internal representation of the field port employs a Norton equivalent circuit, where $Y_i(s)$ is the port admittance defined as the ratio of the i_{ef} to the v_{ef} under no-load condition ($i_o = 0$), and $H_{in}(s)$ represents the ratio of the i_{ef} to the i_o with the field winding shorted ($v_{ef} = 0$). The internal representation of the dc output port uses a Thevenin equivalent circuit, where $Z_o(s)$ is the port impedance defined as the ratio of the v_o to the i_o with the field winding shorted ($v_{ef} = 0$), and $G_o(s)$ is the transfer function from v_{ef} to v_o under no-load condition ($i_o = 0$). Appendix B provides the derivation of the four transfer functions characterizing the two-port equivalent circuit. In addition, the PE and chopper connected to the field port are modeled with a Thevenin equivalent circuit, characterized by a port impedance $Z_{o\_chop}(s)$ and an open-circuit voltage $e_{0\_chop}(s)$. According to [6], it is known that $e_{0\_chop} \approx dV_{dc\_PE}$ and Z_{o_chop} is very small and negligible, i.e., $v_{ef} \approx dV_{dc\_PE}$. V_{dc_PE} is the steady-state chopper input voltage.

In the controller, $H_i(s)$ and $H_v(s)$ are the sampling gains of the ME field current i_{ef} and dc output voltage v_o, respectively. $G_{ci}(s)$ and $G_{cv}(s)$ are the transfer functions of the ME field current regulator and the dc output voltage regulator, respectively. v_o is sensed and compared with its setpoint value v_{o_sp}, and the error is fed into the voltage regulator. The output of the voltage regulator serves as the reference i_{ef_sp} for the current regulator and is compared with the measured field current i_{ef}, and the current error is then sent to the current regulator to generate a duty cycle signal, which is converted via PWM into gate drive signals for controlling the switching devices in the chopper.

Fig. 2(b) shows the corresponding block diagram model of the two-port equivalent circuit. $G_o(s)$ is split into $G_o(s)/Y_i(s)$ and $Y_i(s)$, as shown in Fig. 2(c). Then, i_{ef} is moved between $G_o(s)/Y_i(s)$ and $Y_i(s)$, and the final block diagram is obtained, as shown in Fig. 2(d). As seen, there are two branches from i_o to v_o, and their sum should be equal to $Z_o(s)$ in Fig. 2(c). Thus, $Z_{o0}(s)$ in Fig. 2(d), which is the dc output port impedance when $i_{ef} = 0$, can be derived as

$$Z_{o0}(s) = \left.\frac{v_o}{i_o}\right|_{i_{ef}=0} = Z_o(s) + \frac{G_o(s)\,H_{in}(s)}{Y_i(s)}. \quad (1)$$

According to Fig. 2(a) and (d), the double closed-loop control block diagram of DC-TSG can be obtained, as shown in Fig. 3. The ME field current control loop is the inner loop, shown in the shaded area, while the dc output voltage control loop is the outer loop. The output of the outer loop serves as the reference for the inner loop. The output of the inner loop controller is the duty cycle signal.

It should be noted that there are limits on the outputs of both controllers. The limit of the outer loop controller is used for excitation current protection, while the limit of the inner loop controller is due to the fact that the PWM duty cycle signal can only range within [0, 1]. When designing the controller parameters, the limiters are neglected.

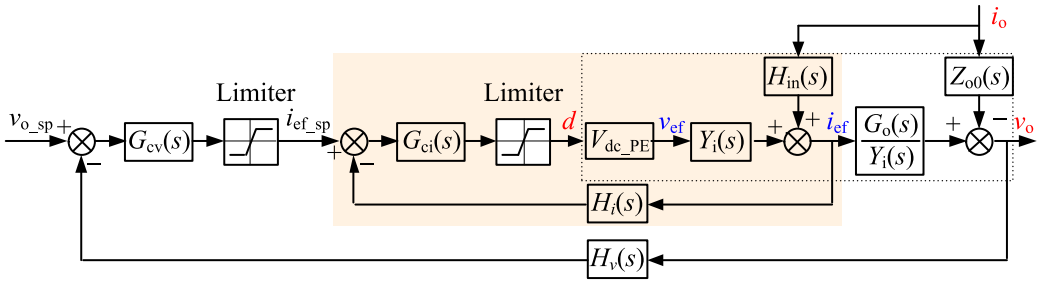

Fig. 3. Block diagram of double closed-loop control for DC-TSG.

IV. Parameter Design of the Controller for DC-TSG

A. Parameters Design of the ME Field Current Loop

The block diagram of the inner loop control is shown in the shaded area of Fig. 3. The relationship between the field current i_{ef}, its reference i_{ef_sp}, and output current i_o can be derived as

$$i_{ef}(s) = \Phi_{ci}(s)\, i_{ef\_sp}(s) + \Phi_{di}(s)\, i_o(s) \tag{2}$$

where $\Phi_{ci}(s)$and $\Phi_{di}(s)$ are expressed as

$$\Phi_{ci}(s) = \left.\frac{i_{ef}}{i_{ef\_sp}}\right|_{i_o=0} = \frac{1}{H_i(s)}\frac{T_{ci}(s)}{1+T_{ci}(s)}$$
$$\Phi_{di}(s) = \left.\frac{i_{ef}}{i_o}\right|_{i_{ef\_sp}=0} = \frac{H_{in}(s)}{1+T_{ci}(s)} \tag{3}$$

where $T_{ci}(s)$ is the inner loop gain and is expressed as

$$T_{ci}(s) = H_i(s)\, G_{ci}(s)\, Y_i(s)\, V_{dc\_PE}. \tag{4}$$

According to (2), i_{ef} comprises two components: one related to i_{ef_sp}, and the other associated with i_o, which serves as a disturbance. For controller parameter design, the disturbance component can be neglected.

$H_i(s)$ includes a notch filter to eliminate the sixth harmonic component in the field current, expressed as

$$H_i(s) = \frac{s^2 + (6\omega_{ME})^2}{s^2 + 2\times 0.707\times 6\omega_{ME}s + (6\omega_{ME})^2} \tag{5}$$

where ω_{ME} is the electrical angular frequency of the ME.

PI compensator is adopted as the inner-loop field current regulator, and its transfer function $G_{ciPI}(s)$ is expressed as

$$G_{ciPI}(s) = K_{cip}\left(1 + \frac{\omega_{ciz}}{s}\right) \tag{6}$$

where K_{cip} is the proportional gain and ω_{ciz} is the corner frequency of the PI compensator.

To better eliminate the influence of high-frequency harmonics and noise on the control system, a first-order low-pass filter is added to the PI compensator, expressed as

$$G_{cif}(s) = \frac{1}{1+T_{cif}s} \tag{7}$$

where T_{cif} is the time constant of the filter. Thus, the transfer function of the current inner loop controller $G_{ci}(s)$ is

$$G_{ci}(s) = G_{ciPI}(s)\, G_{cif}(s). \tag{8}$$

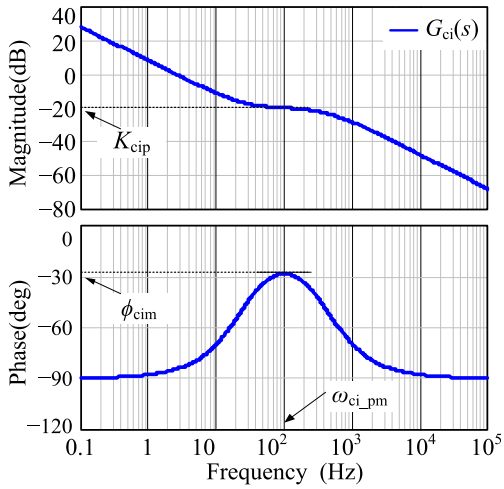

Fig. 4. Bode plot of $G_{ci}(s)$.

The Bode plot of $G_{ci}(s)$ is shown in Fig. 4. As seen, in the low-frequency and high-frequency ranges, the phase of the controller remains at $-90°$, while in the midfrequency range, the controller's phase is elevated above $-90°$ due to the compensating effect of a zero-pole pair in the controller. The maximum phase ϕ_{cim} and its corresponding angular frequency ω_{ci_pm} can be expressed as

$$\begin{cases} \omega_{ci\_pm} = \sqrt{\omega_{ciz}/T_{cif}} \\ \phi_{cim} = -\arccos\frac{1-\omega_{ciz}T_{cif}}{1+\omega_{ciz}T_{cif}} < 0°. \end{cases} \tag{9}$$

At the loop cutoff frequency f_{ci}, the magnitude of the loop gain is unity. According to (4)–(8), we have

$$|T_{ci}(j2\pi f_{ci})| = V_{dc\_PE}K_{cip}\left|\frac{1+\omega_{ciz}/(j2\pi f_{ci})}{1+j2\pi f_{ci}T_{cif}}\right| \times |H_i(j2\pi f_{ci})\, Y_i(j2\pi f_{ci})| = 1. \tag{10}$$

According to (10), K_{cip} can be derived as

$$K_{cip} = \frac{|1+j2\pi f_{ci}T_{cif}|}{V_{dc\_PE}\,|1+\omega_{ciz}/(j2\pi f_{ci})|\,|H_i(j2\pi f_{ci})\, Y_i(j2\pi f_{ci})|}. \tag{11}$$

If the required phase margin at f_{ci} is PM_{ci_req}, the following condition needs to be satisfied:

$$180° + \angle T_{ci}(j2\pi f_{ci}) \geq PM_{ci\_req}. \tag{12}$$

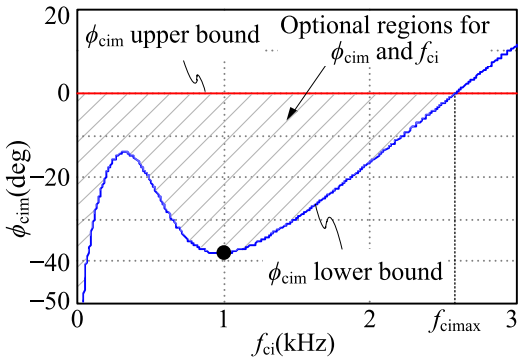

Fig. 5. Feasible regions of f_{ci} and ϕ_{cim} under current loop constraints.

Substituting (6) and (7) into (8), then substituting it and (5) into (4), and further substituting (4) into (12), while setting $\omega_{ci\_pm} = 2\pi f_{ci}$ to fully utilize the controller's phase, the range for ϕ_{cim} is expressed as

$$\phi_{cim} \geq \mathrm{PM}_{ci\_req} - \angle Y_i\left(j2\pi f_{ci}\right) - \angle H_i\left(j2\pi f_{ci}\right) - 180. \quad (13)$$

By substituting $\omega_{ci\_pm} = 2\pi f_{ci}$ into (9), ω_{ciz} and T_{cif} can be determined based on the selected ϕ_{cim} and f_{ci}, i.e.,

$$\begin{cases} \omega_{ciz} = 2\pi f_{ci}\sqrt{\frac{1-\cos\phi_{cim}}{1+\cos\phi_{cim}}} \\ T_{cif} = \frac{1}{2\pi f_{ci}}\sqrt{\frac{1-\cos\phi_{cim}}{1+\cos\phi_{cim}}}. \end{cases} \quad (14)$$

Based on the above-mentioned analysis, the parameter design procedure for the current controller is summarized as follows.

Step 1: Determine the required loop gain phase margin PM_{ci_req}, which typically is within [30°, 60°] to achieve a favorable dynamic response and ensure sufficient system robustness.

Step 2: Determine the upper and lower limits of ϕ_{cim} using (9) and (13), and plot the constraint curve between f_{ci} and ϕ_{cim}, as shown in Fig. 5, and the frequency corresponding to the intersection of the two constraint curves represents the highest cutoff frequency that satisfies the phase margin requirement.

Step 3: Select an appropriate cutoff frequency f_{ci} from the feasible region of f_{ci} and ϕ_{cim}. A higher f_{ci} leads to better dynamic performance. However, f_{ci} should be lower than 1/10 of the switching frequency to avoid the effect of high-frequency harmonics and switching noise.

Step 4: Select an appropriate ϕ_{cim} based on its upper and lower bound constraint curves. Generally, a higher ϕ_{cim} leads to a decrease in low-frequency loop gain and an increase in high-frequency loop gain, which hinders dc steady-state error elimination and high-frequency noise suppression. Therefore, it is recommended to choose ϕ_{cim} near its lower limit while meeting the phase margin requirements.

Step 5: Determine ω_{ciz} and T_{cif} according to (14). Then, determine K_{cip} through (11).

Step 6: Check the loop gain of the current loop to ensure that all the specifications are well satisfied.

B. Parameter Design of the Voltage Outer Loop

After the parameters of the current loop are designed, its closed-loop transfer function can be determined from (2) and (3). Using (2), the control block diagram shown in Fig. 3 can be transformed into the equivalent one shown in Fig. 6. As shown, when deriving the loop gain of the voltage loop, i_o can be regarded as the perturbation and set to zero. Thus, the voltage loop gain is derived as

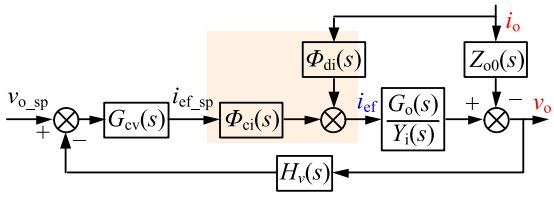

Fig. 6. Block diagram of the voltage outer loop for DC-TSG.

$$T_{cv}\left(s\right) = H_v\left(s\right) G_{cv}\left(s\right) G_v\left(s\right) \quad (15)$$

where $H_v(s)$ includes a sampling coefficient of 0.01 and a notch filter used to eliminate the sixth harmonic in the dc voltage. The expression of $H_v(s)$ is

$$H_v\left(s\right) = \frac{1}{100}\frac{s^2 + \left(6\omega_{MG}\right)^2}{s^2 + 2\times 0.707\times 6\omega_{MG}s + \left(6\omega_{MG}\right)^2} \quad (16)$$

where ω_{MG} is the electrical angular frequency of the MG.

Similar as the inner current loop, a PI compensator combined with a first-order low-pass filter is also adopted as the outer voltage loop controller, expressed as

$$G_{cv}\left(s\right) = K_{cvp}\left(1 + \frac{\omega_{cvz}}{s}\right)\frac{1}{1 + T_{cvf}s} \quad (17)$$

where K_{cvp} and ω_{cvz} are the proportional gain and the crossover frequency of the PI controller, respectively, and T_{cvf} is the time constant of the first-order low-pass filter. The maximum phase ϕ_{cvm} of the controller is located at ω_{cv_pm}. ω_{cv_pm} and ϕ_{cvm} are related to the controller parameters with reference to (9).

$G_v(s)$ in (15) is the transfer function from i_{ef_sp} to v_o under $i_o = 0$ and can be derived from Fig. 6, expressed as

$$G_v\left(s\right) = \left.\frac{v_o}{i_{ref\_sp}}\right|_{i_o=0} = \frac{\Phi_{ci}\left(s\right) G_o\left(s\right)}{Y_i\left(s\right)}. \quad (18)$$

At the cutoff frequency f_{cv} of the voltage control loop, the magnitude of the loop gain is 1. So, substituting (16)–(18) into (15) and setting $s = j2\pi f_{cv}$, we have

$$\left|T_{cv}\left(j2\pi f_{cv}\right)\right| = K_{cvp}\left|\frac{1 + \omega_{cvz}/\left(j2\pi f_{cv}\right)}{1 + j2\pi f_{cv}T_{cvf}}\right|\left|H_v\left(j2\pi f_{cv}\right) G_v\left(j2\pi f_{cv}\right)\right| = 1. \quad (19)$$

According to (19), K_{cvp} can be derived as

$$K_{cvp} = \frac{\left|1 + j2\pi f_{cv}T_{cvf}\right|}{\left|1 + \omega_{cvz}/\left(j2\pi f_{cv}\right)\right|\left|H_v\left(j2\pi f_{cv}\right) G_v\left(j2\pi f_{cv}\right)\right|}. \quad (20)$$

If the phase margin of the loop gain at the cutoff frequency f_{cv} is PM_{cv_req}, the following condition must be satisfied:

$$180 + \angle T_{cv}\left(j2\pi f_{cv}\right) \geq \mathrm{PM}_{cv\_req}. \quad (21)$$

By substituting (15) into (21), and setting the maximum phase position of the controller $\omega_{\text{cv\_pm}} = 2\pi f_{\text{cv}}$ to fully utilize the controller's phase to improve the phase margin, the range of values for ϕ_{cvm} can be obtained as

$$\phi_{\text{cvm}} \geq \text{PM}_{\text{cv\_req}} - \angle G_v\left(j2\pi f_{\text{cv}}\right) - \angle H_v\left(j2\pi f_{\text{cv}}\right) - 180. \tag{22}$$

The upper limit of ϕ_{cvm} can be determined by (9), while the lower limit of ϕ_{cvm} is given by (22). The cutoff frequency f_{cv} corresponding to the intersection of these two constraint curves represents the maximum allowable cutoff frequency for the voltage control loop.

Finally, the remaining controller parameters ω_{cvz} and T_{cvf} can be determined based on the selected values of ϕ_{cvm} and f_{cv}, coupled with $\omega_{\text{cv\_pm}} = 2\pi f_{\text{cv}}$, which are expressed as

$$\begin{cases} \omega_{\text{cv}z} = 2\pi f_{\text{cv}} \sqrt{\frac{1-\cos\phi_{\text{cvm}}}{1+\cos\phi_{\text{cvm}}}} \\ T_{\text{cvf}} = \frac{1}{2\pi f_{\text{cv}}} \sqrt{\frac{1-\cos\phi_{\text{cvm}}}{1+\cos\phi_{\text{cvm}}}}. \end{cases} \tag{23}$$

Based on the above analysis, the parameter design procedure for the voltage loop is similar to that for the current loop and is therefore omitted for brevity.

C. Parameters Design Example and Robustness Analysis

To verify the effectiveness of the proposed parameter design method, a design example is provided here. The generator parameters are listed in Appendix A.

1) Parameter Design of Current Loop: The phase margin $\text{PM}_{\text{ci\_req}} = 45°$ is set for the current loop. According to (9) and (13), the constraint curve for the relationship between f_{ci} and ϕ_{cim} is plotted, as shown in Fig. 5. Within the constraint range in Fig. 5, the cutoff frequency is selected as 1/10 of the chopper switching frequency, i.e., $f_{\text{ci}} = 1$ kHz. Then, based on (13), the corresponding range of ϕ_{cim} values is calculated, and the lower limit is chosen, resulting in $\phi_{\text{cim}} = -37.97°$. Finally, all controller parameters are calculated based on (14) and (11), yielding $\omega_{\text{ciz}} = 2161.44$ rad/s and $T_{\text{cif}} = 54.75$ μs, $K_{\text{cip}} = 11.578$. Once all parameters are determined, the current loop gain can be plotted based on (4), as shown in Fig. 7. As observed, the bandwidth is 1 kHz and the phase margin is 45°.

2) Parameter Design of Voltage Loop: The phase margin $\text{PM}_{\text{cv\_req}} = 45°$ is set for the voltage loop. Based on (9) and (22), the constraint curve for the relationship between f_{cv} and ϕ_{cvm} can be plotted, as shown in Fig. 8, and the cutoff frequency is selected as 1/5 of the inner loop bandwidth, i.e., $f_{\text{cv}} = 200$ Hz. Then, based on (22), the range of ϕ_{cvm} is calculated, and the lower limit is chosen, resulting in $\phi_{\text{cvm}} = -41.2°$, which corresponds to point A in Fig. 8. Finally, all the controller parameters are calculated based on (23) and (20), yielding $\omega_{\text{cvz}} = 472.303$ rad/s, $T_{\text{cvf}} = 0.3$ ms, and $K_{\text{cvp}} = 134.98$. Then, the voltage loop gain can be plotted based on (15), as shown in Fig. 7. As seen, the bandwidth is 200 Hz and the phase margin is 45°.

3) Robustness Evaluation Against Parameter Variations: The proposed parameter design method is based on an accurate DC-TSG model. However, parameter variations inevitably exist in practical engineering applications, and thus, the robustness

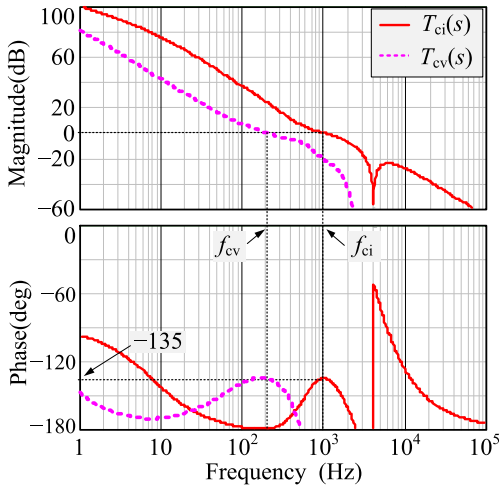

Fig. 7. Bode diagram of the current loop gain $T_{\text{ci}}(s)$ and voltage loop gain $T_{\text{cv}}(s)$.

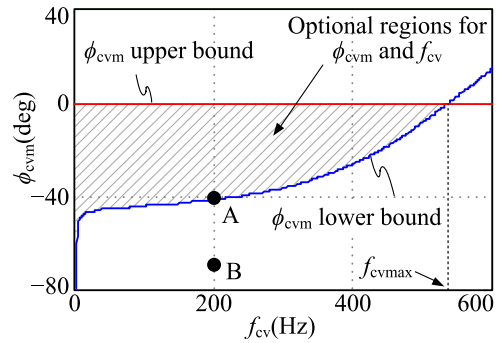

Fig. 8. Feasible regions of f_{cv} and ϕ_{cvm} under voltage loop constraints.

of the proposed method against such variations should also be carefully evaluated. According to the analysis presented in [6], the most influential component in the DC-TSG model is the MG. Therefore, this section focuses on assessing how variations in MG parameters affect the control performance of the system designed using the proposed method.

To evaluate the system's robustness to parameter variations, the Bode diagrams of the voltage loop gain under different MG parameter variations are plotted, as shown in Fig. 9. Fig. 9(a) shows the loop gain variation when all MG winding resistances vary simultaneously by ±20% around their nominal values. It can be observed that the bandwidth deviation is within 3 Hz, and the phase margin variation is within 1°. Fig. 9(b) illustrates the loop gain variation when all MG winding inductances vary by ±20%. The bandwidth variation is around 50 Hz, while the phase margin changes by no more than 5°. Fig. 9(c) presents the loop gain variation when the dc-link filter capacitor changes by ±20%. The bandwidth variation remains within 5 Hz, and the phase margin deviation does not exceed 2°.

These results demonstrate that the system designed with the proposed method exhibits strong robustness against practical parameter variations.

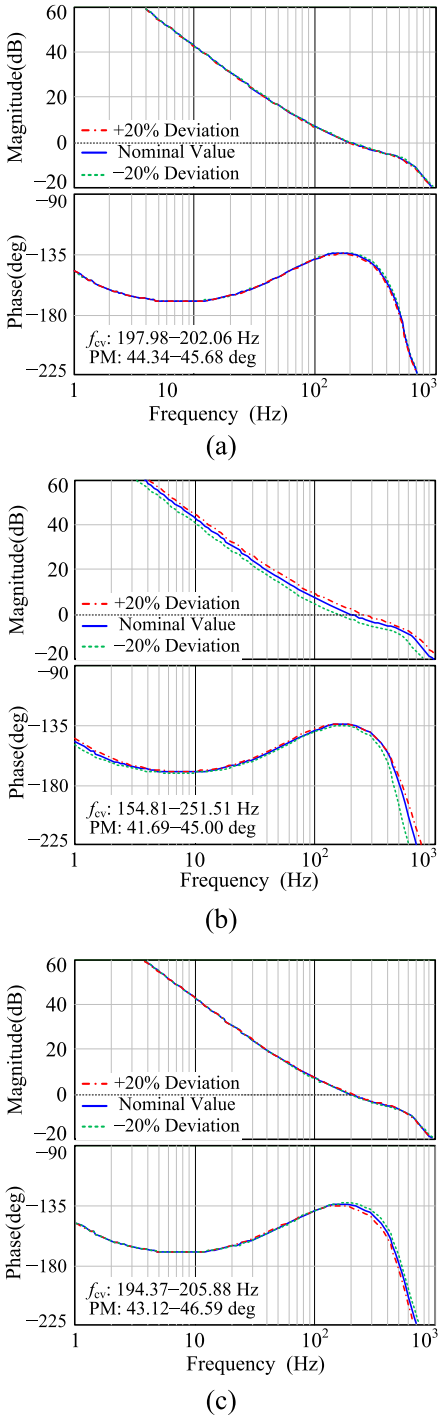

Fig. 9. Bode diagram of the voltage loop gain $T_{cv}(s)$ under ±20% variations of MG parameters. (a) MG winding resistances. (b) MG winding inductances. (c) DC-link filter capacitor.

As can be observed in Fig. 9, the variations in inductance have the most significant impact on control performance. So, a time-domain simulation using a switching generator model in Simulink is conducted to further evaluate the robustness of the proposed design method against inductance variations. Fig. 10 presents the simulation results under a load step between full load and 10% load. As can be seen, the dc output voltage of the generator remains stable in all cases, with only slight differences

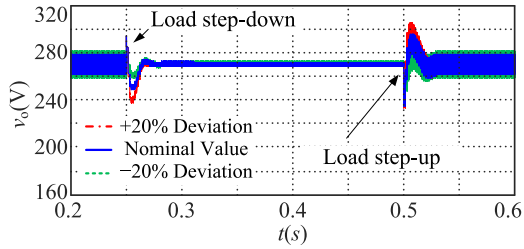

Fig. 10. Simulation waveforms of DC output voltage v_o under variations in MG winding inductance.

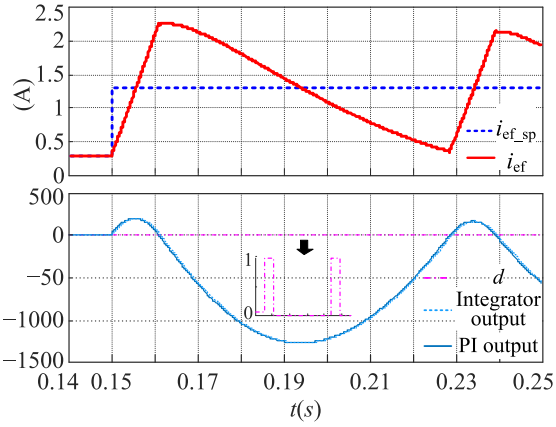

Fig. 11. Simulation waveforms of current loop without antiwindup.

during the transient response. These results confirm the strong robustness of the proposed method, which is consistent with the previous theoretical analysis.

V. Antiwindup Design for PI Controller

A. Integrator Windup Phenomenon

To provide a clearer insight into the integrator windup phenomenon, a simulation is conducted on the current control block diagram shown in Fig. 3 with the current controller parameters designed in Section IV-C, and the simulation results are shown in Fig. 11. At 0.15 s, the field current reference has a step-up change. As seen, at the beginning of the transient, the controller's output signal rapidly increases, attempting to regulate the field current to its reference. However, the duty cycle signal is limited to the maximum value of 1, and the field current increases slowly. The error between the reference and the actual field current leads to continuous accumulation in the integrator component of the controller, which results in integrator windup and causes the controller's output signal to increase progressively. When the field current eventually reaches its reference, the controller's output exceeds the duty cycle upper limit of 1 due to integrator windup. Consequently, the field current continues to increase, causing the error between the reference and the actual one become negative, and the controller's output begins to decline. Nevertheless, due to the large accumulation of the integrator, the process of exiting integrator windup is relatively slow. By the time the controller fully recovers from saturation, the field current has already far exceeded its reference. To eliminate this significant negative

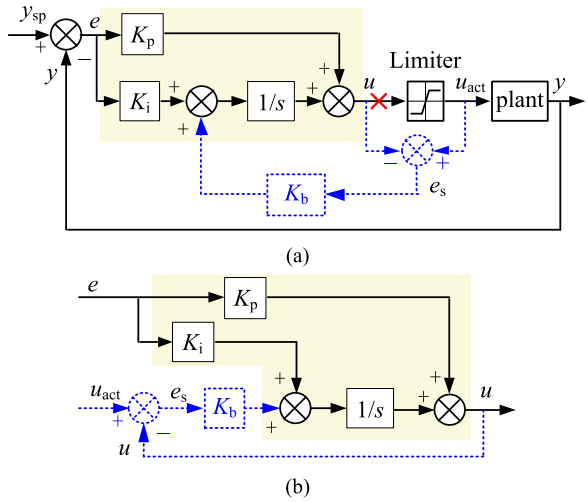

Fig. 12. Block diagram of antiwindup with back-calculation. (a) Original control structure. (b) Equivalent structure under actuator saturation.

error, the controller's output signal continues to decrease rapidly. However, the minimum duty cycle is limited to 0. This prevents the field current from quickly returning to its reference, causing the controller to enter negative integrator windup. When the field current eventually drops to the reference, the controller is already in deep negative integrator windup, and the duty cycle remains at 0, causing the field current to continue decreasing. As a result, the error turns positive, and the value of the integrator begins to rise. When the controller fully exits saturation, the field current is far below the reference. Repeatedly, this results in a periodic oscillation, preventing effective control.

B. Traditional Antiwindup Schemes

Currently, the widely used antiwindup techniques are the back-calculation and the conditional integration.

1) Back-Calculation Method: Fig. 12(a) shows the block diagram of the back-calculation, where y_{sp}, y, u_{act}, and u are the setpoint, plant output, plant input, and controller output, respectively. Here, the shaded area represents the PI controller, and the dashed line represents the back-calculation scheme. This scheme introduces an additional feedback path that utilizes the difference between the limiter's output u_{act} and its input control signal u as the error signal e_s. This error is then fed back to the input of the integrator through a gain $K_b = 1/T_t$, where T_t is the time constant of the back-calculation, referred to as the tracking time constant.

When no saturation occurs, $u_{act} = u$ and $e_s = 0$, and it has no effect on the normal operation. When the actuator output saturates, $u_{act} \neq u$, and e_s is not zero. Meanwhile, the limiter output u_{act} is constrained to a constant value, no longer influenced by u. As a result, the original feedback path is broken, causing the control system operate in an open-loop state. Then, the feedback loop of back-calculation for antiwindup starts to work, and the block diagram of the system can be equivalently represented, as shown in Fig. 12(b).

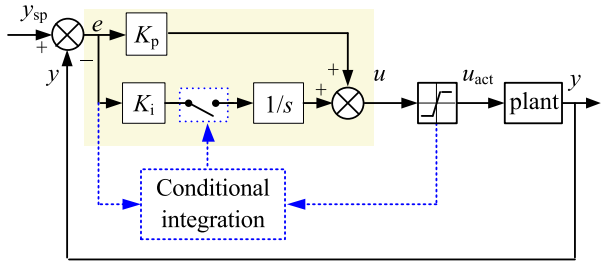

Fig. 13. Block diagram of antiwindup with conditional integration.

According to Fig. 12(b), the controller output u can be expressed in terms of u_{act} and the control error signal e, i.e.,

$$u = u_{act}\frac{1}{1+T_t s} + e\frac{K_i}{K_b}\frac{1+T_i s}{1+T_t s} \tag{24}$$

where $T_i = K_p/K_i$ is the integral time of the PI controller. K_p and K_i are the proportional gain and Integral gain of the PI controller.

As indicated by (24), the controller output signal u will tend toward a certain value at steady state, expressed as

$$u = u_{act} + e\frac{K_i}{K_b}. \tag{25}$$

This prevents integrator windup. The reset rate of the controller output is governed by the feedback gain, $K_b = 1/T_t$. T_t determines the integrator reset speed and should be as small as possible, with $T_t \leq T_i$ recommended [21], [27].

2) Conditional Integration: In this method, the integrator is only activated when certain conditions are detected; otherwise, it is switched OFF and the integral term is kept constant. The method is also called integrator clamping. Fig. 13 shows the block diagram of this method. By obtaining the relevant information from the controller, the integrator is judged to be turned ON or OFF according to the set conditions.

There are several different ways to set the conditions for inhibiting the integrator.

1) The output of the integrator is limited to a set value, and the integration process stops once the set value is reached.
2) The integration is stopped when the control error e exceeds the set value e_{set}, i.e., when $|e| > e_{set}$.
3) Integration stops when the controller saturates, i.e., $u_{act} \neq u$.
4) The integration is stopped when the controller saturates and the controller error has the same sign as the controller output, i.e., when $u_{act} \neq u$. and $e \cdot u > 0$.

The four aforementioned methods have been compared and analyzed in [21] and [27], and method 4 demonstrates the best performance.

Finally, the two antiwindup schemes are applied to the current controller designed in Section IV-C, and the current control block diagram shown in Fig. 3 is simulated. The simulation results, shown in Fig. 14, demonstrate that both the controller employing back-calculation and the controller utilizing conditional integration can well solve the integrator windup problem and achieve a more satisfactory control effect.

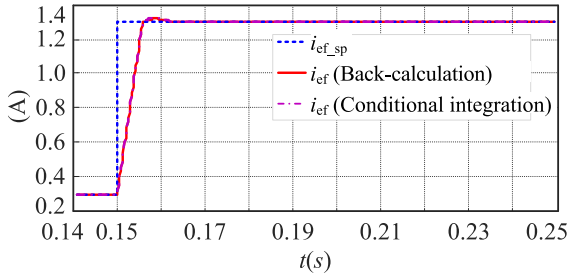

Fig. 14. Simulation waveforms of current loop with antiwindup.

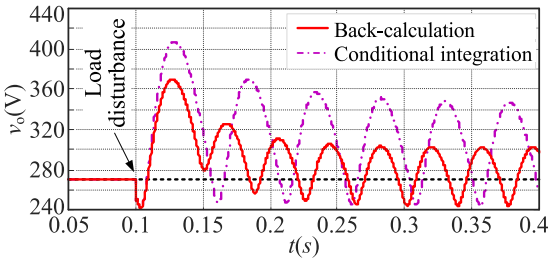

Fig. 15. Simulation waveform of the double loop with the traditional antiwindup scheme under load disturbance.

3) Limitations of the Traditional Antiwindup Schemes: Although the conventional antiwindup techniques perform well in single-loop control systems, they struggle to achieve the desired control performance in the double-loop control system. In such architectures, integrator windup in each control loop is not only caused by its local actuator saturation but also by the dynamic interaction between the inner and outer loops. This interaction leads to a cascade-type integrator windup, which cannot be effectively eliminated by traditional antiwindup schemes applied independently to each loop.

For example, when the system experiences a large disturbance and the dc output voltage v_o exhibits a significant deviation, assume that the initial transient error is positive. To eliminate the error, the controller output rapidly increases. Due to the high bandwidth and faster response of the inner loop, coupled with the duty cycle signal being inherently constrained within the range of [0, 1] by the PWM generator, the inner-loop controller output u_{ci} quickly reaches the duty cycle upper limit of 1 (let the inner-loop reference $i_{ef\_sp} = u_1$, which is also the outer-loop output signal u_{cv} at this moment). Under conventional antiwindup schemes, the inner loop detects saturation and its antiwindup scheme becomes active promptly, suppressing integrator windup. However, the outer-loop controller output u_{cv} has not yet reached its upper limit u_{max} (defined by current-limiting protection related to the inner-loop field current), and thus, its antiwindup remains inactive. The persistent error drives u_{cv} to keep increasing until reaching u_{max}, at which point the outer loop antiwindup finally activates while the inner loop command i_{ef_sp} also changes to u_{max}. This process reveals two critical issues: 1) During the time interval when u_{cv} increases from u_1 to u_{max}, the system remains saturated without timely intervention from the outer loop antiwindup; and 2) although the inner-loop antiwindup is active, the rising reference i_{ef_sp} (from u_1 to u_{max}) paradoxically deepens the inner-loop integrator windup and delays its recovery.

In summary, in a double-loop control structure, conventional antiwindup schemes that operate independently on each loop are insufficient to address the cascade-type integrator windup. Fig. 15 illustrates the performance of the traditional antiwindup techniques for a double-loop control system, under a load disturbance with an amplitude of 120 A, corresponding to the change from half-load to full-load. As shown, when the load current disturbance is large, the traditional antiwindup schemes fail to enable the system to rapidly regain steady state, and both exhibit oscillations.

C. Predictive Antiwindup Scheme for Double-Loop Control

As analyzed above, when the inner loop is saturated due to the duty cycle limit, the outer loop control should activate its antiwindup mechanism at the same time. However, it is not clear what the limit value of the outer-loop controller output should be when the inner loop is saturated. If only the field current limiting is used in the antiwindup scheme for the outer loop, as illustrated in Fig. 15, it does not effectively address the windup issue in the double-loop control system.

Therefore, a predictive antiwindup scheme for the double-loop control is proposed in this article. For a PI controller, there exists a well-defined mathematical relationship between the input command and desired output, which makes the saturation behavior of the inner-loop control output predictable.

The backward difference discretization for a PI controller is expressed as

$$u(k) = K_p\left(y_{sp}(k) - y(k)\right) + K_i T_s\left(y_{sp}(k) - y(k)\right) + u_I(k-1) \tag{26}$$

where u_I denotes the integrator output of the PI controller.

The relationship between the output and input of the limiter can be expressed as

$$u_{act} = \begin{cases} u_{min}, u < u_{min} \\ u, u_{min} \le u \le u_{max} \\ u_{max}, u > u_{max} \end{cases} \tag{27}$$

where u_{max} / u_{min} denote upper/lower limits, respectively.

According to (26) and (27), to ensure that the controller output u remains within $[u_{min}, u_{max}]$, the input command y_{sp} must be constrained within a specific range, i.e.,

$$\begin{cases} y_{sp\_max}(k) = \frac{u_{max} - u_I(k-1)}{K_p + K_i T_s} + y(k) \\ y_{sp\_min}(k) = \frac{u_{min} - u_I(k-1)}{K_p + K_i T_s} + y(k). \end{cases} \tag{28}$$

As seen from (26) and (28), when the setpoint value y_{sp} of the inner-loop PI controller is within the range $[y_{sp\_min}, y_{sp\_max}]$, saturation of the inner-loop controller can be avoided.

When this predictive antiwindup scheme is applied to the inner-loop controller, the final upper and lower limits of the outer-loop controller, u_{max_f} and u_{min_f}, are determined as

$$\begin{cases} u_{max\_f} = \min\{u_{max}, y_{sp\_max}\} \\ u_{min\_f} = \max\{u_{min}, y_{sp\_min}\}. \end{cases} \tag{29}$$

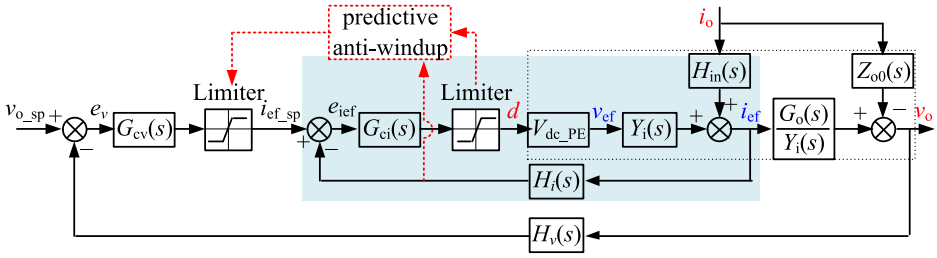

Fig. 16. Block diagram of double closed-loop control for DC-TSG with predictive antiwindup.

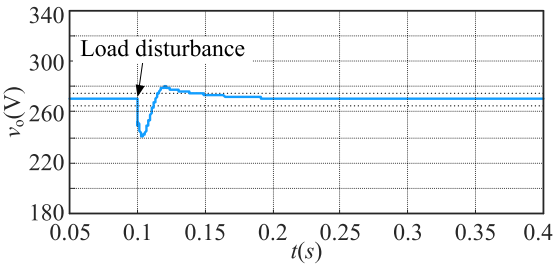

Fig. 17. Simulation waveform of double loop with predictive antiwindup scheme under load disturbance.

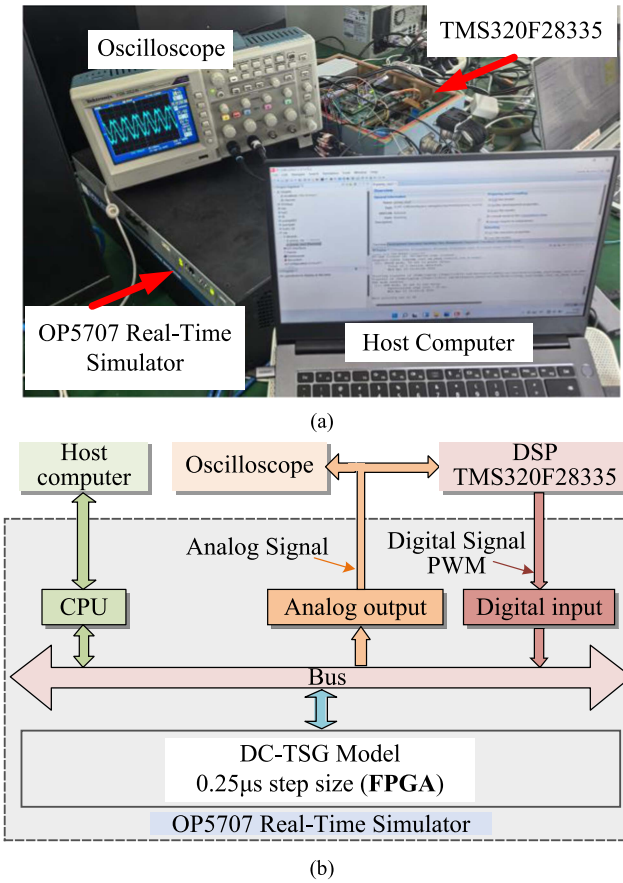

Fig. 18. HIL platform. (a) Platform photograph. (b) Configuration details.

With the limits determined by (29), it is sufficient to use a conventional antiwindup scheme for the outer-loop controller.

The schematic diagram of the predictive antiwindup is shown in Fig. 16. The method features a simple structure and is easy to implement. It not only effectively eliminates integrator windup in the inner loop but also enables accurate antiwindup for the outer loop.

The computational burden of implementing the three aforementioned antiwindup schemes can be intuitively compared: 1) for the back-calculation method, it introduces two additional additions/subtractions and one multiplication operation on top of the baseline control algorithm; 2) the conditional integration (method 4) needs one multiplication, two comparison operations, and one logical operation; and 3) the proposed predictive antiwindup approach, as indicated by (28) and (29), requires four additions/subtractions, two multiplications, and two comparisons. Although the proposed method involves slightly higher computational overhead, this increase remains negligible given the strong processing capabilities of modern digital controllers.

The proposed predictive antiwindup scheme is implemented in the double-loop control system, and the corresponding simulation results are presented in Fig. 17. Compared to Fig. 15, the predictive antiwindup scheme effectively addresses the windup issue in double-loop control systems compared to traditional antiwindup schemes.

The proposed predictive antiwindup method exhibits universal applicability, extendable to all linear controllers with integral terms, including PID controllers. The core idea of the predictive antiwindup strategy can be summarized as follows. First, based on the structure and output limitation of the inner-loop controller, its reference value at saturation is dynamically computed to determine the real-time output limit of the outer-loop controller as follows:

$$u = f_{\mathrm{Gc}}\left(y_{\mathrm{sp}} - y\right) \in [u_{\min}, u_{\max}]$$
$$\Rightarrow y_{\mathrm{sp}} = f_{\mathrm{Gc}}^{-1}\left(u\right) + y \in [y_{\mathrm{sp\_min}}, y_{\mathrm{sp\_max}}]. \quad (30)$$

Then, this real-time limitation is combined with the field current limit to determine the ultimate output limit for the outer loop according to (29).

VI. Verification

To verify the effectiveness of the proposed scheme, the experimental tests are conducted on the HIL platform shown in Fig. 18, with the generator parameters listed in Appendix A The HIL platform mainly comprises a digital signal processor (DSP) TMS320F28335, an RT-LAB real-time simulator from

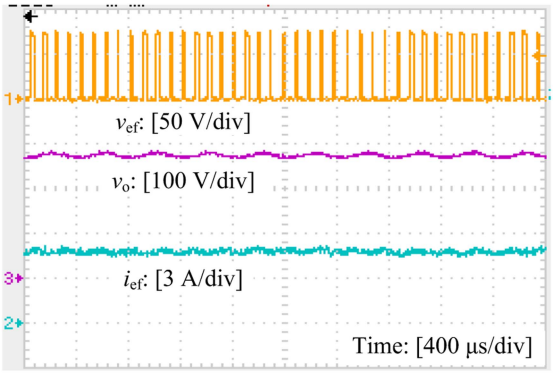

Fig. 19. Steady-state experimental results of the DC-TSG under 90-kW constant power load.

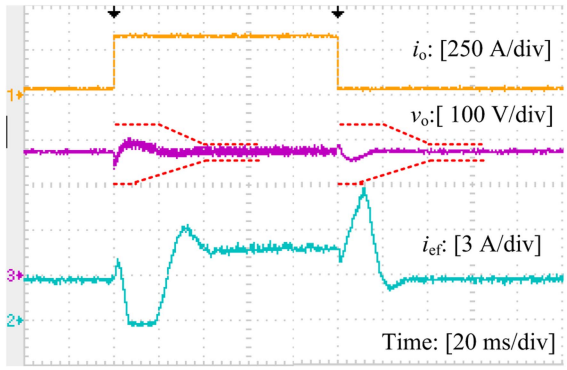

Fig. 20. Transient response of the DC-TSG when load power steps between 10% and 100% of the nominal value.

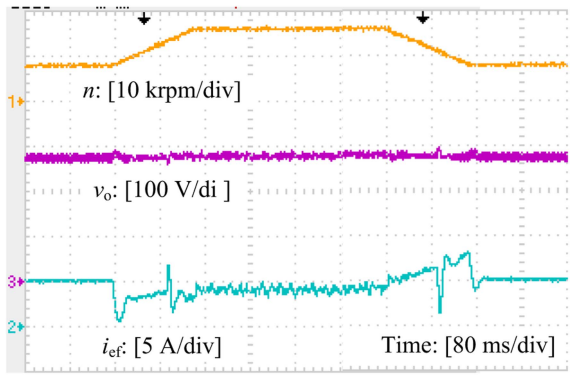

Fig. 21. Transient response of the DC-TSG with speed change between 8 and 16 kr/min.

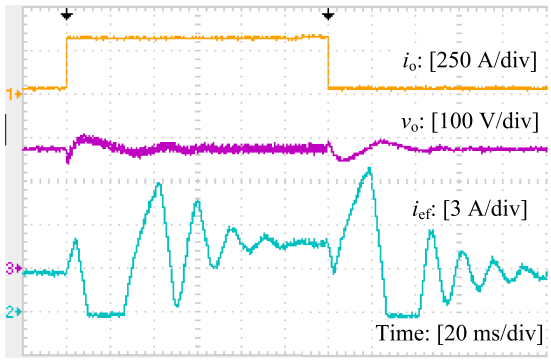

Fig. 22. Transient response of the DC-TSG at 15° phase margin for the outer loop when load power steps between 10% and 100% of the nominal value.

OPAT-RT Company, an oscilloscope for displaying signal waveform, and a computer as an operator interface. The controller in Fig. 1 is implemented on the DSP, while the detailed circuit model of the remaining generator system is executed on the RT-LAB real-time simulator. In the DSP implementation, the control algorithms operate at a frequency of 10 kHz, which is used for feedback signal sampling, PWM generation, and as the switching carrier frequency. The control parameters adopt the optimized values obtained in Section V-C. Specifically, for the current-loop PI controller, the parameters are $K_{\mathrm{cip}} = 11.578$ and $K_{\mathrm{cii}} = 2.502$; for the voltage controller, the parameters are $K_{\mathrm{cvp}} = 134.98$ and $K_{\mathrm{cvi}} = 6.375$.

A. *Steady-State and Dynamic Validation*

First, the steady-state and dynamic experimental tests are conducted based on the double-loop control parameters designed in Section IV-C. Fig. 19 shows the steady-state waveforms of the DC-TSG connected to a 90-kW constant power load, where the traces from top to bottom are the ME field voltage v_{ef}, the dc output voltage of the MG rectifier v_{o}, and the ME field current i_{ef}. As can be seen, the dc voltage is 270 V, with slight ripples caused by the sixth harmonic components (2.4 kHz) introduced by the diode rectifier. The ME field voltage v_{ef} exhibits a dc pulse form due to the chopper action, with a period corresponding to the switching frequency. The experimental results validate that the designed control parameters can ensure stable operation of the system when the DC-TSG is cascaded with a constant power load.

Fig. 20 shows the experimental waveforms of the DC-TSG when the load step changes between full load and 10% load. From top to bottom, the figure displays the load current i_{o}, the dc output voltage v_{o}, and the ME field current i_{ef}. As can be seen, the dc output voltage v_{o} quickly recovers to steady state after load changes, and it is within the transient voltage envelope given by both GJB 181B-2012 and MIL-STD-704F.

Fig. 21 shows the experimental waveforms when the generator speed varies between low speed (8000 r/min) and high speed (16 000 r/min). From top to bottom, the waveforms are the generator speed n, the dc output voltage v_{o}, and the ME field current i_{ef}. The speed change is completed within 0.15 s. As can be seen, with the designed control parameters, the generator output voltage is almost unaffected by the speed changes and can operate stably in all speed ranges. It should be noted that the generator speed variation rate in the experiment is faster than in actual operation. Therefore, in practice, the voltage dynamics will also be minimally affected by speed changes. The reason for this is that the electrical time constant of the machine is typically much smaller than the mechanical time constant, meaning that electrical dynamics are faster than mechanical dynamics. As a result, the impact of speed changes on voltage dynamics is negligible.

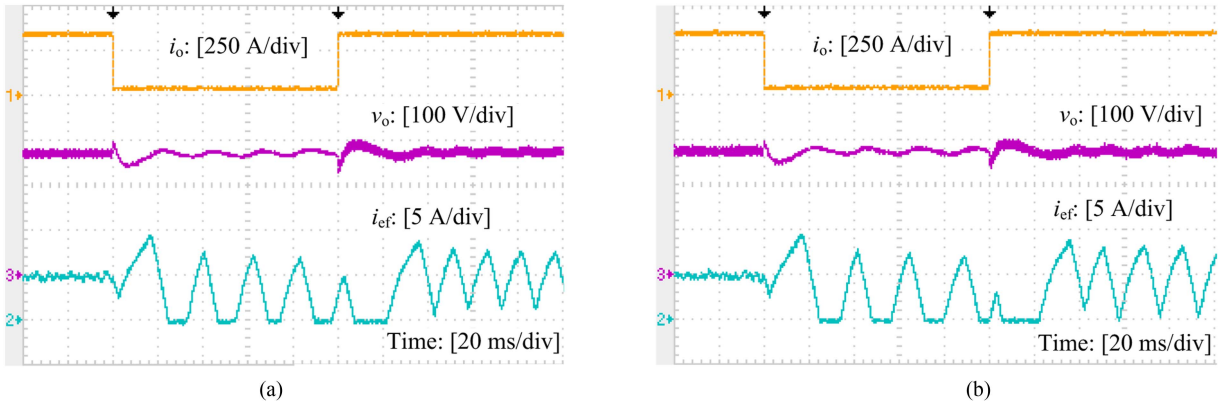

Fig. 23. Transient response of the DC-TSG when the load power steps from the nominal value to 10% with conventional antiwindup strategies. (a) Back-calculation. (b) Conditional integration.

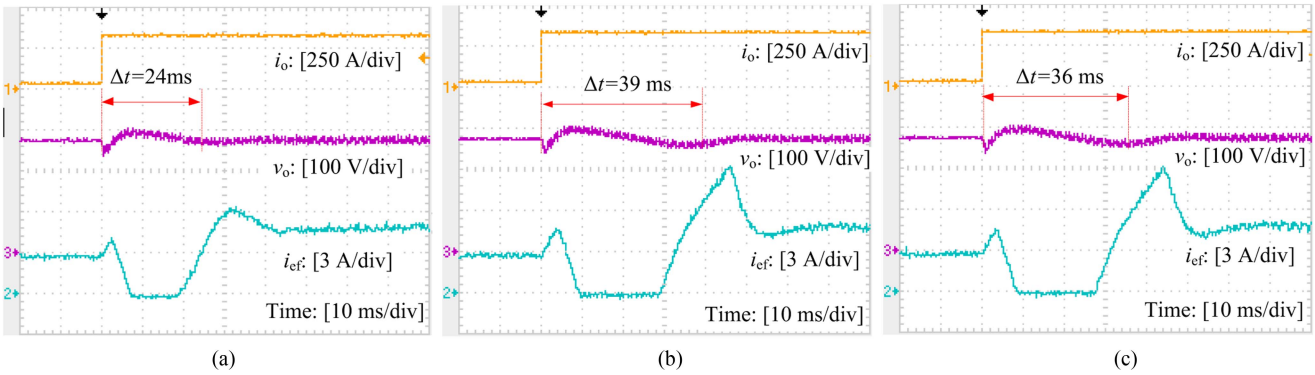

Fig. 24. Transient response of the DC-TSG at 100 Hz bandwidth for the outer loop when the load steps from the nominal value to 10% with three antiwindup strategies. (a) Proposed predictive antiwindup scheme. (b) Conditional integration. (c) Back-calculation.

The experimental results in Figs. 19–21 demonstrate that the DC-TSG has satisfactory steady-state and dynamic performance, which verifies the effectiveness of the proposed parameter design method.

B. Verification of the Double Closed-Loop Parameter Design Method

To further validate the effectiveness of the proposed parameter design method, the controller parameters for the outer loop are designed with $\phi_{\rm cvm}$ decreased to $-71.2°$, which corresponds to point B outsides the optional regions in Fig. 8. In this case, the bandwidth of the outer loop remains 200 Hz, consistent with Fig. 20, but the phase margin is only 15°, which is insufficient to guarantee the desired system dynamic performance. Fig. 22 shows the dynamic experimental results of the load step under this set of controller parameters. As seen, since the phase margin is reduced, both the field current $i_{\rm ef}$ and the dc-link voltage $v_{\rm o}$ exhibit prolonged oscillations during the transient. The experimental results in Fig. 22 are consistent with theoretical predictions and confirm the effectiveness of the proposed method in predicting oscillation behavior caused by improperly designed control parameters.

C. Experimental Validation and Comparative Analysis of Three Antiwindup Schemes

To verify the effectiveness of the proposed predictive antiwindup strategy in double-loop control, experiments under load step changes are conducted and compared with the results obtained using back-calculation and conditional integration. The experiments are performed based on the control parameters designed in Section IV-C, with an outer-loop bandwidth of 200 Hz, an inner-loop bandwidth of 1 kHz, and a phase margin of 45° for both loops. The results are shown in Fig. 23. As can be seen, the conventional antiwindup methods exhibit sustained oscillations after load step change. In contrast, the experimental results shown in Fig. 20, which employ the proposed predictive antiwindup scheme, have the ability of stable operation, which validates the advantages of the proposed predictive antiwindup scheme.

Furthermore, the outer-loop bandwidth is set to a relatively conservative value of 100 Hz, with a phase margin of 45° for parameter design. Load step change experiments are then conducted using three different antiwindup schemes, and the experimental results are shown in Fig. 24. As can be seen, even though the traditional antiwindup schemes can operate stably at lower bandwidths, they have longer regulation times during

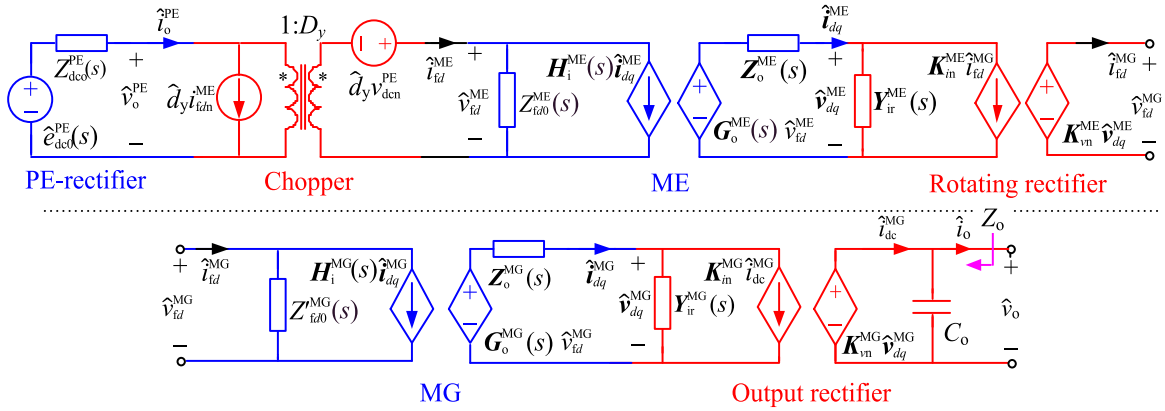

Fig. 25. Overall small-signal equivalent circuit model of the DC-TSG.

dynamic processes than the proposed predictive antiwindup scheme. This comparison further validates the advantages of the proposed predictive antiwindup scheme.

VII. Conclusion

With the rapid development of aircraft toward MEA, higher requirements are put forward for the dynamic characteristics and system stability of the main power source. This article focuses on the controller design and optimization for a DC-TSG in aviation electrical systems. With the modular modeling method of the two-port network, the double-closed- loop control plant model of the DC-TSG is established, and a step-by-step parameter design method is proposed for the double-closed-loop control of the DC-TSG. Exploiting the characteristics of the DC-TSG model and PI controller, the proposed method defines a feasible region for key controller parameters under specified phase margin constraints, thus simplifying the design process, avoiding trial-and-error, and enabling optimal performance. To address integrator windup in PI controllers, the causes of windup and the limitations of conventional antiwindup schemes in double-loop control systems are analyzed, and a predictive antiwindup scheme is proposed to mitigate the impact of inner loop saturation on the outer loop in double-loop control systems. The proposed antiwindup scheme is easy to implement and can effectively suppress double-loop integrator windup, thereby enhancing dynamic performance and stability. The simulations and experiments validate the correctness of the theoretical analysis and the effectiveness of the proposed schemes.

Appendix

A. Parameters of DC-TSG

1) *MG*: 90 kW, 8000 r/min, 6 poles, $r_{\mathrm{s}}^{\mathrm{MG}}=8.02\ \mathrm{m\Omega}$, $L_{\mathrm{ls}}^{\mathrm{MG}}=1.15\mu\mathrm{H}$, $L_{md}^{\mathrm{MG}}=226.4\mu\mathrm{H}$, $L_{mq}^{\mathrm{MG}}=118\mu\mathrm{H}$, $r_{fd}'^{\mathrm{MG}}=2.778\ \mathrm{m\Omega}$, $L_{lfd}'^{\mathrm{MG}}=3.315\mu\mathrm{H}$, $r_{kd}'^{\mathrm{MG}}=1.517\ \mathrm{m\Omega}$, $L_{lkd}'^{\mathrm{MG}}=0.003\mu\mathrm{H}$, $r_{kq}'^{\mathrm{MG}}=33\ \mathrm{m\Omega}$, $L_{lkq}'^{\mathrm{MG}}=0.0004\mu\mathrm{H}$, $N_{\mathrm{sf}}^{\mathrm{MG}}=0.074$, $C_{\mathrm{o}}=2\mathrm{mF}$, $v_{\mathrm{o}}=270\ \mathrm{V}$.
2) *ME*: 10 poles, $r_{\mathrm{s}}^{\mathrm{ME}}=69\ \mathrm{m\Omega}$, $L_{\mathrm{ls}}^{\mathrm{ME}}=250.9\mu\mathrm{H}$, $L_{md}^{\mathrm{ME}}=422.1\mu\mathrm{H}$, $L_{mq}^{\mathrm{ME}}=269.5\mu\mathrm{H}$, $r_{fd}'^{\mathrm{ME}}=5.588\ \mathrm{m\Omega}$, $L_{lfd}'^{\mathrm{ME}}=0.06\mu\mathrm{H}$, $N_{\mathrm{sf}}^{\mathrm{ME}}=0.036$.
3) *PE*: 12 poles, $r_{\mathrm{s}}^{\mathrm{PE}}=235.4\ \mathrm{m\Omega}$, $L_{dd}^{\mathrm{PE}}=L_{qq}^{\mathrm{PE}}=L_{\mathrm{s}}^{\mathrm{PE}}=14.17\mu\mathrm{H}$, $C_{\mathrm{o}}^{\mathrm{PE}}=0.47\mathrm{mF}$, $\psi_{\mathrm{rm}}=0.008937\ \mathrm{Wb}$, $f_{\mathrm{s}}=10\mathrm{kHz}$.

B. Derivation of the Two-Port Model of DC-TSG

As established using a modular modeling approach in [6], the overall model of DC-TSG is represented here for clarity, as shown in Fig. 25.

The four transfer functions representing the two-port model of the DC-TSG in Fig. 2—namely, $Z_{\mathrm{o}}(s)$, $G_{\mathrm{o}}(s)$, $Y_{\mathrm{i}}(s)$, and $H_{\mathrm{in}}(s)$—can be derived from Fig. 25, and are expressed as

$$G_{\mathrm{o}}(s)=\left(1+sC_{\mathrm{o}}Z_{\mathrm{o}}^{\mathrm{MErMGr}}(s)\right)^{-1}G_{\mathrm{o}}^{\mathrm{MErMGr}}(s) \tag{A1}$$

$$Z_{\mathrm{o}}(s)=\left(1+sC_{\mathrm{o}}Z_{\mathrm{o}}^{\mathrm{MErMGr}}(s)\right)^{-1}Z_{\mathrm{o}}^{\mathrm{MErMGr}}(s) \tag{A2}$$

$$Y_{\mathrm{i}}(s)=Y_{\mathrm{i}}^{\mathrm{MErMGr}}(s)+H_{\mathrm{i}}^{\mathrm{MErMGr}}(s)\times\left(1+sC_{\mathrm{o}}Z_{\mathrm{o}}^{\mathrm{MErMGr}}(s)\right)^{-1}sC_{\mathrm{o}}G_{\mathrm{o}}^{\mathrm{MErMGr}}(s) \tag{A3}$$

$$H_{\mathrm{in}}(s)=H_{\mathrm{i}}^{\mathrm{MErMGr}}(s)\left(1+sC_{\mathrm{o}}Z_{\mathrm{o}}^{\mathrm{MErMGr}}(s)\right)^{-1} \tag{A4}$$

where C_{o} denotes the dc-link capacitor, $Z_{\mathrm{o}}^{\mathrm{MErMGr}}$, $G_{\mathrm{o}}^{\mathrm{MErMGr}}$, $Y_{\mathrm{i}}^{\mathrm{MErMGr}}$, and $H_{\mathrm{i}}^{\mathrm{MErMGr}}$ denote the four transfer functions that characterize the equivalent two-port network from the ME field port to the dc output terminal of the MG's rectifier. These transfer functions are obtained by cascading the two-port models of the ME, rotating rectifier, MG, and output rectifier. The explicit expressions of these transfer functions are given as follows:

$$G_{\mathrm{o}}^{\mathrm{MErMGr}}(s)=\boldsymbol{K}_{vn}^{\mathrm{MG}}\left(\boldsymbol{I}+\boldsymbol{Z}_{\mathrm{o}}^{\mathrm{MErMG}}(s)\boldsymbol{Y}_{\mathrm{ir}}^{\mathrm{MG}}(s)\right)^{-1}\boldsymbol{G}_{\mathrm{o}}^{\mathrm{MErMG}}(s) \tag{A5}$$

$$Z_{\mathrm{o}}^{\mathrm{MErMGr}}(s)=\boldsymbol{K}_{vn}^{\mathrm{MG}}\left(\boldsymbol{I}+\boldsymbol{Z}_{\mathrm{o}}^{\mathrm{MErMG}}(s)\boldsymbol{Y}_{\mathrm{ir}}^{\mathrm{MG}}(s)\right)^{-1}\times\boldsymbol{Z}_{\mathrm{o}}^{\mathrm{MErMG}}(s)\boldsymbol{K}_{in}^{\mathrm{MG}} \tag{A6}$$

$$Y_{\mathrm{i}}^{\mathrm{MErMGr}}(s)=Y_{\mathrm{i}}^{\mathrm{MErMG}}(s)+\boldsymbol{H}_{\mathrm{i}}^{\mathrm{MErMG}}(s)\times\left(\boldsymbol{I}+\boldsymbol{Y}_{\mathrm{ir}}^{\mathrm{MG}}(s)\boldsymbol{Z}_{\mathrm{o}}^{\mathrm{MErMG}}(s)\right)^{-1}\boldsymbol{Y}_{\mathrm{ir}}^{\mathrm{MG}}(s)\boldsymbol{G}_{\mathrm{o}}^{\mathrm{MErMG}}(s) \tag{A7}$$

$$H_{\mathrm{i}}^{\mathrm{MErMGr}}(s)=\boldsymbol{H}_{\mathrm{i}}^{\mathrm{MErMG}}(s)\left(\boldsymbol{I}+\boldsymbol{Y}_{\mathrm{ir}}^{\mathrm{MG}}(s)\boldsymbol{Z}_{\mathrm{o}}^{\mathrm{MErMG}}(s)\right)^{-1}\boldsymbol{K}_{in}^{\mathrm{MG}} \tag{A8}$$

where $\boldsymbol{K}_{vn}^{\mathrm{MG}}$, $\boldsymbol{K}_{in}^{\mathrm{MG}}$, $Y_{\mathrm{ir}}^{\mathrm{MG}}$ denote the two-port network parameters of the MG's rectifier, which can be obtained following the modeling approach presented in [6]. $\boldsymbol{Z}_{\mathrm{o}}^{\mathrm{MErMG}}$, $\boldsymbol{G}_{\mathrm{o}}^{\mathrm{MErMG}}$, $Y_{\mathrm{i}}^{\mathrm{MErMG}}$, and $\boldsymbol{H}_{\mathrm{i}}^{\mathrm{MErMG}}$ denote the four transfer functions that characterize the equivalent two-port network from the ME field port to the MG stator terminal. These transfer functions are obtained by cascading the two-port models of the ME, rotating rectifier, and MG. The explicit expressions of these transfer functions are given as

$$\boldsymbol{Z}_{\mathrm{o}}^{\mathrm{MErMG}}(s) = \boldsymbol{Z}_{\mathrm{o}}^{\mathrm{MG}}(s) + \boldsymbol{G}_{\mathrm{o}}^{\mathrm{MG}}(s) \times \left(1 + Z_{\mathrm{o}}^{\mathrm{MEr}}(s) Y_{\mathrm{i}}^{\mathrm{MG}}(s)\right)^{-1} Z_{\mathrm{o}}^{\mathrm{MEr}}(s) \boldsymbol{H}_{\mathrm{i}}^{\mathrm{MG}}(s) \tag{A9}$$

$$\boldsymbol{G}_{\mathrm{o}}^{\mathrm{MErMG}}(s) = \boldsymbol{G}_{\mathrm{o}}^{\mathrm{MG}}(s)\left(1 + Z_{\mathrm{o}}^{\mathrm{MEr}}(s) Y_{\mathrm{i}}^{\mathrm{MG}}(s)\right)^{-1} G_{\mathrm{o}}^{\mathrm{MEr}}(s) \tag{A10}$$

$$Y_{\mathrm{i}}^{\mathrm{MErMG}}(s) = Y_{\mathrm{i}}^{\mathrm{MEr}}(s) + H_{\mathrm{i}}^{\mathrm{MEr}}(s) \times \left(1 + Y_{\mathrm{i}}^{\mathrm{MG}}(s) Z_{\mathrm{o}}^{\mathrm{MEr}}(s)\right)^{-1} Y_{\mathrm{i}}^{\mathrm{MG}}(s) G_{\mathrm{o}}^{\mathrm{MEr}}(s) \tag{A11}$$

$$\boldsymbol{H}_{\mathrm{i}}^{\mathrm{MErMG}}(s) = H_{\mathrm{i}}^{\mathrm{MEr}}(s)\left(1 + Y_{\mathrm{i}}^{\mathrm{MG}}(s) Z_{\mathrm{o}}^{\mathrm{MEr}}(s)\right)^{-1} \boldsymbol{H}_{\mathrm{i}}^{\mathrm{MG}}(s) \tag{A12}$$

where $\boldsymbol{Z}_{\mathrm{o}}^{\mathrm{MG}}$, $\boldsymbol{G}_{\mathrm{o}}^{\mathrm{MG}}$, $Y_{\mathrm{i}}^{\mathrm{MG}}$, and $\boldsymbol{H}_{\mathrm{i}}^{\mathrm{MG}}$ denote the four transfer functions that characterize the two-port network of the MG, which can be obtained following the modeling approach presented in [6]. $Z_{\mathrm{o}}^{\mathrm{MEr}}$, $G_{\mathrm{o}}^{\mathrm{MEr}}$, $Y_{\mathrm{i}}^{\mathrm{MEr}}$, and $H_{\mathrm{i}}^{\mathrm{MEr}}$ denote the four transfer functions that characterize the equivalent two-port network from the ME field port to the dc output terminal of the rotating rectifier. These transfer functions are obtained by cascading the two-port models of the ME and rotating rectifier. The explicit expressions of these transfer functions are given as

$$G_{\mathrm{o}}^{\mathrm{MEr}}(s) = \boldsymbol{K}_{vn}^{\mathrm{ME}}\left(\boldsymbol{I} + \boldsymbol{Z}_{\mathrm{o}}^{\mathrm{ME}}(s)\boldsymbol{Y}_{\mathrm{ir}}^{\mathrm{ME}}(s)\right)^{-1} \boldsymbol{G}_{\mathrm{o}}^{\mathrm{ME}}(s) \tag{A13}$$

$$Z_{\mathrm{o}}^{\mathrm{MEr}}(s) = \boldsymbol{K}_{vn}^{\mathrm{ME}}\left(\boldsymbol{I} + \boldsymbol{Z}_{\mathrm{o}}^{\mathrm{ME}}(s)\boldsymbol{Y}_{\mathrm{ir}}^{\mathrm{ME}}(s)\right)^{-1} \boldsymbol{Z}_{\mathrm{o}}^{\mathrm{ME}}(s) \boldsymbol{K}_{in}^{\mathrm{ME}} \tag{A14}$$

$$Y_{\mathrm{i}}^{\mathrm{MEr}}(s) = Y_{\mathrm{i}}^{\mathrm{ME}}(s) + \boldsymbol{H}_{\mathrm{i}}^{\mathrm{ME}}(s) \times \left(\boldsymbol{I} + \boldsymbol{Y}_{\mathrm{ir}}^{\mathrm{ME}}(s)\boldsymbol{Z}_{\mathrm{o}}^{\mathrm{ME}}(s)\right)^{-1} \boldsymbol{Y}_{\mathrm{ir}}^{\mathrm{ME}}(s) \boldsymbol{G}_{\mathrm{o}}^{\mathrm{ME}}(s) \tag{A15}$$

$$H_{\mathrm{i}}^{\mathrm{MEr}}(s) = \boldsymbol{H}_{\mathrm{i}}^{\mathrm{ME}}(s)\left(\boldsymbol{I} + \boldsymbol{Y}_{\mathrm{ir}}^{\mathrm{ME}}(s)\boldsymbol{Z}_{\mathrm{o}}^{\mathrm{ME}}(s)\right)^{-1} \boldsymbol{K}_{in}^{\mathrm{ME}} \tag{A16}$$

where $\boldsymbol{K}_{vn}^{\mathrm{ME}}$, $\boldsymbol{K}_{in}^{\mathrm{ME}}$, and $\boldsymbol{Y}_{\mathrm{ir}}^{\mathrm{ME}}$ denote the two-port network parameters of the rotating rectifier, and $\boldsymbol{Z}_{\mathrm{o}}^{\mathrm{ME}}$, $\boldsymbol{G}_{\mathrm{o}}^{\mathrm{ME}}$, $Y_{\mathrm{i}}^{\mathrm{ME}}$, and $\boldsymbol{H}_{\mathrm{i}}^{\mathrm{ME}}$ denote the four transfer functions that characterize the two-port network of the ME. The detailed derivation of these parameters and transfer functions can be found in [6].

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