Multilevel Hybrid Frequency Modulation With Adaptive DC Link Voltage Fluctuation and Dead-Time Elimination for Cascaded H-Bridge Inverter

Chunwei Song, *Member, IEEE*, Sa Lu, Gang Li, and Jinlong He

***Abstract*—With the same number of cascaded cells, the asymmetric H-bridge cascaded multilevel inverter (CMLI) achieves more output voltage levels. This article proposes a multilevel hybrid frequency (HF) modulation composed of region-segmented low-frequency modulation and dead-time-eliminated high-frequency modulation for the asymmetric two-cell H-bridge CMLI. To reduce switching losses, high dc-link voltage cascaded cell adopts low-frequency modulation, while low dc-link voltage cell employs high-frequency modulation. After applying the proposed modulation, only one bridge arm operates at high frequency in the two-cell CMLI. Based on the switching patterns of cascaded units, the natural dead time in the driving signals of upper and lower switches within each bridge arm is analytically derived. The current zero-crossing detection debouncing scheme proposed in this article can effectively prevent output current distortion. Based on the output power of each cascaded cell, the two-dimensional plane formed by the dc-link voltage ratio and modulation index is divided into three operating regions. Simulation results verify that the multilevel HF modulation can adaptively respond to dc-link voltage fluctuations and load characteristics. This article has developed an experimental prototype with a combined microcontroller unit (MCU) and field-programmable gate array (FPGA) control system as the core. The results verify the effectiveness of the multilevel HF modulation.**

***Index Terms*—Cascaded, hybrid frequency (HF), inverter, modulation, multilevel.**

NOMENCLATURE

Abbreviation

CMLI	Cascaded multilevel inverter.
LS	Level-shifted.
HF	Hybrid frequency.
PWM	Pulsewidth modulation.
THD	Total harmonic distortion.

Parameters of the cascaded multilevel inverter

k	Voltage ratio.
U_1, U_2	DC-link voltages of cell 1 and cell 2.
V_M	Low-frequency modulated voltage of CMLI.
m	Modulation index .
U	Amplitude of the modulation voltage.
f_0	Fundamental frequency.
v_m	Modulation voltage of Cell 2.
i_o	Output current.
θ_1	Phase value of V_M when $V_M = U_2$.
θ_2	Phase value of V_M when $V_M = U_1$.
θ	Phase angle by which i_o lags behind V_M.
$T_{d\text{-}L11\text{-}P\text{-}N}$, $T_{d\text{-}L11\text{-}N\text{-}P}$	Natural dead times in the drive signals of the switching devices in leg L_{11}.
$T_{d\text{-}L12\text{-}P\text{-}N}$, $T_{d\text{-}L12\text{-}N\text{-}P}$	Natural dead times in the drive signals of the switching devices in leg L_{12}.
$T_{d\text{-}L21}$, $T_{d\text{-}L22}$	Natural dead times in the drive signals of the switching devices in leg L_{21} and leg L_{22}.
v_c	Triangular carrier wave v_c.
T_s	Carrier period.
f_s	Carrier frequency f_s.
P_1, P_2	Pulse signals obtained by comparing the signals $0.5v_m$ and-$0.5v_m$ with v_c.
P_D	Pulse signal generated by performing XOR logic operation on signals P_1 and P_2.
$\overline{P_D}$	Pulse signal obtained by inverting P_D.
IPN, IPN_old, IPN_new, IPN_num, IPN_flag	Integer variables set in the MCU program.
u_{H1}	Fundamental component of cell 1's output voltage.
P_{H1_active}, P_{H2_active}	Active power outputs of Cell1 and Cell2.
Ra	Ratio between P_{H1_active} and P_{H2_active}.
PWMA1, PWMA2, PWMB1, PWMB2, PWMB3, PWMB4, PWMB5, PWMB6	Output levels of the MCU's external pins.
X	Operating region of cell 1.

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I. Introduction

Multilevel inverters enable high-voltage output using low-voltage-rated switching devices, making them suitable for medium-to-high power applications such as photovoltaic grid connection and ac drive systems. Moreover, multilevel inverters exhibit advantages including low voltage change rate, multiple output voltage levels, high efficiency, reduced electromagnetic interference, and superior harmonic characteristics of the output voltage [1], [2]. Compared to diode-clamped and flying capacitor multilevel inverters, the H-bridge cascaded multilevel inverter (CMLI) eliminates the need for clamping diodes and capacitors, thereby avoiding complex capacitor voltage balancing issues [3]. Meanwhile, each H-bridge cell can be independently controlled. Under the condition of the same output voltage levels, the H-bridge CMLI requires the fewest power devices, which facilitates modular design and easy scalability [4].

Compared with traditional symmetric H-bridge CMLI, under the condition of an equal number of cascaded cells, the CMLI with unbalanced dc-link voltage can achieve more output voltage levels while reducing the number of switching devices and dc power sources required [5], [6]. The main circuit of the asymmetric CMLI features H-bridge units with varying voltage ratings and switching frequencies. This design philosophy aligns with contemporary trends in power electronics development, offering significant practical value [7], [8]. The effective suppression of output voltage harmonic content and dynamic maintenance of positive output power in all cascaded cells constitute critical operational requirements for ensuring stable performance of asymmetric CMLI. Therefore, researchers have conducted extensive studies aimed at increasing output voltage levels and optimizing pulse width modulation (PWM) strategies.

Ren et al. [9], [10] proposed a two-cell seven-level inverter with a dc-link voltage ratio of 1:2, based on the traditional H-bridge cascaded inverter topology. By adjusting the dc-bus voltage ratios in a three-cell CMLI to configurations of 1:1:2 [11], [12], 1:2:4 [13], [14], [15], and 1:3:9 [16], [17], the output side can generate PWM voltages with 9-level, 15-level, and 27-level waveforms respectively. This demonstrates that utilizing dc-link voltage imbalance can further increase the output voltage levels of CMLI. From a topology perspective, the common drawback of the modulations proposed in [9], [10], [11], [12], [13], [14], [15], [16] and [17] lies in requiring a dc–dc converter at the input side of each cascaded cell or controlling the output-side dc voltage to maintain fixed ratios among dc-link voltages, which increases system structural complexity and control challenges.

During the operation of CMLI, improper control may cause partial cells to absorb active power. When the dc-side voltage is generated by uncontrolled rectification, this phenomenon will lead to an increase in the voltage across the dc-link filter capacitors. To solve the energy backflow issue, a fully-controlled rectifier circuit can be used to obtain dc-link voltage. However, this method increases circuit costs and reduces system reliability. Ye et al. [12] improved the modulation strategy and successfully derived the range of modulation index that ensures all cascaded cells maintain positive output voltage polarity, thereby avoiding current backflow.

TABLE I

Comparison of Different Modulation Strategies for CMLI

	THD	Adaptability to dc-link voltage fluctuations	Switching losses	Dead-time-free operation
Ahmed et al. [17], Busarello et al. [21]	Highest	No	Low	No
Jiao et al. [23], Jiao et al. [24], Hao et al. [25]	Lower	No	High	No
Mao et al. [22]	Lower	No	High	No
Proposed HF-PWM	Lowest	Yes	High	Yes

The methods proposed in [18], [19], and [20], such as the voltage alteration method along with an optimization algorithm [18], combinational level-shifted (LS) and phase-shifted PWM technique [19], and carrier-reassignment PWM [20], can solve the problem of unbalanced output power among cells in asymmetric CMLI. However, these methods require power devices in all cascaded cells to operate in high-frequency states, resulting in increased switching losses. The power balancing objective is to maintain the ratio of output voltage RMS values among cascaded cells consistent with the dc-link voltage ratios, under the condition that identical currents flow through each cascaded cell. The voltage stress of the power switch depends on the dc-bus voltage, while the output power balance does not affect the voltage stress. Therefore, power balance is not an essential technology directly related to the reliable operation of CMLI or the selection criteria of power devices. When the asymmetric CMLI adopts low-frequency modulation strategies such as nearest level modulation [17] and staircase modulation [21], it is observed that cascaded cells transmitting higher power operate at lower switching frequencies, while those handling lower power operate at higher frequencies. This demonstrates that low-frequency modulation strategies can effectively mitigate the inherent contradiction between transmitted power and operating frequency in power switching devices. However, in scenarios with fewer cascaded power cells, especially when only two cells are utilized, the harmonic performance of the output PWM voltage formed by superimposing the low-frequency voltage outputs from these cells under low-frequency modulation strategies is significantly degraded. Low-frequency modulation needs to be integrated with high-frequency modulation to form a hybrid PWM, thereby addressing the inferior harmonic characteristics of CMLI caused by the sole use of low-frequency modulation. Mao et al. [22] proposed the hybrid modulation strategy combining optimal zero-sequence injection low-frequency modulation with high-frequency PWM, but it is only applicable to symmetric CMLI. A closed-loop harmonic suppression method was proposed in [23] and [24] through phase-shift angle adjustment, but high-frequency operation is required for all switching devices. The selective harmonic elimination scheme in [25], developed through the integration of the stochastic configuration network and the Levenberg–Marquardt algorithm, necessitates high-performance computing resources for offline data training.

It is well known that when the upper and lower switching devices in each H-bridge leg operate in a complementary conduction mode, the dead time must be inserted between the switching signals of the two devices in the same leg. This is implemented to prevent the direct short-circuit fault on the dc-link caused by the simultaneous conduction of both switching devices due to their failure to turn OFF in time. Dead-time effect causes the output voltage of cascaded cell employing high-frequency modulation to deviate from theoretical expectations, while also increasing harmonic components. To address the dead-time effects, numerous dead-time compensation strategies have been proposed for CMLI in [26], [27], and [28]. However, under high switching frequencies, factors such as the nonlinear characteristics of switching devices, the magnitude of output current, ambient temperature variation, and signal transmission delays in the gate drive circuits of switching devices can degrade the efficacy of dead-time compensation. The dead-time elimination modulation strategies proposed in [29], [30], and [31] are specifically designed for nested neutral-point-clamped converters, but they face limitations due to inherent delays in current polarity detection processes.

Table I summarized the performance of different modulation strategies for CMLI in terms of the total harmonic distortion (THD) of the output PWM voltage, adaptability to dc-link voltage fluctuations, switching losses, and dead-time-free operation.

The multilevel hybrid-frequency modulation applicable to dc-link voltage ratio fluctuations is proposed for two-cell CMLI in this article. To minimize power device losses, low-frequency modulation is applied to the high-voltage cascaded cell, while high-frequency dead-time-free modulation strategies are implemented for the low-voltage cascaded cell. The distribution of the total output power between two cascaded cells is analytically derived, and the conditions for preventing reverse power flow are systematically established in this article. The effectiveness of the proposed multilevel hybrid-frequency modulation strategy is verified through simulation and experimental results.

II. MULTILEVEL HYBRID-FREQUENCY MODULATION

The two-cell H-bridge CMLI is illustrated in Fig. 1, where u_o is the output voltage, i_o is the output current, U_1 and U_2 are the dc link voltages of cell 1 and cell 2, respectively.

The voltage ratio k ($k>1$) is given by the following equation:

$$k = \frac{U_1}{U_2}. \tag{1}$$

The traditional phase-shifted carrier PWM can effectively reduce the THD of the output voltage, but simultaneously increases the switching frequency of power devices, adversely affecting system efficiency. In the two-cell CMLI where both cells carry the same current, the power switches in the high-voltage cell exhibit higher switching losses compared to those in the low-voltage cell. To generate high-frequency PWM voltage on the output side while minimizing switching times, the high dc- link voltage cell adopts low-frequency PWM, whereas the low dc-link voltage cell employs high-frequency PWM. Additionally, integrating dead-time elimination techniques into high-frequency modulation can further reduce the THD of the output voltage.

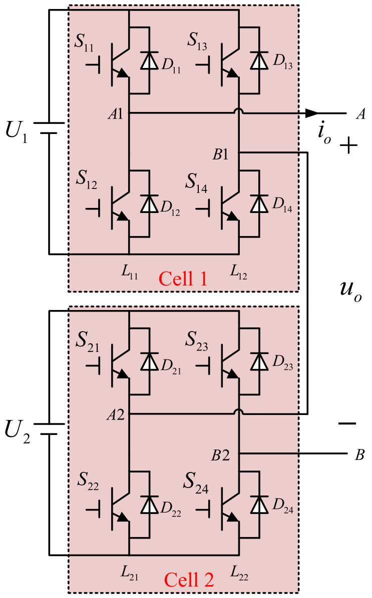


Fig. 1. Topology of the two-cell CMLI with unbalanced DC-link voltages.

TABLE II
OUTPUT LEVEL VOLTAGE OF CELL 1 AND MODULATION VOLTAGE OF CELL 2

Region where V_M is located	Output level voltage of Cell 1	modulation voltage of Cell 2 (v_m)
$U_1 \le V_M \le U_1 + U_2$	$+ U_1$	$V_M - U_1$
$U_2 \le V_M < U_1$	$+ U_1$	$V_M - U_1$
$-U_2 \le V_M < U_2$	0	V_M
$-U_1 \le V_M < -U_2$	$- U_1$	$V_M + U_1$
$-U_1 - U_2 \le V_M < -U_1$	$- U_1$	$V_M + U_1$

The low-frequency modulated voltage V_M of the CMLI and the modulation index m are related as shown in the following equation:

$$\begin{cases} V_M = U \sin(2\pi f_0 t) \\ m = \frac{U}{U_1 + U_2} \end{cases} \tag{2}$$

where U is the amplitude of the modulation voltage, and f_0 is the fundamental frequency. To ensure that the fundamental component of the output voltage u_o is the modulation voltage V_M, based on the region where V_M is located, the output voltage level of cell 1 and the modulation voltage v_m of cell 2 are given in Table II. To prevent over-modulation, the absolute values of all modulation voltages for cell 2 in Table II must be less than U_2. The complete constraint set is formally expressed

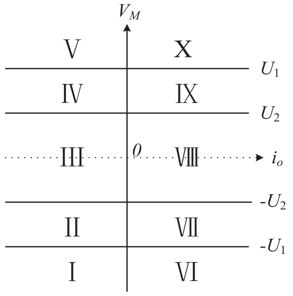


Fig. 2. Distinct regions in the two-dimensional plane composed of V_M and i_o.

TABLE III
DRIVING SIGNAL SCHEME FOR S_{11}, S_{12}, S_{13}, S_{14}, AND CONDUCTING DEVICES IN EACH OPERATING REGION

Regions	S_{11}	S_{12}	S_{13}	S_{14}	Conducting Devices
I	0	1	1	0	S_{12}, S_{13}
II	0	1	1	0	S_{12}, S_{13}
III	0	0	1	0	S_{13}, D_{11}
IV	0	0	0	0	D_{11}, D_{14}
V	0	0	0	0	D_{11}, D_{14}
VI	0	0	0	0	D_{12} D_{13}
VII	0	0	0	0	D_{12} D_{13}
VIII	1	0	0	0	S_{11} D_{13}
IX	1	0	0	1	S_{11} S_{14}
X	1	0	0	1	S_{11} S_{14}

by

$$\begin{cases} -U_2 \leq V_M - U_1 \leq U_2 & \text{when } \ U_1 \leq V_M \leq U_1 + U_2 \\ -U_2 \leq V_M - U_1 \leq U_2 & \text{when } U_2 \leq V_M < U_1 \\ -U_2 \leq V_M \leq U_2 & \text{when } -U_2 \leq V_M < U_2 \\ -U_2 \leq V_M + U_1 \leq U_2 & \text{when } -U_1 \leq V_M < -U_2 \\ -U_2 \leq V_M + U_1 \leq U_2 & \text{when } -U_1 - U_2 \leq V_M < -U_1. \end{cases} \tag{3}$$

From (3), it can be derived that the voltage ratio *k* and the modulation index *m* must satisfy the following condition:

$$\begin{cases} 1 \leq k \leq 2 \\ 0 \leq m \leq 1. \end{cases} \tag{4}$$

A. Region-Segmented Low-Frequency Modulation for the Cell With High-Voltage DC Link

The plane formed by the modulation voltage V_M and the output current i_o is divided into ten regions as shown in Fig. 2. The driving signal scheme for S_{11}, S_{12}, S_{13}, S_{14}, and conducting devices in cell 1 given in Table III is provided based on the regions where V_M and i_o are located, as well as the output level requirements of cell 1 as given in Table II. When the operating state is in regions I, II, IX, or X, the desired voltage level is generated by two conducting switching devices. In regions IV, V, VI, and VII, two freewheeling diodes conduct to produce the target voltage level. For regions III and VIII, a single conducting switching device combined with a freewheeling diode generates the required zero voltage level.

TABLE IV
STATE VARIATIONS WITHIN A FUNDAMENTAL PERIOD UNDER DIFFERENT LOAD CONDITIONS

Range of angle θ	State variations within a fundamental period
$-\theta_1 \leq \theta \leq \theta_1$	VIII→IX→X→IX→VIII→III→II→I→II→III
$\theta_1 < \theta \leq \theta_2$	III→IV→IX→X→IX→VIII→VII→II→I→II
$\theta_2 < \theta \leq \pi/2$	III→IV→V→X→IX→VIII→VII→VI→I→II
$-\theta_2 \leq \theta < -\theta_1$	VIII→IX→X→IX→IV→III→II→I→II→VII
$-\pi/2 \leq \theta < -\theta_2$	VIII→IX→X→V→IV→III→II→I→VI→VII

TABLE V
DURATIONS OF THE NATURAL DEAD TIME

Range of angle θ	$T_{d\text{-}L11\text{-}P\text{-}N}$	$T_{d\text{-}L11\text{-}N\text{-}P}$	$T_{d\text{-}L12\text{-}P\text{-}N}$	$T_{d\text{-}L12\text{-}N\text{-}P}$
$-\theta_1 \leq \theta \leq \theta_1$	$\theta_1/2\pi f_0$	$\theta_1/2\pi f_0$	$\theta_1/2\pi f_0$	$\theta_1/2\pi f_0$
$\theta_1 < \theta \leq \theta_2$	$(\theta-\theta_1)/2\pi f_0$	$(\theta+\theta_1)/2\pi f_0$	$(\theta+\theta_1)/2\pi f_0$	$(\theta-\theta_1)/2\pi f_0$
$\theta_2 < \theta \leq \pi/2$	$(\theta-\theta_1)/2\pi f_0$	$(\theta+\theta_1)/2\pi f_0$	$(\theta+\theta_1)/2\pi f_0$	$(\theta-\theta_1)/2\pi f_0$
$-\theta_2 \leq \theta < -\theta_1$	$(-\theta+\theta_1)/2\pi f_0$	$(-\theta-\theta_1)/2\pi f_0$	$(-\theta-\theta_1)/2\pi f_0$	$(-\theta+\theta_1)/2\pi f_0$
$-\pi/2 \leq \theta < -\theta_2$	$(-\theta+\theta_1)/2\pi f_0$	$(-\theta-\theta_1)/2\pi f_0$	$(-\theta-\theta_1)/2\pi f_0$	$(-\theta+\theta_1)/2\pi f_0$

To improve the dc-bus voltage utilization, it is generally required that the amplitude U of the modulation voltage V_M be greater than U_1. Within the range of [0, $\pi/2$], when V_M is at phase θ_1, $V_M = U_2$, and when V_M is at phase θ_2, $V_M = U_1$. The values of θ_1 and θ_2 can be calculated using the following equations:

$$\begin{cases} \theta_1 = \arcsin \frac{U_2}{U} \\ \theta_2 = \arcsin \frac{U_1}{U}. \end{cases} \tag{5}$$

The output current i_o lags behind the modulated voltage V_M by a phase angle θ. Within each fundamental period [$2\pi n$, $2\pi n+2\pi$]($n = 0, 1, 2, 3 \ldots$), based on V_M, U_1, U_2, θ and Fig. 2, the operating process of cell1 is divided into different regions. The switching sequence of these regions within the fundamental period is given in Table IV. The drive signals for the four switching devices in cell 1 are correspondingly illustrated in Fig. 3. The generation of the zero output level requires the coordinated conduction of either switches S_{11} and S_{13} or S_{12} and S_{14} with the freewheeling diode. If the zero output level is generated by the coordinated conduction of switches S_{11} and S_{12} or S_{13} and S_{14} with the freewheeling diode, dead time must necessarily be set between the drive signals of the upper and lower switching devices in both bridge legs.

In cell1, the natural dead time exists between the drive signals of the upper and lower switching devices in each bridge leg during the output current polarity transition. The specific durations of the natural dead time are given in Table V. For example, $T_{d\text{-}L11\text{-}P\text{-}N}$ denotes the natural dead time in the drive signals of the switching devices in leg L_{11} when the output current polarity changes from positive to negative.

B. Dead-Time Elimination High-Frequency Modulation for the Cell With Low-Voltage DC Link

The average output voltage of cell 2 with high-frequency modulation is v_m within each carrier period T_s. As shown in Fig. 4, the signals $0.5v_m$ and-$0.5v_m$ are compared with the triangular carrier wave v_c with an amplitude of $0.5U_2$, generating the output signals P_1 and P_2. The signals P_1 and P_2 are

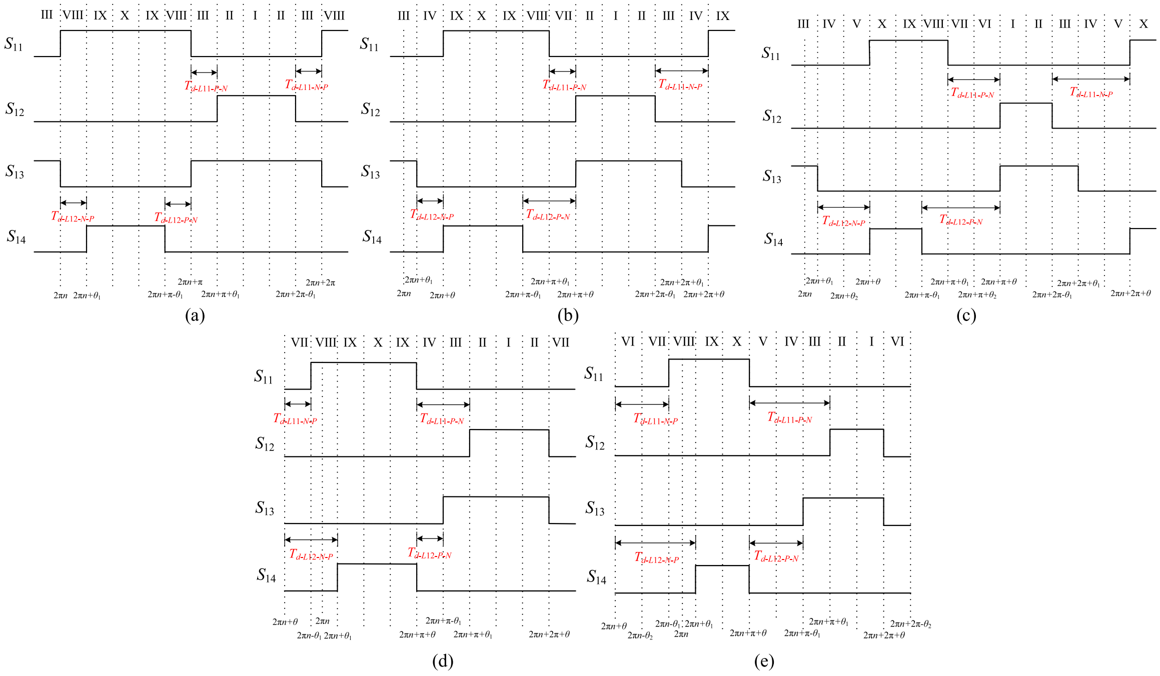


Fig. 3. Drive signals for the four switching devices in cell 1. (a) When $-\theta_1 \leq \theta \leq \theta_1$. (b) When $\theta_1 < \theta \leq \theta_2$. (c) When $\theta_2 < \theta \leq \pi/2$. (d) When $-\theta_2 \leq \theta < -\theta_1$. (e) When $-\pi/2 < \theta \leq -\theta_2$.

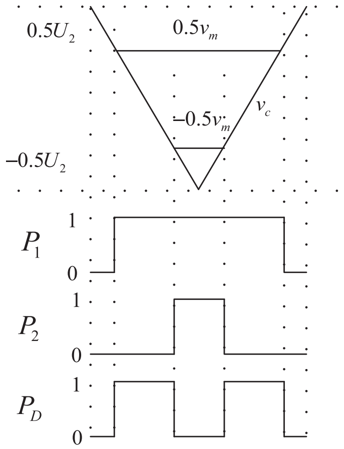


Fig. 4. Generation process of the signal characterizing the average output voltage of cell 2 within one carrier period.

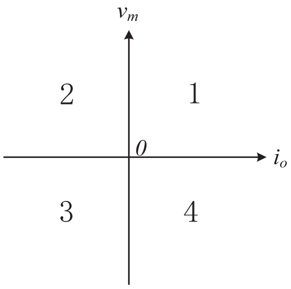


Fig. 5. Operating regions of cell 2.

TABLE VI
DRIVE SIGNALS FOR EACH SWITCHING DEVICE AND CONDUCTING DEVICES IN DIFFERENT OPERATING REGIONS

Regions	S_{21}	S_{22}	S_{23}	S_{24}	Conducting Devices
1	P_D	0	0	1	If P_D=1, S_{21} and S_{24} are ON. If P_D=0, D_{22} and S_{24} are ON.
2	0	$\overline{P_D}$	0	0	If $\overline{P_D}$ =1, S_{22} and D_{24} are ON. If $\overline{P_D}$ =0, D_{21} and D_{24} are ON.
3	0	P_D	1	0	If P_D=1, S_{22} and S_{23} are ON. If P_D=0, D_{21} and S_{23} are ON.
4	$\overline{P_D}$	0	0	0	If $\overline{P_D}$ =1, S_{21} and D_{23} are ON. If $\overline{P_D}$ =0, D_{22} and D_{23} are ON.

processed by an XOR logic operation to generate the signal P_D, which characterizes the average output voltage of cell 2. The instantaneous PWM voltage output of cell 2 is given by $U_2{*}P_D$.

The plane formed by the modulation voltage v_m of cell 2 and the output current i_o is divided into four operating regions as shown in Fig. 5. The leg L_{21} operates at high frequency, while leg L_{22} operates at low frequency. As given in Table VI, the drive signals for each switching device and conducting devices in different operating regions are listed, where $\overline{P_D}$ is the signal obtained by inverting P_D.

Within the fundamental period [0, 2π], the variations of the drive signals for each switching device in cell 2 are shown in Fig. 6. It can be observed that natural dead time exists at the points where the polarity of the output current changes. $T_{d\text{-}L21}$ and $T_{d\text{-}L22}$ represent the natural dead time in the drive signals of the switching devices in leg L_{21} and leg L_{22}, respectively, which can be calculated by (6) and (7). Particularly when the load characteristic is resistive, there is no natural dead time in the drive signals of S_{23} and S_{24}, and additional dead time needs

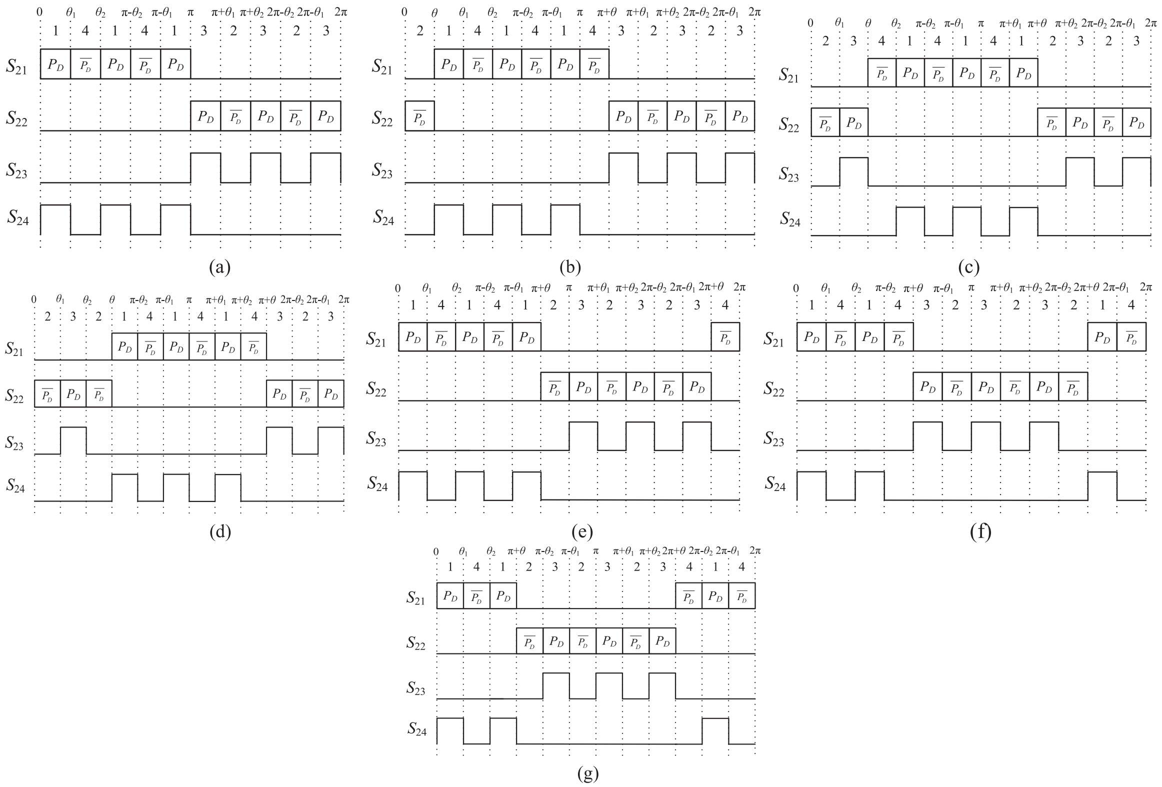


Fig. 6. Drive rules for the four switching devices in cell 2. (a) When $\theta = 0$. (b) When $0 < \theta \leq \theta_1$. (c) When $\theta_1 < \theta \leq \theta_2$. (d) When $\theta_2 < \theta \leq \pi/2$. (e) When $-\theta_1 \leq \theta < 0$. (f) When $-\theta_2 \leq \theta < -\theta_1$. (g) When $-\pi/2 \leq \theta < -\theta_2$.

to be added

$$T_{d-L21} = \begin{cases} 0.25T_s & \text{when } \theta = 0 \\ 0.25T_s - 0.25T_s U \sin\theta / U_2 & \text{when } 0 < \theta \leq \theta_1 \\ 0.25T_s - 0.25T_s (U_1 - U \sin\theta)/U_2 & \text{when } \theta_1 < \theta \leq \theta_2 \\ 0.25T_s - 0.25T_s (U \sin\theta - U_1)/U_2 & \text{when } \theta_2 < \theta \leq 0.5\pi \\ 0.25T_s + 0.25T_s U \sin\theta / U_2 & \text{when } -\theta_1 \leq \theta < 0 \\ 0.25T_s - 0.25T_s (U_1 + U \sin\theta)/U_2 & \text{when } -\theta_2 \leq \theta < -\theta \\ 0.25T_s + 0.25T_s (U_1 + U \sin\theta)/U_2 & \text{when } -0.5\pi \leq \theta < -\theta_2 \end{cases} \tag{6}$$

$$T_{d-L22} = \begin{cases} 0 & \text{when } \theta = 0 \\ \theta / 2\pi f_0 & \text{when } 0 < \theta \leq \theta_1 \\ (\theta_2 - \theta)/2\pi f_0 & \text{when } \theta_1 < \theta \leq \theta_2 \\ (\theta - \theta_2)/2\pi f_0 & \text{when } \theta_2 < \theta \leq 0.5\pi \\ -\theta / 2\pi f_0 & \text{when } -\theta_1 \leq \theta < 0 \\ (\theta_2 + \theta)/2\pi f_0 & \text{when } -\theta_2 \leq \theta < -\theta \\ (-\theta - \theta_2)/2\pi f_0 & \text{when } -0.5\pi \leq \theta < -\theta_2. \end{cases} \tag{7}$$

C. Impacts and Mitigation Of Electrical Parameter Measurement

For cell 1, when the detected voltage U_1 exhibits minor fluctuations, it may cause alternating occurrences between state IX and state X, or between state I and state II. But this has no impact on the drive signals of the switching devices within cell 1. If U_2 measurements display slight variations in the detected voltage, it may cause alternating occurrences between state VIII and state IX, leading to an increased switching frequency of S_{14}; similarly, alternations between state II and state III will result in more frequent switching of S_{12}.

For cell 2, when fluctuations are detected in the dc-side voltages U_1 and U_2, the operating region alternates between region 1 and region 4. Under such conditions, the drive signals of power switching devices S_{22} and S_{23} remain unaffected. However, the switching frequency of S_{24} increases, and the drive signal of S_{21} switches between P_D and $\overline{P_D}$. Additionally, when alternating between operating region 2 and region 3, the switching sequences of S_{21} and S_{24} remain unaffected. However, the switching frequency of S_{23} increases, and the drive signal of S_{22} switches between PD and $\overline{P_D}$.

To avoid phenomena caused by fluctuations in the detected values of U_1 and U_2, the sampling frequency for dc-side voltage measurements is set to the fundamental frequency f_0. Due to the zero drift in the output current detection circuit, the detected value jitters around the current zero-crossing point, leading to repeated alternations in the current polarity detection results. During the jitter process, the drive signals of S_{21} and S_{22} in leg L_{21} will change. Assuming the cell 2 modulation voltage remains approximately constant, and P_D maintains symmetry within a carrier period, the natural dead time between the drive signals of S_{21} and S_{22} remains unchanged. Current polarity detection jitter also does not affect the natural dead time between the drive signals of the two switching devices in leg L_{22}. However, the switching times of S_{23} and S_{24} will increase. The microcontroller unit (MCU) assigns initial values to relevant integer variables during initialization: IPN = 0, IPN_old = 0, IPN_new = 0, IPN_num = 0, IPN_flag = 1. The flowchart of the debounce routine executed within each carrier period T_s is illustrated in

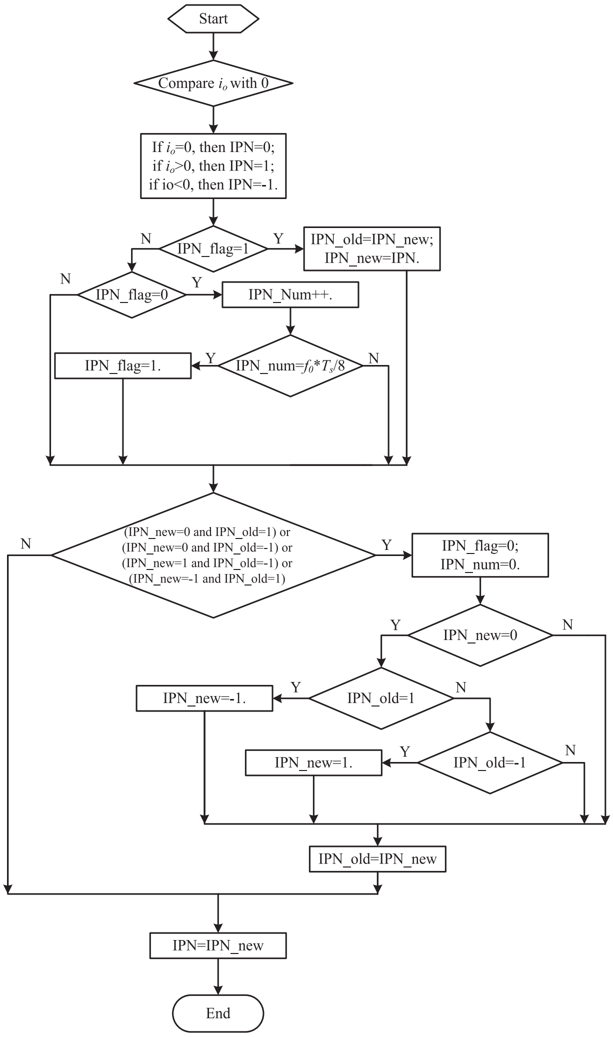


Fig. 7. Flowchart of current polarity detection with debounce.

Fig. 7. Upon detection of an output current polarity alteration, the updated polarity determination is preserved without modification. Polarity detection results are disregarded during the subsequent one-eighth of the fundamental period. A re-evaluation of whether the polarity has been altered is performed only after the output current transitions into a large-signal condition. The debounce routine ensures that the polarity change determination is exclusively triggered once at the output current zero-crossing point. If the current polarity change is prematurely determined, it is inferred from the proposed high-frequency modulation that all switching devices cannot be effectively activated. The current charges the dc link until it decays to zero, after which the switching devices operate to reverse the current polarity.

III. ANALYSIS OF OUTPUT POWER FOR EACH CELL IN CMLI

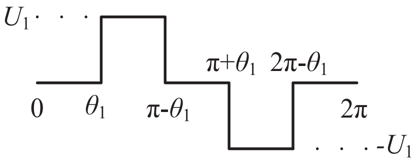


Fig. 8. Output PWM voltage of cell 1.

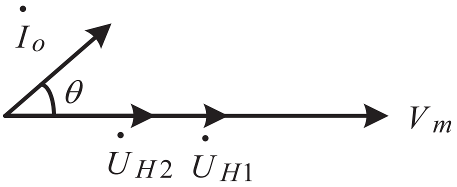


Fig. 9. Vector diagram of fundamental frequency components.

As given in Table II, the output voltage of cell 1 becomes zero when $U \leq U_2$. According to Fig. 3 showing the drive signals of each switching device in cell 1, the output voltage of cell 1 remains independent of load variations within the fundamental period [0, 2π] when $U > U_2$. The corresponding PWM voltage waveform is illustrated in Fig. 8. Through Fourier decomposition analysis, the fundamental component u_{H1} of cell 1's output voltage can be calculated as follows:

$$u_{H1} = \frac{4}{\pi} U_1 \cos\theta_1 \sin 2\pi f_0 \text{when } U > U_2. \tag{8}$$

By neglecting the harmonic components in the output current, the vector relationships of the fundamental frequency components are illustrated in Fig. 9. Under different modulation voltage conditions, the active power output of each cell can be calculated using

$$\begin{cases} P_{H1\_\text{active}}|_{U \leq U_2} = 0 \\ P_{H2\_\text{active}}|_{U \leq U_2} = \frac{1}{2} U I_o \end{cases} \tag{9}$$

$$\begin{cases} P_{H1\_\text{active}}|_{U > U_2} = \frac{2}{\pi} U_1 I_o \sqrt{1 - \left(\frac{U_2}{U}\right)^2} \cos\theta \\ P_{H2\_\text{active}}|_{U > U_2} = \frac{1}{2} \left(U - \frac{4}{\pi} U_1 \sqrt{1 - \left(\frac{U_2}{U}\right)^2} \right) I_o \cos\theta \end{cases} \tag{10}$$

where P_{H1_active} is the active power output of cell 1, and P_{H2_active} is the active power output of cell 2. Combining (1) and (2), the ratio Ra between P_{H1_active} and P_{H2_active} can be calculated as

$$Ra|_{U \leq U_2} = 0 \tag{11}$$

$$Ra|_{U > U_2} = \frac{4km(k+1)\sqrt{(km+m)^2 - 1}}{\pi m^2 (k+1)^2 - 4k\sqrt{(km+m)^2 - 1}}. \tag{12}$$

From (9), when $U \leq U_2$, the active power output of cell1 becomes zero, while the active power output of cell 2 must remain positive. Under this operating condition, no energy backflow to the dc link will occur, and the corresponding parameters k and m must satisfy the following inequalities:

$$\begin{cases} m \leq \frac{1}{(k+1)} \\ 1 \leq k \leq 2. \end{cases} \tag{13}$$

From (10), when $U > U_2$, Cell1's active power output must be positive while cell 2's active power output is also required to be

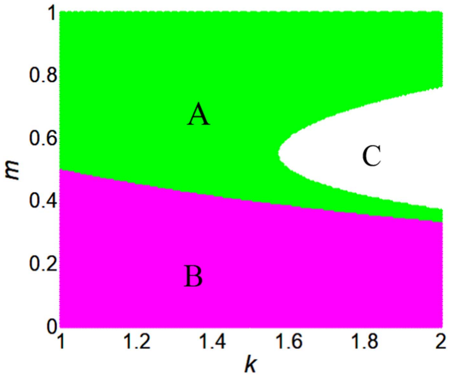


Fig. 10. Three regions obtained by dividing the plane formed by $0 \leq m \leq 1$ and $1 \leq k \leq 2$.

TABLE VII
SIMULATION MODEL PARAMETERS

Parameters	Values
Total voltage of all dc-links (U_1+U_2)	69 V
Carrier frequency f_s	24 kHz
Modulation voltage frequency f_0	50 Hz

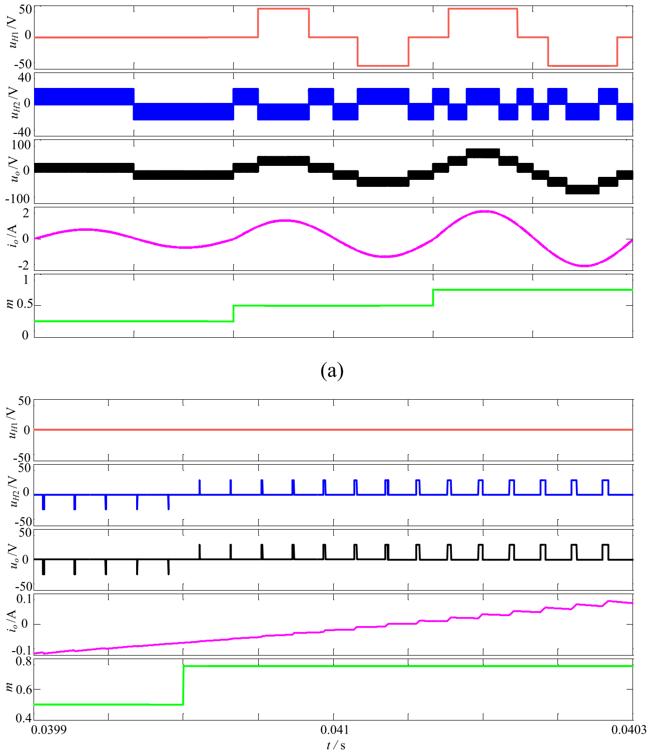
positive. The following constraint relationship must be satisfied:

$$\begin{cases} 1/(k+1) < m \leq 1 \\ \pi m^2(k+1)^2 > 4k\sqrt{k^2m^2+2km^2+m^2-1} \\ 1 \leq k \leq 2. \end{cases} \tag{14}$$

In Fig. 10, the plane formed by $0 \leq m \leq 1$ and $1 \leq k \leq 2$ is divided into three regions. Region A satisfies (14), region B satisfies (13), and the rest is region C. When the parameters k and m fall within region B, the active power output of cell1 is 0, meaning that cell 1 is not being utilized effectively. When operating in region C, cell 2 outputs negative active power, leading to power backflow to the dc link. Therefore, the values of k and m in regions B and C are not advisable, while Region A represents the permissible range.

IV. SIMULATION RESULTS

The model is established in MATLAB/Simulink to verify the proposed modulation, with simulation parameters as specified in Table VII. When $U_1 = 45$V, $U_2 = 24$ V, $m = 0.25, 0.5, 0.75$, and the load is a series connection of an inductor L(5 mH) and a resistor R(30Ω), the output results are given in Fig. 11. It can be found that when $m = 0.25$, $U < U_2$, the output level of cell 1 is zero, and u_o is a three - level PWM voltage. At $m = 0.5$ and $m = 0.75$, Cell1 generates low-frequency PWM voltages. Correspondingly, the output voltage u_o exhibits seven-level and nine-level PWM voltages under these operating conditions. Thus, it can be seen that the power quality of the output voltage and the utilization rate of the dc-link voltage can be improved when $m > U_1/(U_1+U_2)$. Furthermore, the zoom of Fig. 11(a) during the step change of the modulation index m from 0.5 to 0.75 reveals that the simulation model successfully avoids output current zero-crossing jitter.



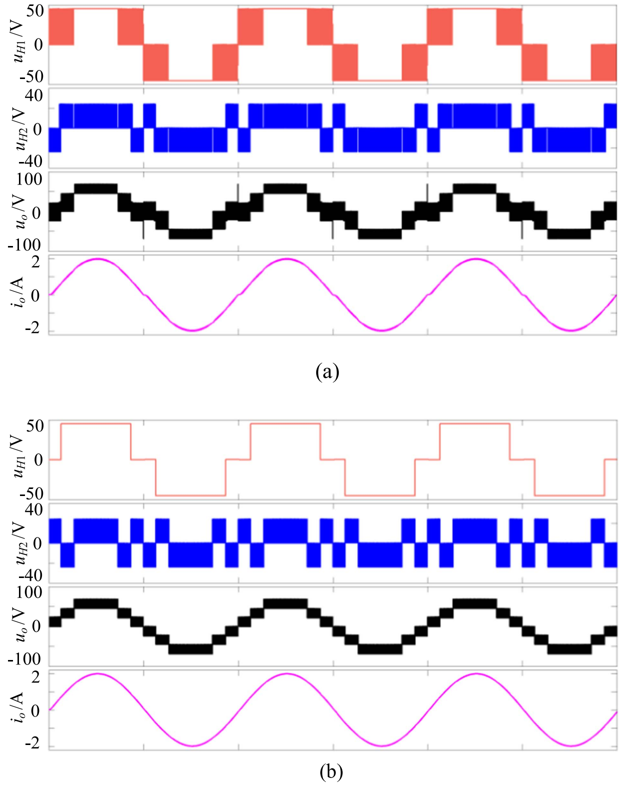
(a)

(b)

Fig. 11. Output results of the CMLI under different modulation coefficients using hybrid frequency modulation. (a) Output results when $m = 0.25, 0.5, 0.75$. (b) Zoom for Fig. 11(a) during the step change of m from 0.5 to 0.75.

When U is set to 60 V ($m = 0.88$) and $k = 1.875$ ($U_1 = 45$V and $U_2 = 24$V), Fig. 12(a) show the output results of the CMLI using LS modulation with dead times of 2 μs. Fig. 12(b) presents the output voltage when hybrid frequency modulation is applied. It can be observed that under LS modulation both cells are operating at high frequency, while under hybrid frequency modulation only one cell is engaged in high-frequency operation. Additionally, the distortion in the output current waveform is caused by the dead time. Fig. 13 presents the FFT analysis results of each output PWM voltage in Fig. 12 respectively. Due to the 180° phase shift between the driving signals of the upper and lower switches in each bridge arm under LS modulation, dead time must be inserted into the driving signals to prevent shoot-through. The dead time inevitably leads to an increase in harmonic content, with a significant rise in THD observed when a dead time of 2 μs is implemented.

The variations of THD in output PWM voltage under HF-PWM and LS–PWM with 2 μs dead time are demonstrated in Fig. 14(a), where k is varied from 1 to 2. When the value of k is the same, the PWM output voltage generated by HF–PWM exhibits lower THD compared to LS–PWM under identical operating conditions. In addition, when employing HF–PWM, the THD of the PWM output voltage decreases monotonically with increasing voltage ratio k. While adopting LS-PWM, the THD of the PWM output voltage demonstrates a non-monotonic variation pattern characterized by an initial decrease followed by a subsequent increase as k escalates.



(a)

(b)

Fig. 12. Output results of the CMLI under different modulation strategies with $m = 0.88$ and $k = 1.875$. (a) Output voltage and current waveforms under level-shifted modulation with a dead time of 2 μs. (b) Output voltage and current waveforms under hybrid frequency modulation.

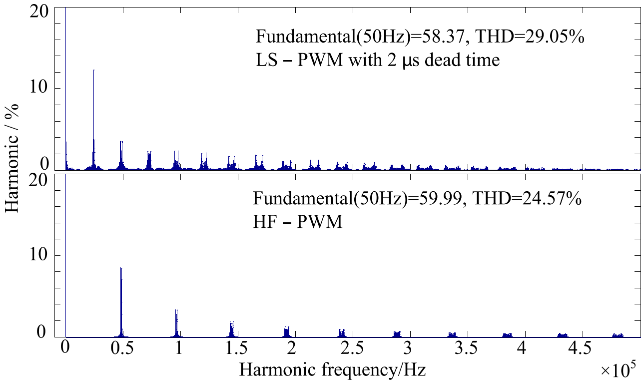
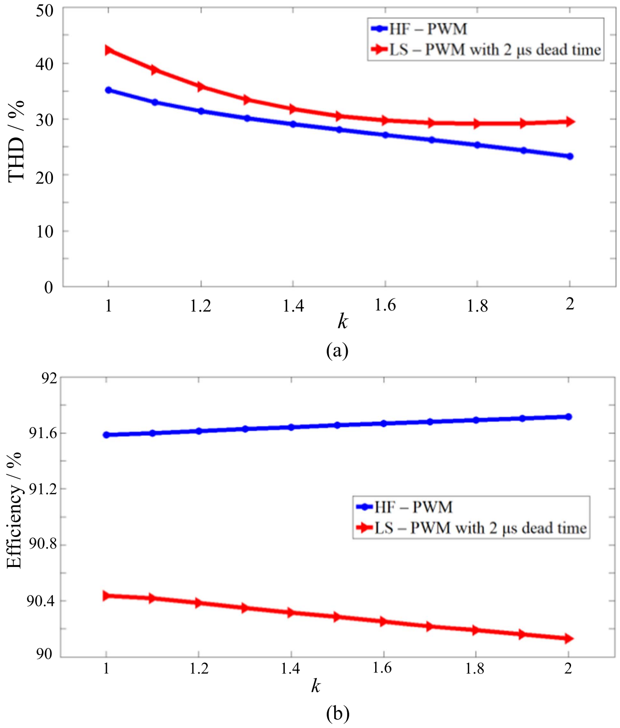


Fig. 13. FFT analysis results of each output PWM voltage in Fig. 12 respectively.



(a)

(b)

Fig. 14. Simulation comparison results of THD in output PWM voltage and efficiency of CMLI under different modulation strategies. (a) Variations of THD in PWM output voltage as k increases from 1 to 2. (b) Efficiency variations as k increases from 1 to 2.

TABLE VIII
CORRESPONDING RELATIONSHIP BETWEEN LOAD PARAMETERS AND POWER ANGLE

θ	R	L	C
17.43°	5 Ω	5 mH	/
57.51°	1 Ω	5 mH	/
–17.89°	5 Ω	5 mH	1000 μF
–58.23°	1 Ω	5 mH	1000 μF

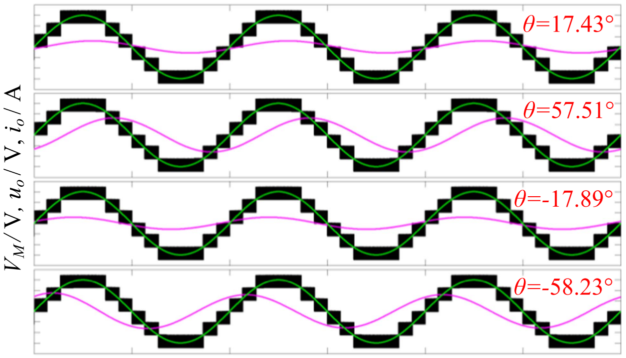


Fig. 15. Test results of hybrid frequency modulation under different load characteristics.

The comparison simulation results of CMLI efficiency under different modulation strategies, considering switching losses, are shown in Fig. 14(b). It can be observed that under identical test conditions, the efficiency of the HF-PWM CMLI is higher than that of the LS-PWM CMLI. Moreover, as the voltage ratio k increases, the efficiency of the HF-PWM CMLI improves, whereas the efficiency of the LS-PWM CMLI decreases.

By selecting *RL* or *RLC* as the load configuration, diverse load characteristics can be achieved through parameter adjustments. The corresponding relationship between load parameters and power angle θ is given in Table VIII. The test results of hybrid frequency modulation under different load characteristics are illustrated in Fig. 15. In the figure, the black waveform represents the output voltage u_o, the red waveform corresponds to the output current i_o, and the green waveform depicts the modulation voltage V_M. These results conclusively demonstrate that the proposed hybrid frequency modulation exhibits adaptability to diverse load characteristics.

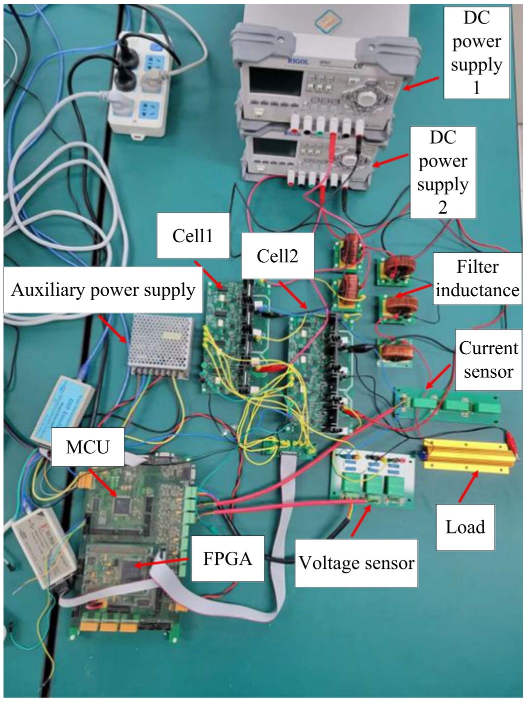


Fig. 16. Experimental prototype.

TABLE IX
EXPERIMENTAL PARAMETERS

Specifications	Values
U_1	45 V
U_2	24 V
f_0	50 Hz
U	60 V
f_s	24 kHz
R	30 Ω
L	5 mH

TABLE X
MODELS OF KEY COMPONENTS

Components	Models
MCU	TMS320F28335 from Texas Instruments
FPGA	XC3S400-5PQG208C from Xilinx
IGBT	GT60M303 from Toshiba
Optocoupler	HCPL-316J
Voltage sensor	HNV025A
Current sensor	HNC50LA

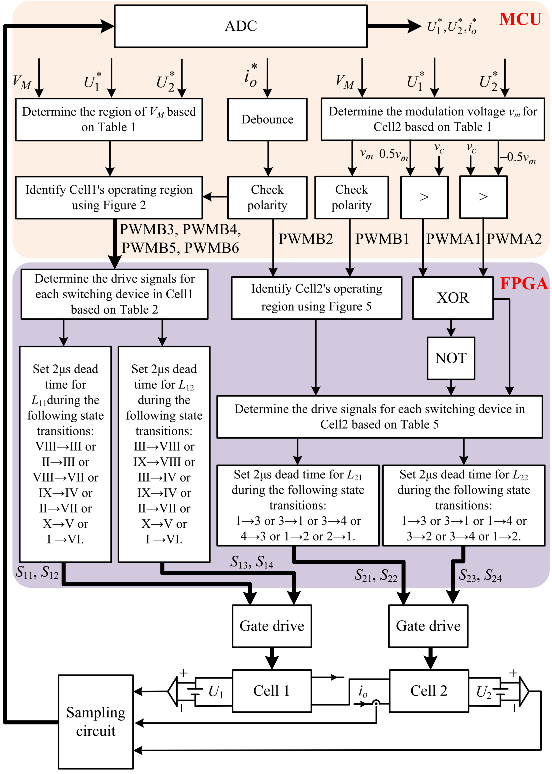


Fig. 17. Block diagram of the system structure.

V. EXPERIMENTAL RESULTS

The experimental prototype, as shown in Fig. 16, is utilized to validate the effectiveness of the proposed hybrid frequency modulation. The experimental parameters are given in Table IX. The experimental prototype is composed of the main power circuit and the control circuit. The main power circuit includes two adjustable dc power supplies with a range of 0–60 V and a maximum output current of 2A, two IGBT-based H-bridge power conversion modules, and a load formed by an inductor and a resistor connected in series. The control circuit consists of LEM voltage and current sensors for measuring actual electrical parameters, IGBT gate drive circuits based on optocoupler devices, and a digital control unit combining an MCU and an field-programmable gate array (FPGA). The models of key components are given in Table X. The tasks executed by the MCU and FPGA are illustrated in Fig. 17.

When the period value of the MCU timer is reached, the built-in ADC conversion module is triggered to obtain the sampled values U_1^*, U_2^* and i_o^* of U_1, U_2 and i_o. Upon ADC conversion completion, the program enters the ADC interrupt subroutine. The current i_o^* is processed through the debounce routine to determine the output current polarity, which is then output via the external pin PWMB2. The relationship between polarity of i_o and voltage level is defined by the following equation:

$$\mathrm{PWMB2} = \begin{cases} 1 & \text{when } \ i_o \geq 0 \\ 0 & \text{when } \ i_o < 0. \end{cases} \tag{15}$$

Based on Fig. 2, the operating region X of Cell1 is determined by V_M and the polarity of i_o. This region X is output through external pins PWMB3, PWMB4, PWMB5 and PWMB6. The correlation between the pin levels and operating region X is mathematically represented by the formula below:

$$X = \mathrm{PWM}B3 * 2^3 + \mathrm{PWM}B4 * 2^2 + \mathrm{PWM}B5 * 2^1 + \mathrm{PWM}B6 * 2^0 + 1. \tag{16}$$

The modulation voltage v_m of cell 2 is calculated based on Table II, and its polarity is output through the external pin PWMB1. The relationship between polarity of v_m and

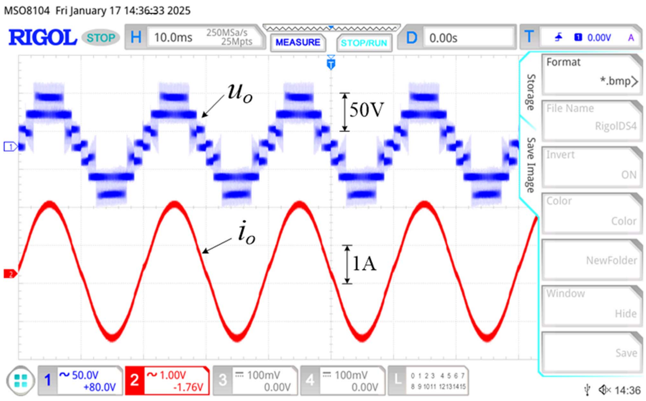


Fig. 18. Waveforms of the output PWM voltage and current.

voltage level is expressed by the following equation:

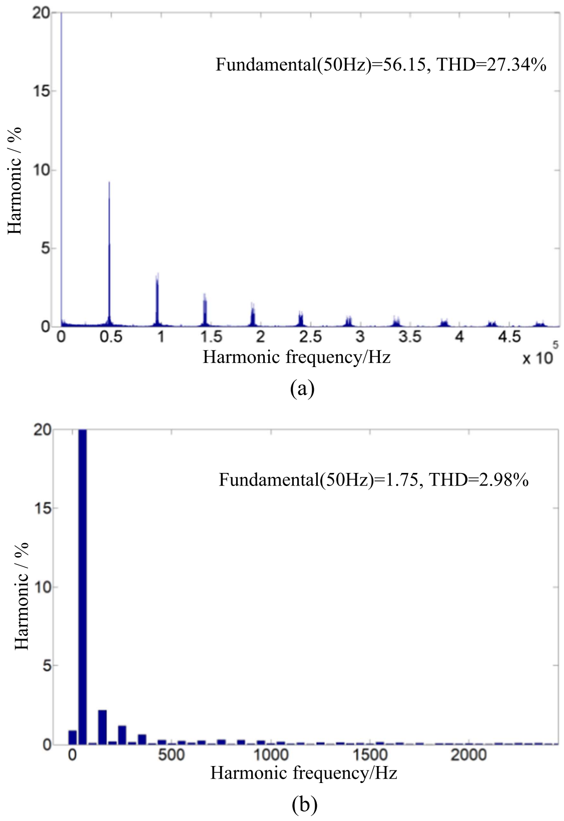
$$\text{PWMB1} = \begin{cases} 1 & \text{when } \; v_m \geq 0 \\ 0 & \text{when } \; v_m < 0. \end{cases} \tag{17}$$

The MCU timer operates in up-down mode with a period value of P, generating a triangular carrier wave v_c. The signals $0.5v_m$ and $-0.5v_m$ are normalized to the range of 0 to P. The PWM signals obtained by comparing $0.5v_m$ and $-0.5v_m$ with the triangular carrier wave are output through external pins PWMA1 and PWMA2 respectively. The level signals output by the MCU are updated simultaneously when the timer period value is reached.

The waveforms of the output PWM voltage and current are displayed in Fig. 18. It can be observed that the output voltage exhibits a nine-level characteristic, while the current waveform approaches a sine wave.

The results of the FFT analysis on the output PWM voltage and current are presented in Fig. 19. Fig. 19 reveals that the output voltage has a fundamental component amplitude of 56.15 V with an absolute error of 3.85 V and a THD of 27.34%, while its harmonic components are concentrated at 48 kHz, aligning with simulation results. Additionally, the output current exhibits a significantly lower THD of only 2.98%. As shown in Fig. 20, the output results without debounce processing for current polarity detection exhibit significant waveform distortion near the current zero-crossing points.

Fig. 21 shows the driving signals of the switching devices in cell 1. The signal frequency is observed to be 50 Hz. Furthermore, as indicated in the zoom view, the natural dead times between the driving signals of the upper and lower switching devices in legs L_{11} and L_{12} are measured to be approximately 1150 and 1500 μs, respectively. The driving signals of the switching devices in cell 2 are illustrated in Fig. 22. A high-frequency operation of 48 kHz is identified for leg L_{21}, while a low-frequency operation of 150 Hz is detected for leg L_{22}. Also, from the zoom view, the natural dead times between the upper and lower switching devices driving signals in legs L_{21} and L_{22} are observed with measured durations of approximately 10 and 125 μs, respectively. It is thus demonstrated that the natural dead times of all legs exceed the preset 2 μs threshold. The predefined dead time settings have no impact on the driving signals of switching devices, thereby maintaining the CMLI in a completely dead-time-free operational state.



(a)

(b)

Fig. 19. Results of the FFT analysis on the output PWM voltage and current. (a) Result of the FFT analysis on the output PWM voltage. (b) Result of the FFT analysis on the output current.

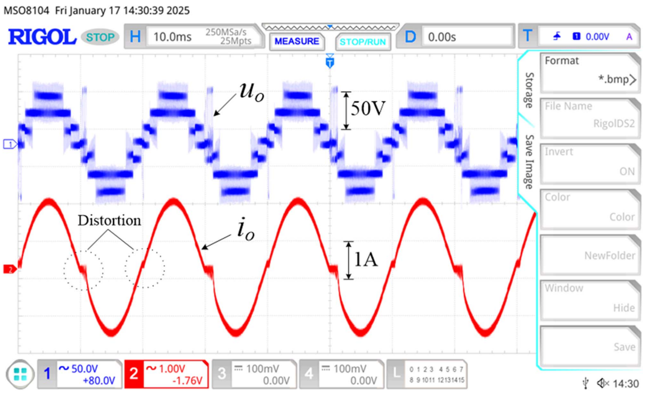


Fig. 20. Output results without debounce processing for current polarity detection.

The performance of hybrid frequency modulation against dc-link voltage fluctuations is experimentally validated in Fig. 23. Figure 23(a) and (b) demonstrates test conditions where the dc-link voltage of cell 1 abruptly changes between 38 and 48 V, while Fig. 23(c) and (d) presents scenarios with Cell2's dc-link voltage transitioning between 23V and 33 V. Notably, the output current waveforms are observed to maintain fundamental stability throughout the dc-link voltage variations.

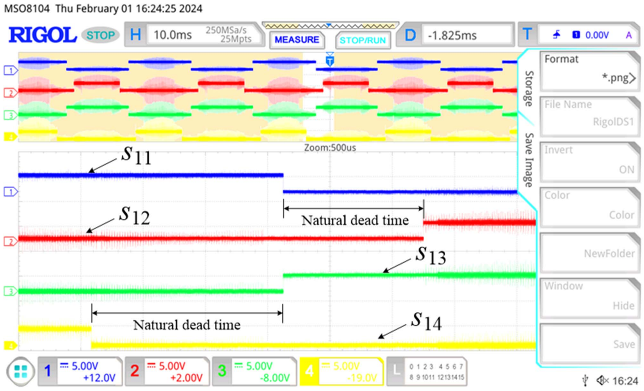


Fig. 21. Driving signals of the switching devices in cell 1.

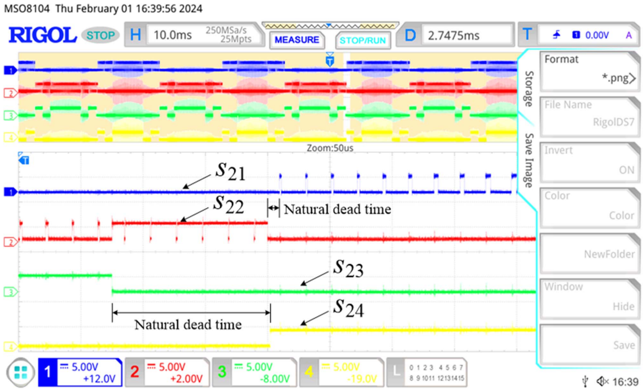
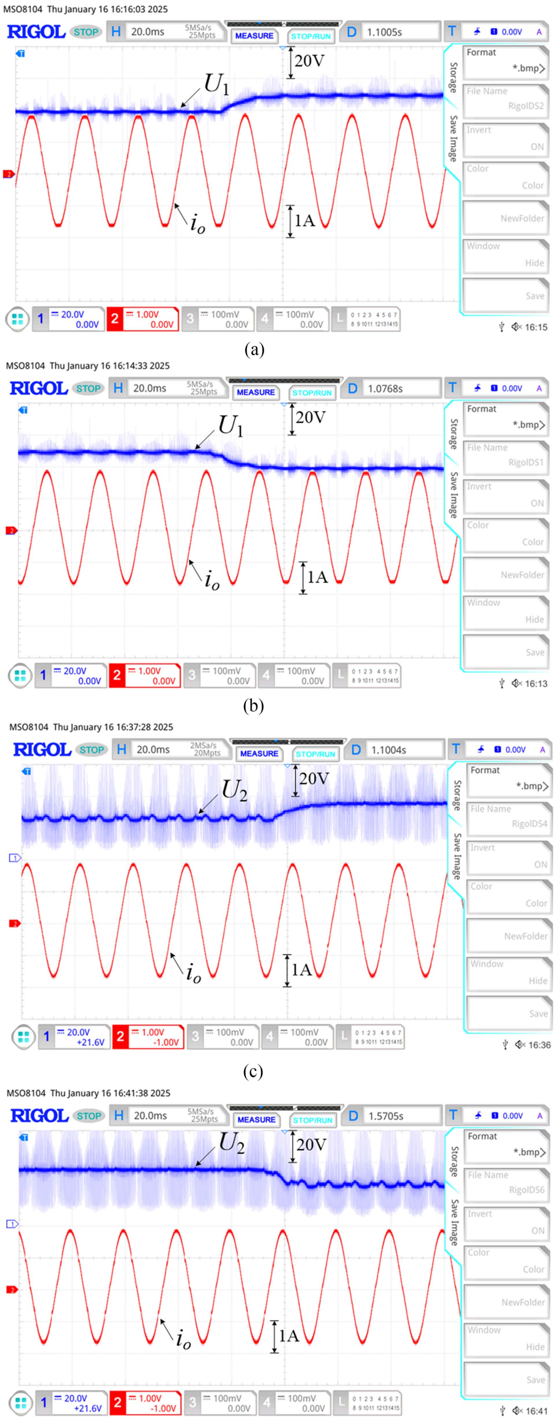


Fig. 22. Driving signals of the switching devices in cell 2.

The dynamic test results of CMLI initial start-up and sudden load step are illustrated in Fig. 24. As shown in Fig. 24(a), during the start-up phase, the two dc-link voltages transition from $U_1 = 45$V, $U_2 = 0$ V to $U_1 = 45$ V, $U_2 = 24$ V, while the output voltage u_0 immediately shifts from an irregular low-frequency voltage to the desired high-frequency PWM voltage. As can be seen from the dynamic test for sudden load step shown in Fig. 24(b), during the transition of the load resistance from 60 to 30 Ω, the voltage across the load only exhibits slight fluctuation during the switching transient and then remains stable.

The comparison results of THD in output PWM voltage and efficiency of CMLI under different modulation strategies are shown in Fig. 25. It is evident from Fig. 25(a) that the CMLI employing HF-PWM exhibits a lower THD in its output PWM voltage. Fig. 25(b) demonstrates that under identical test conditions, as the voltage ratio k increases from 1 to 2, the efficiency of CMLI adopting HF-PWM increases accordingly and surpasses that of CMLI using LS-PWM.

Compared with the simulation model, the operation results of the experimental prototype are affected by the nonlinear characteristics and measurement errors. By comparing the results in Figs. 12(b) and 18, it can be observed that the CMLI outputs a nine-level PWM voltage in both scenarios. However, the output current in the simulation results exhibits no distortion at the zero-crossing point, whereas slight distortion is present in the experimental results. Comparing the results in Fig. 13(b) and Fig. 19 reveals that the harmonic distributions of the output PWM voltage waveforms exhibit close alignment. Specifically, the matching degrees between simulation and experimental results for the fundamental amplitude and THD are calculated as 56.15/59.99 = 93.6% and 24.57/27.34 = 89.9%, respectively.



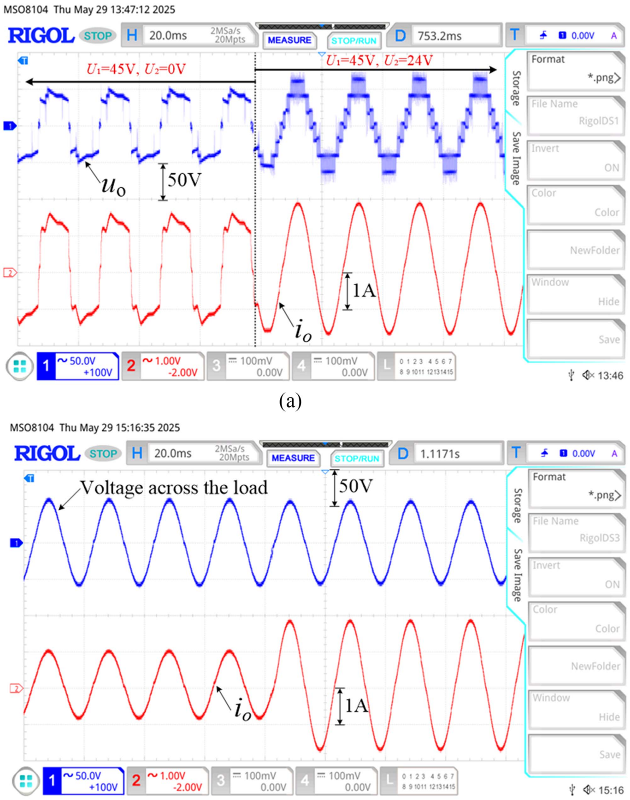
(a)

(b)

(c)

(d)

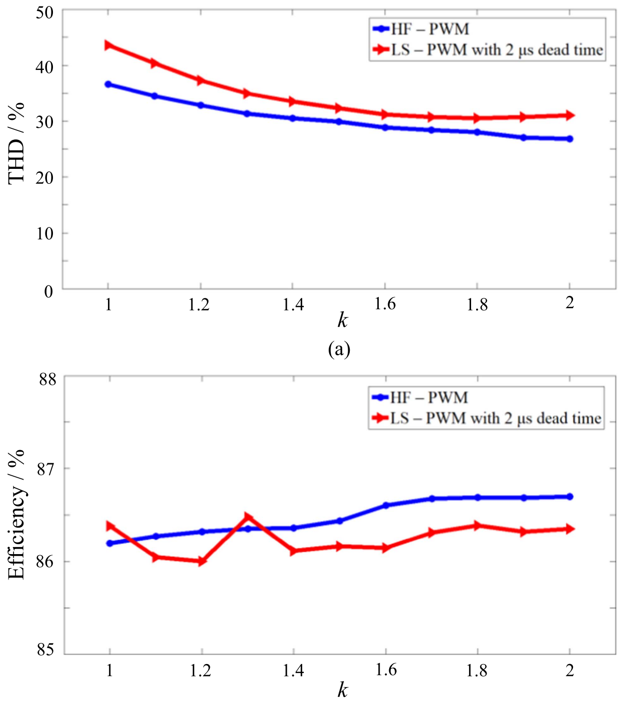
Fig. 23. Test results of the performance of the hybrid frequency modulation against DC-link voltage fluctuations. (a) Output current waveform when U_1 changes from 38 V to 48 V. (b) Output current waveform when U_1 changes from 48 V to 38 V. (c) Output current waveform when U_2 changes from 23 V to 33 V. (d) Output current waveform when U_2 changes from 33 V to 23 V.



(a)

(b)

Fig. 24. Dynamic test results of CMLI initial start-up and sudden load step. (a) Output results of the initial start-up phase. (b) Output results of the transient process during switching the load from 60Ω to 30Ω.



(a)

(b)

Fig. 25. Comparison results of THD in output PWM voltage and efficiency of CMLI under different modulation strategies. (a) Variations of THD in PWM output voltage as k increases from 1 to 2. (b) Efficiency variations of CMLI as k increases from 1 to 2.

Regarding the variations of THD in PWM output voltage as k increases from 1 to 2, the experimental results in Fig. 25(a) exhibit strong agreement with the simulation outcomes shown in Fig. 14(a). The difference from the experimental results in Fig. 25(b) is that the simulation efficiency results in Fig. 14(b) are approximately 4% higher than the experimental efficiency, and the linearity of the simulation efficiency curve is better, while there is similarity in the overall trend of the curves.

VI. CONCLUSION

The multilevel hybrid frequency modulation is proposed for two-cell CMLI in this article. The proposed HF-PWM is composed of region-segmented low-frequency modulation for the cell with high-voltage dc link and dead-time-eliminated high-frequency modulation for the cell with low-voltage dc link. The main contributions can be highlighted as follows.

1) The driving strategy for the four switching devices in each cell that can self-adapt to dc-link voltage fluctuations is proposed. Additionally, based on the driving strategy, the variation pattern of the driving signal for each switching device within each fundamental period under different load characteristics are revealed.
2) The natural dead-time existing in the upper and lower switch gate drive signals of each leg under hybrid frequency modulation are derived.
3) To address the zero-drift issue in the output current detection circuit, this article proposes an effective debouncing scheme for current zero-crossing detection.
4) Theoretical derivations of output power for each cascaded cell are conducted in the article, with operational constraints provided to avoid current backflow.

Finally, the effectiveness of hybrid frequency modulation was rigorously demonstrated through both simulation and experimental results.

Building upon the solution framework proposed in this article, the future work will focus on developing a generalized hybrid frequency modulation applicable to multilevel converters with three or more cascaded cells.

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