Letters

Low-Power Power Management Unit With Adaptive Dynamic Load Power Tracking for Millimeter-Scale Computing Systems

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***Abstract*—This article proposes a power management unit (PMU) for a millimeter-scale, multilayer-stacked computing system, designed to efficiently manage significant load current variations between low-power sleep mode and high-performance active mode. The system ensures a reliable power supply across different chip layers, rapidly increasing output driving strength in response to active-mode requests from any layers. In addition, the circuit adaptively manages the switching frequency of its power converters for dynamic frequency scaling, compensating for temperature changes by using an oscillator that replicates the processor's clock. The proposed design is fabricated using a 180-nm process and integrated with other chip layers in a millimeter-scale system. The system's PMU eliminates voltage drop during transitions to active mode by utilizing a constant energy-per-cycle oscillator with a wide frequency range of 1.89 Hz–104 MHz, along with a replica oscillator of the processor. It achieves over 50% power conversion efficiency across a load power range of 41 nW–409 μW.**

***Index Terms*—Adaptive frequency scaling, canary oscillator, millimeter-scale computing system, power management.**

I. Introduction

THE trend toward miniaturizing computing systems has led to the widespread adoption of small Internet-of-Things devices in daily life. Recently, these systems have been scaled down to the millimeter range, enabling innovative sensing applications in ecological, biomedical, and security domains [1], [2], [3]. For example, Fig. 1 illustrates a millimeter-scale, layer-stacked system constructed by vertically stacking bare dies to maximize planar circuit area within a constrained volume [1], [4], [5].

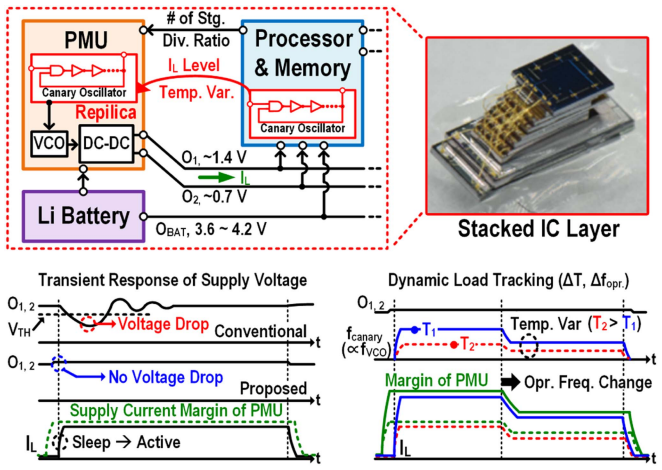

Fig. 1. Millimeter-scale computing system and significant voltage drop in the PMU induced by the load current change.

However, as computing systems are miniaturized, battery capacity is also reduced, limiting the energy available to power these systems. For instance, a 9.8-mm^2 thin-film lithium battery can store only 15 μAh of charge [6], supporting an average current draw of just 21 nA (equivalent to 84 nW), which allows for a system lifetime of only one month. Moreover, these lithium batteries often provide a higher voltage (e.g., 4 V) than standard complementary metal-oxide-semiconductor (CMOS) transistors can safely handle, necessitating a highly efficient power management unit (PMU) to convert the battery's voltage to a lower, more manageable level (under 1.8 V).

Given the constraints on size, PMUs for these compact systems are typically designed with on-chip capacitors [4], [7], [8], [9] rather than bulkier discrete inductors [10]. To minimize average power consumption, these systems operate on a duty

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cycle, turning-OFF most circuits during sleep mode. The PMU must convert power efficiently, handling power levels ranging from tens of nW in sleep mode to tens or hundreds of μW in active mode [4].

Previous research [7] adaptively controls the switching frequency of the power converter in a feedback loop by monitoring the output voltage. When a sudden change in load current occurs, such as transitioning from sleep-to-active mode, the system detects a voltage drop exceeding a predetermined threshold and maximizes the switching frequency, as shown in Fig. 1. A small threshold reduces the output voltage drop but also increases the risk of noise during sleep mode, which can erroneously initiate high-speed switching, causing significant energy loss. Similarly, while multiphase and feedforward methods [11] enhance the load transient response of switched-capacitor (SC) converters, they also increase design complexity and the controller's power consumption. A preemptive control scheme [12] was proposed to improve the dynamic response of the PMU by forecasting and adjusting the inductor current in advance based on the system's repetitive load pattern. A similar approach is introduced in [13], where load transition signals are fed into the feedback loop to combine feedforward and predictive control for managing large load current steps in inductive dc–dc converters. However, when the load behavior deviates from the learned profile, the system must undergo a recalibration process, which limits adaptability. Moreover, due to the inherent delay in changing the inductor current, voltage droop or overshoot can still occur during transient events.

Therefore, it is crucial to develop a PMU that can efficiently down-convert the battery voltage to a stable level, ensuring high power conversion efficiency (PCE) across varying temperatures and operation frequency, while also preventing energy loss due to output voltage noise.

This article discusses a low-power PMU for a millimeter-scale, multilayer-stacked computing system designed to handle significant load current variations between low-power sleep mode and high-performance active mode, introduced in [9]. Adaptive frequency scaling using output feedback and a replica oscillator enables the PMU to anticipate mode transitions via early signals from the processor. This dynamic predictive control not only minimizes voltage drop during mode transitions but also closely tracks the application's actual power consumption during active mode, improving PCE. Furthermore, since the replica oscillator inherently reflects temperature-induced frequency shifts as shown in Fig. 1, the PMU adaptively adjusts its power delivery without requiring additional compensation circuits. This article is significantly different from [9] by focusing on PMU's adaptive operation with nonlinear relationship between replica oscillator and PMU's frequencies and their mismatch impacts.

II. Overall Architecture and Operation of Adaptive Dynamic Load Power Tracking

Fig. 2 presents a block diagram of the proposed PMU, which effectively manages significant load current changes between low-power sleep mode and high-performance active mode. Conventional feedback loop control mechanisms, which adjust a voltage-controlled oscillator (VCO) frequency in response to regulated voltage changes, struggle to prevent significant voltage drops when transitioning from sleep to active mode. This is due to the delayed increase in the control voltage of the VCO compared to the rapid load current changes. To address this issue, the proposed PMU synchronizes the mode transition with the bus communication of the computing system. It rapidly increases the switching frequency in proportion to the processor and memory controller's clock frequencies, which dominate power consumption in the 1.5 and 0.7 V power domains during active mode, using a canary oscillator replicated from the processor layer.

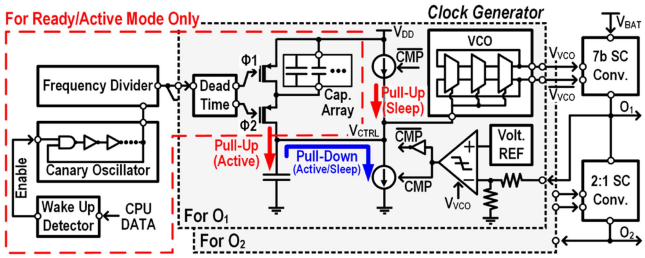


Fig. 2. Overall architecture of the proposed PMU with the adaptive dynamic load power tracking method.

The proposed PMU integrates an SC dc–dc converter that steps down the Li-ion battery voltage (3.6–4.2 V) to 1.5 and 0.7 V for digital logic. It supports wide power delivery and fast feedback control using a leakage-based VCO built on a constant energy-per-cycle ring oscillator (CERO) [14]. This VCO provides a wide frequency range, from hundreds of Hz to tens of MHz, while consuming low power. Leveraging this range and the voltage conversion ratio, the PMU sustains high PCE across sleep (nW) to active modes (tens to hundreds of μW).

A. Frequency Acceleration With the Canary Oscillator

The proposed PMU controls the VCO frequency of the SC converter by using both the feedback from the output voltage (O_1) and the operation frequency information of the processor and memory. The PMU preemptively increases the VCO frequency of the SC converter before the main system enters active mode. Fig. 2 illustrates the VCO control voltage (V_{CTRL}) generator, which consists of a "For Ready/Active Mode Only" part and a conventional feedback loop part that monitors the output voltage. The frequency acceleration technique sets V_{CTRL} through pull-up and pull-down charge balancing, synchronized by the canary oscillator with a capacitor array and the current sinking operation of the charge pump.

Fig. 3 illustrates the operation details of capacitive switching used for pull-up (active) using a canary oscillator during frequency acceleration. Different from a straight-forward design with linear relationship between canary oscillator and VCO frequencies [see Fig. 3 (left)], the proposed circuit provides V_{CTRL} boosting with small nonlinearity on purpose [see Fig. 3 (middle)]. In the first phase ($\emptyset_1$), the stored charge in C_{UP} is 0, while C_{CTRL} holds a charge of $C_{\mathrm{CTRL}} \times V_{\mathrm{CTRL}}$. In the

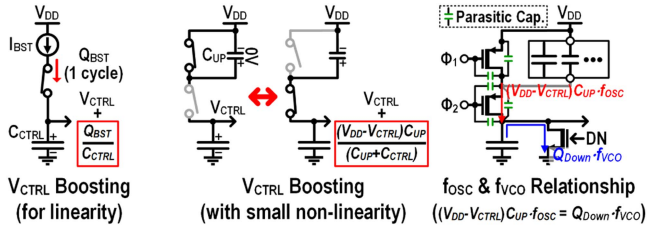
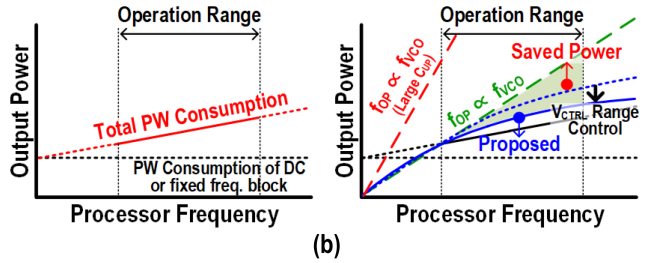


Fig. 3. Switching operation of V_{CTRL} boosting.

	VCO clock frequency synchronized with the canary oscillator (f_{OSC}, kHz)							
	1	10	100	1k	10k	100k	1M	10M
V_{CTRL} (V)	0.151	0.245	0.336	0.42	0.518	0.64	0.831	1.24
f_{VCO} (MHz)	15.59	145.8	1.28k	10.7k	106k	773k	7.22M	46.5M
f_{VCO}/f_{OSC}	**15.59**	**14.58**	**12.8**	**10.7**	**10.63**	**7.73**	**7.22**	**4.65**

(a)



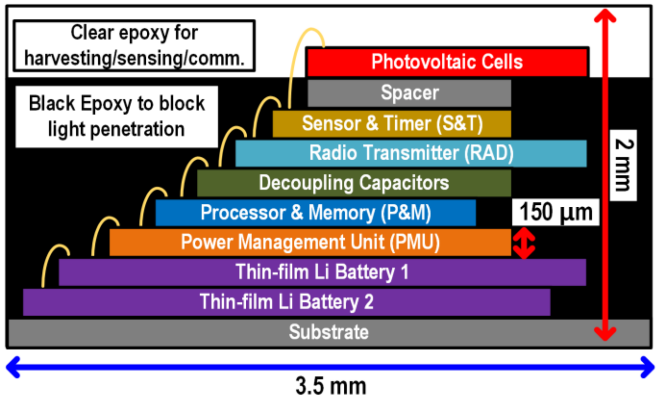
(b)

Fig. 4. Relationship between the canary oscillator and VCO. (a) V_{CTRL} voltage and VCO frequency versus canary OSC frequency. (b) Case of power reduction according to the $f_{\mathrm{VCO}}/f_{\mathrm{OSC}}$ ratio decreasing.

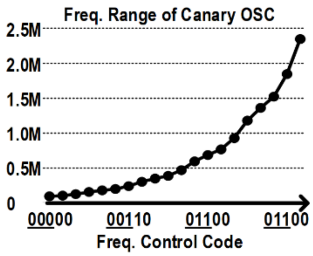
next phase, the voltage V_{CTRL} across C_{CTRL} increases due to charge sharing with C_{UP}, which is connected to V_{DD}. Although parasitic capacitances of the MOSFET switch, such as gate–source (C_{GS}), gate–drain (C_{GD}), and drain–source (C_{DS}), introduce coupling and charge sharing effects during the boosting operation [as illustrated in Fig. 3 (right)], their impact is negligible since C_{GS} and C_{GD} are about 1–2 fF and C_{DS} is around 1 aF, all of which are much smaller than C_{UP} (∼100 fF, tunable) and C_{CTRL} (∼7.2 pF). The increased voltage ΔV can be expressed as follows:

$$\Delta V = \frac{(V_{DD} - V_{\mathrm{CTRL}}) \cdot C_{\mathrm{UP}}}{(C_{\mathrm{UP}} + C_{\mathrm{CTRL}})}. \tag{1}$$

Equation (1) shows that the V_{CTRL} level affects ΔV, which in turn impacts the linear relationship between the oscillation frequency of the canary oscillator and the VCO. As V_{CTRL} changes by about 1.089 V when the canary oscillator frequency shifts from 1 Hz to 10 MHz [as shown in Fig. 4(a)], the nonlinear factor reduces the ratio between the VCO frequency (f_{VCO}) and the canary oscillator frequency (f_{OSC}) introduced by V_{CTRL}. As shown in Fig. 4(b), this operating method improves energy efficiency by allowing a smaller power supply margin compared to an approach where f_{VCO} and f_{OSC} are strictly proportional, with the slope of their relationship controlled by the capacitor array responsible for V_{CTRL} boosting, as shown in Fig. 3 (right).



(a)



Frequency Control Code		Code (Number of Stage)			
		00(13)	01(11)	10(9)	11(7)
Code (Division Ratio)	000(*16)	86.2k	96.4k	117k	149k
	001(*8)	172k	193k	234k	298k
	010(*4)	345k	386k	468k	596k
	011(*2)	689k	771k	937k	1.19M
	100(*1)	1.38M	1.54M	1.87M	2.39M

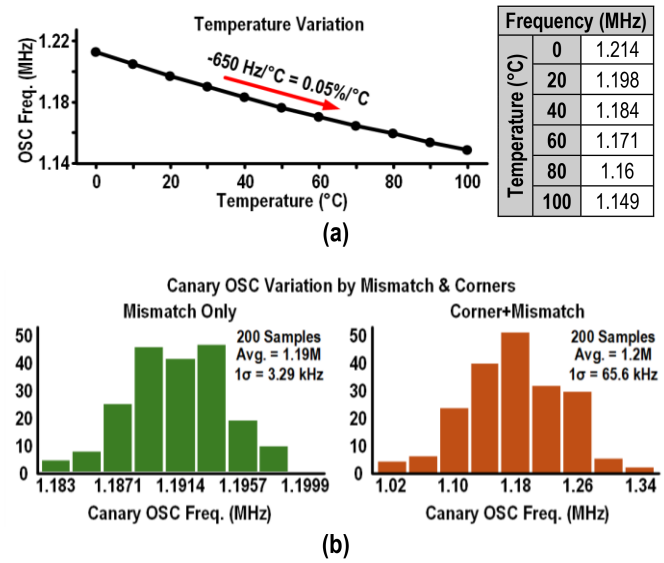
(b)

Fig. 5. (a) Layer structure of the millimeter-scale computing system. (b) Operation frequency of the canary oscillator.

This is because certain blocks in the computing system, such as always-ON circuits, draw nearly constant current regardless of operating mode. In addition, in the case of CERO, the extent of frequency variation due to V_{CTRL} is influenced by how much of the target f_{VCO} range lies within the subthreshold versus saturation region. In the implemented design, V_{CTRL} spans both regions, and by adjusting the proportion of operation in each, the system can control the degree of nonlinearity: a higher subthreshold ratio results in weaker nonlinearity, while a higher saturation ratio enhances it, enabling flexible tuning of the $f_{\mathrm{VCO}}/f_{\mathrm{OSC}}$ relationship.

B. Temperature and Process Variation of the Oscillator

The proposed system integrates nine thinned dies (<1.35 mm × 3.10 mm × 150 μm each) and two chip-scale rechargeable batteries into a compact 3.5 mm ×1.5 mm × 2.0 mm form factor, encapsulated in dual-color epoxy for protection, as shown in Fig. 5(a) [5]. Although temperature-induced frequency variation between the processor's oscillator and the canary oscillator within the PMU can potentially affect synchronization, its practical impact remains negligible in this application. In the millimeter-scale computing system, the processor and memory chip are stacked directly above the PMU, as shown in Fig. 5(a). For thermal estimation, we assume that the processor die has the same area as the PMU die (2500 μm × 1050 μm), with a chip thickness of 150 μm and an interdie epoxy thickness of 15 μm. Since heat primarily flows through the silicon substrate rather than through the gate oxide or interconnect layers, the thermal conductivity of bulk silicon [15] [148 W/(m·K)] is used for the chip, while 0.14 W/(m·K) is used for the epoxy. Based on



Temperature (°C)	Frequency (MHz)
0	1.214
20	1.198
40	1.184
60	1.171
80	1.16
100	1.149

Fig. 6. (a) Temperature variation of the canary oscillator. (b) Monte Carlo simulation results considering the mismatch and corner of the canary oscillator.

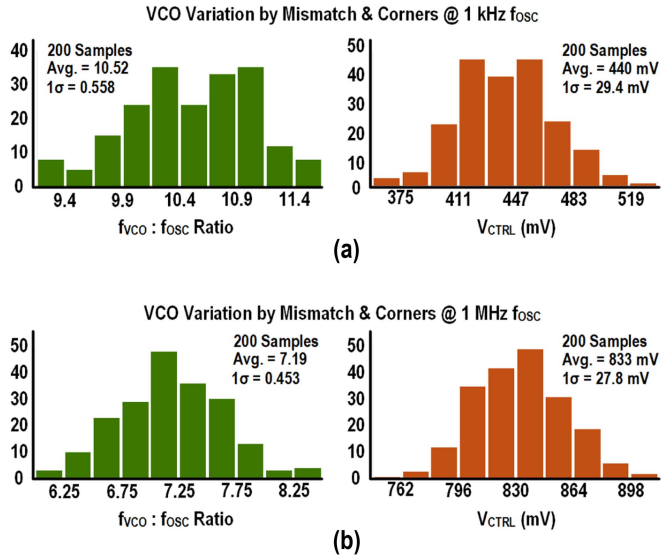


Fig. 7. (a) Monte Carlo simulation results of the f_{VCO}:f_{OSC} ratio and the V_{CTRL} voltage at $f_{\mathrm{OSC}} = 1$ kHz. (b) Monte Carlo simulation results of the $f_{\mathrm{VCO}}/f_{\mathrm{OSC}}$ ratio and the V_{CTRL} voltage at $f_{\mathrm{OSC}} = 1$ MHz.

these values, the vertical thermal resistances are approximately 0.386 K/W for the silicon layer and 40.8 K/W for the epoxy layer. The total thermal resistance is thus estimated to be about 41.2 K/W.

If we consider that the processor power consumption is under 1 mW, then the resulting temperature difference between the processor and the PMU is lower than 0.1 °C. Furthermore, simulation data in Fig. 6(a) show the frequency variation of the canary oscillator to be approximately 650 Hz/°C (∼0.05% of 1.19 MHz at 27 °C), confirming that temperature effects can be safely neglected in the proposed PMU frequency tracking scheme.

However, the canary oscillator embedded in the PMU chip layer and the one in the processor chip layer exhibit differences in operating characteristics due to mismatch and corner variations, leading to errors in the synchronization between the PMU's power delivery and the processor's operating frequency. The canary oscillator uses a ring structure with four configurable stages and a 4-bit counter combined with a five-step frequency divider, providing 20 frequency steps as shown in Fig. 5(b). Fig. 6(b) shows frequency deviations from mismatch and corner variations, with standard deviations (σ) of 3.29 and 65.6 kHz at 1.19 MHz, corresponding to 0.28% and 5.51%. While the impact of mismatch is negligible, the corner variation can noticeably affect synchronization between the processor and PMU. Moreover, as shown in Fig. 3 (right), the sinking charge (Q_{Down}) of the N-type metal-oxide-semiconductor (NMOS) also varies from the corner variations. To address this, the proposed PMU includes a mechanism to adjust the $f_{\mathrm{VCO}}/f_{\mathrm{OSC}}$ ratio using a 3-bit V_{CTRL} boosting capacitor array and frequency divider, which also serves as a calibration scheme for robust synchronization across variations.

While the intentional nonlinearity in the $f_{\mathrm{VCO}}/f_{\mathrm{OSC}}$ relationship enables flexible power tracking and improves energy efficiency, it also increases sensitivity to structural and process variations between the canary oscillator and the PMU's VCO. Since these two oscillators differ in architecture and physical location, such variations can cause shifts in both the $f_{\mathrm{VCO}}/f_{\mathrm{OSC}}$ ratio and the corresponding equilibrium V_{CTRL} voltage, potentially disrupting the intended frequency-tracking behavior. To evaluate the impact of these variations, Monte Carlo simulations were conducted by fixing the canary oscillator frequency at 1 kHz and 1 MHz while applying process and corner variations to the VCO, as shown in Fig. 7. At 1 kHz, the $f_{\mathrm{VCO}}/f_{\mathrm{OSC}}$ ratio exhibits a mean of 10.54 with a standard deviation of 0.541, while the corresponding V_{CTRL} voltage shows a mean of 441.6 mV with a 1σ deviation of 29.8 mV. At 1 MHz, the ratio has a mean of 7.186 with a standard deviation of 0.4526, and V_{CTRL} averages 832.7 mV with a deviation of 27.78 mV. These results demonstrate that while variation in the $f_{\mathrm{VCO}}/f_{\mathrm{OSC}}$ slope can be effectively compensated using the tunable capacitor array in the charge-pump circuit, shifts in the absolute level of V_{CTRL} influence the degree of nonlinearity in the VCO's frequency response. Although the 1σ variation in V_{CTRL} is not excessively large compared to its mean, additional calibration of the VCO's frequency-to-V_{CTRL} transfer function may still be required to preserve the intended nonlinearity characteristics and ensure accurate frequency tracking under mismatch and corner variations. By integrating both slope and voltage-level compensation mechanisms, the system maintains robust and precise synchronization.

III. Measurement Results

A. Test Results With the Millimeter-Scale Computing System

Fig. 8 shows the chip photograph and measured performance of the proposed PMU, fabricated in a 180 nm process. The processor operates at frequencies ranging from 256 kHz to 2.73 MHz, delivering a total load power of 50 to 496 μW to outputs O_1 and O_2, as shown in Fig. 8(b). Fig. 8 also shows that,

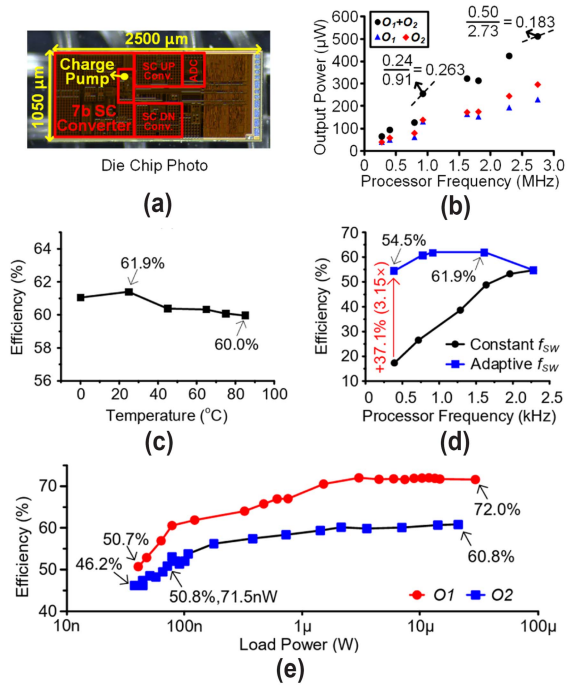


Fig. 8. Measured PMU in active mode. (a) Chip photo. (b) Output power versus frequency. (c) Efficiency versus temperature. (d) Efficiency versus frequency. (e) Efficiency versus load power in sleep mode.

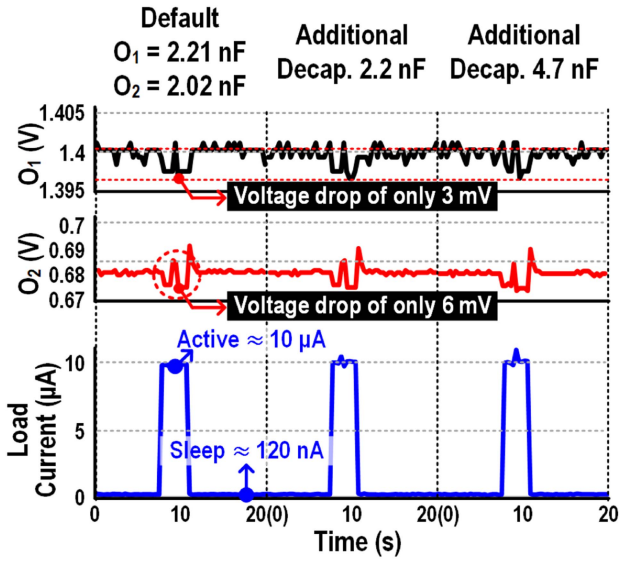


Fig. 9. Measured PMU during mode transition.

due to constant-current blocks within the system, the processor's current consumption increases sublinearly with f_{OSC} motivating the introduction of nonlinearity in the $f_{\mathrm{VCO}}/f_{\mathrm{OSC}}$ relationship. To control the VCO, the PMU adaptively adjusts its output drive strength using a f_{OSC} and achieves a PCE of 60%–62% over a temperature range of 0 °C–85 °C, as shown in Fig. 8(c), without requiring any dedicated adjustments for these variations. Under dynamic load conditions, the adaptive PMU achieves a PCE of 54%–62% by adjusting its switching frequency, representing an improvement of up to 37%, or 3.2 times better, compared to a PMU with a constant switching frequency, as depicted in Fig. 8(d). Fig. 8(e) illustrates the measured performance of the proposed PMU in sleep mode. In this mode, without the use of the canary oscillator, the PMU achieves an efficiency range of 51%–72% for O_1 and 46%–61% for O_2.

B. Adaptive Dynamic Load Power Tracking of the PMU

Maintaining a stable supply voltage during transitions between active and sleep modes is also crucial. During a fast load transient where the load current changes abruptly from 120 nA to 10 μA, the PMU responds preemptively based on mode transition information from the processor, effectively minimizing voltage disturbances. A slight voltage drop of only 3 mV at O_1 and 6 mV at O_2 is observed during the transition, and the steady-state ripple voltage remains small, ∼3 mV at both outputs, due to the integrated decoupling capacitors (Decap) within the Decap layer (2.21 nF for O_1 and 2.02 nF for O_2), as illustrated in Fig. 5(a).

In addition, Fig. 9 includes measurement results with external decaps added at the outputs. When additional 2.2 or 4.7 nF decaps were added to both outputs, only minor improvements in ripple voltage were observed, particularly at O_2, while the overall transient behavior remained nearly unchanged.

This stability is further enhanced by the use of an SC converter. Unlike inductive converters (see [12] and [13]), which inherently supply current through an inductor and may cause overshoot when preemptively increasing supply current, due to gradual inductor current settling and voltage rising above the load requirement, the SC converter inherently limits output current as the output voltage approaches its target voltage conversion ratio. In fact, due to the discrete nature of charge transfer in SC converters, once the output voltage exceeds the ideal conversion ratio, charge cannot flow from the input to the output, effectively blocking further voltage rise. This intrinsic behavior prevents excessive voltage overshoot even when the PMU momentarily supplies more current than the load demands, enabling preemptive regulation without requiring additional control blocks to maintain voltage stability.

C. Performance Comparison

Table I compares PMUs, with boldface indicating the advantages of this work over others. The proposed PMU exhibits negligible voltage variation (<6 mV) during load transients when transitioning from sleep to active mode (120 nA to 10 μA). This is achieved by using a replica canary oscillator that adaptively adjusts the power delivery of the SC converter. Compared to the PMUs in [7] and [16], our design experiences 26.6× and 4.5× smaller output drop during mode transitions, despite the load current change in our measurements ranging from 0.83× and 6.41× that of the references. Other PMUs do not report metrics for significant load transitions. This work also demonstrates strong temperature resilience, with less than 1.9% variation in PCE over a 0 °C–85 °C range. The PMU in [18] covers a significantly wide temperature range while reporting a 5% variation. However, it requires manual adjustment of the f_{VCO} to accommodate load current and temperature changes.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH LOW-POWER SC PMUS

Parameters		This Work	[17] SSCL '24	[16] ESSCIRC '21	[7] ISSCC '16	[4] JSSC '13
Technology (nm)		180	12	65	180	180
Topology		7b Binary, 2:1	8:7	4:1	7b Binary, 2:1, 1:3	5:1, 6:1
# of VCR		127	1	1	127	2
V_{IN} (V_{BAT}, V)		1.5 – 4.2	0.8	2.5 – 3	0.9 – 4.2	3.6 – 4.2
V_{OUT} (V)		1.2 – 1.8 (O_1) 0.6 – 0.9 (O_2)	0.7	0.55, 1.2, 1.8	0.6, 1.2, 3.3	0.6, 1.2
VCO Frequency (f_{VCO}) Range (Hz)		**1.89 – 104 M (× 55 M)**	100 k – 40 M (Manual)	N/A	50 –10 M (× 0.2M)	340 (Sleep) 404 k (Active)
f_{SW} Control (Mode Transition)		**Adaptive w/ a canary OSC**	Fixed	Inv. Based Comparator	Droop detectors	Start-up Message
ΔV_{OUT} (V) in Mode Trans. (A)		**3 m(O_1)/ 6 m(O_2)** (120 n–10 µ)	N/A	27 m (10 – 130 µ)	160 m (10 n – 1 µ)	N/A
PCE Temp. Variation		**60 – 61.9% (0 – 85 °C)**	75 – 80% (-250 – 127 °C)	N/A	N/A	N/A
PCE > 50% (W)	**Sleep**	**41 n – 29 µ (O_1) 72 n – 21 µ (O_2)**	35 µ – 0.5 m	22 – 93.5 µ	5 n – 500 µ	5–22 n
	Active	**79 – 409 µ (O_1+O_2)**				10–20 µ

For automatic operation, an adaptive f_{VCO} control scheme, like the one proposed in this work, would be necessary.

IV. CONCLUSION

This article presents a PMU for millimeter-scale computing systems that achieves only a 3-mV / 6-mV voltage drop during load transitions (120 nA to 10 μA) by preadjusting the SC converter's power delivery using a replica canary oscillator. The proposed design achieves over 50% PCE across the full load range from 41 / 72 nW to 29 / 21 μW in sleep mode and from 79 to 409 μW in active mode. It also ensures stable efficiency, with less than 1.9% variation across 0 °C to 85 °C, making it well suited for energy-constrained, ultra-small systems.

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