# High-Frequency Self-Synchronized Load-Independent Class-E Rectifier Using Fixed-Point Crossing Detection

Wenqi Zhu, *Member, IEEE*, Ayano Komanaka, *Graduate Student Member, IEEE*, Yutaro Komiyama, *Graduate Student Member, IEEE*, Kien Nguyen, *Senior Member, IEEE*, Hirotaka Koizumi, *Member, IEEE*, and Hiroo Sekiya, *Senior Member, IEEE*

***Abstract*—This article presents an intracycle self-synchronized load-independent (LI) class-E rectifier based on a novel fixed-point crossing detection method. Through circuit analysis, we identify that the drain-to-source voltage of the LI class-E rectifier consistently crosses a fixed voltage threshold at a specific phase angle prior to turn-ON, independent of load resistance. This fixed crossing point serves as a reliable trigger for gate-drive signal generation. Therefore, the proposed approach enables intracycle synchronization without the need for additional resonant components or control circuitry. Analytical expressions for the fixed point are derived, and a systematic design procedure is provided. A 6.78 MHz, 20 W WPT prototype was implemented and tested. The rectifier maintained robust load-independent performance, demonstrating nearly constant output voltage and input reactance across varying loads. Compared with the zero-crossing detection-based intracycle synchronization, the proposed method achieved more precise switching, eliminating reverse conduction and switching losses, and reducing total rectifier effectively.**

***Index Terms*—Class-E rectifier, load-independent, synchronous rectifier, wireless power transfer, zero-voltage switching (ZVS).**

## I. Introduction

GALLIUM Nitride (GaN) semiconductors are revolutionizing switching power supplies, including resonant power converters [1], [2], [3], [4], [5], [6], [7], [8] and wireless power transfer (WPT) systems [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23]. GaN FETs enable power converters to operate at multimegahertz frequencies, such as ISM bands (6.78 MHz, 13.56 MHz, etc.). The high-frequency operation reduces the size of resonant coils and output filters significantly. However, higher switching frequencies also lead to increased switching losses, lowering overall efficiency. To maintain high efficiency in multimegahertz operation, zero-voltage switching (ZVS) is a critical design requirement.

Among various high-frequency wireless power receiver topologies, the class-E rectifier [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [24], [25] is widely adopted due to its intrinsic ZVS capability and simple circuit structure. However, the original class-E rectifier is highly sensitive to load variations, causing its voltage gain to vary with changes in load resistance [25]. As a result, additional regulation is required to stabilize the output voltage. Furthermore, the input reactance of the original class-E rectifier also varies with the load, which may detune the magnetic resonance and cause non-ZVS operation of the power transmitter. Due to these limitations, the original class-E rectifier is unsuitable for WPT applications with wide load variations. To overcome these challenges, the load-independent (LI) class-E rectifier was proposed [12]. The LI class-E rectifier maintains a constant output voltage gain regardless of load resistance, eliminating the need for additional regulation. Moreover, it features a constant input reactance, which is desirable for WPT systems because the resonant frequency of the power receiver remains stable across varying loads.

An LI class-E rectifier requires an active switch capable of bidirectional conduction, making a diode unsuitable. Thus, a precise synchronization method is essential for accurate gate-drive timing. At multimegahertz operating frequencies, delays introduced by digital controllers and gate drivers become significant. One approach to mitigate these delays is intercycle synchronization, where the turn-ON event is aligned with switching cycles in subsequent periods [12], [13], [14], [15], [16]. This strategy extends the time window available for delay compensation, enabling more precise turn-ON timing and reducing reverse-conduction loss.

While intercycle synchronization can achieve accurate switching, it may slow the circuit's dynamic response and require additional digital circuitry for state tracking and pulse scheduling. Alternatively, intracycle synchronization methods generate the gate-drive signal based on circuit states within the same switching cycle. This approach improves response speed

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Wenqi Zhu and Hirotaka Koizumi are with the Department of Electrical Engineering, Tokyo University of Science, Tokyo 162-8601, Japan (e-mail: zhu@rs.tus.ac.jp; littlespring@ieee.org).

Ayano Komanaka, Yutaro Komiyama, Kien Nguyen, and Hiroo Sekiya are with the Department of Informatics, Graduate School of Informatics, Chiba University, Chiba 263-8522, Japan (e-mail: komanaka.ayano@chiba-u.jp; y.komiyama@chiba-u.jp; nguyen@chiba-u.jp; sekiya@faculty.chiba-u.jp).

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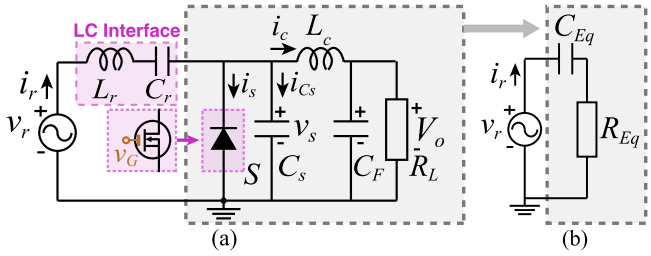


Fig. 1. Circuit topologies. (a) Circuit topology of the class-E rectifier. (b) Equivalent input circuit at the fundamental frequency $f$.

and eliminates the need for historical state storage. However, the limited available time window makes the use of a digital controller impractical due to its inherent latency. In [17], precise intracycle synchronization was achieved by introducing a resonant inductor to produce a phase-compensated gate signal. However, this added inductor increases both circuit complexity and size. There remains a clear need for an intracycle synchronization method for LI class-E rectifiers that can robustly compensate for propagation delays without requiring additional resonant components or digital controllers.

This article presents an intracycle self-synchronized LI class-E rectifier based on a novel fixed-point crossing detection (FPXD) method. Through circuit analysis, we identify that the drain-to-source voltage of the LI class-E rectifier consistently crosses a fixed voltage threshold at a specific phase angle prior to turn-ON, independent of load resistance. This fixed crossing point serves as a reliable trigger for gate-drive signal generation. Therefore, the proposed approach enables intracycle synchronization without the need for additional resonant components or control circuitry. Analytical expressions for the fixed point are derived, and a systematic design procedure is provided. A 6.78 MHz, 20 W WPT prototype was implemented and tested. The rectifier maintained robust load-independent performance, demonstrating nearly constant output voltage and input reactance across varying loads. Compared with the zero-crossing detection (ZXD)-based intracycle synchronization, the proposed method achieved more precise switching, eliminating reverse conduction and switching losses, and reducing total rectifier loss effectively.

## II. LI Class-E Rectifier

### A. Circuit Topology

Fig. 1 shows the circuit topology of the class-E rectifier. The rectifier is driven by an ac voltage source $v_r$ at an angular frequency $\omega = 2\pi f$ through an $L_r - C_r$ interface. When used in WPT or isolated converters, $L_r$ is usually the receiving coil, and $v_r$ is induced via magnetic coupling. The $L_r - C_r$ interface has a high quality factor to ensure a sinusoidal input current $i_r$. The rectifier consists of a main switch $S$, a shunt capacitor $C_s$, an output inductor $L_c$, and an output filter capacitor $C_F$. The load resistance $R_L$ varies depending on the operating conditions.

Fig. 1(b) shows the equivalent circuit of the class-E rectifier at the fundamental frequency $f$. The input impedance of the class-E rectifier is capacitive, modeled using an equivalent input resistance $R_{Eq}$ and capacitance $C_{Eq}$.

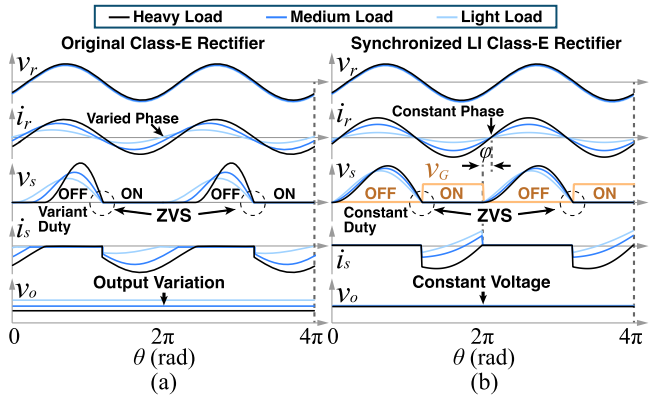


Fig. 2. Typical waveforms of the class-E rectifier. (a) The original class-E rectifier using a diode. (b) Self-synchronized LI class-E rectifier using an active switch.

### B. Original Class-E Rectifier

The original class-E rectifier uses a diode as the switch $S$. A sufficiently large choke inductor $L_c$ is used to ensure that the current $i_c$ is purely dc.

Fig. 2(a) shows the typical waveforms of an original class-E rectifier under load variation. While ZVS turn-ON is inherently achieved, the rectifier exhibits high sensitivity to load variations. The duty cycle of $v_s$ varies with the load. In addition, the output voltage $v_o$ also varies, caused by a variable rectifier voltage gain $G_R$. To maintain a constant output voltage, an additional regulator stage is required, which increases system size and complexity.

Furthermore, the input reactance of the rectifier, $X_{Eq} = 1/(\omega C_{Eq})$, also varies with load changes, affecting the phase of $i_r$ as shown in Fig. 2(a). In WPT applications, this variation can detune the input LC resonant circuit, introducing a load-dependent reactance seen from the transmitter side. As a result, it may cause non-ZVS operation in the power transmitter. Due to these limitations, the original class-E rectifier is unsuitable for WPT systems with significant load variations.

### C. Load-Independent Class-E Rectifier

To address the load-sensitivity problem, the LI class-E rectifier was proposed in [12]. The LI class-E rectifier uses a finite output choke inductor $L_c$, which resonates with $C_s$ at a specific resonant frequency $\omega_s = 1/\sqrt{L_c C_s}$.

Fig. 2(b) shows the typical waveforms of the LI class-E rectifier. Unlike the original class-E rectifiers, $i_s$ flows bidirectionally, necessitating an active switch such as a GaN FET as $S$. A passive diode is unsuitable.

If the gate voltage $v_G$ is properly determined to drive $S$, the rectifier voltage gain $G_R$ remains constant regardless of load variations. This eliminates the need for additional regulation stages. Moreover, the input reactance $X_{Eq}$ remains constant, leading to a fixed phase of $i_r$, as can be seen in Fig. 2(b). This characteristic is highly desirable in WPT systems, as it ensures that the resonant frequency of the receiver remains unaffected by load variations.

In addition, the switch voltage maintains a constant off-duty ratio $D$ and ensures ZVS operation regardless of load variations,

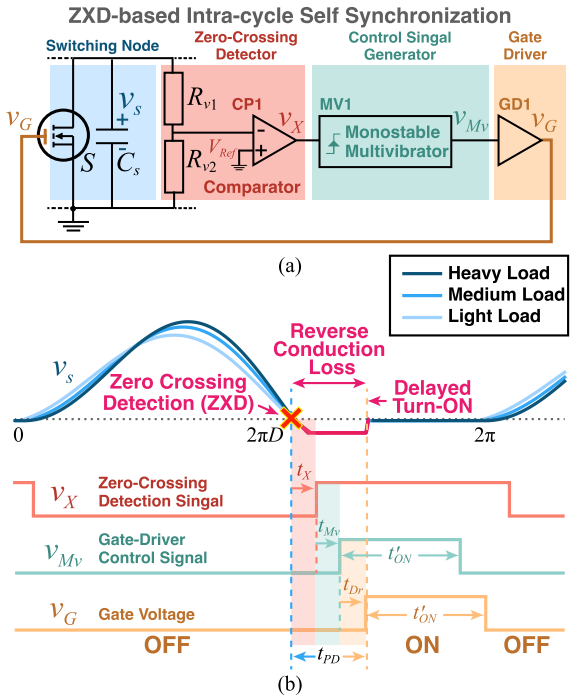


Fig. 3. Intracycle synchronous control of the LI class-E rectifier using ZXD of $v_s$. (a) Controller circuit. (b) Example control waveforms.

as given by

$$v_s(2\pi D^-) = 0. \tag{1}$$

Therefore, switching loss in the GaN FET is eliminated, enabling high power efficiency even at multimegahertz frequencies. Due to these advantages, the LI class-E rectifier is a strong candidate for high-frequency WPT and isolated power converters operating under varying load conditions.

## III. Self-Synchronization of the Class-E Rectifier

To achieve ZVS turn-ON and maintain a constant output voltage, the LI class-E rectifier requires precise synchronization of the gate voltage $v_G$, as shown in Fig. 2(b). A premature turn-ON causes hard switching, leading to switching losses, while a delayed turn-ON results in reverse conduction, increasing power dissipation due to the inherently high freewheeling losses of GaN FETs. To avoid these losses, $v_G$ must be triggered precisely at the negative zero-crossing of $v_s$, which becomes increasingly challenging for MHz intracycle self synchronization.

### A. Intracycle Self-Synchronization Using Zero-Crossing Detection

To achieve intracycle synchronization, a straightforward approach is to detect the negative zero-crossing of the switch voltage $v_s$ using a ZXD circuit, as shown in Fig. 3(a).

In this method, $v_s$ is scaled down by a voltage divider $R_{v1} - R_{v2}$ and then compared to a zero reference voltage $V_{Ref} = 0$ V by a comparator (CP1). The comparator generates a detection signal $v_X$, which rises when the zero crossing occurs. The rising edge of $v_X$ triggers a monostable multivibrator (MV1), which generates a driving signal $v_{Mv}$ with fixed-pulse width $t'_{ON}$. This signal controls the gate driver (GD1), finally pulling up the gate voltage $v_G$ and turning ON $S$.

However, at multimegahertz frequencies, the propagation delays, including those from the comparator ($t_X$),[1] the monostable multivibrator ($t_{Mv}$), and the gate driver ($t_{Dr}$), become significant. These delays result in an overall turn-ON delay of

$$t_{PD} = t_X + t_{Mv} + t_{Dr}. \tag{2}$$

This delay introduces a critical issue: during $t_{PD}$, the negative switch current $i_s$ continues freewheeling through $S$ while its gate voltage $v_G$ remains low, as can be seen in Fig. 3(b). In typical implementations, $t_{PD}$ exceeds 20 nanoseconds, which is nonnegligible because the ON-duration in ISM band applications is often on the order of tens of nanoseconds. As a result, the GaN FET experiences high reverse-conduction loss.

Increasing the reference voltage $V_{Ref}$ above zero can trigger the comparator earlier, reducing the turn-ON delay to some extent [16]. However, at multimegahertz operation, a high $V_{Ref}$ is required for adequate delay compensation, which introduces a load-dependent turn-ON time due to variations in the falling slope of $v_s$, as shown in Fig. 3(b). Consequently, lossless switchings cannot be ensured under load variations.

### B. Intracycle Self-Synchronization Using Fixed-Point Crossing Detection

Fig. 4 shows the proposed self-synchronization method based on FPXD.

For the LI class-E rectifier, we notice that the switch voltage $v_s$ inherently crosses a specific voltage level $V_{Fix}$ at a fixed time $t_{Fix}$ before turn-ON, as shown in Fig. 4(b). Notably, both $V_{Fix}$ and $t_{Fix}$ remain constant regardless of load variations, which will be mathematically proven in the following Section IV. In this research, we refer to this as the "fixed point." Our core idea is to detect this fixed voltage point of $v_s$ for intracycle self-synchronization.

Unlike the ZXD method, the comparator reference voltage $V_{Ref}$ is set to a positive level. $V_{Ref}$ is carefully determined so that the comparator output $v_X$ rises when $v_s$ crosses $V_{Fix}$ in the positive direction. $V_{Ref}$ is derived from the dc output voltage $V_o$ using a voltage divider $R_{v3} - R_{v4}$.

The rising edge of $v_X$ triggers the first monostable multivibrator (MV1), which generates a pulse $v_{Mv1}$ of width $t_{Cps}$. $t_{Cps}$ is tuned to compensate for propagation delays, ensuring precise turn-ON timing. The falling edge of $v_{Mv1}$ then triggers the second monostable multivibrator (MV2), which generates $v_{Mv2}$ with width $t_{ON}$. This pulse finally controls the gate voltage $v_G$ via the gate driver.

As shown in Fig. 4(b), the total propagation delay in the proposed method is given by

$$t_{PD} = t_X + t_{Mv1} + t_{Cps} + t_{Mv2} + t_{Dr} \tag{3}$$

[1] $t_X$ includes delays caused by the parasitic capacitances in the voltage divider and the comparator.

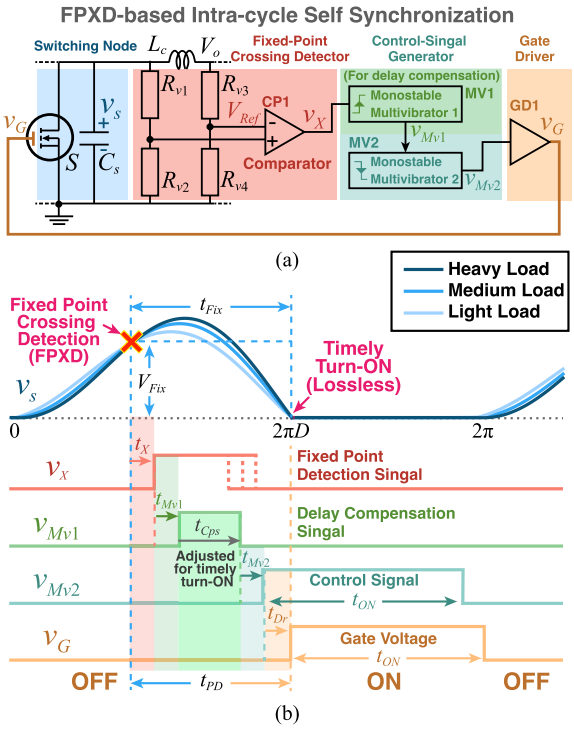


Fig. 4. Proposed intracycle synchronous control of the LI class-E rectifier using FPXD of $v_s$. (a) Controller circuit. (b) Example control waveforms.

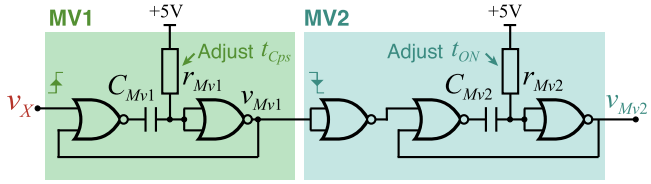


Fig. 5. Implementation of monostable multivibrators using five NOR gates and passive components.

where $t_{Mv1}$ and $t_{Mv2}$ are the propagation delay of MV1 and MV2, respectively. To ensure precise synchronization, $t_{Cps}$ should be adjusted so that

$$t_{PD} = t_{Fix}. \tag{4}$$

With this condition met, the gate voltage $v_G$ is pulled up precisely when $v_s$ reaches zero, achieving timely turn-ON without switching loss or reverse-conduction loss, as shown in Fig. 4(b).

Fig. 5 shows an implementation example of the two monostable multivibrators. MV1 is constructed using two NOR gates. MV2 uses three, with one acting as an input inverter for falling-edge triggering. The pulse widths of MV1 and MV2, $t_{Cps}$ and $t_{ON}$, are adjusted by tuning the resistances $r_{Mv1}$ and $r_{Mv2}$, respectively. A key advantage of the proposed method is that it requires only a single comparator and five logical gates to compensate for propagation delays and achieve precise turn-ON timing. The proposed method eliminates the need for additional resonant inductors or digital controllers, simplifying the design and reducing the overall cost significantly.

TABLE I
DEFINITIONS OF NORMALIZED QUANTITIES AND CIRCUIT PARAMETERS

| Quantity | Notation | Base quantity | Definition |
|---|---|---|---|
| Voltage | $v^*$ | $V_o$ | $v_x^* = v_x/V_o$ |
| Current | $i^*$ | $V_o/R_{Lr}$ | $i_x^* = i_x R_{Lr}/V_o$ |
| Angular Freq. | $\omega^*$ | $\omega$ | $\omega_x^* = \omega_x/\omega$ |
| Resistance | $R^*$ | $R_{Lr}$ | $R_x^* = R_x/R_{Lr}$ |
| Capacitance | $C^*$ | $1/\omega R_{Lr}$ | $C_x^* = C_x \omega R_{Lr}$ |

## IV. Analytical Derivation of the Fixed Point

### A. Assumptions

To prove the existence of the fixed voltage point and derive its analytical expression, circuit analysis is performed. For simplification, the following assumptions are made:

1) The rectifier input current $i_r$ is sinusoidal, expressed as
$$i_r(\theta) = I_r \sin(\theta + \varphi) \tag{5}$$
where $\theta$ is the phase angle. $\varphi$ is the phase shift between $i_r$ and the switch turn-OFF instant, shown in Fig. 2(b).
2) $S$ is considered ideal, with zero ON-resistance and infinite OFF-resistance. Its output capacitance $C_{OSS}$ is absorbed into $C_s$.
3) All passive components in the circuit are linear and ideal, with no parasitic resistances.
4) The output capacitance $C_F$ is sufficiently large to maintain a dc output voltage $V_o$.

To generalize the analysis, circuit parameters and quantities are normalized and denoted by superscript $^*$, as summarized in Table I. Here, subscript $x$ denotes any arbitrary variable or parameter, while subscript $r$ represents values at the rated condition. This normalization ensures that the derived results remain independent of specific circuit specifications.

### B. Waveform Equations

The normalized charging current through the shunt capacitance $C_s$ is given by

$$i_{Cs}^*(\theta) = \begin{cases} -\sin(\omega_s^*\theta)\alpha_1 - \cos(\omega_s^*\theta)\alpha_2 - \dfrac{I_r^* \sin(\theta+\varphi)}{\omega_s^{*2}-1}, \\ \qquad\qquad (0 \le \theta < 2\pi D), \\ 0, \qquad\qquad (2\pi D \le \theta < 2\pi) \end{cases} \tag{6}$$

where $\alpha_1$, $\alpha_2$ are arbitrary coefficients, and the normalized resonant frequency $\omega_s^*$ is defined as

$$\omega_s^* = \frac{\omega_s}{\omega} = \frac{1}{\omega\sqrt{C_s L_c}}. \tag{7}$$

The normalized current flowing through the FET $i_s^*$ is expressed as

$$i_s^*(\theta) = \begin{cases} 0, \qquad\qquad (0 \le \theta < 2\pi D), \\ I_r^* \sin(\theta+\varphi) - \alpha_2 + (\theta - 2\pi) C_s^* \omega_s^{*2} - \\ \dfrac{I_r^* \sin(\varphi)\omega_s^{*2}}{\omega_s^{*2}-1}, \qquad (2\pi D \le \theta < 2\pi). \end{cases} \tag{8}$$

The normalized switch voltage $v_s^*$ is given by

$$v_s^*(\theta) = \begin{cases} \dfrac{1}{C_s^*}\left[\dfrac{\alpha_1\cos(\omega_s^*\theta) - \alpha_1 - \alpha_2\sin(\omega_s^*\theta)}{\omega_s^*} \right. \\ \left. + \dfrac{\cos(\theta+\varphi) - \cos\varphi}{\omega_s^{*2}-1} I_r^*\right], & (0 \le \theta < 2\pi D), \\ 0, & (2\pi D \le \theta < 2\pi). \end{cases} \tag{9}$$

At the turn-ON instant, the charging current of the shunt capacitance $i_{Cs}$ is instantaneously redirected to the switch current $i_s$, ensuring current continuity as

$$i_{Cs}^*(2\pi D^-) = i_s^*(2\pi D). \tag{10}$$

In addition, the volt-second balance condition in the inductor $L_c$ requires

$$V_o^* = V_o/V_o = 1 = \frac{1}{2\pi}\int_0^{2\pi D} v_s^*(\theta)d\theta. \tag{11}$$

Substituting the waveform (6) and (8) into (10), and substituting (9) into (11), we obtain two equations. Solving them simultaneously, we derive the closed-form expressions for $\alpha_1$ and $\alpha_2$ as

$$\alpha_1 = \omega_s^*\left\{\frac{(1-D)\pi}{\tan(\pi D\omega_s^*)}C_s^*\omega_s^* - \frac{\sin(\pi D)\left[\sin(\pi D+\varphi) + \frac{\cos(\pi D+\varphi)}{\tan(\pi D\omega_s^*)}\omega_s^*\right]}{\omega_s^{*2}-1} I_r^*\right\}, \tag{12}$$

$$\alpha_2 = \omega_s^*\left\{-(1-D)\pi C_s^*\omega_s^* + \frac{\sin(\pi D)\left[\cos(\pi D+\varphi)\omega_s^* - \frac{\sin(\pi D+\varphi)}{\tan(\pi D\omega_s^*)}\right]}{\omega_s^{*2}-1} I_r^*\right\}. \tag{13}$$

### C. Load-Independent Conditions

Substituting the coefficients (12), (13) into the waveform (9), the ZVS condition (1) becomes

$$\left[1 + \frac{(1-D)\pi\omega_s^*}{\tan(\pi D\omega_s^*)}\right] R_L^* = \frac{\cos(\pi D+\varphi)}{V_r^* C_s^*(\omega_s^{*2}-1)}\left[\frac{\sin(\pi D)\omega_s^*}{\tan(\pi D\omega_s^*)} - \cos(\pi D)\right]. \tag{14}$$

If both sides in (14) are nonzero, ZVS will only be achieved at a specific value of $R_L^*$. To eliminate this dependency, (14) must hold as an identity with the form as $0 \cdot R_L^* = 0$. Setting the left-hand side to zero, we have

$$1 + \frac{(1-D)\pi\omega_s^*}{\tan(\pi D\omega_s^*)} = 0. \tag{15}$$

This equation gives the relationship between $D$ and $\omega_s^*$ to achieve LI ZVS. Because (15) is transcendental, $\omega_s^*$ does not have a closed-form solution but can be solved numerically. Fig. 6(a) shows the curve of $\omega_s^*$ as a function of $D$.[2]

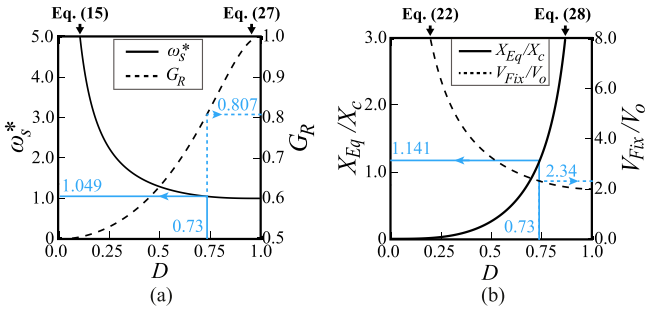


Fig. 6. Parametric curves of the LI class-E rectifier as functions of the off-duty ratio $D$. (a) Normalized resonant frequency $\omega_s^*$ and voltage gain $G_R$. (b) Reactance ratio $X_{Eq}/X_c$ and fixed drain-voltage point $V_{Fix}/V_o$.

In addition, the required phase shift $\varphi$ can be derived by setting the right-hand side of (14) to zero, given by

$$\varphi = \pi/2 - \pi D. \tag{16}$$

### D. Fixed Point of Switch Voltage

Substituting LI conditions (15) and (16) into (12) and (13), the coefficients $\alpha_1$ and $\alpha_2$ can be simplified as follows:

$$\alpha_1 = -\omega_s^*\left[C_s^* + \frac{\sin(\pi D)}{\omega_s^{*2}-1}I_r^*\right], \quad \alpha_2 = -\omega_s^*\left[(1-D)\pi\omega_s^* C_s^* + \frac{\sin(\pi D)}{(\omega_s^{*2}-1)\tan(\pi D\omega_s^*)}I_r^*\right]. \tag{17}$$

Substituting the LI conditions (15) and (16), along with the coefficient expressions (17), into the waveform (9), the normalized switch voltage $v_s^*$ during the OFF period can be decomposed into two parts

$$v_s^*(\theta, R_L^*) = v_{s1}^*(\theta) + v_{s2}^*(\theta, R_L^*), \quad (0 \le \theta < 2\pi D) \tag{18}$$

where $v_{s1}^*(\theta)$ is independent of the load resistance $R_L^*$, while $v_{s2}^*(\theta, R_L^*)$ depends on $R_L^*$. They are given by

$$v_{s1}^*(\theta) = 1 - \cos(\omega_s^*\theta) + \pi(1-D)\sin(\omega_s^*\theta)\omega_s^* \tag{19}$$

and

$$v_{s2}^*(\theta, R_L^*) = \frac{2}{R_L^* C_s^*(\omega_s^{*2}-1)}\left\{-\sin(\theta-\pi D) + \frac{\sin(\pi D)}{\sin(\omega_s^*\pi D)}\sin\left[(\theta-\pi D)\omega_s^*\right]\right\}. \tag{20}$$

Observing (20), we notice that $v_{s2}^*(\theta, R_L^*) = 0$ at the phase of $\theta = \pi D$. This implies that at this phase, the switch voltage $v_s^*$ is solely determined by $v_{s1}^*$. Defining this voltage as

$$V_{Fix}^* = v_s^*(\pi D) = v_{s1}^*(\pi D) \tag{21}$$

[2]Because of the periodic nature of the tangent function in (15), there are multiple $D$-$\omega_s^*$ curves mathematically. However, only one curve near ($D = 0.5$, $\omega_s^* = 1.29$) is practical for the LI operation. The other curves result in a high peak voltage at the switch.

we obtain

$$V_{Fix}^* = \frac{V_{Fix}}{V_o} = 1 - \cos(\omega_s^* \pi D) + \pi(1-D)\sin(\omega_s^* \pi D)\omega_s^*. \tag{22}$$

This ratio is independent of both the load resistance $R_L^*$ and the shunt capacitance $C_s^*$. It depends only on the off-duty ratio $D$. Fig. 6(b) shows the parameter curve of $V_{Fix}/V_o$ as a function of $D$.

At the fixed point, the slope of the normalized switch voltage $v_s^*$ is given by

$$\frac{dv_s^*(\theta)}{d\theta}\Big|_{\theta=\pi D} = \frac{i_{Cs}^*(\pi D)}{C_s^*} = \frac{I_r^*}{C_s^*}\frac{\frac{\sin(\pi D)\omega_s^*}{\sin(\omega_s^* \pi D)} - 1}{\omega_s^{*2} - 1}. \tag{23}$$

Assuming lossless operation where input power equals output power ($P_I = P_o$), and noting that $V_o^* = V_o/V_o = 1$, we have

$$\frac{1}{2}V_r^* I_r^* = \frac{V_o^{*2}}{R_L^*} = \frac{1}{R_L^*}. \tag{24}$$

Substituting (24) into (23) yields

$$\frac{dv_s^*(\theta)}{d\theta}\Big|_{\theta=\pi D} = \frac{2}{R_L^* C_s^* V_r^*}\frac{\frac{\sin(\pi D)\omega_s^*}{\sin(\omega_s^* \pi D)} - 1}{\omega_s^{*2} - 1}. \tag{25}$$

This result indicates that the slope of $v_s^*$ at the fixed point is inversely proportional to the load resistance $R_L^*$. In particular, under open-circuit conditions ($R_L^* = \infty$), the slope approaches zero.

In addition, the time interval from this fixed point to the next turn-ON of $S$, denoted as $t_{Fix}$, is given by

$$t_{Fix} = \frac{2\pi D - \pi D}{2\pi f} = \frac{D}{2f}. \tag{26}$$

In conclusion, we have demonstrated that in the LI class-E rectifier, the switch voltage $v_s$ inherently crosses a fixed voltage point $V_{Fix}$, as shown in Fig. 4(b). This crossing occurs at a predictable and constant time interval $t_{Fix}$ before the next turn-ON event of $S$. In this research, we propose using this crossing for phase detection, which enables precise compensation of propagation delays without the need for additional digital controllers or resonant inductors. By ensuring timely turn-ON of $S$, the proposed method effectively eliminates reverse conduction and switching losses, significantly improving rectification efficiency at high operating frequencies.

### E. Rectifier Characteristics

*1) Voltage Gain:* Applying Fourier analysis to the switch voltage $v_s$, the normalized output voltage (voltage gain) $G_R$ is derived as

$$G_R = \frac{\pi(\omega_s^{*2} - 1)}{2\omega_s^{*2}\Big[\pi(1-D)\cos(\pi D) + \sin(\pi D)\Big]} \tag{27}$$

which remains independent of the load resistance $R_L^*$. Fig. 6(a) shows the voltage gain $G_R$ as a function of $D$ under the class-E LI condition.

TABLE II
CIRCUIT PARAMETERS FOR THE PROPOSED CLASS-E RECTIFIER

| $D$ | $\omega_s^*$ | $G_R$ | $X_{Eq}/X_c$ | $V_{Fix}/V_o$ |
|---|---|---|---|---|
| 0.20 | 2.730 | 0.519 | 0.014 | 7.93 |
| 0.25 | 2.239 | 0.530 | 0.028 | 6.37 |
| 0.30 | 1.914 | 0.543 | 0.050 | 5.33 |
| 0.35 | 1.686 | 0.560 | 0.082 | 4.58 |
| 0.40 | 1.518 | 0.580 | 0.126 | 4.03 |
| 0.45 | 1.390 | 0.603 | 0.187 | 3.60 |
| 0.50 | 1.292 | 0.629 | 0.266 | 3.26 |
| 0.55 | 1.214 | 0.660 | 0.370 | 2.99 |
| 0.60 | 1.154 | 0.694 | 0.505 | 2.76 |
| 0.65 | 1.106 | 0.733 | 0.683 | 2.57 |
| 0.70 | 1.070 | 0.776 | 0.923 | 2.42 |
| 0.73* | 1.049 | 0.807 | 1.141 | 2.34 |
| 0.75 | 1.042 | 0.822 | 1.259 | 2.29 |
| 0.80 | 1.023 | 0.869 | 1.760 | 2.18 |

* Designed parameters.

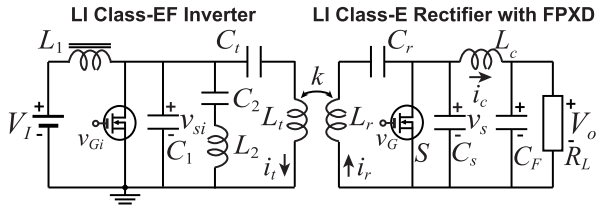


Fig. 7. Circuit topology of the implemented WPT system using the proposed FPXD rectifier.

*2) Phase-Shift Condition:* The input reactance of the LI class-E rectifier, given by $X_{Eq} = 1/(\omega C_{Eq})$ can be derived via Fourier analysis as

$$\frac{X_{Eq}}{X_c} = \frac{\omega_s^{*2}}{2\pi(\omega_s^{*2}-1)^2}\Bigg\{2\pi D + \sin(2\pi D) - \frac{4\omega_s^* \sin^2(\pi D)}{\tan(\pi D \omega_s^*)} + \omega_s^{*2}\Big[\sin(2\pi D) - 2\pi D\Big]\Bigg\}. \tag{28}$$

This result indicates that $C_{Eq}$ is determined solely by $D$ and $X_c = \omega L_c$, independent of the load resistance $R_L^*$. This characteristic is critical for WPT applications, as it ensures that the receiver resonant frequency remains stable despite load variations. Fig. 6(b) shows the curve of $X_{Eq}/X_c$ as a function of $D$.

For quick reference, Table II provides precomputed values of $D$, $\omega_s^*$, $G_R$, $X_{Eq}/X_c$, and $V_{Fix}/V_o$ for designing the LI class-E rectifier.

## V. CIRCUIT DESIGN STRATEGY

### A. Circuit Specifications

To validate the proposed rectifier, we designed and implemented a 6.78 MHz WPT system with a 48 V input and a target output voltage of 24 V. The system delivers a maximum output power of $P_{or} = 20$ W, corresponding to a nominal load resistance of $R_{Lr} = 28.8\ \Omega$. Fig. 7 shows the circuit topology of the implemented WPT system.

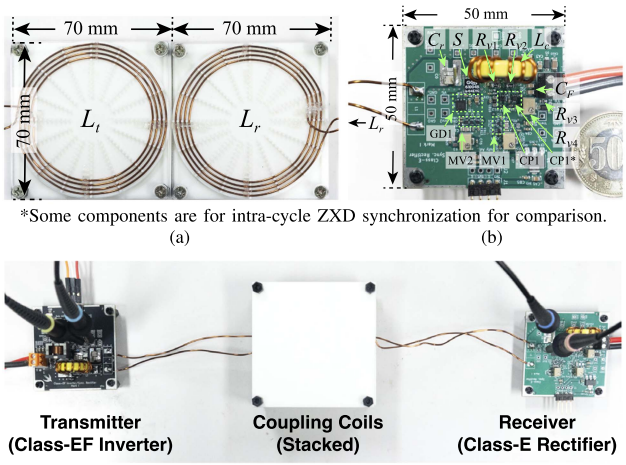


Fig. 8. Photograph of the implemented WPT system. (a) Coupling coils. (b) Implemented class-E rectifier. (c) Overview of the system.

TABLE III
DESIGNED AND MEASURED CIRCUIT COMPONENTS VALUES

| Param. | Designed | Measured | Difference | ESR (mΩ) |
|---|---|---|---|---|
| $C_1$ | 164.1 pF | 163.7 pF | –0.24 % | – |
| $C_2$ | 268.9 pF | 268.7 pF | –0.07 % | – |
| $C_t$ | 461.9 pF | 461.7 pF | –0.04 % | – |
| $L_1$ | – | 46.7 $\mu$H | – | 25.0 $(f)$ |
| $L_2$ | 820.7 nH | 813.6 nH | –0.87 % | 202 $(2f)$ |
| $L_t$ | – | 1.875 $\mu$H | – | 354 $(f)$ |
| $L_r$ | – | 1.900 $\mu$H | – | 360 $(f)$ |
| $L_c$ | – | 314.3 nH | – | 39.7 $(f)$ |
| $C_r$ | 357.4 pF | 357.2 pF | –0.06 % | – |
| $C_{Ext}$[1] | 1427 pF | 1437 pF | +0.70 % | – |
| $C_F$ | – | 2.940 $\mu$F | – | |

[1] See Appendix for the derivation of the external shunt capacitance $C_{Ext}$.

*1) Power Transmitter:* An LI class-EF inverter is employed as the power transmitter. The inverter is driven by an input dc voltage of $V_I = 48$ V and operates at a frequency of $f = 6.78$ MHz. It provides a constant output ac current of $I_t = 1.59$ A. The detailed inverter design was provided in [12] and is omitted in this article for brevity. Table III gives the designed component values used in the LI class-EF inverter.

*2) Magnetic Coupling:* The transmitter and receiver coils, denoted as $L_t$ and $L_r$, were implemented using identical spiral coils, as shown in Fig. 8(a). These coils were wound with AWG20 copper wire on 3-D printed formers, each with an outer diameter of 66.5 mm and four turns. The system operates with a coupling distance of 17 mm, with a measured coupling coefficient of $k = 0.233$. The inductances and ac resistances of $L_t$ and $L_r$ were experimentally measured, given in Table III.

To achieve load-independent operation, a series-series compensation topology is employed. To ensure ZVS of the class-EF inverter, the compensation capacitor $C_r$ is designed to achieve complete resonance, maintaining a constant output reactance for the inverter.

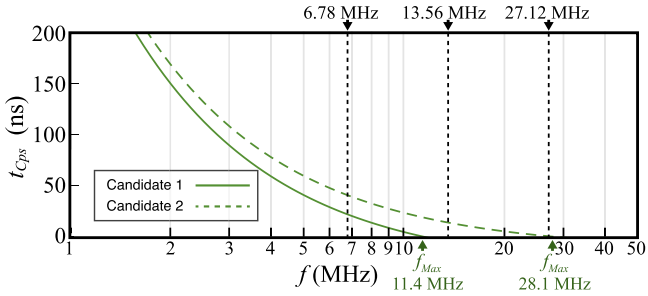


Fig. 9. Required pulse width $t_{Cps}$ of MV1 as a function of switching frequency $f$.

TABLE IV
PROPAGATION DELAYS OF TWO IMPLEMENTATION CANDIDATES

Candidate 1 ($f_{Max}$=11.4 MHz)

| Compon. | Model | Notation | Delay (ns) |
|---|---|---|---|
| CP1 | TI LMV7219 | $t_X$ | 8.60 |
| MV1 | 2x Diodes 74LVC1G02 | $t_{MV1}$ | 3.45 |
| MV2 | 3x Diodes 74LVC1G02 | $t_{MV2}$ | 4.54 |
| GD1 | TI UCC27516 | $t_{Dr}$ | 15.32 |

Candidate 2 ($f_{Max}$=28.1 MHz)

| Compon. | Model | Notation | Delay (ns) |
|---|---|---|---|
| CP1 | TI TLV3602 | $t_X$ | 2.50 |
| MV1 | 2x Diodes 74LVC1G02 | $t_{MV1}$ | 3.45 |
| MV2 | 3x Diodes 74LVC1G02 | $t_{MV2}$ | 4.54 |
| GD1 | TI LMG1020 | $t_{Dr}$ | 2.50 |

### B. Rectifier Design

According to (27), $D$ significantly influences the rectifier voltage gain $G_R$ and therefore must be carefully selected when a specific output voltage is required. In our prototype, the input ac voltage $V_r$ of the rectifier is determined by

$$V_r = \omega k I_t \sqrt{L_t L_r} = 29.7 \text{ V} \tag{29}$$

where the parameters $k$, $I_t$, $L_t$, and $L_r$ are set by the fixed specifications of the transmitter and coupling coils. To achieve the target output voltage $V_o = 24$ V, the rectifier must be designed to deliver the corresponding voltage gain

$$G_R = V_o / V_r = 0.807. \tag{30}$$

Substituting (30) into (27) yields a parametric relationship between $D$ and $\omega_s^*$.

In addition, the load-independent ZVS condition requires (15) to be satisfied, providing a second equation linking $D$ and $\omega_s^*$. By solving (27) and (15) simultaneously, we obtain a unique solution: $D = 0.73$ and $\omega_s^* = 1.049$, which satisfy both the required voltage gain and the ZVS condition. These values are visually illustrated in Fig. 6(a).

For the implementation, a Micrometals Mix-6 powder core with six turns of AWG18 wire was selected for $L_c$, resulting in an inductance of 314.3 nH. The corresponding shunt capacitance to achieve $\omega_s^* = 1.049$ is

$$C_s = \frac{1}{(\omega_s^* \omega)^2 L_c} = 1.592 \text{ nF}. \tag{31}$$

TABLE V
COMPARISON OF RECENT SELF-SYNCHRONIZED CLASS-E RECTIFIERS

| Research | Circuit Topology | $f$ (MHz) | Extra Resonant Method | Synchronization Components | Eff. (%) $\eta_{WPT}/\eta_{Rct}$ | Controller Complexity |
|---|---|---|---|---|---|---|
| [12] | Class-E | 13.56 | $v_s$ ZXD | None | – / 94.0[2] | Low |
| [13] | Push-Pull Class-E | 6.78 | External (Aux. Coil) | 3L 1C | 86.7 / 94.6 | Low |
| [14] | Class-E[1] | 6.78 | Input Current Sensing | 1L 1C | – / 81.6 | High (Computer) |
| [15] | Push-Pull Class-E | 6.78 | $v_s$ ZXD | None | 91.6 / 97.0 | High (FPGA) |
| [16] | Class-E | 1 | $v_s$ ZXD | None | – / – | High (DSP) |
| [17] | Class-E | 13.56 | $L_s$ voltage ZXD | 1L 1C | – / 93.1 | Low |
| Proposed | Class-E | 6.78 | $v_s$ FPXD | None | 87.6 / 96.8 | Low |

[1] The nonlinear output capacitance of the GaN FET is considered. [2] Efficiency tested using an external driving signal. Estimated efficiency based on the GaN FET thermal image and simulation. The self-synchronous version was implemented on a drone without direct efficiency measurement.

Substituting $D$ and $\omega_s^*$ into (28), we derive $X_{Eq}/X_c = 1.141$ as shown in Fig. 6(b). Thus, the equivalent input capacitance of the class-E rectifier is

$$C_{Eq} = \frac{1}{1.141\,\omega^2 L_c} = 1.538 \text{ nF}. \tag{32}$$

To maintain a constant reactance as seen by the inverter, $C_r$ should be selected such that the series combination $C_r' = C_r||C_{Eq}$ resonates with $L_r$ at $\omega$, which is

$$\omega = \frac{1}{\sqrt{L_r C_r'}}. \tag{33}$$

Namely, the required value of $C_r'$ is

$$C_r' = \frac{1}{\omega^2 L_r} = 290.0 \text{ pF}. \tag{34}$$

This leads to the component value of

$$C_r = \frac{C_{Eq} C_r'}{C_{Eq} - C_r'} = 357.4 \text{ pF}. \tag{35}$$

Table III gives the designed circuit component values for the implemented WPT system.

### C. Maximum Operating Frequency

To ensure a timely turn-ON of the switch, the propagation delays introduced by the synchronization circuit must be compensated. Substituting (4) and (26) into (3), the required pulse width $t_{Cps}$ of MV1 is calculated as

$$t_{Cps} = \frac{D}{2f} - t_X - t_{Mv1} - t_{Mv2} - t_{Dr}. \tag{36}$$

Namely, the required $t_{Cps}$ decreases as the frequency increases, as shown in Fig. 9. If the frequency becomes too high, (36) results in a negative $t_{Cps}$, which is physically unrealizable.

Consequently, the maximum feasible switching frequency $f_{\text{Max}}$ for a given set of components is determined by the critical condition $t_{Cps} = 0$. The components must be selected such that

$$f_{\text{Max}} = \frac{1}{2(t_X + t_{Mv1} + t_{Mv2} + t_{Dr})} \geq f. \tag{37}$$

Table IV gives the propagation delays for two candidate component sets. Candidate 1 employs cost-effective components, while Candidate 2 uses high-speed ones with higher costs. Fig. 9 shows the required pulse width $t_{Cps}$ as a function of switching frequency $f$. The maximum operating frequencies of the two candidates are 11.4 MHz and 28.1 MHz, respectively.

In this study, Candidate 1 was selected due to its cost efficiency, which sufficiently supports the target frequency 6.78 MHz. However, for higher ISM band frequencies such as 13.56 MHz or 27.12 MHz, Candidate 2 is required. According to (36), the required pulse width of MV1 was $t_{Cps} = 21.9$ ns.

### D. Self-Synchronous Circuit Design

From (22), we have

$$\frac{V_{Fix}}{V_o} = 1 - \cos(\omega_s^*\theta) + \pi(1-D)\sin(\omega_s^*\theta)\omega_s^* = 2.34 \tag{38}$$

as visually shown in Fig. 6(b). This leads to an absolute voltage of $V_{Fix} = 56.1$ V.

To scale $v_s$ within the safe operating range of the comparator, the voltage divider resistors were chosen as $R_{v1} = 27.8$ kΩ, $R_{v2} = 1.48$ kΩ. This results in a reference voltage $V_{Ref}$ given by

$$V_{Ref} = \frac{R_{v2}}{R_{v1} + R_{v2}} V_{Fix} = \frac{R_{v4}}{R_{v3} + R_{v4}} V_o = 2.84 \text{ V}. \tag{39}$$

## VI. PARAMETER SENSITIVITY

The sensitivity of the proposed FPXD method to circuit parameters is crucial for ensuring reliable operation. This section analyzes the impact of variations in the turn-ON timing, reference voltage, circuit components, and working conditions on the circuit performance.

### A. Sensitivity to $C_r$ and $L_r$

The tolerance of the circuit components may affect the shape of the waveform of $v_s$, which in turn influences the fixed-point crossing time $t_{Fix}$. Fig. 10(a) and (b) show simulation rated-load waveforms with $\pm 10\%$ changes in $C_r$ and $L_r$, respectively. Fig. 11(a) shows the variation in fixed-point crossing time $t_{Fix}$ with these changes. It can be observed that $C_r$ and $L_r$ influence the circuit similarly, as $1/\sqrt{(C_r||C_{Eq})L_r}$ determines the resonant frequency of the receiver. A decrease in either $L_r$ or $C_r$ results in an earlier ZVS, i.e., a negative $\Delta t_{Fix}$. Conversely, $t_{Fix}$ is less sensitive to increases in $L_r$ or $C_r$. A 10% increase in either component results in a change of less than $\pm 2\%$ variation in $t_{Fix}$.

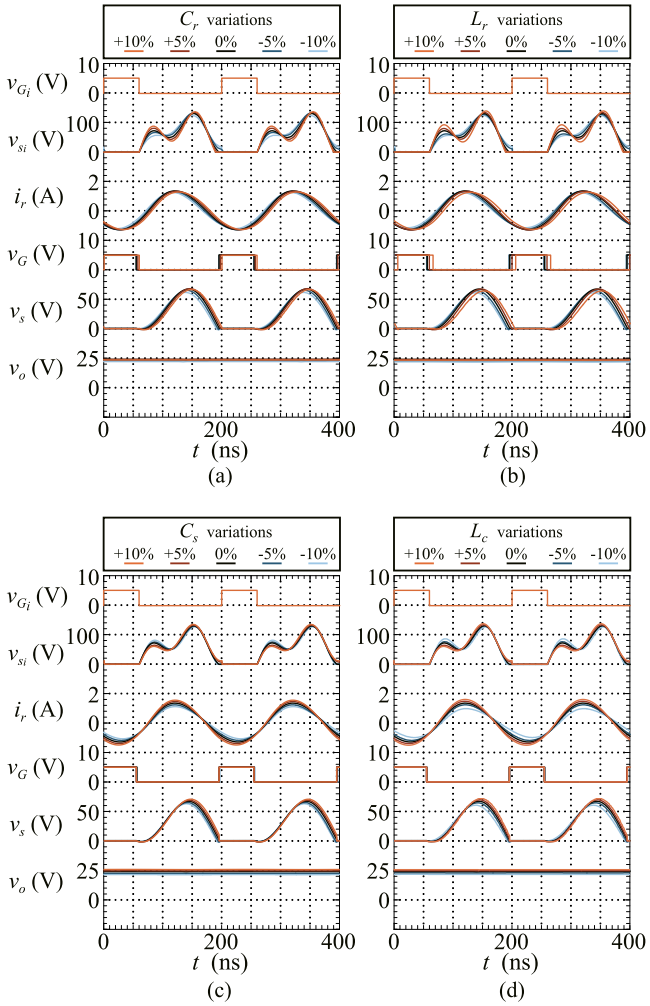


Fig. 10. Simulation waveforms of the WPT system under rated load with variations in circuit component values. (a) Variation in $C_r$. (b) Variation in $L_r$. (c) Variation in $C_s$. (d) Variation in $L_c$.

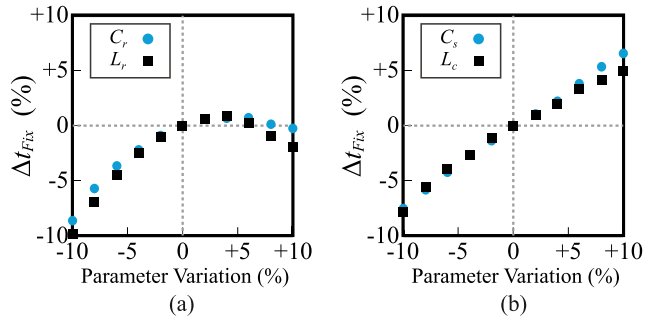


Fig. 11. Change in $t_{Fix}$ with variations in circuit component values. (a) Variation in $C_r$ and $L_r$. (b) Variation in $C_s$ and $L_c$.

Furthermore, as shown in Fig. 10(a) and (b), the power transmitter switch voltage $v_{si}$ suffers from non-ZVS when $L_r$ or $C_r$ decreases. This behavior is attributed to a deviation from the resonant condition in (33). In conclusion, the system is relatively robust against increases in $L_r$ and $C_r$, but sensitive to decreases in them. Setting a positive bias of within 0%–5% in either parameter is considered a good balance for compensating component value variations while preserving reliable system performance.

### B. Sensitivity to $C_s$ and $L_c$

The simulation waveforms under rated-load conditions with changes in the shunt capacitance $C_s$ and the output inductance $L_c$ are shown in Fig. 10(c) and (d), respectively. Fig. 11(b) shows how $t_{Fix}$ varies with these changes. Note that variations in the FET output capacitance $C_{OSS}$ effectively appear as changes in $C_s$. $C_s$ and $L_c$ influence the circuit similarly, as $1/\sqrt{C_s L_c}$ determines $\omega_s$. As shown in Fig. 11(b), $t_{Fix}$ is sensitive to variations in these components: a $\pm 5\%$ bias in either $C_s$ or $L_c$ leads to an approximate $\pm 3\%$ shift in $t_{Fix}$.

Fig. 10(c) and (d) further show that an increase in $C_s$ or $L_c$ results in an insufficient discharge of $C_s$, causing non-ZVS in the rectifier voltage $v_s$. These variations can also disrupt ZVS in the inverter because the equivalent input reactance $X_{Eq}$ of the rectifier, predicted in (28), is no longer preserved.

### C. Sensitivity to $V_r$

In some applications, the input ac voltage $V_r$ of the rectifier, defined in (29), may vary due to changes in the coupling coefficient $k$ (e.g., from coil misalignment) or inverter output current $i_t$ (e.g., from input dc-voltage variations). These changes result in a proportional scaling of the switch voltage waveform $v_s$, which in turn scales the fixed-point voltage $V_{Fix}$. If a fixed detection threshold $V_{Ref}$ is used, such variation in $V_r$ may cause incorrect timing. In extreme cases, the peak value of $v_s$ may fall below the origin level of $V_{Fix}$ without crossing it, leading to a missed driving pulse.

To address this, the proposed circuit does not use a fixed $V_{Ref}$, but derives it from the rectifier output voltage $V_o$ instead. This is realized using a resistor divider as shown in Fig. 4(a). This implementation yields

$$V_{Ref} = \frac{R_{v4}}{R_{v3}+R_{v4}} V_o = \frac{R_{v4}}{R_{v3}+R_{v4}} G_R V_r. \tag{40}$$

As a result, the detection threshold $V_{Ref}$ also scales proportionally with $V_r$, thereby tracking the change in $V_{Fix}$. In other words, the ratio of $V_{Fix}/V_{Ref}$ remains constant and independent of rectifier input $V_r$. This ensures consistent gate-drive timing even under variations in the coupling coefficient or input dc voltage. Furthermore, if regulated output is required, a voltage regulator can be connected downstream of the rectifier without compromising the synchronization performance.

### D. Sensitivity to $t_{PD}$ and $t_{Fix}$

To achieve optimal switching performance, the propagation delay $t_{PD}$ should match the fixed-point crossing time $t_{Fix}$, as defined in (4). However, in practical implementations, both $t_{PD}$ and $t_{Fix}$ may deviate due to component tolerances, resulting in timing mismatches and additional turn-ON power loss. This time mismatch can be quantified as

$$\beta = (t_{PD} - t_{Fix})/t_{Prd} \tag{41}$$

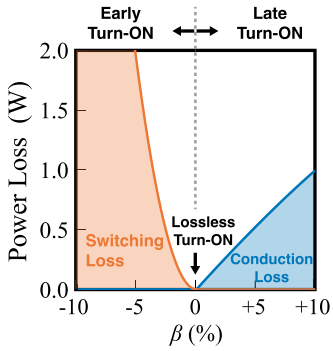


Fig. 12. Extra turn-ON power loss as a function of $\beta$ under rated-load conditions.

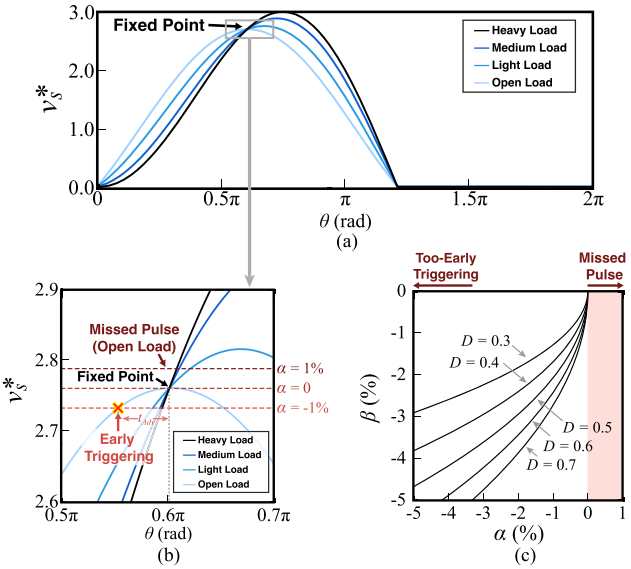


Fig. 13. Typical waveform of the switch voltage. (a) Overall view. (b) Zoomed-in view of switch voltage and threshold voltage for different $\alpha$ values. (c) Normalized switching-time misalignment $\beta$ as a function of $\alpha$ under various $D$ values under open-load condition (the worst case).

where $t_{Prd} = 1/f$ is the switching period. Fig. 12 shows the relationship between $\beta$ and the additional turn-ON power loss under rated-load conditions. A positive $\beta$ corresponds to a late turn-ON event, leading to reverse conduction loss, similar to what is observed in the intracycle ZXD-based rectifier. Conversely, a negative $\beta$ implies early turn-ON, which induces hard-switching loss. To mitigate this sensitivity and achieve $\beta = 0$, a tunable resistor (PVG5A502C01R00) was used for $R_{Mv1}$ to fine-turning $t_{Cps}$. This allows precise alignment of the gate signal with the negative zero-crossing of $v_s$ against potential variations in $t_{PD}$.

### E. Sensitivity to $V_{Ref}$

The slope of the switch voltage $v_s$ is influenced by the load resistance $R_L$ according to (25). Under open-circuit conditions, the slope approaches zero, as shown in Fig. 13(a) and (b). This makes it difficult to reliably detect the zero-crossing of $v_s$, because even a small positive deviation in the detection threshold $V_{Ref}$ may cause the comparator to miss the crossing entirely, leading to a missed gate-driving pulse. In such cases, the FET will fail to receive a gate-driving pulse, and the rectifier will operate in a degraded passive mode through body-diode conduction.

To address this issue in practice, a small negative offset can be applied to $V_{Ref}$ to ensure reliable detection of the crossing point, as shown in Fig. 13(b). The adjusted reference voltage $V'_{Ref}$ is defined as

$$V'_{Ref} = V_{Ref}(1 + \alpha) \tag{42}$$

where $\alpha$ is the offset factor.

However, introducing this offset results in an earlier switching event, i.e., a negative timing mismatch $\beta$, which becomes significant under light-load or open-circuit conditions. Fig. 13(c) shows the relationship between the normalized switching-time misalignment $\beta$ and the offset factor $\alpha$ for various duty ratios $D$. As shown, $\beta$ becomes more negative as $\alpha$ becomes more negative. The value of $\alpha$ must therefore be carefully chosen to balance robustness against missed pulses and accuracy of turn-ON timing. For $D = 0.7$, setting $\alpha = -1\%$ ensures that $\beta$ remains below 3% even under open-circuit conditions, which is acceptable for practical applications. This leads to $V'_{Ref} = 0.99\ V_{Ref} = 2.81\ V$. For deriving $V'_{Ref}$ from output voltage $V_o$, we selected $R_{v3} = 33.0\ \text{k}\Omega$ and $R_{v4} = 4.32\ \text{k}\Omega$.

## VII. Experimental Validation

### A. Experimental Prototype

An experimental prototype was developed based on the design results in Section V. A close-up view of the implemented rectifier is shown in Fig. 8(b), while Fig. 8(c) shows the overview of the WPT system. Our goal is to verify the effectiveness of the proposed FPXD method for achieving intracycle self-synchronization.

The self-synchronous components (CP1, MV1, MV2, and GD1) are powered by a 5 V dc source, which is derived from the rectified output voltage $V_o$ using a CJ78L05 LDO. A key feature of the proposed rectifier is its self-starting mechanism. At startup, when no driving signal is present, switch $S$ initially operates as a diode, allowing the circuit to function as a passive rectifier. This enables the instant charging of the output capacitor $C_F$, which then powers the self-synchronous circuit.

For the rectifier, we used a GS61004B GaN FET from Infineon (formerly GaN Systems) as the switching component. VJ HIFREQ Series capacitors from Vishay were used for resonant and shunt capacitances.

The external shunt capacitance $C_{Ext}$ was calculated considering the nonlinear output capacitance $C_{OSS}$ of the GaN FET, as detailed in the Appendix.

For the class-EF inverter, we used an EPC2012 C GaN FET from EPC, driven at 6.78 MHz via a TI LMG1020 gate driver. The high-order resonant inductor $L_2$ was implemented using a T-68-6 toroidal core from Micrometals.

An LI class-E rectifier with intracycle ZXD, shown in Fig. 3, was also implemented for comparison. The main power circuits of both rectifiers were identical, with the only difference being

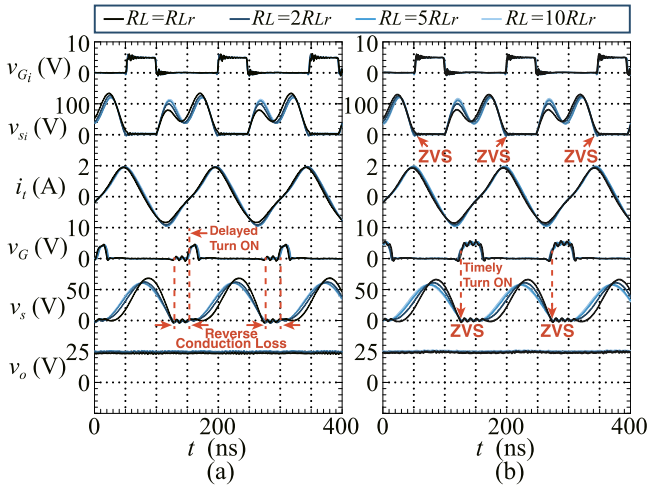


Fig. 14. Experimental waveforms of the class-E rectifier. (a) Intracycle ZXD. (b) Proposed intracycle FPXD.

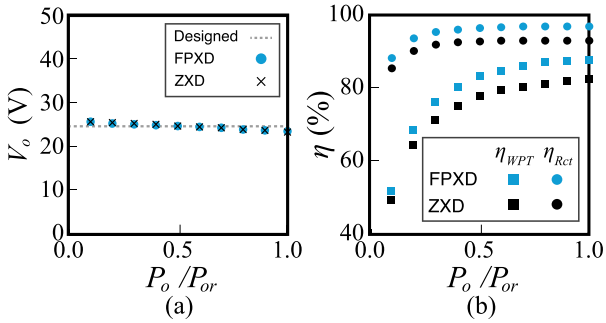


Fig. 15. Measured characteristics of the proposed rectifier as functions of normalized output power. (a) Output voltage. (b) Power conversion efficiency.

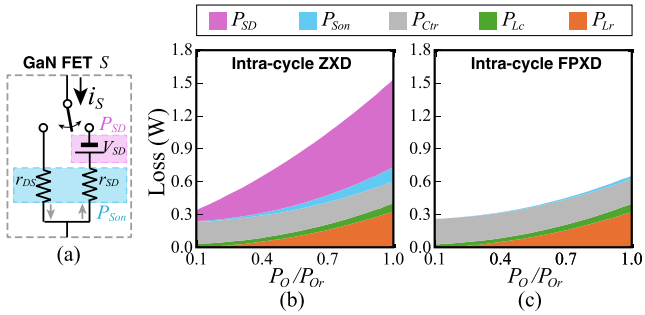


Fig. 16. Breakdown of power losses in the proposed rectifier. (a) Power loss model of GaN FET $S$. (b) Intracycle ZXD rectifier. (c) Intracycle FPXD rectifier.

their self-synchronous circuits. Both rectifiers were powered by the same class-EF inverter wirelessly. In addition, the gate voltage width $t'_{ON}$ of the intracycle ZXD rectifier was adjusted to ensure that switch $S$ maintained the same turn-ON duration as in the FPXD rectifier, ensuring a fair comparison.

### B. Steady-State Waveforms

A Kikusui PLZ205 W electronic load was used to sweep the load resistance from 28.8 Ω ($R_{Lr}$) to 288 Ω ($10R_{Lr}$). The measured waveforms of both circuits are shown in Fig. 14.

It can be observed that the intracycle ZXD rectifier exhibited a significantly delayed turn-ON due to propagation delays. In contrast, the proposed intracycle FPXD rectifier maintained a phase-locked gate voltage, independent of load variations. The rising edge of $v_G$ in the FPXD rectifier aligned precisely with the negative zero-crossing of $v_s$, effectively eliminating both switching loss and reverse-conduction loss. These results confirm that the fixed point was successfully detected and that propagation delays were properly compensated.

In addition, the inverter output current $i_t$ maintained a constant phase angle regardless of load variation. This is because the input reactance $X_{Eq}$ remained constant, as given in (28). This stability enabled the class-EF inverter to sustain ZVS operation. Furthermore, Fig. 15(a) shows the measured output voltage $V_o$ as a function of output power. The voltage reached the designed value of 24 V and remained nearly constant, validating the LI operation of the rectifier.

### C. Efficiency and Power Losses

Fig. 15(b) shows the measured dc–dc efficiency $\eta_{WPT}$ of the WPT system. The efficiency was measured using two Iwatsu VOAC7523H digital multimeters and is calculated as

$$\eta_{WPT} = P_o/P_I = \frac{V_o I_o}{V_I I_I}. \tag{43}$$

The WPT system with the intracycle ZXD rectifier achieved a maximum efficiency of 82.8%, whereas the WPT with the proposed FPXD rectifier reached 87.6%. This efficiency improvement is attributed to the reduced power losses in the proposed rectifier.

To evaluate the ac–dc efficiency of the rectifier, we performed a power loss analysis. The power-loss model of the GaN FET is shown in Fig. 16(a), where $r_{DS} = 19.2$ mΩ, $r_{SD} = 105$ mΩ, and $V_{SD} = 1.7$ V. $P_{Son}$ is the FET conduction loss due to the ON-state resistances, while $P_{SD}$ is the loss caused by the reverse voltage drop $V_{SD}$. Other power losses include the inductor loss in $L_c$ ($P_{Lc}$), the receiving-coil loss in $L_r$ ($P_{Lr}$), and the self-synchronous circuit loss ($P_{Ctr}$). $P_{Ctr}$ includes the power consumption of the comparator, multivibrators, and gate driver, which were measured experimentally.

Fig. 16(b) shows the power loss breakdown of the intracycle ZXD rectifier. The dominant power loss was the reverse voltage-drop loss $P_{SD}$. This loss occurred due to the delayed turn-ON of the switch. Since the rectifier was designed with a high off-duty ratio to achieve the target gain $G_R$, the propagation delay $t_{PD}$ exceeds half of $t_{on}$, making the impact of delayed turn-ON particularly significant. This result confirmed the limitation of the ZXD method for achieving intracycle synchronization.

Fig. 16(c) shows the power loss breakdown of the proposed FPXD rectifier. The proposed rectifier eliminates $P_{SD}$ by ensuring timely turn-ON, achieving a total loss reduction of 56.9% at heavy load conditions compared to the intracycle ZXD version. This result verified the effectiveness of the proposed FPXD

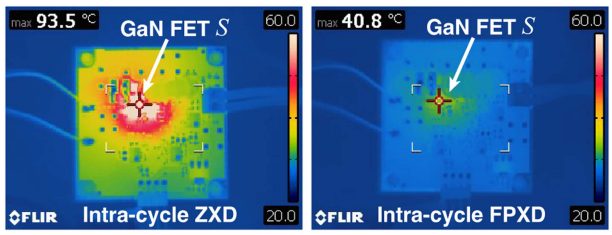


Fig. 17. Thermal images of the rectifiers after 30 minutes of heavy-load operation. (a) Intracycle ZXD rectifier. (b) Intracycle FPXD rectifier. *Test conditions: Same PCB design with switchable self-synchronous circuits. $S$ mounted on an FR4 PCB (25 cm$^2$, 1 oz copper land). Room temperature: 23 °C. No forced air cooling. $V_I$ reduced to 36 V in both circuits to prevent thermal runaway in the ZXD rectifier. Thermal images were captured using a FLIR E50 infrared camera.

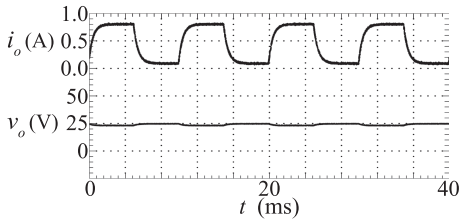


Fig. 18. Transient response of the proposed rectifier against sudden load change.

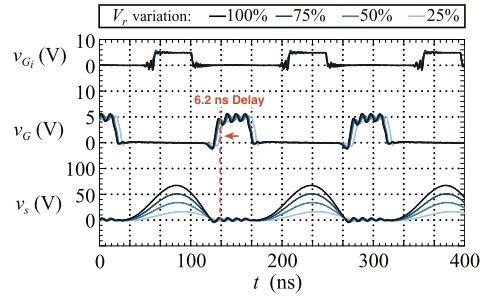


Fig. 19. Input voltage variation of the proposed rectifier. All waveforms were captured phase-aligned to the inverter gate signal $v_{Gi}$.

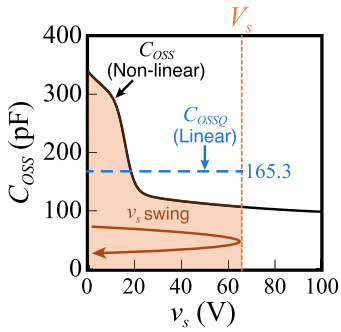


Fig. 20. Nonlinear output capacitance $C_{OSS}$ of the GaN FET and the charge-based equivalent output capacitance $C_{OSSQ}$ as functions of the drain-to-source voltage $v_s$.

method for achieving intracycle self-synchronization. Under heavy-load conditions, the receiver coil $L_r$ was the largest source of power loss, whereas under light-load conditions, losses in the self-synchronous circuit dominated because they did not scale with the load resistance.

Based on the loss prediction, the ac–dc efficiency of the proposed rectifier $\eta_{Rct}$ was estimated as

$$\eta_{Rct} = P_o/(P_o + P_{Loss}) \tag{44}$$

where $P_{Loss}$ represents the total power loss in the rectifier.

Fig. 15(b) shows the estimated rectifier ac–dc efficiency $\eta_{Rct}$. The proposed intracycle FPXD rectifier achieved a maximum efficiency of 96.2%, compared to 91.3% for the intracycle ZXD rectifier. Fig. 17 shows thermal images of the two rectifiers after 30 minutes of operation at maximum output power $P_{or}$. The proposed intracycle FPXD rectifier exhibited significantly lower GaN FET temperatures than the intracycle ZXD version, confirming its reduced power losses.

### D. Transient-State Waveforms

To evaluate the robustness of the proposed rectifier against sudden load variations, a 100 Hz periodic step change in load resistance was applied, alternating between $R_{Lr}$ (28.8 Ω) to $10R_{Lr}$ (288 Ω). Fig. 18 shows the transient response of the proposed FPXD rectifier. The output voltage remained nearly constant throughout the load transition, verifying that the self-synchronization mechanism maintained robust operation without loss of control.

### E. Input Variation

An additional experiment was performed to validate the circuit robustness against input ac voltage $V_r$ caused by coupling coefficient $k$ variations or input dc voltage variations. The rectifier input voltage $V_r$ was varied from 25% to 100% of the nominal value by adjusting the supply voltage of the class-EF inverter. The measured waveforms are shown in Fig. 19. It can be observed that the phase of the gate voltage $v_G$ remained nearly constant for 50%, 75%, and 100% input conditions. However, a delay of 6.2 ns in the turn-ON timing was observed at 25% input. This is attributed to the increased output capacitance $C_{OSS}$ of the GaN FET under low-voltage operation. This variation has a similar effect to increasing $C_s$, which distorts the shape of $v_s$, and shifts the fixed point, as discussed in Section VII-B.

Based on the experimental results, we confirmed that the proposed FPXD method achieved high efficiency and robustness for achieving intracycle self-synchronization.

## VIII. Research Comparison

To compare the proposed approach with existing methods, we conducted a literature review of recent studies on self-synchronized class-E rectifiers, summarized in Table V on the top of page 12. Compared with existing methods, the proposed rectifier achieves intracycle synchronization without requiring additional resonant inductors or digital controllers. This contributes to reduced circuit complexity, improved miniaturization, and lower system cost for compact WPT applications. By

applying the FPXD method, precise turn-ON timing is achieved, enabling consistent ZVS operation across varying loads. As a result, switching losses are significantly reduced, leading to high power conversion efficiency.

## IX. Conclusion

This article presented an intracycle self-synchronized LI class-E rectifier based on a novel FPXD method. Through circuit analysis, we identified that the drain-to-source voltage of the LI class-E rectifier consistently crosses a fixed voltage threshold at a specific phase angle prior to turn-ON, independent of load resistance. This fixed crossing point serves as a reliable trigger for gate-drive signal generation. Therefore, the proposed approach enables intracycle synchronization without the need for additional resonant components or control circuitry. Analytical expressions for the fixed point were derived, and a systematic design procedure was provided. A 6.78 MHz, 20 W WPT prototype was implemented and tested. The rectifier maintained robust load-independent performance, demonstrating nearly constant output voltage and input reactance across varying loads. Compared with the ZXD-based intracycle synchronization, the proposed method achieved more precise switching, eliminating reverse conduction and switching losses, and reducing total rectifier effectively.

As part of our future work, we plan to explore methods to enhance robustness against component variations, particularly in parameters such as $C_s$ and $L_c$. In addition, we aim to extend the proposed FPXD method to other topologies, such as the class-EF rectifier. Like the LI class-E rectifier, the LI class-EF topology also exhibits a fixed voltage crossing point suitable for synchronization. However, due to its characteristic double-peak switch voltage waveform, implementing FPXD in this topology will require the development of a selective detection circuit capable of isolating the correct crossing point. Addressing this challenge will be a key focus of our subsequent research.

## Appendix
## Shunt Capacitance of the Class-E Rectifier

The shunt capacitance of the class-E rectifier includes the external capacitor $C_{Ext}$ and the output capacitance $C_{OSS}$ of the GaN FET. $C_{OSS}$ is nonlinear depending on the drain-to-source voltage $v_s$. For the GS61004B GaN FET used in our prototype, we extracted an approximation of $C_{OSS}(v_s)$ from the device's LTspice model [26], which is

$$C_{OSS}(v_s) = 92.8 + \frac{178.3 \times e^{0.115(-8-v_s)}}{1+e^{0.115(-8-v_s)}} + \frac{2.145 \times e^{0.0429(80-v_s)}}{1+e^{0.0429(80-v_s)}} + \frac{157.5 \times e^{0.5(16-v_s)}}{1+e^{0.5(-16-v_s)}} + \frac{50.7 \times e^{0.03(31-v_s)}}{1+e^{0.03(31-v_s)}} \quad (45)$$

where $C_{OSS}$ is in pF and $v_s$ is in V. Fig. 20 shows the output capacitance $C_{OSS}$ as a function of $v_s$.

To account for this nonlinearity during the design process, we used a practical approach based on the charge-equivalent capacitance method. The charge-based equivalent capacitance $C_{OSSQ}$ is computed by integrating the charge over the operating voltage range

$$C_{OSSQ} = \frac{1}{V_s}\int_0^{V_s} C_{OSS}(v_s')dv_s' = 165.3 \text{ pF} \quad (46)$$

where $V_s = 65.8$ V is the peak drain-to-source voltage derived from waveform equation. This formulation ensures that the integrated charge of the nonlinear $C_{OSS}(v_s)$ over a voltage swing from 0 to $V_s$ is equivalent to that of a linear $C_{OSSQ}$, as shown in Fig. 20. Then, $C_{OSSQ}$ was subtracted from the total calculated shunt capacitance $C_s$ to determined the external capacitor $C_{Ext}$ as

$$C_{Ext} = C_s - C_{OSSQ} = 1.427 \text{ nF}. \quad (47)$$

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