Fully Soft Switched Ultra-High Step-Up Quadratic Converter Without Reverse Recovery Issue

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***Abstract*—This article presents a new ultrahigh step-up converter with fully soft switching conditions. In the proposed converter, ultrahigh voltage gain (VG) is obtained by combining the coupled inductors (CIs), voltage multiplier cell, and the quadratic structure. To provide soft switching conditions, an active clamp circuit is used to recover the leakage inductances energy as well as boost the VG. As a result, the switching and capacitive losses are reduced. The reverse recovery problem of the input diodes in quadratic converters is a major challenge. Due to the presence of CIs leakage inductances, all diodes experience low reverse recovery characteristic. Since the proposed converter has a low number of utilized components and because of the mentioned benefits, high efficiency is attained. In addition, the presented structure has common ground between the input and output while input current is continuous. The experimental results are achieved utilizing a laboratory prototype developed for 48–650 V at nominal output power of 200 W to validate the proposed converter theoretical analysis.**

***Index Terms*—Low reverse recovery (LRR), ultrahigh step-up converter, voltage multiplier cell (VMC), zero voltage switching (ZVS).**

I. Introduction

HIGH step-up dc–dc converters have become increasingly important in recent years as the demand for renewable energy and electric vehicles has grown. Because of the low output voltage of renewable energy systems, it is necessary to increase the voltage level of the grid using the high step-up converters [1]. Although the conventional step-up converter has a low number of elements and price, but due to the existence of parasitic elements, it cannot provide high voltage gain (VG) and due to the high voltage stress across the output diode and the switch, this converter is not suitable for high output voltage applications [2].

Two-winding and three-winding coupled inductors (CIs) are used as regular methods to increase the VG in high step-up converters [3], [4]. Also, in addition to increasing the VG, low reverse recovery (LRR) conditions can be created for diodes by the leakage inductance. However, the stored energy in the leakage inductance causes voltage spikes across the active switch, which requires the use of passive or active clamp circuits to recover this energy [5], [6].

The quadratic or cascaded converters and their combination with two-winding and three-winding CIs and VMC are presented in [7], [8], [9], [10], [11], and [12]. In [7] and [8] three-winding CIs are combined with a quadratic structure, resulting in a high VG. However, due to the placement of the inverse winding, the duty cycle of these converters is limited. Also, the VG in [9] is low in compared with the number of elements. In addition, a family of two-switches cascaded converters are proposed in [10], [11], and [12]. These converters achieve ultrahigh VG and feature switches that turn ON under zero current switching (ZCS) condition. However, these converters still experience capacitive turn ON losses and turn OFF switching losses.

To recover the leakage inductance energy, some converters with active clamp circuit are introduced in [13], [14], and [15]. In these converters, in addition to the solving of voltage spikes at the switches, zero voltage switching (ZVS) conditions are provided for the main and auxiliary switches and the capacitive losses of the switches are eliminated. The ZVS high step-up converters in [16], [17], [18], [19], [20], [21], and [22] are based on the quadratic structure or cascaded structures combined with CIs. In [16], the proposed converter is fully LRR although it has low VG employing three active switches and three cores, which increases the volume and control circuit complexity. In addition, Alavi et al. [17] and Mohseni et al. [18] introduce cascaded converters that utilize three and four active switches, respectively. Consequently, the cost and complexity of these converters are increased. Additionally, the presented converters in [19], [20], [21], and [22] have ultrahigh VG but the common ground is lost in [19] and [21]. It should be noted that these converters require increased number of VMCs to achieve an ultrahigh VG which increases the converter components count.

Additionally, the converter presented in [22] has three magnetic cores, which increases the converter volume. Moreover, the input diodes of converters in [19], [20], [21], and [22] experience high reverse recovery.

This article proposes a quadratic ultrahigh step-up converter utilizing CIs and an auxiliary circuit which provide ZCS conditions for the quadratic structure input and output diodes to overcome the reverse recovery problem and improve efficiency. The auxiliary circuit consists of a voltage multiplier cell (VMC) that significantly increases the proposed converter VG. Moreover,

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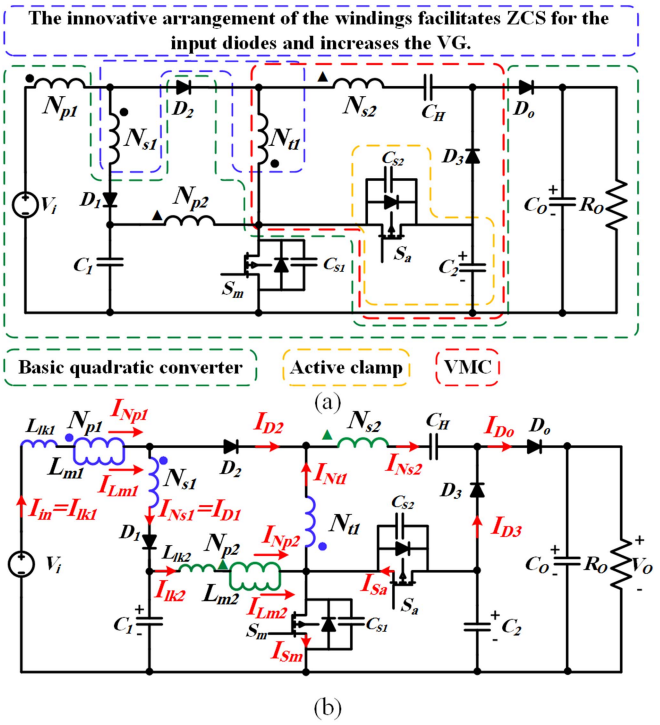

Fig. 1. (a) Proposed ultrahigh step-up converter. (b) Equivalent circuit.

the converter has employed an active clamp circuit delivering ZVS conditions for the switches at turn ON and turn OFF which eliminates capacitive losses. The suggested structure provides many benefits, including ultrahigh VG, very low diodes reverse recovery, full soft switching condition, absorbing the leakage inductances stored energy, common ground between the input and output, high efficiency and low number of elements.

II. State Analysis of the Proposed Converter

The proposed ultrahigh step-up quadratic converter is shown in Fig. 1. As shown, a three winding CIs is added to a quadratic converter. A ZVS cell including an active switch S_a and clamp capacitor C_2 is utilized to create soft switching conditions for switches. Also, this converter includes diodes D_1, D_2, D_3, and D_o, capacitors C_1, C_H, and C_o and a two-winding CIs. The CIs are modeled by ideal transformers with magnetizing inductances L_{m1} and L_{m2} as well as leakage inductances L_{lk1} and L_{lk2} on the primary side. N_{p1}, N_{s1}, N_{t1}, N_{p2}, and N_{s2} represent the turns numbers of the primary, the secondary and the tertiary of the three winding CI and the primary and secondary the two winding CI, respectively. Therefore, the turn ratio of the three winding and two winding CIs are clarified as $n_1 = N_{s1}/N_{p1}$, $n_2 = N_{t1}/N_{p1}$ and $m = N_{s2}/N_{p2}$ respectively. Also, diode D_3 and capacitor C_H been defined as the VMC. Because of the circuit resonance conditions, C_H is chosen to ripple around its average voltage. While the capacitors C_1, C_2, and C_o are large enough to be expected to have a constant voltage. Furthermore, L_{m1} is large enough that its current is considered to remain constant, but L_{m2} is chosen that its current being negative.

The proposed converter has six operating states during one switching cycle. Figs. 2 and 3 show the equivalent circuit as well as key waveforms within a switching period, respectively. It should be noted that before the first state, S_m is not conducting, S_a is conducting, and D_1 is forward biased.

State I [t_0, t_1]: At t_0, S_a is turned OFF at ZVS conditions due to C_{S2} and i_{Lm2} which is negative, charges C_{S2} and discharges C_{S1} toward V_{C2} and zero, respectively. When V_{Sm} reaches V_{C1}, D_2 is forward biased as well as D_1 and D_2 conduct together. In addition, due to the positive polarity on L_{m2}, this inductor is being charged. Due to the presence of L_{lk1}, I_{D1} and I_{s1} decrease with a same slope until they reach zero and D_1 turns OFF under ZCS states, which eliminates the reverse recovery problem. Moreover, I_{D2} and I_{t1} increase with the opposite slope of I_{D1}. Also, when V_{Sm} reaches zero, its body diode starts to conduct and its current increases linearly. Due to the conduction of S_m body diode, S_m can be turned ON under zero voltage-zero current switching (ZVZCS) condition. This state continues as long as D_3 starts to conduct.

State II [t_1, t_2]: When D_1 is reverse biased, the voltage across L_{m1} becomes positive and starts charging. In addition, D_3 forward biases and a resonance occurs with frequency f_{r1} while, C_H charges through N_{s2} and C_2. The current through S_m is the summation of I_{t1} and I_{lk2}. This state continues until half-cycle of resonance is finished and I_{D3} reaches zero and D_3 turns OFF under ZCS condition

$$f_{r1} = \frac{1}{2\pi\sqrt{L_{\text{eq1}}C_{\text{eq1}}}} \tag{1}$$

where

$$L_{\text{eq1}} = n_2 L_{\text{lk1}} + \left(m\left(1-n_2\right)\right)^2 L_{\text{lk2}} \tag{2}$$

$$C_{\text{eq1}} = \frac{C_1 C_2 C_H}{\left(1-n_2\right)^2\left[m^2 C_2 C_H + C_1 C_H + C_1 C_2\right]}. \tag{3}$$

State III [t_2, t_3]: At t_2, D_3 reverse biases with a small voltage close to zero. In this state, I_{Lk1} and I_{Lt1} are equal and flowing in opposite directions. Also, I_{Sm} is rising linearly. By turning OFF S_m, this state is completed.

State IV [t_3, t_4]: At t_3, S_m is turned OFF under ZVS condition because of the snubber capacitor C_{S1}. At the same time that C_{S1} is charged towards V_{C2}, the capacitor C_{S2} is discharged by the summation of I_{Lm2} and I_{lk1}. When V_{Sm} reaches V_{C1}, diodes D_1 and D_2 conduct and their currents increase and decrease with opposite slopes, respectively. When I_{D2} reaches zero, D_2 turns OFF under ZCS with mitigated reverse recovery. Also, when V_{Sa} reaches zero, the body diode of S_a conducts and this switch can be turned ON under ZVZCS. Since, the sum of V_{CH}, V_{C2}, and V_{s2} is less than V_o, D_O is still in reverse bias condition. This state ends when the output diode D_O is forward biased.

State V [t_4, t_5]: At t_4, D_o turns ON and a resonance occurs with frequency f_{r2} as described by (4) and the stored energy in C_H, L_{m1}, and L_{m2} is released to the load and C_O through N_{s2}, and N_{t1}. Also, the current through the main switch S_a is the difference of I_{t1} and I_{lk2}. This state continues until the half-cycle of resonance is reached and I_{Do} reaches zero causing D_o to turn

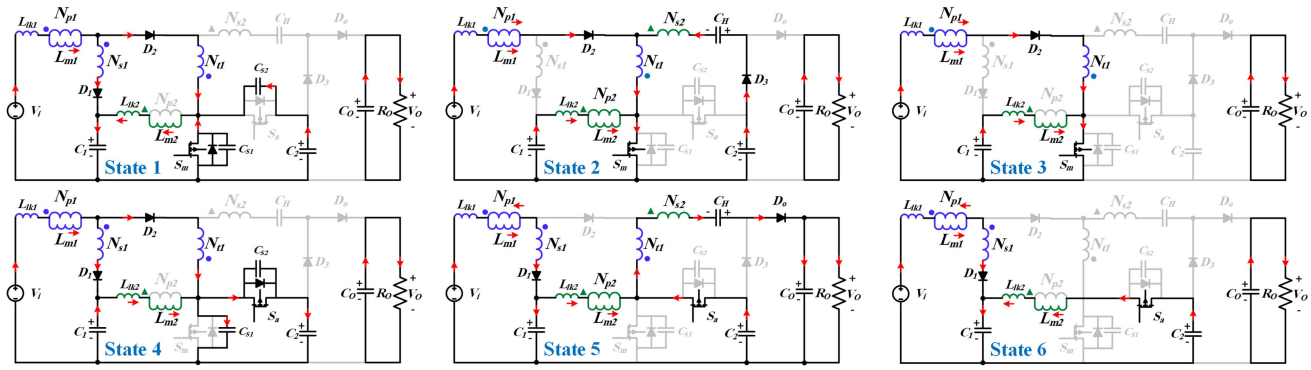

Fig. 2. Equivalent circuit of each state.

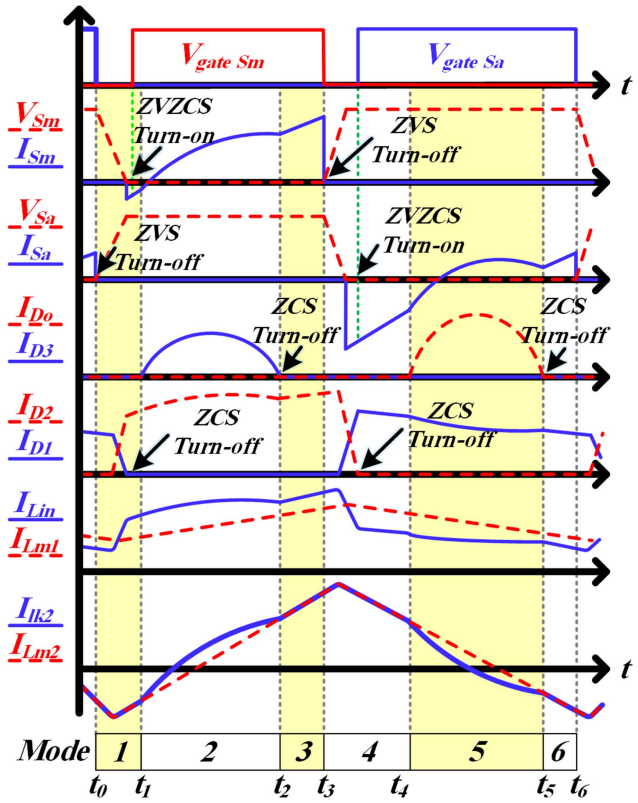

Fig. 3. Theoretical key waveforms of the proposed converter.

OFF under ZCS condition

$$f_{r2} = \frac{1}{2\pi\sqrt{L_{\text{eq2}}C_{\text{eq2}}}} \tag{4}$$

where

$$L_{\text{eq2}} = {n_2}^2 L_{\text{lk1}} + \left(m\left(1+n_1\right)\right)^2 L_{lk2} \tag{5}$$

$$\frac{1}{C_{\text{eq2}}} = \frac{\left(m\left(1+n_1\right)-n_2\right)\left(m-n_2\right)}{C_1} + \frac{\left(1+n_1\right)\left(m+1\right)^2}{C_2} + \frac{\left(1+n_1\right)}{C_H}. \tag{6}$$

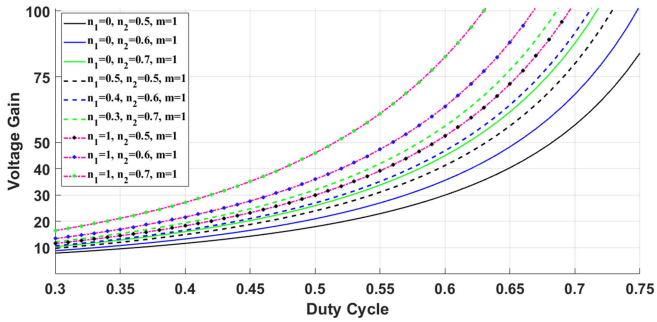

Fig. 4. Voltage gain of proposed converter with different n_1 and n_2.

State VI [t_5, t_6]: When D_o is reverse biased and its voltage clamps to V_o-V_{Cc}. Moreover, I_{Lm2} passes through S_a and the current of this switch becomes linear. This state continues until S_a is turned OFF.

III. Steady-State Analysis

A. Capacitors Voltage and VG

Applying the volt-second principle on L_{m1} and L_{m2}, without considering of the leakage inductances effect, and Kirchhoff's voltage law (KVL) in both modes II and IV, the voltages of C_1, C_2, and C_H are obtained as follows:

$$V_{C1} = \frac{V_{\text{in}}\left(1+Dn_1-n_2\left(1-D\right)\right)}{\left(1-D\right)\left(1-n_2\right)} \tag{7}$$

$$V_{C2} = \frac{V_{\text{in}}\left(1+Dn_1-n_2\left(1-D\right)\right)}{\left(1-D\right)^2\left(1-n_2\right)} \tag{8}$$

$$V_{CH} = m{*}V_{C1} + V_{C2} + \frac{n_2 V_{\text{in}}}{\left(1-n_2\right)}. \tag{9}$$

The output voltage is attained using KVL in mode *V* which leads to the proposed converter ideal VG as follows:

$$\frac{V_o}{V_{\text{in}}} = \frac{\left(2+m\right)\left(1+Dn_1\right)-n_2\left(1-D\right)\left(1+m\right)}{\left(1-D\right)^2\left(1-n_2\right)}. \tag{10}$$

Fig. 4 shows the VG of the proposed converter for different values of *n1* and *n2*. The n_1 and n_2 windings not only solve

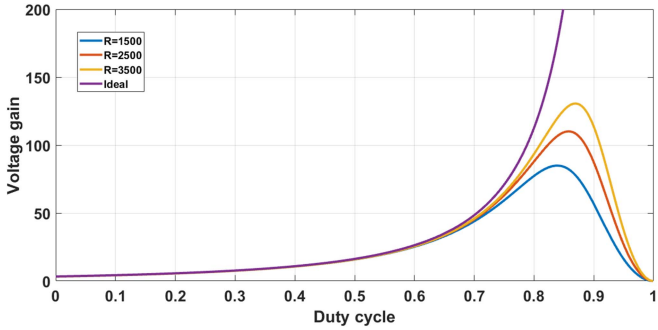

Fig. 5. Voltage gain versus duty cycle at various loads.

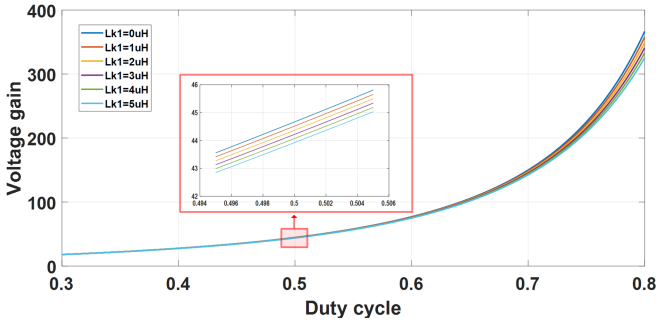

Fig. 6. Voltage gain with leakage inductance effect.

the reverse recovery issue of input diodes in the quadratic boost topology but also significantly increase the VG of the presented converter. These improvements result in a higher VG while using a smaller turns ratio, leading to reduced conductive losses.

In (6), the effect of leakage inductances is neglected. By defining $D_{\text{eff}}T_s$ as the charging time of the L_{m1} and L_{m2}, the VG equation is obtained by considering L_{lk1} as

$$D_{\text{eff}} = D - D_{\text{loss}} \tag{11}$$

$$D_{\text{loss}}\, T_s = \frac{L_{\text{lk1}} I_i}{V_{\text{in}} + \frac{(1-n_2)V_{C1}}{n_1+n_2}} \tag{12}$$

$$\frac{V_o}{V_{\text{in}}} = \frac{(2+m)\,(1+D_{\text{eff}}n_1) - n_2\,(1-D_{\text{eff}})\,(1+m)}{(1-D)\,(1-D_{\text{eff}})\,(1-n_2)}\,. \tag{13}$$

Figs. 5 and 6 show the effect of elements resistance at various loads and leakage inductances on the VG, respectively.

B. Voltage and Current Stresses of Elements

Upon turning OFF one switch, the snubber capacitors complete their charge and discharge cycle, the voltage across the other switch is clamped to the V_{C2}. By using KVL in states II and V, the voltage stress of switches is calculated as

$$V_{S1} = V_{S2} = \frac{V_O\,(1+Dn_1-n_2\,(1-D))}{(2+m)\,(1+Dn_1)-n_2\,(1-D)\,(1+m)}. \tag{14}$$

Applying KVL in states *II* and *IV*, the highest reverse peak voltage of diodes is obtained as follows:

$$V_{D1} = \frac{(1+n_1D)\,(1-D)}{(1+Dn_1)\,(2+m)-n_2\,(1-D)\,(1+m)}\,V_O \tag{15}$$

$$V_{D2} = \frac{D\,(1+n_1-2n_2\,(1-D))}{(1+Dn_1)\,(2+m)-n_2\,(1-D)\,(1+m)}\,V_O \tag{16}$$

$$V_{D3} = V_{Do} = \frac{(1+m)\,(1+Dn_1)-n_2m\,(1-D)}{(1+Dn_1)\,(2+m)-n_2\,(1-D)\,(1+m)}\,V_o. \tag{17}$$

The average of I_{Lm1} is the input current I_i. Based on the general inductor relation $\Delta I = V_L \Delta t/L$, the minimum and maximum of I_{Lm1} is expressed as follows:

$$I_{Lm1}^{\min,\max} = I_i \;\pm \frac{V_i D}{2\,(1-n_2)\,L_{m1} f_s}. \tag{18}$$

By using the amp-sec law for C_1, the average current of I_{Lm2} is obtained as follows:

$$I_{Lm2} = I_i\;(1-D)\,. \tag{19}$$

The minimum and maximum current of I_{Lm2} are expressed as follows:

$$I_{Lm2}^{\min,\max} = I_i\;(1-D) \pm \frac{V_i\,(1+Dn_1-n_2\,(1-D))\,D}{2\,(1-D)\,(1-n_2)\,L_{m2} f_s}. \tag{20}$$

By using KCL in states III and VII, the maximum current of the active switches and the diodes D_1 and D_2 are written as follows:

$$I_{Sm}^{\max} = \frac{I_{Lm1}^{\max}}{1-n_2} + I_{Lm2}^{\max} \tag{21}$$

$$I_{Sa}^{\max} = -I_{Lm2}^{\min} \tag{22}$$

$$I_{D1}^{\max} = I_{D2}^{\max} = \frac{I_{Lm1}^{\max}}{1-n_2}\,. \tag{23}$$

The peak current of D_3 and D_o can be obtained according to amp-sec law for C_H and C_O capacitors, which are given by following:

$$I_{Dm}^{\max} = \frac{\omega_1 I_o}{2f_s}, I_{Do}^{\max} = \frac{\omega_2 I_o}{2f_s}. \tag{24), (25}$$

C. Passive Elements Design

To certify continuous conduction mode (CCM) for I_i while considering for 0.2 current ripple, based on the L_{m1} average current given in the previous section, L_{m1} can define as follows:

$$L_{m1} \geq \frac{V_i D}{0.2\,(1-n_2)\,I_i f_s}. \tag{26}$$

When the main switch S_m is turned OFF, C_1 and C_2 are charged by I_iD and $I_i(1\text{-}D)$- $\frac{\omega_2 I_o}{4f_s}$, respectively. Moreover, C_o is discharged by I_o. These capacitors equations can be written

as follows:

$$C_1 \geq \frac{I_i D\,(1-D)}{f_s \Delta V_{C1}}, C_2 \geq \frac{\left[I_i\,(1-D) - \frac{\omega_2 I_o}{4 f_s}\right]}{f_s \Delta V_{C2}}, C_o x \geq \frac{I_o D}{f_s \Delta V_{Co}}. \tag{27}$$

In addition, to verify ZCS turn OFF condition for D_3 and D_O, the state II and the state V must be lower than the duration that S_m and S_a are ON, respectively. As a result, by using (1) and (4), value of the capacitor C_H is achieved as follows:

$$\pi \sqrt{L_{\text{eq1}} \frac{C_H}{(1-n_2)^2}} \leq D T_s \tag{28}$$

$$\pi \sqrt{L_{\text{eq2}} \frac{C_H}{(1+n_2)}} \leq (1-D)\,T_s. \tag{29}$$

D. Soft Switching Condition

As described in state *I*, I_{Lm2} charges and discharges C_{s1} and C_{s2}, respectively. As a result, I_{Lm2} at t_0 should be negative to discharges C_{s1} and charges C_{s2}. Also, to create ZVZCS condition for S_m, I_{Sm} at t_1 should be lower than zero. Moreover, the inductive energy available must be enough to completely discharge and charge the snubber capacitors. So, soft switching conditions are

$$I_{Lm2}\,(t_0) < 0 \tag{30}$$

$$I_{Sm}\,(t_1) < 0 \tag{31}$$

$$\frac{1}{2} L_{m2} I_{Lm2}^2\,(t_0) \geq \frac{1}{2}\,(C_{s1}+C_{s2})\,{V_{C2}}^2. \tag{32}$$

By using the (8), (18), and (20), the above equations are rewritten as follows:

$$L_{m2} < \frac{V_i\,(1+Dn_1-n_2\,(1-D))\,D}{2 I_i (1-D)^2\,(1-n_2)\,f_s} \tag{33}$$

$$L_{m2} < \frac{V_i\,(1+Dn_1-n_2\,(1-D))\,D}{2 f_s \left[I_i (1-D)^2\,(1-n_2) + I_i\,(1-D) - \frac{V_i D(1-D)}{2(1-n_2) L_{m1}}\right]} \tag{34}$$

$$L_{m2} < \frac{(1-D)^2 D^2}{4 {f_s}^2\,(C_{s1}+C_{s2})}. \tag{35}$$

The gate pulses of two switches are complementary. Also, the time delay between two pulses occurs during the main switch OFF time, while the delay between pulses are very small. This delay is considered because of charging and discharging of the two switches snubber capacitors. These time intervals are illustrated in Fig. 7 and can be calculated as follows:

$$t_m > \frac{(V_{C2})\,(C_{S1}+C_{S2})}{-i_{lm2,\min}} \tag{36}$$

$$t_a > \frac{(V_{C2})\,(C_{S1}+C_{S2})}{i_{\text{lk1,max}} + i_{lm2,\max}}. \tag{37}$$

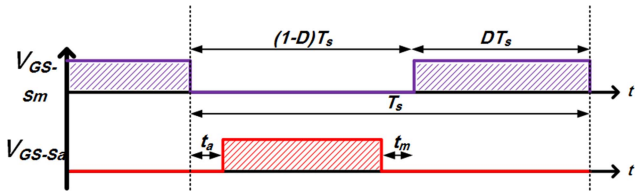

Fig. 7. Gate signal waveforms of the main and the auxiliary switches.

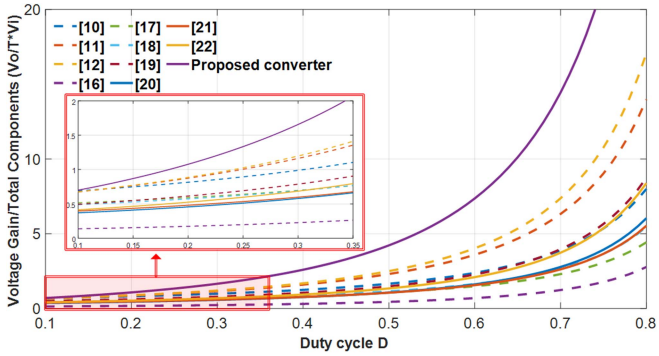

Fig. 8. Comparison of voltage gain per number of used components versus duty cycles.

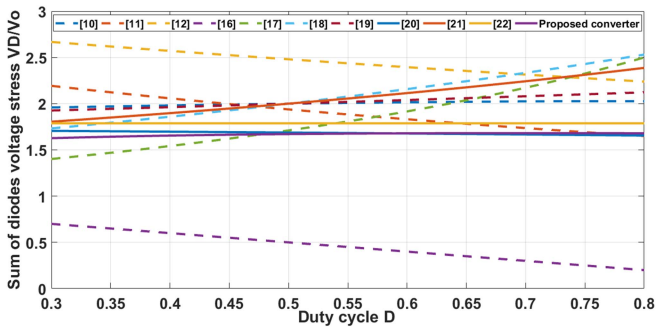

Fig. 9. Comparison of normalized sum of diodes voltage stresses versus duty cycles.

IV. Comparison With Similar Topologies

To display the advantages of the proposed converter, a comparative discussion is done between the introduced high step-up dc–dc converter and other similar topologies in [10], [11], [12] and [16], [17], [18], [19], [20], [21], [22]. Table I, Figs. 8, and 9 show the results obtained from the comparison. As observed, the presented converter has minimum number of components, common ground, adequately ultrahigh VG as well as low voltage stress across diodes. Also, soft-switching operation at ZVS is provided with very low elements and capacitive turn ON losses are eliminated. high step-up dc–dc converter and other similar topologies in [10], [11], [12] and [16], [17], [18], [19], [20], [21], [22]. Table I, Figs. 8, and 9 show the results obtained from the comparison. As observed, the presented converter has minimum number of components, common ground, adequately ultrahigh VG as well as low voltage stress across switches

TABLE I
PERFORMANCE COMPARISON AMONG HIGH GAIN CONVERTERS

Ref.*	To*/S*/D*/ BC*/I*/CI*/T*	Voltage Gain (VG)	Normalized Sum of Diodes Voltage Stresses	Normalized Max. Switch Voltage Stress	**VG** ∑n=2, D=0.5	SSC* For switches	RR* of Diodes H*	RR* of Diodes L*
Rezaie and Abbasi [10]	Ca*/2/5/ 5/1/1/14	$\frac{3+2n-D(3+n-D)}{(1-D)^2}$	$\frac{5-3D+2n(2-D)}{3+2n-D(3+n-D)}$	$\frac{1}{3+2n-D(3+n-D)}$	19	--------	3	2
Abbasi et al. [11]	Ca*/2/5/ 5/1/1/14	$\frac{2+2n+nD(1-D)}{(1-D)^2}$	$\frac{(4n+2-2nD)+(n+1)(2-D)}{2+2n+nD(1-D)}$	$\frac{1}{2+2n+nD(1-D)}$	26	--------	2	3
Abbasi et al. [12]	Ca*/2/5/ 5/0/2/14	$\frac{nm+n(1+D)+2m+D+2}{(1-D)^2}$	$\frac{2(n+2)(m+2)-D}{nm+n(1+D)+2m+D+2}$	$\frac{1+(1+n)D}{nm+n(1+D)+2m+D+2}$	32	--------	2	3
Korada and Ayyanar [16]	Q*/3/1/ 2/3/0/9	$\frac{1}{(1-D)^2}$	$(1-D)$	1	4	ZVS	0	1
Alavi et al. [17]	Ca*/3/4/ 5/0/2/14	$\frac{(2-D)(n+m(1-D))+(1-D)}{(1-D)^2}$	$\frac{7-D}{(2-D)(n+m(1-D))+(1-D)}$	$\frac{1}{(2-D)(n+m(1-D))+(1-D)}$	11	ZVS	0	4
Mohseni et al. [18]	Ca*/4/4/ 5/0/2/15	$\frac{n(2-D)+(1-D)^2}{(1-D)^2}$	$\frac{3n+(1-D)}{n(2-D)+(1-D)^2}$	$\frac{1}{n(2-D)+(1-D)^2}$	14	ZVS	0	4
Rao and De [19]	Q*/2/5/ 5/0/2/14	$\frac{2+n+m(2-D)}{(1-D)^2}$	$\frac{4+2n+3m}{2+n+m(2-D)}$	$\frac{1}{2+n+m(2-D)}$	18	ZVS	2	3
Mohseni et al. [20]	Q*/2/4/ 4/0/2/12	$\frac{1+n+m(1-D)}{(1-D)^2}$	$\frac{1+2n+2m(1-D)}{1+n+m(1-D)}$	$\frac{1}{1+n+m(1-D)}$	10	ZVS	2	2
Izadi et al. [21]	Q*/2/4/ 5/1/1/14	$\frac{2+n+m-(1+m)D}{(1-D)^2}$	$\frac{3+2n+m}{2+n+m-(1+m)D}$	$\frac{1}{2+n+m-(1+m)D}$	12	ZVS	3	1
Hajilou and Farzane hfard [22]	Q*/2/4/ 5/1/2/14	$\frac{2+n+m}{(1-D)^2}$	$\frac{3+2(n+m)}{2+n+m}$	$\frac{1}{2+n+m}$	16	ZVS	2	2
Prop.*	Q*/2/4/ 4/0/2/12	Equation (10)	X*	Equation (14)	40	ZVS	0	4

Ref*: Reference, To*: Topology, S*: Switches, D*: Diodes, BC*: Bulky Capacitors, I*: Inductors, CI*: Coupled Inductors, T*: Total, SSC*: Soft Switching Condition, RR*: Reverse Recovery, H*: High, L*: Low, Ca*: Cascade, Q*: Quadratic, , Prop*: Proposed Converter $X^*=\frac{1+Dn_1(2-D)+2(1+m)(1+Dn_1-n_2(1-D))}{(1+Dn_1)(2+m)-n_2(1-D)(1+m)}V_o$.

and diodes. Also, soft-switching operation at ZVS is provided with very low elements and capacitive turn ON losses are eliminated.

high step-up dc–dc converter and other similar topologies in [10], [11], [12] and [16], [17], [18], [19], [20], [21], [22]. Table I, Figs. 8, and 9 show the results obtained from the comparison. As observed, the presented converter has minimum number of components, common ground, adequately ultrahigh VG as well as low voltage stress across switches and diodes. Also, soft-switching operation at ZVS is provided with very low elements as well as capacitive turn ON losses are eliminated. Because the snubber capacitors values are very small, these capacitors are omitted from the capacitors count. In addition, due to switch OFF diodes in ZCS, reverse recovery problem of all diodes is solved. According to Table I and Fig. 8, the VG, and the VG per elements of the proposed converter are significantly higher than other similar converters. Also, the maximum switch voltage stress of the presented converter is lower than converters in [16], [17] and [20], [21]. Although, switches of the converters in [10], [11], [12], [18], [19], and [22] experience lower voltage stress than the proposed converter, the converters in [10], [11], and [12] suffer from hard switching, and converters in [18] and [22] have four switches and three magnetic cores, respectively. Moreover, these converters have higher number of elements compared to the proposed converter. Also, the main drawback of the converter in [19] is the lack of CG between the input and the output. Moreover, the sum of diodes voltage stresses in the proposed converter is lower than all of converters except the converter in [17], which has three switches and this issue increases size, cost and control complexity. In addition, the reverse recovery problem has eliminated in the proposed converter but the converters in [10], [11], [12] and [19], [20], [21], [22] suffer from high reverse recovery. It should be noted the converter in [16], [17], and [18] experience LRR, but these converters have three switches, three switches and, four switches, which is downside.

Comparing the power density according to the prototype converters in the references cannot be performed since the sizes of the laboratory prototype converters are not reported in many cases. For an approximate and fair comparison, it is assumed that all converters operate at the same conditions in terms of input and output voltages, output power and switching frequency while the same technology elements are employed. Thus, the number of elements can approximate their total volume. Magnetic cores and active switches are usually the bulkiest elements in converters and their effect on power density is greater than diodes and capacitors thus, the larger number of magnetic cores and active switches leads to high converter volume. In this comparison, the proposed converter, and the converters in [20], and Izadi et al. [21] have relatively high power density. However, the converters in [20] and [21] suffer from high reverse recovery losses, especially for input diodes of the quadratic structure. Also, the converter in [21] does not possess common ground between the input and the output. Increasing the switching frequency decreases the size of passive components. However, increasing the switching frequency also leads to higher switching and capacitive turn-ON losses. Therefore, by providing soft switching operation in the proposed converter, it is possible to increase the switching frequency while minimizing the losses and the size of passive elements. In this comparison, converters in [16], [17], [18], and [22] achieve low power density, because of the number of magnetic cores and active switches. Additionally, in this comparison, the converters in [10], [11], [12], and [19] are considered as medium power density, as they have fourteen elements and two magnetic cores. It should be mentioned that hard switching operation is the main disadvantage of the converters in [10], [11], and [12]. This comparison indicates that the proposed converter

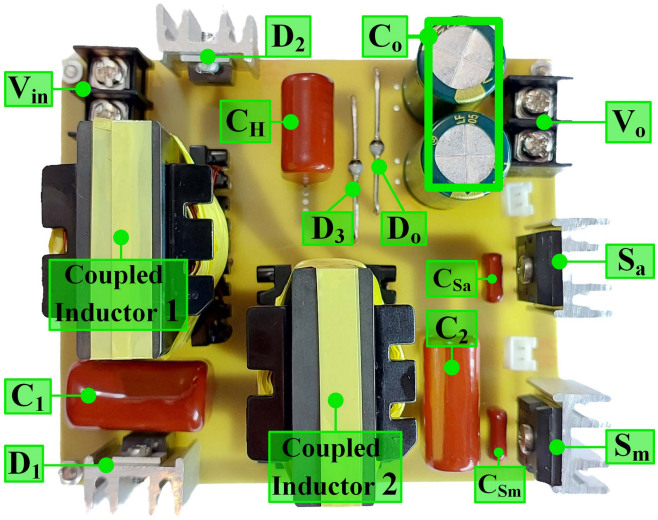

Fig. 10. Implemented proposed converter prototype.

TABLE II
COMPONENTS OF THE IMPLEMENTED PROTOTYPE

PARAMETERS	VALUES
Input and output voltages: V_{in} , V_o	48 V and 650 V
Output power and duty cycle: P_o , D	200 W , 0.46
Switching frequency: f_s	100 kHz
Switches: S_m and S_a	IXTH96N25T, $R_{DS,ON}$ = 29 mΩ
Diodes: D_1, D_2	V30202C
Diodes: D_o, D_3	BYW-52
First CI: $N_{p1}/N_{s1}/N_{t1}$, L_{m1} , L_{lk1}	40/8/10, 200 μH, 5.5 μH
Second CI: N_{p2}/N_{s2}, L_{m2}, L_{lk2}	48/48, 31μH, 1 μH
Capacitors: C_1, C_2 and C_H	Polyester 10 μF,4.7 μF *and 1.5* μF
Capacitor: C_o	2 series capacitors 100 μF
Snubber capacitor: C_{S1} and C_{S2}	2.2 nF

has a high power density due to soft switching and low number of elements especially magnetic cores and active switches.

V. EXPERIMENTAL VERIFICATION

To confirm the theoretical analysis in previous sections, a laboratory prototype is realized and tested as displayed in Fig. 10 based on the specifications presented in Table II. Since the converter input is directly connected to a battery, its voltage remains relatively stable. Therefore, experimental waveforms are recorded at the nominal voltages of lead-acid and $LiFePO_4$ batteries. The proposed converter with its high VG can easily compensate for the input voltage variations. Fig. 11 displays the experimental results of the presented converter. The voltage and current of S_m as well as S_a at full load are demonstrated in Fig. 11(a) and (b). As observed, ZVZCS condition at turning ON and ZVS at turning OFF for S_m and S_a are attained. In addition, the voltage along S_m and S_a is clamped at around 210 V. Fig. 11(c) and (d) shows the current and voltage of S_m and S_a under light load (40 W). As shown, soft switching conditions are provided. The voltage and current waveforms of all diodes are displayed in Fig. 11(e)–(h). As shown, ZCS at turning OFF is established for all diodes, which terminates reverse recovery issue for all diodes. In addition, the voltage of D_1, D_2, D_3, and D_o are clamped at about 120 V, and 440 V. Fig. 11(i) displays

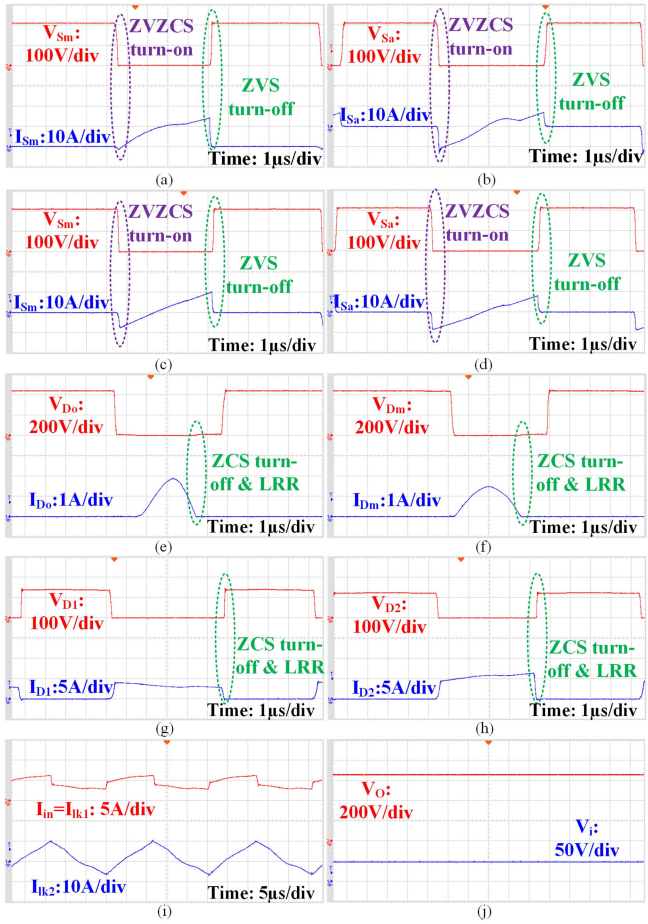

Fig. 11. Experimental waveforms of (a) S_m at full load. (b) S_a at full load. (c) S_m at light load. (d) S_a at light load. (e) D_o. (f) D_3. (g) D_1. (h) D_o. (i) I_{lk1} (I_{in}) and I_{lk2}, (j) input and output voltages.

TABLE III
EXPERIMENTAL PEAK VALUES OF SWITCHES AND DIODES

Condition	Parameter	Experimental values
P_O=200 W V_{in}=48 V V_O= 650 V D=0.46	Max. voltage stress on the main switch S_m (V_{Sm})	212 V
	Peak current of the main switch S_m (I_{Sm})	14 A
	Max. voltage stress on the auxiliary switch S_a (V_{Sa})	212 V
	Peak current of the auxiliary switch S_a (I_{Sa})	7 A
	Max. voltage stress on the diode D_1 (V_{D1})	138 V
	Peak current of the diode D_1 (I_{D1})	4 A
	Max. voltage stress on the diode D_2 (V_{D2})	120 V
	Peak current of the diode D_2 (I_{D2})	6.5 A
	Max. voltage stress on the diode D_3 (V_{D3})	440 V
	Peak current of the diode D_3 (I_{D3})	1.5 A
	Max. voltage stress on the diode D_O (V_{Do})	440 V
	Peak current of the diode D_O (I_{Do})	1.9 A

I_{lk1} and I_{lk2}. As observed, I_{lk2} becomes negative, because of the preparing ZVZCS conditions for the switches. Also, converter operates at CCM condition. Fig. 11(j) shows the input and output voltage of the presented converter. The switches and diodes peak voltage and current values are given in Table III. For the dynamic response, a basic control circuit is utilized to ensure stable

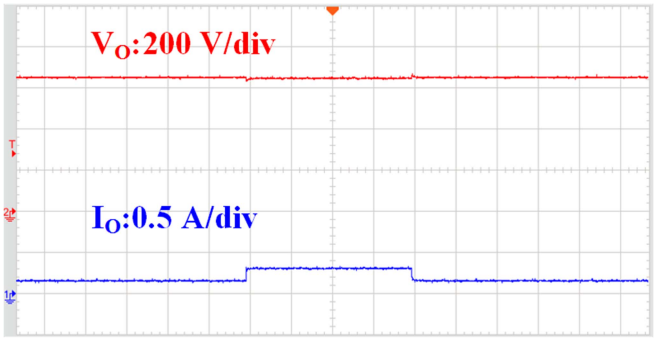

Fig. 12. Experimental dynamic response waveforms to abrupt-load variations.

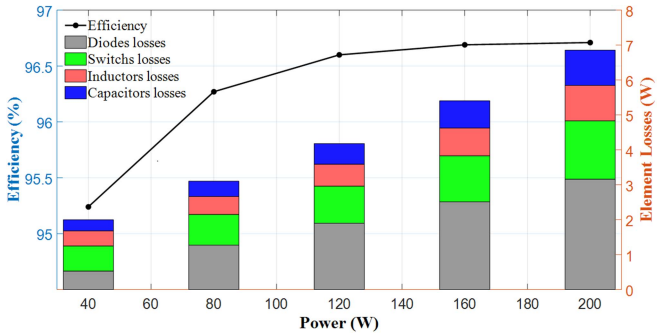

Fig. 13. Efficiency and loss breakdown in various output powers.

TABLE IV
LOSS ANALYSIS OF PROPOSED CONVERTER

Type	Equation
Core losses	$K(f)^{\alpha}(\frac{\Delta B_{CI1,2}}{2})^{\beta}$
Windings conduction losses	$R_{lk} i_{lk}^{RMS^2}$
Switches conduction losses	$R_{DS,ON} i_S^{RMS^2}$
Diodes conduction losses	$V_{FD} I_{D,avg}$
Capacitors losses	$R_C (i_C^{RMS})^2$

operation. The dynamic response of the proposed converter is achieved by abruptly-changing the load from full load to half load and vice versa as shown in Fig. 12.

The proposed converter efficiency diagram and loss breakdown at various output powers are displayed in Fig. 13. Loss breakdown is performed based on the theoretical given in Table IV. Fully soft switching operation, elimination of switching and capacitive turn ON loss and mitigation of diodes reverse recovery are led to about 96.71% converter efficiency at full load condition. To compare efficiencies, the converters in [11], [12], and [19] are designed (inductors and capacitors are designed and the semiconductor voltage stresses are calculated) and then, the converters are simulated under the same operating conditions as the proposed converter at $V_i = 48$ V, $V_O = 650$ V, $f_{\text{sw}} = 100$ kHz, and P_O (full load output power) $= 200$ W. The results of the efficiency comparison for the proposed converter and most relevant counterparts in Table I are given in Table V. The converter in [19] like the proposed converter benefits from soft switching operation and switching and capacitive turn-ON losses are approximately zero, but the switching losses exist for the converters in [11] and [12]. As observed, the converters in [11] and [12] have lower efficiencies relative to the proposed converter and [19], mainly caused by the switching losses. Although the converter in [19] has an acceptable efficiency, this converter suffers from the lack of common ground the input and the output. Notably, the proposed converter is superior to [19] in terms of VG per total elements. It should be noted that in this comparison, the reverse recovery losses are not considered, since the precise theoretical reverse recovery loss calculation is complex. Moreover, in the implemented prototype, the reverse recovery losses are not significant, but this can considerably affect efficiency at high powers and switching frequencies in converters which have not solved this problem.

TABLE V
CONVERTERS EFFICIENCIES AT VARIOUS OUTPUT POWERS

Converter	Abbasi et al. [11]	Abbasi et al. [12]	Rao and De [19]	Proposed	Output power
Efficiency	95.32	94.75	96.5	96.71	200W
	95.68	94.95	96.24	96.69	160W
	95.6	95.09	96.07	96.6	120W
	95.46	94.72	95.5	96.27	80W
	95	93.24	94.5	95.24	40W

VI. CONCLUSION

In this article, a novel ultrahigh step-up quadratic-based converter is presented, which benefits from interesting features such as high VG, low voltage stress on all semiconductor elements, fully soft switching operation, elimination of capacitive turn ON loss, eliminated reverse recovery for all diodes, and recovering the leakage inductance energy as well as sending it to the output. In the presented converter, VG can be controlled with more flexibility. Also, the converter topology is simple, which consists of a low number of components compared to similar high step-up converters with the same characteristics. Also, the converter has common ground, which expands its applicability. The performed comparison verifies the presented converter benefit to other quadratic structures. Finally, the experimental results from a laboratory prototype of 48–650 V/200 W and the efficiency analysis verify the converter features.

REFERENCES

[1] M. Packnezhad and H. Farzanehfard, "Fully soft switched bidirectional buck–Boost converter with improved voltage conversion ratio and single auxiliary switch," *IEEE Trans. Ind. Electron.*, vol. 71, no. 1, pp. 380–387, Jan. 2024.

[2] R. Rafiee and Y. Batmani, "On the design of novel single-switch low loss boost converters with high step-up voltages," *IEEE Trans. Power Electron.*, vol. 40, no. 6, pp. 8206–8215, Jun. 2025.

[3] M. Hajilou and H. Farzanehfard, "Single switch ultra-high step-up quadratic converter with low input current ripple," *IEEE Trans. Ind. Electron.*, vol. 72, no. 1, pp. 411–418, Jan. 2025.

[4] R. Heidari, M. A. Ghanbari, E. Adib, and M. Rivera, "Coupled inductor-based soft-switched boost-Ćuk converter for microinverter applications," *IEEE Trans. Power Electron.*, vol. 40, no. 7, pp. 9543–9555, Jul. 2025.

[5] X. Ding, K. Jiang, C. Zhang, P. Zhang, and Z. Yan, "A single-switch ZVS high step-up DC-DC converter with stacked voltage multiplier cell," *IEEE Trans. Power Electron.*, vol. 40, no. 6, pp. 8292–8304, Jun. 2025.

[6] M. Rezayat, B. M. Dehkordi, and M. Niroomand, "Quadratic high step-up DC-DC converter with passive clamp circuit," in *Proc. 11th Iranian Conf. Renewable Energy Distrib. Gener.*, 2024, vol. 11, pp. 1–8.
[7] P. Talebi, M. Packnezhad, and H. Farzanehfard, "Single-switch high step-up Y-source-boost converter for renewable energy applications," *IEEE Trans. Ind. Electron.*, vol. 71, no. 11, pp. 14067–14074, Nov. 2024.
[8] Y. Hu, W. Zhan, S. Li, and M. A. Azam, "A single-switch trans-inverse high step-up semiquadratic DC–DC converter based on three-winding coupled inductor," *IEEE Trans. Power Electron.*, vol. 39, no. 7, pp. 8786–8799, Jul. 2024.
[9] H. M. Jazi, R. R. Khorasani, E. Adib, P. Zanchetta, G. Velasco-Quesada, and H. Martínez-García, "A high-efficient single-switch, soft-switching high step-up DC–DC converter with a simple structure and continuous input current for renewable energy integration," *IEEE Trans. Power Electron.*, vol. 39, no. 8, pp. 9814–9826, Aug. 2024.
[10] M. Rezaie and V. Abbasi, "Ultrahigh step-up DC–DC converter composed of two stages boost converter, coupled inductor, and multiplier cell," *IEEE Trans. Ind. Electron.*, vol. 69, no. 6, pp. 5867–5878, Jun. 2022.
[11] V. Abbasi, N. Talebi, M. Rezaie, A. Arzani, and F. Y. Moghadam, "Ultrahigh step-up DC–DC converter based on two boosting stages with low voltage stress on its switches," *IEEE Trans. Ind. Electron.*, vol. 70, no. 12, pp. 12387–12398, Dec. 2023.
[12] V. Abbasi, S. Rostami, S. Hemmati, and S. Ahmadian, "Ultrahigh step-up quadratic boost converter using coupled inductors with low voltage stress on the switches," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 7733–7743, Dec. 2022.
[13] X. Zhang et al., "Novel high step-up soft-switching DC–DC converter based on switched capacitor and coupled inductor," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9471–9481, Sep. 2020.
[14] P. Talebi, M. Packnezhad, and H. Farzanehfard, "Fully soft-switched ultra-high step-up converter with very low switch voltage stress," *IEEE Trans. Power Electron.*, vol. 38, no. 3, pp. 3523–3530, Mar. 2023.
[15] R. B. Kalahasthi, M. R. Ramteke, H. M. Suryawanshi, and A. K. Singh, "A ZVS-based non-isolated high step-up DC–DC converter with low voltage stress for renewable applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 3, pp. 2793–2804, Jun. 2023.
[16] N. Korada and R. Ayyanar, "Novel quadratic high gain boost converter with adaptive soft-switching scheme and reduced conduction loss," *IEEE Trans. Ind. Application*, vol. 58, no. 6, pp. 7421–7431, Nov./Dec. 2022.
[17] P. Alavi, P. Mohseni, E. Babaei, and V. Marzang, "An ultra-high step-up DC–DC converter with extendable voltage gain and soft-switching capability," *IEEE Trans. Ind. Electron.*, vol. 67, no. 11, pp. 9238–9250, Nov. 2020.
[18] P. Mohseni, S. H. Hosseini, and M. Maalandish, "A new soft switching DC–DC converter with high voltage gain capability," *IEEE Trans. Ind. Electron.*, vol. 67, no. 9, pp. 7386–7398, Sep. 2020.
[19] B. T. Rao and D. De, "A coupled inductor-based high-gain ZVS DC–DC converter with reduced voltage stresses," *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 15956–15967, Dec. 2023.
[20] P. Mohseni, S. Mohammadsalehian, M. R. Islam, K. M. Muttaqi, D. Sutanto, and P. Alavi, "Ultrahigh voltage gain DC–DC boost converter with ZVS switching realization and coupled inductor extendable voltage multiplier cell techniques," *IEEE Trans. Ind. Electron.*, vol. 69, no. 1, pp. 323–335, Jan. 2022.
[21] M. Izadi, A. Mosallanejad, and A. L. Eshkevari, "An improved coupled inductor-based quadratic step-up DC–DC converter with a high step-up factor and reduced voltage overshoot on the power switch," *IET Power Electron.*, vol. 17, no. 9, pp. 986–1004, Aug. 2023.
[22] M. Hajilou and H. Farzanehfard, "Nonisolated ultra-high step-up quadratic converter with ZVS operation and low switch voltage stress," *IEEE Trans. Power Electron.*, vol. 39, no. 5, pp. 5982–5991, May 2024.
[23] M. Karimi, H. Farzanehfard, M. Packnezhad, and M. Esteki, "Bidirectional ZVS buck–Boost converter with single auxiliary switch and continuous current at low voltage source," *IEEE Trans. Ind. Electron.*, vol. 69, no. 3, pp. 2480–2487, Mar. 2022.

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