Extended Dual Side Asymmetric Phase Shift Modulation and Smooth Mode Transition Method for Dual Active Bridge Converter

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***Abstract*—Dual active bridge (DAB) converters are widely used in dc microgrids due to their advantages of electrical isolation, wide voltage range operation, and bidirectional power flow. When the voltage conversion ratio is mismatched, the conventional symmetric phase shift modulation method has a narrow zero voltage switching (ZVS) range, low light-load efficiency, and uncontrollable inductor current oscillations caused by abrupt changes in variables during mode switching. In order to solve the above-mentioned problems, an extended dual side asymmetric phase shift modulation (EDAPSM) and smooth mode transition method is proposed in this article. Analytical solutions over the entire power range are derived based on the proposed approximation method. The inherent cause of variable discontinuities during mode transitions is identified, and a novel approach to achieve smooth mode switching is presented, thereby improving the efficiency of the DAB converter over a wide voltage range, particularly under light-load conditions. A 1-kW DAB prototype is constructed, and the modulation method can achieve a maximal efficiency of 98.03%. The experimental results verify the correctness and effectiveness of the method proposed in this article.**

***Index Terms*—Dual active bridge (DAB) converters, efficiency, extended dual side asymmetric phase shift modulation (EDAPSM), smooth mode transition, zero voltage switching (ZVS).**

I. Introduction

DC microgrids consist of distributed power sources, loads, energy storage units, and grid-connected units. They have received increasing attention in recent years due to their advantages in high energy efficiency, high supply reliability, and high power quality. [1], [2]. The isolated dc–dc converter serves as a key power interface between the distributed energy storage units and the dc bus. When distributed power sources generate electricity, the energy must be delivered to the load side through the isolated dc–dc converter or stored in the distributed energy storage units via the same converter. Therefore, the isolated dc–dc converter plays a vital role in the operation of dc microgrids. The dual active bridge (DAB) converter, as a typical topology of isolated dc–dc converters, is widely used in dc microgrids due to its many advantages, such as electrical isolation, zero voltage switching (ZVS), bidirectional power flow, wide voltage ratio range, high efficiency, and high power density [3], [4]. With the increasing voltage and current levels at the input and output terminals, the series-parallel configuration of the DAB converter has become one of the most popular isolated dc–dc converter topologies in dc microgrids due to the limited voltage-withstanding capability of power switches [5]. Single-phase shift (SPS) modulation is a conventional control strategy for DAB converters. It has been widely adopted due to the simplicity of its control structure, which involves only a single control variable. However, under mismatched voltage conversion ratios, the SPS method suffers from several drawbacks, including a limited ZVS range, high circulating power, and consequently reduced overall efficiency. To address these issues, existing improved modulation techniques can be broadly categorized into the following two directions.

One approach to improvement is from the hardware perspective. Mahdavifard et al. [6] and Mahdavifard and Khajehoddin [7] introduced dc-blocking capacitors on both the primary and secondary sides of the transformer. By employing the proposed asymmetric duty cycle modulation (ADM) strategy, the ZVS range of the power switches can be effectively extended, the root-mean-square (rms) value of the inductor current can be reduced, and thus the overall efficiency of the DAB converter is improved. However, the addition of dc-blocking capacitors leads to a reduction in power density and an increase in component losses. Furthermore, due to the complexity of the modulation method, an analytical solution was derived using nonlinear polynomial fitting, which significantly compromises the practical effectiveness and ease of implementation of the modulation strategy. Xu et al. [8] added a dc-blocking capacitor in series on the secondary side of the transformer. By employing the proposed hybrid extended phase shift (EPS) modulation strategy, dual voltage matching points are achieved through the switching between full-bridge and half-bridge operation modes. However, this method is constrained by the selection of the dc-blocking capacitor's capacitance, which results in increased volume and cost of the DAB converter.

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On the other hand, improvements have been made from a software perspective, where the DAB converter's topology remains unchanged. The main categories are symmetric phase shift modulation and ADM (the inductor satisfies the voltage-second balance principle within a single switching cycle). Symmetric phase shift modulation mainly includes dual phase shift modulation [9], EPS modulation [10], and triple phase shift (TPS) modulation [11], [12], [13], [14]. Gong et al. [11] employed a time-domain analysis method and applied a multiobjective optimization strategy to reduce the current stress in the DAB converter, widen the ZVS range, and introduce the concept of unified ZVS current. This approach ensures that all switching devices can dynamically adjust in real-time to achieve ZVS over a wide voltage operating range. During the start-up process of the DAB converter, a variable frequency combined with EPS modulation was utilized to enable ultrafast and wide safety margin start-up [15]. However, during the mode transition, there are still two power switches that fail to achieve ZVS. Li et al. [14] employed a time-domain analysis method to optimize the peak value of the inductor current. By establishing a detailed model of the commutation process of the power switches, they determined the ZVS current requirement necessary for achieving ZVS during the switching transitions. The dead time was then dynamically adjusted based on the voltage conversion ratio and output power, ensuring ZVS for the power switches and consequently enhancing the overall efficiency of the DAB converter. However, the problem of smooth mode transition was not addressed in the switching process between operation modes. Currently, based on symmetrical modulation, a significant amount of research has started to explore asymmetrical modulation by adjusting the duty cycles of the power switches, to further improve the efficiency of the DAB converter [16], [17], [18], [19], [20], [21], [22], [23].

Mou et al. [16] proposed an ADM strategy, which is built upon the SPS modulation. By adjusting the 50% duty cycles of the power switches in both the primary full-bridge and secondary full-bridge, the ADM method achieves a wider ZVS range while maintaining a lower rms value of inductor current, thereby enhancing the efficiency of the DAB converter under light-load conditions. However, this study only considered the buck operation mode, and the boost mode was not discussed in detail. Building upon previous research, Mou et al. [17] proposed a five-degree-of-freedom (5-DOF) optimized modulation strategy. Based on ADM modulation, the strategy introduces inner phase-shift angles for both the primary and secondary full-bridge circuits, effectively reducing the rms value of the inductor current in the DAB converter. However, the use of a 5-DOF modulation scheme results in increased computational complexity and poor real-time performance, which can negatively impact the overall performance of the DAB converter. Similarly, Li et al. [18] adopted a 5-DOF optimization strategy, in which the rms value of the inductor current was minimized using frequency-domain analysis methods. However, after Fourier decomposition, the optimization objective becomes a sum of infinite terms, which reduces the accuracy of the optimization model. Moreover, the optimization variables can only be implemented in the digital signal processor via lookup table methods, significantly degrading the effectiveness and efficiency of the optimization. Tian et al. [22] proposed the dual-side asymmetrical duty modulation (DADM) method, which models the commutation process taking into account the nonideal factors such as junction capacitance and dead time, and effectively extends the ZVS range. However, the proposed method is not applicable to cover the whole power range. Therefore, in [23], the operating mode is expanded to effectively widen the power range. However, the mode transition process is not discussed, and due to the complexity of the method, analytical solutions for the optimization variables are not available, necessitating the use of lookup table methods instead, which reduces the effectiveness of the modulation strategy.

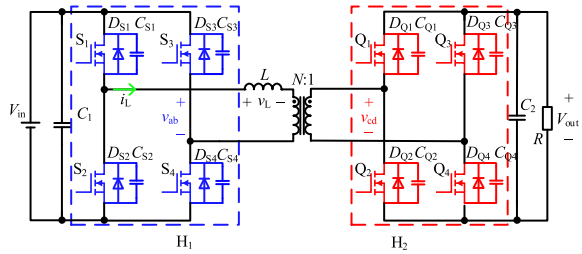

Fig. 1. DAB converter topology.

To address the aforementioned issues, this article proposes an extended dual side asymmetric phase shift modulation (EDAPSM) method, enabling the DAB converter to operate efficiently over a wide voltage range. The commutation process of the power switches is thoroughly discussed, yielding the correct ZVS current value. Based on the proposed modulation strategy, a multiobjective efficiency optimization approach is formulated, aiming to minimize the peak-to-peak inductor current, expand the ZVS range of the power switches, and reduce the circulating power. An analytical solution over the entire power range is obtained using the proposed approximation method, which also reduces the rms value of the inductor current. The underlying cause of variable discontinuity during mode transitions is revealed, and a smooth mode transition method is proposed, effectively improving the converter efficiency across a wide voltage range, particularly under light-load conditions.

The rest of this article is organized as follows. Section II introduces the EDAPSM, provides the steady-state waveforms in different modes, and mathematically models and analyzes the soft switching characteristics of the commutation process to determine the precise current values to achieve the ZVS. The approximate solution of the multiobjective efficiency optimization method is given in Section III, and the mode smooth transition method is proposed to solve the problem of abrupt change of optimization variables. The effectiveness of the proposed method is verified in Section IV. Section V concludes this article.

II. Proposed EDAPSM Method

The topology of the DAB converter is shown in Fig. 1. The primary full-bridge H_1 consists of power switches S_1–S_4, and the secondary full-bridge H_2 consists of power switches

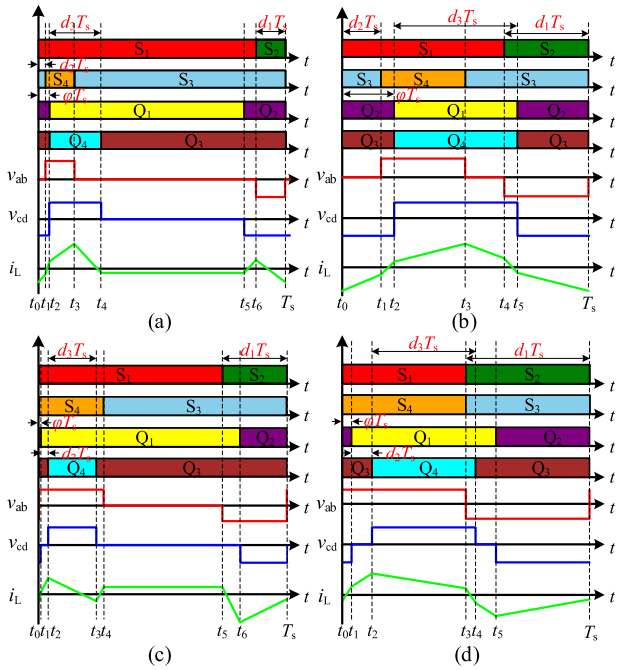

Fig. 2. EDAPSM mode classification. (a) EDAPSM mode A. (b) EDAPSM mode B. (c). EDAPSM mode C. (d) EDAPSM mode D.

Q_1–Q_4. The D_{Si} and D_{Qi} represent the antiparallel diodes of the power switches S_i and Q_i, respectively, and the C_{Si} and C_{Qi} represent the junction capacitances of the power switches S_i and Q_i, respectively. The C_1 and C_2 represent the filter capacitances of the input side and the output side, respectively. The turn ratio of the high-frequency transformer is N. The v_{ab} and v_{cd} represent the midpoint voltages of the primary and secondary full-bridges, respectively. The DAB converter changes the waveforms of the inductor currents i_L by modifying the corresponding positions of the primary and secondary full-bridge midpoint voltage v_{ab} and v_{cd}, and thus performs the control of the energy.

A. Operating Mode Classification

The voltage conversion ratio is defined as $M = N\,V_{\mathrm{out}} / V_{\mathrm{in}}$. To enable the DAB converter to operate stably over a wide voltage range under the proposed EDAPSM, Fig. 2 shows the steady-state waveforms of the proposed modulation method. The conducting time of the primary side power switches S_2 and S_4 is defined as d_1T_s (the value range of d_1 is [0, 0.5]), and the conducting time of the secondary side power switches Q_2 and Q_4 is defined as d_3T_s (the value range of d_3 is [0, 0.5]). Under the buck operation condition, the shift ratio between the primary side power switches S_1 and S_4 is defined as d_2T_s (the value range of d_2 is [0, 1]), as shown in Fig. 2(a) and (b). Under the boost operation condition, the shift ratio between the secondary power switches Q_1 and Q_4 is defined as d_2T_s, as shown in Fig. 2(c) and (d). The shift ratio between the primary side power switch S_1 and the secondary side power switch Q_1 is defined as φT_s (the value range of φ is [0, 0.5]).

TABLE I
UNIFIED TRANSMISSION POWER AND PEAK-TO-PEAK INDUCTOR CURRENT

Mode	Unified transmission power P_n	Unified peak-to-peak inductor current $I_{p\_p\_n}$
EDAPSM mode B	$0.5M\pi(4\varphi-1-4(d_1^2+d_2^2+d_1(d_2-1)-2d_2\varphi+2\varphi^2))$	$2\pi(2M\varphi-d_2M+d_1(1-M))$
EDAPSM mode C	$2M\pi(d_3(d_2+2\varphi)-\varphi^2)$	$2\pi(d_2+2\varphi+d_3(M-1))$
EDAPSM mode D	$0.5M\pi(4\varphi-1-4d_3^2-4d_3(d_2-1)-4d_2(d_2-1)-8\varphi d_2-8\varphi^2)$	$2\pi(d_2+2\varphi+d_3(M-1))$

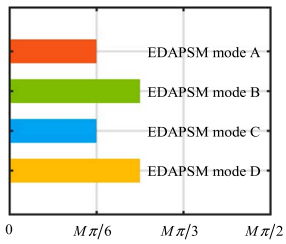

Fig. 3. Maximum unified transmission power graph.

B. Steady-State Characteristics

With the time-domain analysis, the DAB converter transmission power P and the rms value of the inductor current I_{rms} can be obtained by exploiting the inductor current segment linearization and the principle of volt-second equilibrium of the inductor. Considering EDAPSM mode A as an example for derivation, the transmission power is unified for ease of expression as $P_{\mathrm{b}} = v^2{}_{\mathrm{ab}}\,T_{\mathrm{s}} / 2\pi L$, $I_b = v_{ab}T_s / 2\pi L$. The unified obtained transmission power P_n of the DAB converter in steady-state is shown in the following equation:

$$P_n = \frac{1}{T_sP_b}\int_0^{T_s} v_{ab}(t)i_L(t)\mathrm{d}t = 2M\pi(2\varphi(d_1+d_2)-d_2(d_1+d_2)-\varphi^2). \quad (1)$$

In EDAPSM mode A, the unified peak-to-peak inductor current $I_{p\_p\_n}$ is shown in the following equation:

$$I_{p\_p\_n} = I_{p\_p}/\,I_b = 2\pi(2M\varphi - d_2M + d_1(1-M)). \quad (2)$$

Table I offers the unified transmission power and inductor current peak-to-peak formulas for the remaining mode, and the maximum unified transmission power that can be achieved by the four modes under the constraints is shown in Fig. 3.

C. Mathematical Model of the Commutation Process

Taking the commutation process of power switches S_3 and $Q_1(Q_4)$ in EDAPSM mode A as an example, the mathematical model incorporates the junction capacitance C_{Si} (C_{Qi}) of the power switches and the dead time effect. According to the datasheet of the power switch C3M0045065K [24], the relationship between its junction capacitance C_{oss} and the drain-source voltage V_{DS} is illustrated in Fig. 4. It can be observed that C_{oss} varies nonlinearly with the change in V_{DS}. To address the issue of nonlinear variation, the linear charge-equivalent method [25]

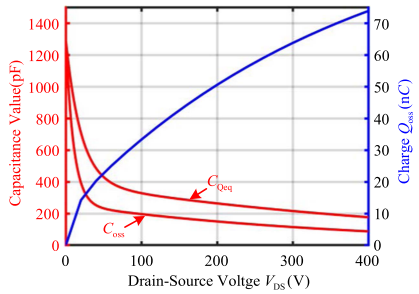

Fig. 4. Relationship between the nonlinear junction capacitance C_{oss}, linear charge-equivalent capacitance C_{Qeq}, charge Q_{oss}, and the drain-source voltage V_{DS} of the power switch.

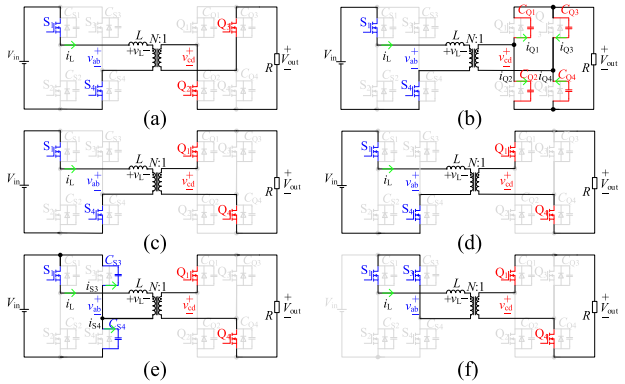

Fig. 5. Equivalent circuits of the power switches S_3, Q_1 (Q_4) during the commutation process. (a) Q_1 (Q_4) before commutation. (b) Q_1 (Q_4) during the dead time. (c) Q_1 (Q_4) after commutation. (d) S_3 before commutation. (e) S_3 during the dead time. (f) S_3 after commutation.

is employed, in which a linear charge-equivalent capacitance is used to approximately replace the nonlinear junction capacitance of the power switches. Using (3), the charge Q_{oss} stored in the junction capacitance C_{oss} of the power switch can be determined

$$Q_{\mathrm{oss}} = \int_0^{V_{\mathrm{DS}}} C_{\mathrm{oss}}(v)\mathrm{d}v. \tag{3}$$

The linear charge-equivalent capacitance can be derived using (4), and it exhibits the same charge as the nonlinear junction capacitance at a given drain-source voltage

$$C_{\mathrm{Qeq}} = \frac{Q_{\mathrm{oss}}}{V_{\mathrm{DS}}} = 901.66e^{-0.05V_{\mathrm{DS}}} + 394.4e^{-0.002V_{\mathrm{DS}}}. \tag{4}$$

Fig. 4 also presents the variation of the charge Q_{oss} and the linear charge-equivalent capacitance C_{Qeq} with the drain-source voltage V_{DS} of the power switch. It can be observed that, within different voltage ranges, the linear charge-equivalent capacitance is consistently higher than the nonlinear junction capacitance, maintaining a margin of approximately twice the value. Therefore, it is more favorable for the power switches to achieve ZVS. Fig. 5 illustrates the equivalent circuit diagrams of power switches S_3 and Q_1 (Q_4) before commutation, during the dead time, and after commutation, respectively.

The equivalent circuit diagrams of the power switches Q_1 (Q_4) during the commutation process are shown in Fig. 5(a)–(c).

Then, the commutation point is expressed as

$$\begin{cases} i_{\mathrm{L}}(t_2') = I_{\mathrm{ZVSQ1Q4}} \\ u_{\mathrm{C_{Q1}}}(t_2') = u_{\mathrm{C_{Q4}}}(t_2') = V_{\mathrm{out}} \\ u_{\mathrm{C_{Q2}}}(t_2') = u_{\mathrm{C_{Q3}}}(t_2') = 0 \end{cases}. \tag{5}$$

In (5), t_2' denotes the start time of commutation for power switches Q_1 (Q_4), while I_{ZVSQ1Q4} represents the current required for the power switches to achieve ZVS.

During the dead time, the junction capacitors C_{Q1} and C_{Q4} of power switches Q_1 and Q_4 begin discharging, while the junction capacitors C_{Q2} and C_{Q3} of power switches Q_2 and Q_3 start charging. When the primary inductor is referred to the secondary side via the transformer, the junction capacitors and inductor form a resonant network. Based on Kirchhoff's Voltage Law equation and the initial conditions given by (5), the inductor current $i_{\mathrm{L}}(t)$ and the voltage $u_{\mathrm{CQ1}}(t)$ across capacitor C_{Q1} during the dead time can be expressed as

$$\begin{cases} i_{\mathrm{L}}(t) = I_{\mathrm{ZVSQ1Q4}}\cos\frac{N}{\sqrt{LC_{oss}}}t + \frac{V_{\mathrm{in}}+NV_{\mathrm{out}}}{L\omega_1}\sin\frac{N}{\sqrt{LC_{\mathrm{oss}}}}t \\ u_{\mathrm{CQ1}}(t) = -\frac{V_{\mathrm{in}}}{2N} + \frac{V_{\mathrm{out}}}{2} - \frac{L\omega_1 I_{\mathrm{ZVSQ1Q4}}}{2N^2}\sin\frac{N}{\sqrt{LC_{\mathrm{oss}}}}t \\ \qquad + \frac{V_{\mathrm{in}}+NV_{\mathrm{out}}}{2N}\cos\frac{N}{\sqrt{LC_{\mathrm{oss}}}}t \end{cases}. \tag{6}$$

The equivalent circuits of power switch S_3 before and after commutation are shown in Fig. 5(d)–(f). By applying the same analytical approach, the inductor current $i_L(t)$ and the voltage $u_{\mathrm{CS3}}(t)$ across junction capacitor C_{S3} during the dead time can be derived as follows:

$$\begin{cases} i_{\mathrm{L}}(t) = I_{\mathrm{ZVSS3}}\cos\frac{1}{\sqrt{2LC_{\mathrm{oss}}}}t + \frac{V_{\mathrm{in}}-NV_{\mathrm{out}}}{L\omega}\sin\frac{1}{\sqrt{2LC_{\mathrm{oss}}}}t \\ u_{\mathrm{CS3}}(t) = NV_{\mathrm{out}} - L\omega_2 I_{\mathrm{ZVSS3}}\sin\frac{1}{\sqrt{2LC_{\mathrm{oss}}}}t \\ \qquad + (V_{\mathrm{in}} - NV_{\mathrm{out}})\cos\frac{1}{\sqrt{2LC_{\mathrm{oss}}}}t \end{cases}. \tag{7}$$

D. ZVS Current Value

In [17], the direction of the current required to achieve ZVS for power switches is specified. When the direction of the ZVS current satisfies the requirement, the magnitude of different ZVS currents significantly impacts whether power switches can achieve ZVS. Taking the commutation process of power switch S_3 as an example, under ideal conditions, ZVS can be achieved efficiently by turning on S_3 when the voltage across capacitor C_{S3} is zero. The minimum current required for power switch $\mathrm{S_3}$ to achieve ZVS is defined as I_{minZVS}. The time t_3' denotes the start of commutation for power switch $\mathrm{S_3}$, while t_3 represents the end of commutation. During the commutation process, the voltage across junction capacitor C_{S4} of power switch $\mathrm{S_4}$ rises from 0 V to V_{in} through charging, while the voltage across junction capacitor C_{S3} of power switch S_3 decreases from V_{in} to 0 V through discharging. During this time interval, the stored energy in junction capacitor C_{S3} is fully transferred to C_{S4}, i.e., $E_{\mathrm{t3'\_CS3}} = E_{\mathrm{t3\_CS4}}$. According to the law of energy conservation, the energies before and after commutation can be expressed as

$$E_{t_3'} = E_{t_3}. \tag{8}$$

At time t_3', the stored energy in inductor L and junction capacitor C_{S3} can be expressed as

$$E_{t3'\_iL} + E_{t3'\_CS3} = \frac{1}{2} L I_{minZVS}{}^2 + E_{t3'\_CS3}. \quad (9)$$

At time t_3, the stored energy in junction capacitor C_{S4} and the energy E_c consumed during the dead time by input voltage V_{in} and output voltage V_{out} can be expressed as

$$E_{t3\_CS4} + E_c = E_{t3\_CS4} + \int_{t_3'}^{t_3} (NV_{out} i_L(t) - i_{CS4}(t) V_{in}) dt$$
$$= E_{t3\_CS4} + V_{in}^2 C_{oss}(2M-1). \quad (10)$$

Substituting (9) and (10) into (8) yields the minimum current value I_{minZVS} required for power switch S_3 to achieve ZVS, as shown in the following equation:

$$I_{minZVS} = \sqrt{2V_{in}^2 C_{oss}(2M-1)/L}. \quad (11)$$

To achieve ZVS for power switch S_3 at the commutation instant, the ZVS current value must exceed the minimum required current I_{minZVS}. Therefore, the ZVS current value at the commutation instant can be expressed as

$$I_{ZVSS3} \geq \begin{cases} \sqrt{2V_{in}^2 C_{oss}(2M-1)/L} & 0.5 < M < 1 \\ 0 & 0 < M < 0.5 \end{cases}. \quad (12)$$

Applying the same analytical method, the required minimum current for achieving ZVS in all power switches across the remaining modes can be derived.

III. Multiobjective Efficiency Optimization Method Based on Minimum Peak-to-Peak Current

A. Optimization Method

Taking EDAPSM Mode A as an example, Fig. 2(a) shows the steady-state waveforms of EDAPSM mode A. The midpoint voltage is zero at times t_4 and t_5, during which no power is transferred. To reduce the rms value of the inductor current and ensure ZVS for the power switches, the current values at t_4 and t_5 are set to the minimum current required to achieve ZVS. Since the minimum current values required to achieve ZVS at t_4 and t_5 are different, and higher current values are more conducive to ZVS realization, the current values at t_4 and t_5 are set to I_{ZVSQ2}. At t_0, the inductor current reaches its maximum value, and at t_3, it reaches its minimum value. Therefore, the power switches S_1 and S_3 can easily achieve ZVS.

As shown in Fig. 3, when the power level increases, the EDAPSM mode A transitions to EDAPSM mode B. At the boundary between the two modes, power switches S_2, Q_2, and Q_3 conduct simultaneously. However, the direction of the inductor current of power switch S_2 to achieve ZVS conflicts with the direction of the inductor current of power switches Q_2 and Q_3 to achieve ZVS. Therefore, two scenarios arise at the mode transition point:

1) S_2 achieves ZVS, while Q_2 and Q_3 undergo hard-switching.
2) Q_2 and Q_3 achieve ZVS, while S_2 undergoes hard-switching.

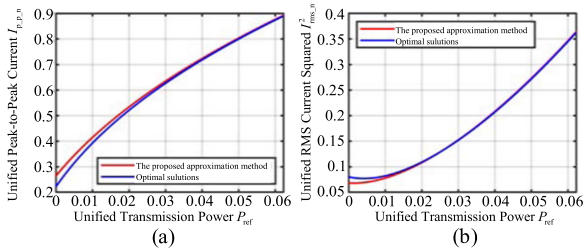

Fig. 6. Comparison between the approximate method and the optimal solution. (a) Unified peak-to-peak current $I_{p\_p\_n}$. (b) Unified rms current squared $I2$ rms_n.

This article selects the second scenario as the optimization method to reduce the number of hard-switching events and minimize switching losses. The optimization standard for this method can be formulated as follows:

$$\begin{cases} \min I_{p\_p\_n} = 2\pi(2M\varphi - d_2 M + d_1(1-M)) \\ \text{s.t. } P_{ref} - P_{n\_modeA} = 0 \\ 2\pi(d_1(d_1+d_2) - d_3^2 M) - I_{ZVSQ2} = 0 \\ 2\pi(M(d_2+d_3-d_3^2-\varphi) + d_1 d_2 + d_1^2 - d_1) - I_{ZVSS4} \leq 0 \\ I_{ZVSQ1Q4} - 2\pi(M(d_3-d_3^2)+\varphi-d_2+d_1 d_2+d_1^2-d_1) \leq 0 \end{cases}. \quad (13)$$

B. Approximate Solution and Smooth Mode Transition Method

In the low power range of EDAPSM mode A, analytical solutions cannot be obtained due to the equality constraint of the power transfer equation, the equality constraints of power switches Q_2 and Q_3, and the inequality constraint for achieving ZVS on power switch S_4. To ensure the real-time capability of the EDAPSM method, this article proposes an approximate solution approach by adding an inequality constraint for achieving ZVS on power switch Q_1 (Q_4) to the original set of constraints. The approximately analytical solution and optimized solution are substituted into the expressions for the peak-to-peak inductor current and the squared rms value of the inductor current for quantification. The quantification results are shown in Fig. 6. Fig. 6(a) shows a comparison of the peak-to-peak inductor current between the two solutions. It can be observed that in the low power range, the optimized solution yields a lower peak-to-peak current than the approximately analytical solution. In Fig. 6(b), a comparison of the squared rms value of the inductor current is presented. In this case, the approximately analytical solution results in a smaller value than the optimal solution. This is because, in the multiobjective optimization process, the complex rms of the inductor current is replaced by the simpler peak-to-peak inductor current as the optimization objective to obtain an analytical solution over the entire power range. Consequently, the optimized solution ensures the minimum peak-to-peak current. Conduction losses are related to the rms value of the inductor current. The proposed approximate solution method not only enables obtaining an analytical solution over the entire power range, but also helps reduce conduction losses in the low power range. Therefore, it is reasonable to derive the analytical expressions for the optimization variables

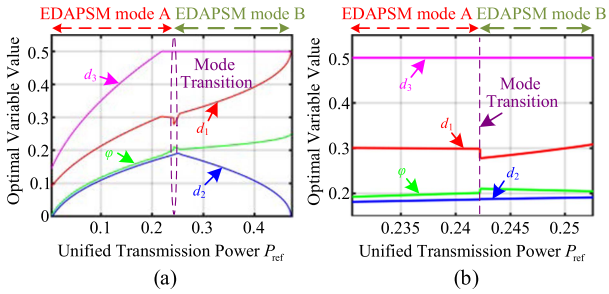

Fig. 7. Relationship between optimized variables and unified transmitted power at $M = 0.6$. (a) Global view. (b) Local magnification.

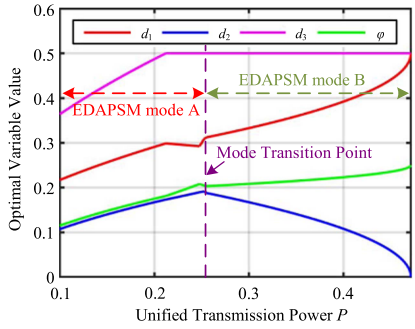

Fig. 8. Relationship between optimized variables and unified transmitted power at $M = 0.6$ after applying the proposed smooth mode transition method.

across the entire power range using the proposed approximation and the KKT conditions.

The changes in the optimization variables obtained are shown in Fig. 7(a). Fig. 7(b) presents a magnified view of the mode transition transient, clearly illustrating abrupt variable changes during the transition between operating modes. This phenomenon arises due to the discrepancy in the minimum current requirements for ZVS of power switches Q_2 and Q_3 in the two distinct modes. In practical applications, as power increases, it leads to uncontrollable inductor current oscillations and system instability. In EDAPSM mode A, the minimum current value required for ZVS of power switches Q_2 and Q_3 are given by the following equation:

$$I_{\mathrm{ZVSQ2Q3\_A}} = -2\pi M\sqrt{2LC_{\mathrm{oss}}}\Big/ NT. \tag{14}$$

In EDAPSM mode B, the minimum current value required for ZVS of power switches Q_2 and Q_3 is defined by the following equation:

$$I_{\mathrm{ZVSQ2Q3\_B}} = -4\pi\sqrt{MLC_{\mathrm{oss}}}\Big/ T. \tag{15}$$

Based on the analysis of (14) and (15), it can be observed that the absolute value of $I_{\mathrm{ZVSQ2Q3\_B}}$ is consistently larger than that of $I_{\mathrm{ZVSQ2Q3\_A}}$. As demonstrated in Section II-C, a higher ZVS current value at the commutation instant facilitates the ZVS of the power switches. To ensure smooth mode transition and the realization of ZVS for power switches Q_2 and Q_3 in EDAPSM mode A, the ZVS current value at the commutation instant for these power switches is set as defined in the following equation:

$$I_{\mathrm{ZVSQ2}} = I_{\mathrm{ZVSQ2Q3\_B}} = I_{\mathrm{ZVSQ2Q3\_A}} = -4\pi\sqrt{MLC_{\mathrm{oss}}}\Big/ T. \tag{16}$$

Fig. 8 presents the variation of optimization variables after applying the proposed smooth mode transition method. It can be observed that all optimization variables vary continuously, and no abrupt changes occur at the mode transition points, which validates the effectiveness of the proposed approach.

C. Comparison of ZVS Range

As demonstrated in the preceding analysis, at the mode transition points, power switches Q_2 and Q_3 are selected

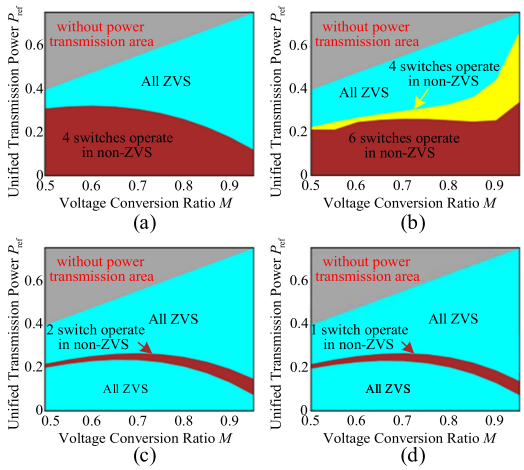

Fig. 9. ZVS ranges of different modulation methods. (a) SPS. (b) CSO-TPS. (c) Near-ALL-ZVS. (d) EDAPSM.

to achieve ZVS, whereas power switch S_2 undergoes hard-switching. Fig. 9 presents the ZVS range comparison among the proposed EDAPSM method and the SPS [1], CSO-TPS [13], and near-ALL-ZVS [14] modulation methods. Under SPS modulation at light-load conditions, only the power switches in the primary full-bridge can achieve ZVS, while those in the secondary full-bridge undergo hard-switching. For the CSO-TPS modulation method, only two power switches can achieve ZVS under light-load conditions, and as the power increases, only the power switches in the primary full-bridge maintain ZVS capability. The near-ALL-ZVS modulation method considers the conditions for power switches to achieve ZVS. However, at the mode transition point, two power switches still undergo hard-switching. In contrast, the proposed EDAPSM method ensures that only one switch operates in hard-switching near the mode transition points, thereby reducing switching losses.

IV. Experimental Results and Analysis

A. Experimental Platform

A 1-kW DAB prototype was constructed as shown in Fig. 10, with parameters detailed in Table II. The processor employed is the TMS320F28337. To validate the effectiveness of the

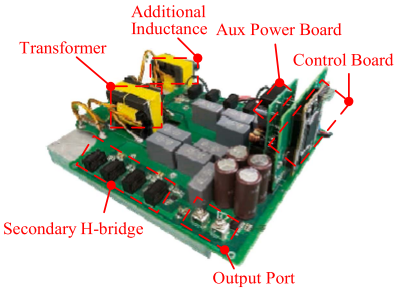

Fig. 10. Experimental prototype.

TABLE II
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Parameters	Value
Transformer turns ratio (N)	1 : 1
Inductor (L)	29.56 μH
Switching frequency (f)	100 kHz
Rated power (P)	1 kW
Power switches (S_1-S_4, Q_1-Q_4)	C3M0045065K

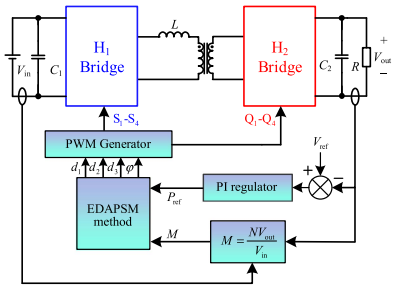

Fig. 11. Control block diagram.

proposed EDAPSM method, a PI controller was adopted as the closed-loop regulator. The control block diagram is shown in Fig. 11. Input voltage V_{in} and output voltage V_{out} are sampled to calculate the voltage conversion ratio M. The PI controller outputs the unified transmission power P_{ref}. Based on M and P_{ref}, the EDAPSM method is used to compute the optimized variable d_1, d_2, d_3, and φ.

B. Steady-State Characteristics

To validate the stable operation of the proposed EDAPSM method across a wide voltage range, experimental results are provided under both buck and boost conditions. In the buck conditions with a voltage conversion ratio $M = 0.6$, steady-state waveforms of EDAPSM mode A and EDAPSM mode B, along with pre- and postmode-transition steady-state waveforms, are demonstrated. Similarly, under boost conditions with $M = 1.25$, corresponding waveforms for EDAPSM mode C and EDAPSM mode D, as well as pre- and postmode-transition steady-state waveforms, are presented.

At $M = 0.6$, the experimental setup configures an input voltage of 200 V, and the output voltage is regulated to 120 V via closed

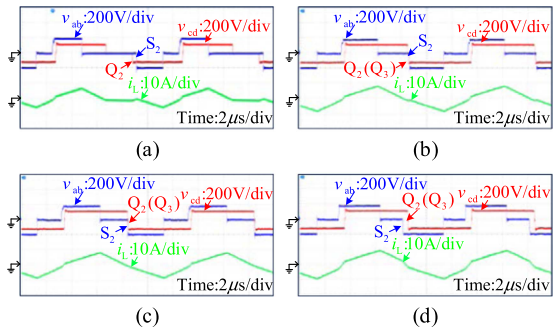

Fig. 12. Steady-state waveforms at $M = 0.6$. (a) EDAPSM mode A. (b) EDAPSM mode A before mode transition. (c) EDAPSM mode B after mode transition. (d) EDAPSM mode B.

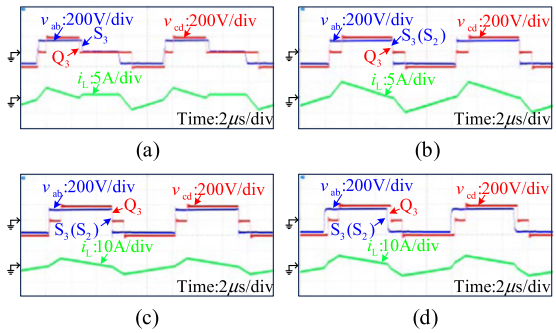

Fig. 13. Steady-state waveforms at $M = 1.25$. (a) EDAPSM mode C. (b) EDAPSM mode C before mode transition. (c) EDAPSM mode D after mode transition. (d) EDAPSM mode D.

loop control, as shown in Fig. 12. Fig. 12(a) shows the steady-state waveforms of EDAPSM mode A, where the drive pulse of power switch S_2 lags behind that of power switch Q_2. In Fig. 12(b), the steady-state waveforms of EDAPSM mode A before mode transition are presented. At this moment, the drive pulses of Q_2 and Q_3 coincide. Since the converter remains in EDAPSM mode A, the drive pulse of S_2 still lags behind those of $Q_2(Q_3)$. Fig. 12(c) illustrates the steady-state waveforms of EDAPSM mode B after mode transition. Here, the drive pulse of S_2 leads ahead of those of $Q_2(Q_3)$. Fig. 12(d) depicts the steady-state waveforms in EDAPSM mode B, where the drive pulse of S_2 occurs before those of $Q_2(Q_3)$.

At $M = 1.25$, the experimental setup employs an input voltage of 160 V, with the output voltage regulated to 200 V via closed-loop control. The results are shown in Fig. 13. Fig. 13(a) illustrates the steady-state waveforms of EDAPSM mode C, where the drive pulse of power switch S_3 lags behind that of Q_3. Fig. 13(b) depicts the steady-state waveforms of EDAPSM mode C before mode transition. Here, the drive pulses of S_2 and S_3 coincide, and consequently, the drive pulses of $S_2(S_3)$ still lag behind those of $Q_2(Q_3)$ since the converter remains in EDAPSM mode C. Fig. 13(c) shows the steady-state waveforms of EDAPSM mode D after the mode transition. In this scenario, the drive gates of $S_2(S_3)$ lead those of Q_3. Fig. 13(d) presents the steady-state waveforms in EDAPSM mode D, where the drive pulses of S_2 (S_3) occur before those of Q_3.

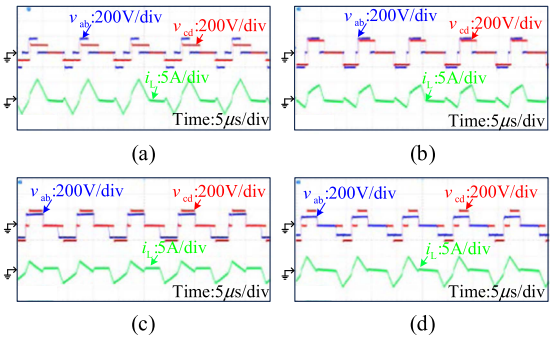

Fig. 14. Steady-state waveforms under different voltage conversion ratios at $P = 200$ W. (a) $M = 0.5$. (b) $M = 0.8$. (c) $M = 1.25$. (d) $M = 1.6$.

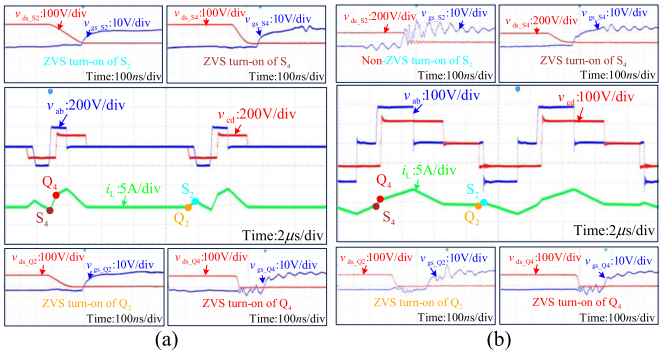

Fig. 15. ZVS characteristics at $M = 0.6$. (a) $P = 50$ W. (b) $P = 500$ W.

Fig. 14 presents the steady-state waveforms under different voltage conversion ratios using the proposed EDAPSM method at a transmission power of $P = 200$ W. As demonstrated in the results, the proposed EDAPSM method is effective across various voltage conversion ratios, enabling the converter to achieve stable operation over a wide voltage range.

C. ZVS Characteristics

Fig. 15 illustrates the ZVS characteristics of the power switches at transmission power levels of $P = 50$ W and $P = 500$ W under $M = 0.6$. At $P = 50$ W, the ZVS conditions shown in Fig. 15(a) indicate that all switches achieve ZVS during the low power stage of EDAPSM mode A. When the transmission power increases to $P = 500$ W, as depicted in Fig. 15(b), the converter remains in EDAPSM mode A before mode transition. As the power increases, a mode transition inevitably occurs, which results in the hard-switching of power switch S_2. However, the remaining switches still maintain ZVS operation. The above analysis validates the effectiveness of the proposed optimization method.

D. Dynamic Characteristics

To ensure that the EDAPSM method can be implemented within a single interrupt cycle and meet the required computational time, the interrupt frequency is set to 0.2 times the switching frequency in experiments. Since the reduction in interrupt frequency leads to a worsened dynamic response, the integral gain coefficient K_i is increased by a factor of five to approximately compensate for this degradation. To validate the dynamic response capability of the proposed modulation method, the dynamic performance is tested using the load step and output voltage step changes in experiments. Fig. 16(a) shows the dynamic waveforms when the input voltage V_{in} is 200 V, and the voltage conversion ratio M is 0.6, corresponding to a power transition from 400 W to 800 W with a response time of 27 ms. Fig. 16(b) presents the dynamic waveforms for a power transition from 800 W to 400 W, with a response time of 29.5 ms. Fig. 16(c) shows the dynamic waveforms when the input voltage V_{in} is 200 V and the load resistance is 30 Ω, for a step change in output voltage V_{out} from 120 V to 160 V, with a response time of 26 ms. Fig. 16(d) presents the dynamic waveforms for the output voltage V_{out} step change from 160 V to 120 V, with a response time of 30 ms. From the above results, it can be concluded that the proposed modulation method, despite its computational burden, still exhibits favorable dynamic characteristics through the approximate adjustment of the integral coefficient K_i.

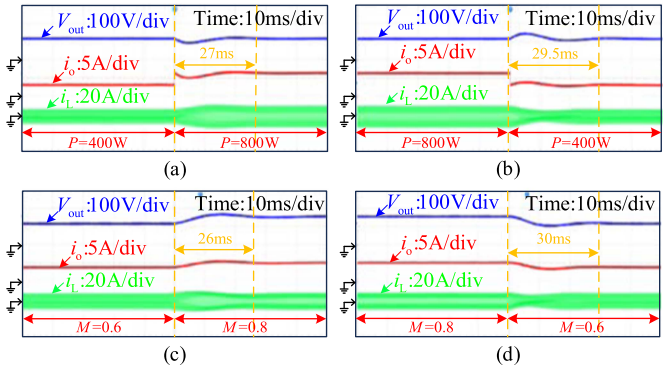

Fig. 16. Transient experimental results under load step and output voltage step changes. (a) Power step change from 400 to 800 W. (b) Power step change from 800 to 400 W. (c) Voltage step change from 120 to 160 V. (d) Voltage step change from 160 to 120 V.

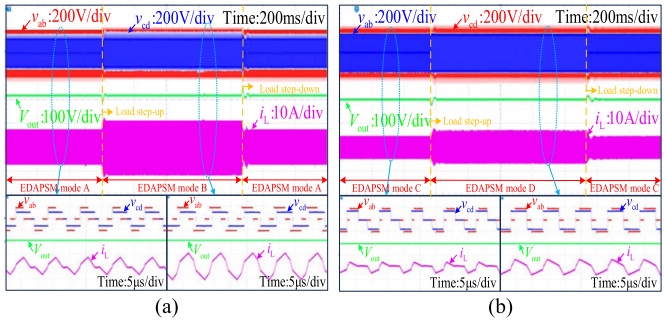

Fig. 17. Transient experimental results of mode switching. (a) $M = 0.6$. (b) $M = 1.25$.

In Fig. 17, the dynamic processes of different mode transitions are presented under step-up and step-down conditions. Fig. 17(a) shows the dynamic switching waveforms between EDAPSM mode A and EDAPSM mode B, when the voltage conversion ratio M is 0.6. Fig. 17(b) presents the dynamic

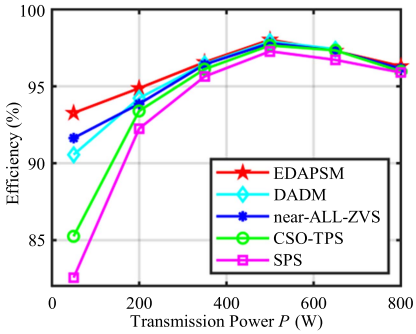

Fig. 18. Efficiency comparison of the five modulation methods at $M = 0.6$.

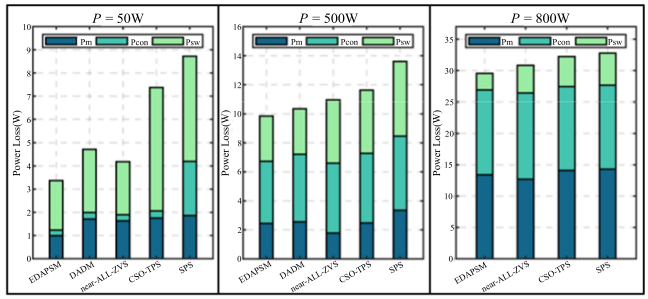

Fig. 19. Power loss breakdown of the five modulation methods at $P = 50$, 500, and 800 W under $M = 0.6$.

TABLE III
EFFICIENCY IMPROVEMENT COMPARISON RELATIVE TO THE SPS MODULATION METHOD

Modulation method	Light-load efficiency improvement	Maximum efficiency improvement
CSO-TPS	2.69%	0.38%
near-ALL-ZVS	9.08%	0.53%
DADM	8%	0.65%
EDAPSM	10.71%	0.75%

TABLE IV
COMPARISON OF EXECUTION TIME AND MEMORY USAGE FOR FIVE MODULATION METHODS

Modulation method	Execution time	Memory usage
SPS	4.095 μs	2.43 KB
CSO-TPS	11.895 μs	2.93 KB
near-ALL-ZVS	76.92 μs	6.1 KB
DADM	10.835 μs	$(2.997 + 0.0117n)$ KB
EDAPSM	31.02 μs	4.642 KB

switching waveforms between EDAPSM mode C and EDAPSM mode D, when the voltage conversion ratio M is 1.25. Thanks to the proposed smooth mode transition method, all variables undergo continuous changes during the mode switching process, and the inductor current i_L achieves a smooth transition.

E. Efficiency and Computational Burden Comparison

Fig. 18 presents the efficiency comparison among the EDAPSM method, the SPS modulation method, the CSO-TPS modulation method, the near-ALL-ZVS modulation method, and the DADM [22] method at a voltage conversion ratio $M = 0.6$. It is worth noting that the DADM method, due to its power limitations, can only transfer a maximum power of approximately 677 W at a voltage conversion ratio of $M = 0.6$, and therefore, the efficiency at 800 W is not shown in Fig. 18. Table III summarizes the comparison of efficiency improvement over the SPS modulation method at both maximum efficiency and light-load conditions for the CSO-TPS modulation method, the near-ALL-ZVS modulation method, the DADM method, and the EDAPSM method. The EDAPSM method achieves an efficiency of 93.27% at a light-load, showing improvements of 1.63%, 2.71%, 8.02%, and 10.71% over the near-ALL-ZVS modulation method, the DADM method, the CSO-TPS modulation method, and the SPS modulation method, respectively. The maximum efficiency of the EDAPSM method reaches 98.03%, which is an improvement of 0.1%, 0.22%, 0.37%, and 0.75% compared to the DADM method, the near-ALL-ZVS modulation method, the CSO-TPS modulation method, and the SPS modulation method, respectively.

At $M = 0.6$, the power loss breakdown of the five modulation methods under different transmitted power levels is shown in Fig. 19. When $P = 50$ W, switching losses dominate the total losses. Since all power switches in the EDAPSM, DADM, and near-ALL-ZVS methods can achieve ZVS, they exhibit significantly lower losses. When $P = 500$ W, the EDAPSM and near-ALL-ZVS methods require mode switching to accommodate the higher transmitted power, leading to increased switching losses. However, the switching losses in EDAPSM are still lower than those in near-ALL-ZVS, as only one power switch fails to achieve ZVS during the mode transition in EDAPSM, thereby reducing switching losses. Compared to the DADM method, EDAPSM exhibits lower conduction losses due to its reduced rms value of inductor current, resulting in overall lower power losses. When $P = 800$ W, all power switches in the modulation methods can achieve ZVS, resulting in minimal differences in power losses among them.

To quantify the computational burden of the five modulation methods, a comparison of their execution time and memory usage was conducted using the Code Composer Studio software. The quantification results are presented in Table IV. The SPS modulation method, which involves only one optimization variable and is directly provided by a PI closed-loop, requires an execution time of 4.095 μs and occupies 2.43 KB of memory. The CSO-TPS modulation method, due to the computation of two optimization variables, has a longer execution time of 11.895 μs compared to SPS, but its memory usage is slightly lower at 2.93 KB. The near-ALL-ZVS modulation method, which involves numerous square root operations, has the longest execution time of 76.92 μs, and consumes 6.1 KB of memory. The DADM modulation method, employing a lookup table, exhibits shorter execution time but requires significant data storage, where n represents the size of the required array. Although the EDAPSM method needs 31.02 μs of execution time and 4.642 KB of memory, it still demonstrates excellent performance compared to the DADM and near-ALL-ZVS methods.

TABLE V
COMPREHENSIVE COMPARISON BETWEEN THE EDAPSM METHOD AND ADVANCED MODULATION METHODS

Modulation method	Analytical method	Implementation Method	Computational burden	Peak-to-peak current	Wide voltage range	ZVS range	Efficiency	
							Light-load	Heavy-load
[1]	TDA	Online	★	★★★★★	★★★★★	★	★	★★★
[11]	TDA	Online	★★★	★★★	★★★★	★★★	★★★	★★★★
[12]	FDA	Offline	★★	★★★	\	\	★★	★★★
[13]	TDA	Online	★★★	★★★★	★★★	★★★	★★	★★★
[14]	TDA	Online	★★★★	★★★	★★★	★★★	★★★	★★★★
[16]	TDA	Online	★★★	★★★	\	★★★	★★★	★★★★
[17]	TDA	Online	★★★★★	★	\	★★★★★	★★★★	★★★★★
[18]	FDA	Offline	★★	★	\	★★★★★	★★★	★★★★
[22]	TDA	Offline	★★	★★	\	★★★★	★★★	★★★★
The proposed	TDA	Online	★★★★	★	★★★★★	★★★★★	★★★★	★★★★★

Very small (narrow): ★. Small (Narrow): ★★. Medium: ★★★. Large (Wide): ★★★★. Very large (wide): ★★★★★. \: Not Considered

F. Comprehensive Evaluation

To further demonstrate the advantages of the proposed EDAPSM method, Table V provides a comprehensive comparison between EDAPSM and existing advanced modulation methods. From Table V, it can be observed that existing advanced modulation methods require a tradeoff between computational burden and performance. In contrast, the proposed EDAPSM method achieves better performance while reducing a portion of the computational burden compared to the 5-DOF modulation method. By accurately modeling the resonant process during the dead time, the power switches can achieve more precise ZVS, reducing unnecessary circulating power and effectively improving efficiency under both light-load and full-load conditions. In addition, by employing the proposed multiobjective optimization approach, the EDAPSM method achieves a wider ZVS range and lower peak-to-peak inductor current. Thanks to the introduced approximation method and the flexible inner phase-shift angle d_2, the EDAPSM method can be implemented online over a wide voltage and full power range, thereby offering enhanced adaptability for DAB converters with different parameters. This avoids the need for reanalysis of look-up table methods when applied to DAB converters with varying parameters.

V. CONCLUSION

This article proposes an EDAPSM modulation method for DAB converters operating over a wide voltage range. A detailed modeling and analysis of the ZVS conditions for the power switches is presented. A multiobjective optimization scheme is established based on the proposed modulation method, and an approximation method is introduced to obtain analytical solutions across the entire power range. Although the approximation method increases the peak-to-peak value of the inductor current to some extent, it reduces the rms value of the inductor current, thereby decreasing conduction losses. To address the issue of abrupt changes in the optimization variables during mode transitions, a smooth mode transition method is proposed, which effectively prevents uncontrolled oscillations in the inductor current. Compared with SPS modulation, CSO-TPS modulation, near-ALL-ZVS modulation, and the DADM method, the proposed approach significantly reduces the rms of the inductor current across the full power range, expands the ZVS range of the power switches, and effectively improves the overall efficiency of the DAB converter, especially under light-load conditions. Due to the complexity of the analytical solution of the proposed modulation method, which leads to a high computational burden, the interrupt frequency in the digital signal processor is set to 0.2 times the switching frequency. To compensate for the degraded dynamic response caused by the reduced interrupt frequency, the integral coefficient K_i is approximately increased by a factor of five. Finally, experimental results verify that the DAB converter can achieve high efficiency and stable operation over a wide voltage range with the proposed method, along with good dynamic performance.

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