Experimental Investigation-Based Practical Design Guideline of 50 kW Three-Phase AC/DC Converter for Fast Charger Power Module

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***Abstract*—The demand for high-power dc fast chargers has increased to reduce electric vehicle charging time, driving the active adoption of power modules to enhance charger power capacity. As the power capacity per module increases and the number of parallel modules decreases, the overall system volume and cost are reduced. Thus, the development of high-power modules has become increasingly important. Therefore, this article provides practical guidelines for implementing a 50 kW three-phase power factor correction (PFC) converter, commonly used as an ac–dc converter module in dc fast charger. A quantitative analysis of the volume, performance, cost, and efficiency of different filter types for a three-phase PFC designed under identical conditions is conducted, providing selection criteria based on design priorities. Additionally, a stable startup method using feedforward compensation is proposed to regulate the inrush current. The effects of gain variations on steady-state and dynamic characteristics, along with current total harmonic distortion (THD), are analyzed. Furthermore, hardware implementation and thermal design considerations for the reliable parallel operation of SiC MOSFETS are presented. As a result, the implemented three-phase PFC converter achieves a maximum efficiency of 98.65% and an efficiency of 97.10% under full-load conditions, while maintaining a current THD within 5% in the primary operating range.**

***Index Terms*—AC–DC converter module, dc fast charging, electric vehicles (EVs), SiC-MOSFET.**

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I. Introduction

RECENTLY, as the driving range of electric vehicles (EVs) has become a critical factor in their widespread adoption, the demand for high-power dc fast charging system has rapidly increased [1], [2], [3], [4] In general, to simplify the design process and facilitate convenient implementation, the output power of a dc fast charging system is increased by connecting identical modules in parallel [3]. Depending on the parallel connection structure, the dc fast charging systems are classified into ac bus-connected system and dc bus connected system, as shown in Fig. 1. The ac bus-connected system is structured by simply increasing the number of parallel modules combined with power factor correction (PFC) and dc–dc converters, which facilitates implementation and ensures high stability [2]. In contrast, the dc bus-connected system integrates a single PFC converter with multiple dc–dc converters [4]. This structure enables efficient integration with photovoltaic systems and energy storage systems that generate dc power, allowing for various charging system configurations [5], [6]. Recently, as the demand for high-power fast charging systems to reduce charging time has increased, the development of higher-capacity ac–dc and dc–dc converter modules has accelerated to accommodate both ac bus- and dc bus-connected configurations. In general, increasing the output power of a dc–dc converter adds more challenges to step-up voltage conversion and magnetic component design, leading to the use of multiple parallel modules to enhance power capacity [7], [8]. In contrast, since an ac–dc converter is less constrained by these issues, it is designed to handle higher power capacity within feasible limits, with parallel modules applied when further capacity expansion is required. For this reason, the application of high-power ac–dc converter design technology improves the flexibility of fast charging systems regardless of ac or dc bus configuration while also reducing cost and volume by minimizing the number of parallel modules.

Moreover, as wide bandgap (WBG) devices, such as SiC MOSFETS, are increasingly adopted in various systems, their application in three-phase PFC converters continues to expand. Compared to conventional Si-based systems, WBG devices enable higher switching frequencies, which reduce filter volume and enhance power density. Additionally, their fast-switching characteristics and low conduction resistance contribute to an overall improvement in system efficiency. However, owing to the

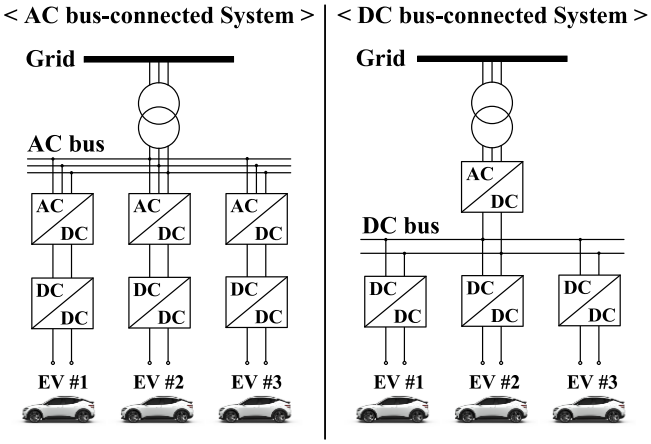


Fig. 1. Parallel connection structure of a DC fast charging system.

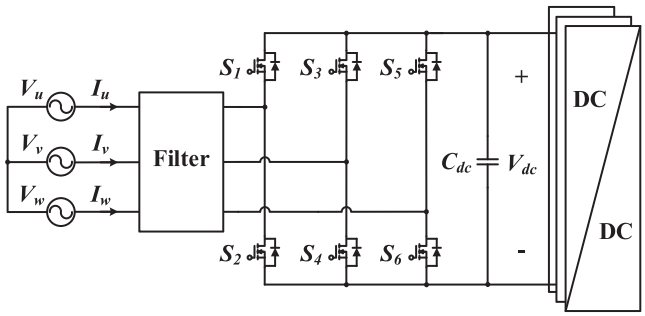


Fig. 2. Circuit diagram of three-phase PFC converter.

fast-switching characteristics of WBG devices and the increasing output power, three critical factors should be considered in PFC converter design: 1) filter design considering system priorities, 2) stable controller design, and 3) efficient hardware design and implementation. Therefore, this article presents and experimentally verifies a practical approach to the design, control, and implementation of the three aforementioned factors in a 50 kW SiC MOSFET-based three-phase PFC converter, as shown in Fig. 2, which is widely used as an ac–dc converter module in fast charging systems.

The filter in a three-phase PFC determines the input current ripple and prevents switching noise from propagating to the grid. In particular, the high *dv/dt* and *di/dt* of SiC-based systems intensify noise issues compared to Si-based systems, potentially affecting multiple power conversion systems on the same grid and thereby emphasizing the importance of filter design [9]. *L*, *LC*, and *LCL* filters, which are commonly applied in three-phase PFCs, have well-established and validated design methods [10], [11], [12]. For this reason, subsequent studies have focused on optimizing filter performance through optimal parameter design [13], [14] and enhancing performance using auxiliary circuits [15]. However, most studies focus on *LCL* filters, while systematic comparisons of *L*, *LC*, and *LCL* filters in terms of cost, performance, size, and efficiency remain limited. In [16], *L* and *LCL* filters were compared in a 2 kW inverter system. However, since the design conditions for each filter were not identical, a fair comparison was challenging, and only a basic

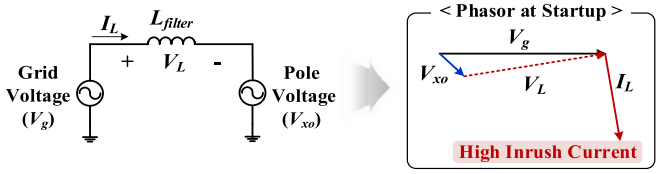


Fig. 3. Single-phase equivalent circuit and phaser diagram of three-phase PFC.

performance evaluation was conducted. In [17], *L*, *LC*, and *LCL* filters were compared, but the results were inconclusive and primarily based on simulation data. To address these limitations, this article presents a fair and objective comparison of *L*, *LC*, and *LCL* filters designed under equivalent conditions. The filters are experimentally evaluated in terms of performance, size, and efficiency. The results provide practical guidance for filter selection based on system priorities and are expected to reduce the design and implementation time for three-phase PFC systems.

Next, the inrush current during the startup of the three-phase PFC should be considered. As shown in Fig. 3, immediately after PWM control starts, the lower pole voltage V_{xo} relative to the grid voltage V_g induces a high voltage across the filter inductor, resulting in excessive inrush current [18]. Therefore, duty-cycle soft-start control, which linearly increases the duty cycle during startup, was proposed in [19] and [20]. In addition, a ramp-based reference control method that gradually increases the reference value was proposed in [21]. However, these methods have an inherent limitation in that reducing the inrush current requires extending the soft-start duration, which inevitably increases the overall startup time. In [22] and [23], the relationship between input/output voltage and duty cycle was used to derive the feedforward compensation components, which was added to the controller output. These methods demonstrated improvements in current total harmonic distortion (THD) and power factor; however, the reduction in inrush current was not verified. In [24], a nonlinear voltage controller that incorporates the square of the error in an integral controller was proposed to improve the control response, reducing both inrush current and settling time compared to the conventional PI controller. However, since the proposed control method is error-based, its response characteristics may be slightly inferior to those achieved through feedforward compensation.

Therefore, the proposed controller employs feedforward compensation components to enhance startup responsiveness. However, since these components are derived from sensing values and directly influence the control output, sensing errors, particularly those induced by switching noise, can compromise system stability. To mitigate this issue, a startup control method is proposed to reduce the impact of noise-induced errors in the feedforward components. Experimental results confirm that the proposed method achieves both fast startup and effective inrush current suppression. Additionally, the three-phase PFC applied to the ac–dc converter module in the fast charger should maintain a stable dc link voltage even under no-load conditions, thereby enabling an immediate response to various load connections. Therefore, this article validates the suitability of the proposed controller for the fast charger through no-load startup performance and load connection experiments.

In this article, a conventional PI controller is used for feedback control, excluding the feedforward compensation. Various methods for determining PI controller gains have been described in numerous studies [25], [26], [28]. These studies have derived optimal gains based on mathematical formulations [25], [26] or have selected gains for several cases and then determined the optimal gain by analyzing system response characteristics through bode plots and simulations [27], [28]. These methods are expected to enable optimal gain selection when accurate system modeling is ensured and to allow the actual system response to match the simulation results. However, in practical systems, parasitic elements vary depending on hardware, PCB design, and overall system configuration, which limits the accuracy of system modeling. Additionally, simulations have limitations in accurately reflecting minor delays and sensing errors, making it difficult to accurately evaluate controller responsiveness. As a result, the gains derived solely from simulations or mathematical formulations may not be directly applicable in practice, necessitating experimental tuning. For this reason, this article presents a practical gain tuning guideline based on experimental observations, detailing the impact of PI gain variation on current waveforms and THD. This approach enables designers to optimize controller parameters without relying on complex system modeling, thereby facilitating efficient implementation in practical applications.

Commonly, high-power PFCs use power modules with high current ratings. However, since these modules are more expensive than discrete devices and may also have limitations in adopting high-rated WBG devices, this article implements the PFC hardware using three parallel-connected discrete SiC MOSFETS. When driving devices in parallel, it is essential to consider the temperature and current imbalance between the devices. In particular, SiC MOSFETS exhibit an increase in turn-ON delay time at high temperatures, and their temperature-dependent variations in I-V characteristics are more pronounced than those of Si devices. As a result, temperature imbalances between parallel-connected devices can lead to current imbalances [29], [30], [31]. Therefore, this article proposes a hardware implementation method that includes a detailed PCB layout and liquid-cooled thermal design suitable for high-power systems, aiming to mitigate temperature and current imbalances between parallel-connected switches. The effectiveness of the proposed approach is experimentally validated through temperature saturation tests, confirming balanced thermal behavior under full-load operation.

Consequently, based on the aforementioned considerations, this article presents the design, control, and hardware implementation strategies of a 50 kW three-phase PFC as follows.

1) In Section II, *L*, *LC*, and *LCL* filters are designed under identical conditions, and their cost, volume, and efficiency are compared through experimental results.
2) In Section III, a control strategy for limiting inrush current in the three-phase PFC converter is described, and the effects of PI gain on system characteristics are evaluated.
3) In Section IV, hardware implementation methods, including PCB layout design for stable SiC MOSFET operation and thermal management for efficient heat dissipation, are explained.

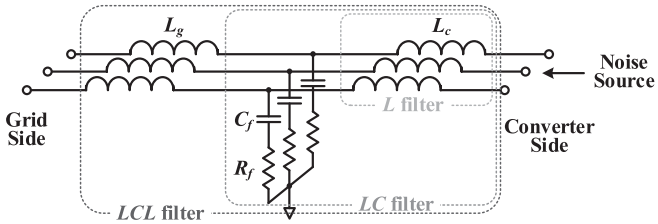


Fig. 4. Commonly applied filter types for three-phase PFC.

4) In Section V, experimental results and key design considerations are summarized.

II. Effective Filter Selection Based on Filter Design and Performance Comparison

A. L, LC, and LCL Filters Design

The filter inductor L_c shown in Fig. 4 is a critical parameter in determining the current ripple. Its value is defined by the

$$L_c = \frac{V_{\rm dc}}{6 f_{sw} \Delta I_{in,\max}} \tag{1}$$

$$f_c = \frac{1}{2\pi\sqrt{L_c C_f}} \tag{2}$$

$$L_g = \frac{\sqrt{\frac{1}{k_a^2}} + 1}{C_f (2\pi f_{sw})^2} \tag{3}$$

$$L_g = \gamma L_c \tag{4}$$

$$10 f_g < f_{ref} < 0.5 f_{sw} \tag{5}$$

voltage-current relationship of the inductor, as expressed in (1) [10]. In (1), $V_{\rm dc}$ represents the maximum output voltage of the PFC, f_{sw} is the switching frequency, and $I_{\rm in,max}$ is the maximum input current. In addition, $\Delta I_{\rm in,max}$ denotes the maximum allowable current ripple, which is limited to 10% of $I_{\rm in,max}$ in this article. Next, the filter capacitor C_f is designed based on the cutoff frequency f_c, as expressed in (2). In this article, f_c is set to approximately 1/10 of the f_{sw}. The grid-side inductor L_g is calculated using (3) and can be expressed as a fixed ratio γ of L_c, as shown in (4) [10], and [11]. In (4), k_a represents the harmonic current ratio between the input and output of the filter. As k_a decreases, the harmonic attenuation performance of the filter improves, while a larger L_g is required, which negatively impacts power density. Unlike *L* and *LC* filters, the *LCL* filter allows for various design parameters by adjusting the ratio between L_g and L_c while maintaining similar performance. Therefore, this article determines the optimal parameters by comparing the volume and cost of various *LCL* filter design cases and then evaluates the final selected *LCL* filter against the previously designed *L* and *LC* filters in terms of cost, volume, and efficiency.

Table I provides filter design conditions, while Table II presents the design parameters for each filter type, calculated using (1)–(4). Additionally, C_f is fixed at 4.8 μF for all filter types, corresponding to the design requirements of (2) for the

TABLE I
FILTER DESIGN CONDITIONS

Parameters	Values	[Unit]
Line-to-line voltage V_{LL}	380	[V_{rms}]
Grid frequency f_g	60	[Hz]
Maximum output power, P_o	50	[kW]
Dc link voltage V_{dc}	800	[V]
Maximum input current ripple, $\Delta I_{in,max}$	10	[A]
Switching frequency f_{sw}	25	[kHz]
Current THD	< 5%	-

TABLE II
DESIGN PARAMETERS OF FILTER INDUCTORS

Parameter	Filter types and values				
	L / LC	Case 1	Case 2	Case 3	Case 4
k_a / γ	-	0.25 /0.24	0.30 / 0.15	0.40 / 0.08	0.55 / 0.04
L_c [μH]	533	150	200	300	400
L_g [μH]	-	35.5	30	23.2	17.9

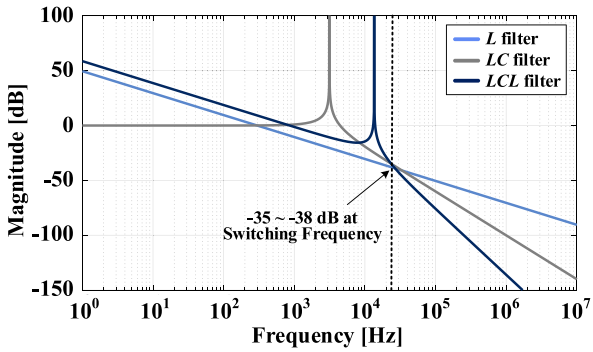


Fig. 5. Bode plot of designed L, LC, and LCL filters (LCL filter corresponds to case 1).

LC filter and (5) for the LCL filter. To compare the performance of different filter types under identical conditions, each filter is designed with the same maximum current ripple and similar attenuation performance near the switching frequency, as shown in Fig. 5. Since both the L and LC filters use a single filter inductor, the value of L_c required to satisfy the maximum allowable current ripple remains consistent. However, in the case of LCL filter, the addition of L_g allows the maximum allowable current ripple to be satisfied with a smaller L_c compared to other filters. Moreover, Fig. 6 presents four LCL filter design cases with different k_a and γ that satisfy the same design conditions.

B. Hardware Design of L, LC, and LCL Filters

Inductor hardware design should consider the reduction in inductance caused by dc bias. Neglecting this effect may result in current distortion from saturation, which, in extreme cases, can lead to system failure caused by a short circuit [32], [33]. Therefore, this article follows the design guidelines provided below for hardware implementation, based on empirical principles.

1) The inductance should meet the design value at 50% of the maximum current.
2) At the maximum current, the inductance should retain at least 30% of the design value.

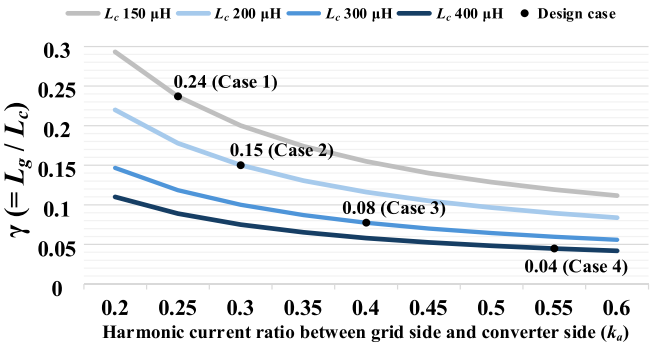


Fig. 6. LCL filter design cases according to k_a and γ values.

TABLE III
HARDWARE INFORMATION OF L_c

Filter type	Volume [cm^3]	Turns	Core material	Inductance [µH] 0 [A]	50 [A]	107 [A]
L	180.8	80	Mega flux	1322	574	214
LC						
Case 1	124.3	25		227	166	90
Case 2	138.4	35		338	229	114
Case 3	152.5	45		502	309	141
Case 4	159.6	60		850	429	172

TABLE IV
HARDWARE INFORMATION OF L_g

Filter type	Volume [cm^3]	Turns	Core material	Inductance [µH] 0 [A]	50 [A]	107 [A]
Case 1	21.4	20	High flux	112	40	10
Case 2	14.0	21		41	29	13
Case 3	10.5	21		36	24	10
Case 4	8.2	19		25	18	7

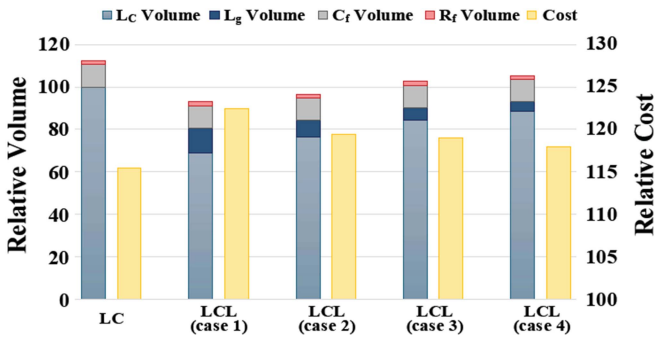


Fig. 7. Comparison of hardware volume and cost for different filter types.

Tables III and IV present the inductor hardware details implemented in this article. For the relatively large inductance of L_c, a block core is employed, whereas a toroidal core is used for L_g. The comparison results of the volume and cost of each filter are shown in Fig. 7. The volume and cost of the L filter are set as reference values of 100, while those of the other filters are calculated as relative values to facilitate comparison.

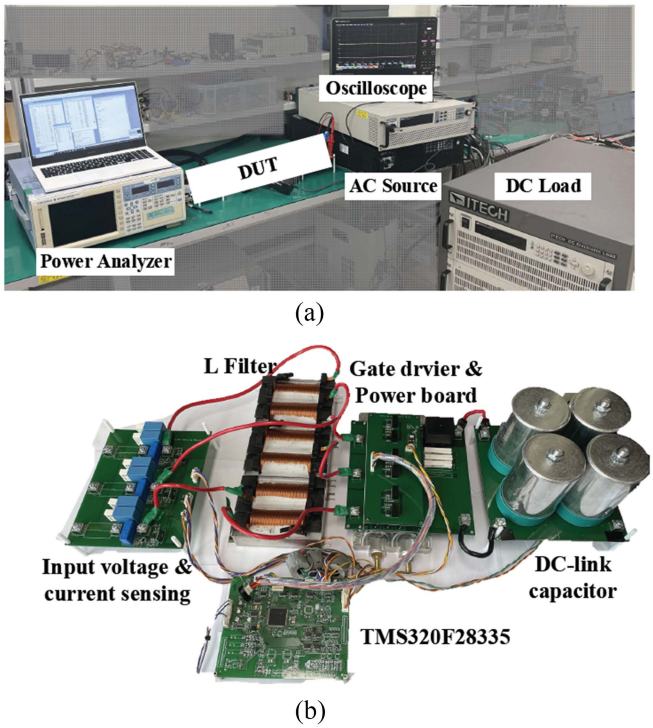


Fig. 8. Experimental setup and hardware of three-phase PFC. (a) Experimental Setup. (b) Hardware.

From this result, a tradeoff is observed as the cost decreases while the volume increases from Case 1 to Case 4. Considering these trends, Case 2 is selected as the optimal parameter for the *LCL* filter, as it demonstrates a relatively smaller volume increase compared to the significant cost reduction. Therefore, the following sections present the comparison results of the *L* and *LC* filters along with Case 2 of the *LCL* filter.

C. Performance Comparison and Analysis Based on Filter Types

Fig. 8 shows the experimental setup and hardware configuration used to measure current THD for each filter type. The experimental conditions are identical to Table I, and the current THD measurement results under load variation are shown in Fig. 9. To satisfy the hardware design guidelines described in Section II-B, the filter inductor exhibits a higher inductance than the designed value under light-load conditions. As a result, the current THD is lower when applying *L* and *LC* filters (1322 μH to 574 μH) compared to the *LCL* filter (338 μH to 229 μH). However, as the load increases, the difference in current THD across the three filter types decreases, and the target of 5% current THD is achieved at one-third of the rated power, confirming that they are designed to deliver similar performance. As shown in Fig. 10, the experimental waveforms for each filter type under the 18 kW load condition are presented. As shown in Fig. 9, the current waveforms in Fig. 10(a) and (b) are similar. In contrast, Fig. 10(a) shows that applying the *L* filter introduces a significant amount of high frequency noise in the line-to-line voltage. The observed waveforms indicate that switching noise from the switching leg

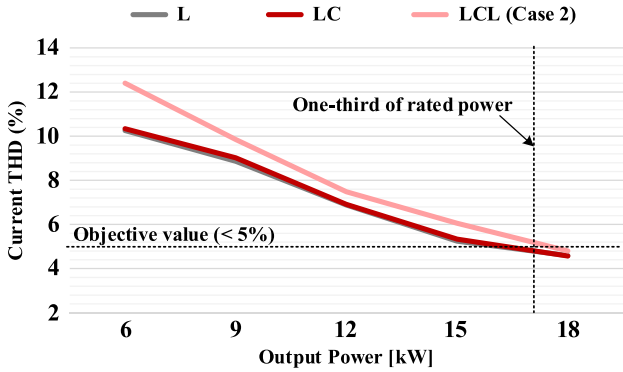


Fig. 9. Comparison results of current THD for different filter types.

is directly propagated to the grid side. This switching noise can adversely affect multiple power conversion devices connected to the same grid, necessitating mitigation through the addition of filter capacitors, as shown in Fig. 10(b) and (c). In actual systems, the addition of an EMI filter reduces noise on the grid even when using an *L* filter; however, the design burden of the EMI filter increases compared to *LC* and *LCL* filters with filter capacitors. Considering the ongoing trend of increasing switching frequencies with the use of WBG devices, relying exclusively on an *L* filter may present challenges.

Next, Fig. 11 represents the efficiency comparison of the overall system for each filter type. Previous experimental results have demonstrated that the *L* filter is difficult to apply in high-frequency systems. Additionally, since its efficiency is nearly identical to that of the *LC* filter, the analysis focuses on the efficiency difference between the *LC* and *LCL* filters. For the *LC* filter, the maximum efficiency $\eta_{\max \cdot LC}$ is 98.65% at a 12 kW load, and the full-load efficiency $\eta_{\text{full} \cdot LC}$ is 97.10% at a 50 kW load. For the *LCL* filter, the maximum efficiency, $\eta_{\max \cdot LCL}$ is 98.53% at a 15 kW load, and the full-load efficiency $\eta_{\text{full} \cdot LCL}$ is 97.08% at a 50 kW load. Consequently, the system efficiency is higher when the *LC* filter is applied under all load conditions, with the maximum efficiency difference $\Delta\eta_{\max}$ observed to be 0.34% p in the main operating range.

In summary of the previous experimental results, when minimizing system volume is the primary consideration in the design of a three-phase PFC converter, applying an *LCL* filter is more effective. On the other hand, when cost reduction, efficiency maximization, and low current THD over a wide load range are prioritized, applying an *LC* filter is more effective. Considering this tradeoff, the system implemented in this article selects the *LC* filter. Therefore, all experimental data presented in the following sections reflect the results obtained with the *LC* filter.

III. Practical Implementation Strategies for a Stable Three-Phase PFC Controller

A. Control Method for Inrush Current Reduction and Fast Startup

Fig. 12 presents the inrush current waveforms during startup without feedforward control. Since excessive inrush current causes hardware damage, experiments are conducted under low

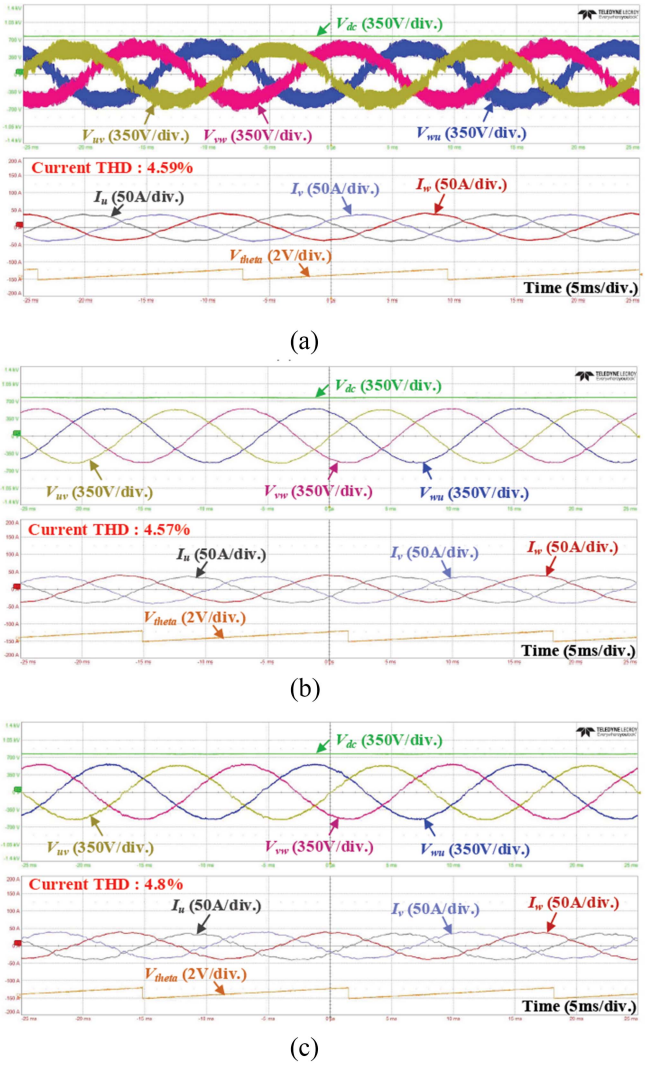


Fig. 10. Experimental waveforms at 18 kW for different filter types. (a) *L* filter. (b) *LC* filter. (c) *LCL* filter.

input and output conditions (V_{LL} : 220 $V_{\rm rms}$, $V_{\rm dc}$: 400 V, P_o : 3 kW) to ensure that the hardware remains undamaged during inrush events. As a result, the inrush current is measured at approximately 100 A, which occurs because of the significantly low pole voltage V_{xo} at startup compared to

$$V_{d,ref} = \left(k_{d,p} + \frac{k_{d,i}}{s}\right)(i_d - i_{d,ref}) + V_d \tag{6}$$

$$V_{q,ref} = \left(k_{q,p} + \frac{k_{q,i}}{s}\right)(i_q - i_{q,ref}) + V_q \tag{7}$$

the grid voltage V_g, as shown in Fig. 3. For this reason, the conventional feedforward compensation method involves adding the grid voltage magnitude V_d and phase V_q information to the controller output, as shown in (6) and (7). As shown in Fig. 13, this method increases the pole voltage V_{xo} of each phase to match the magnitude and phase of the grid voltage V_g when the PWM control is initiated, thereby significantly reducing the magnitude of the input current I_L. In this process, the relationship among

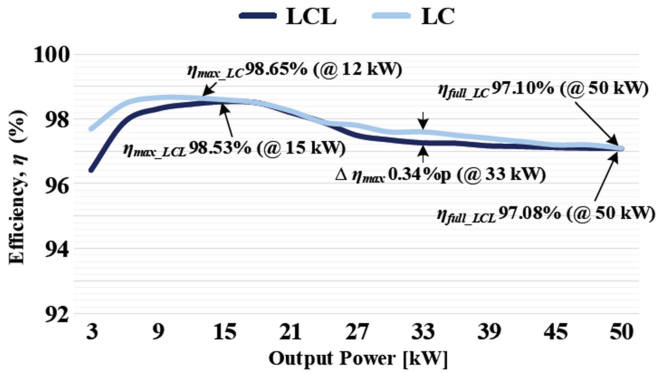


Fig. 11. Efficiency comparison results based on filter types.

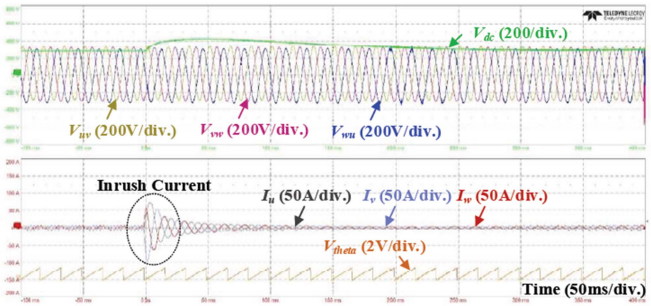


Fig. 12. Experimental waveform without feedforward control (V_{LL}: 220 $V_{\rm rms}$, $V_{\rm dc}$: 400 V, P_o: 3 kW).

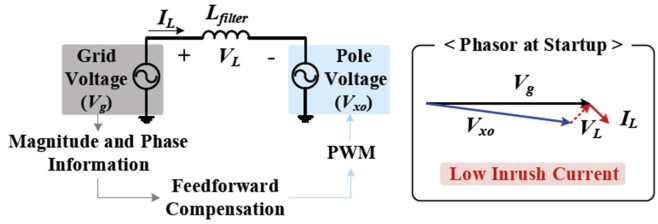


Fig. 13. Single-phase equivalent circuit and phaser of three-phase PFC.

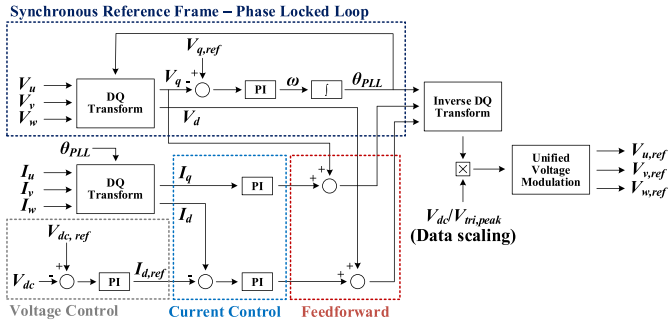


Fig. 14. Control block diagram of three-phase PFC.

the pole voltage, the modulation index m_a, and the dc-link voltage $V_{\rm dc}$ is considered, and a data scaling process is applied to match the actual duty ratio. The control algorithm block diagram reflecting this process is shown in Fig. 14, where the overall controller performs DQ transformation using the phase information $\theta_{\rm PLL}$ obtained based on synchronous reference

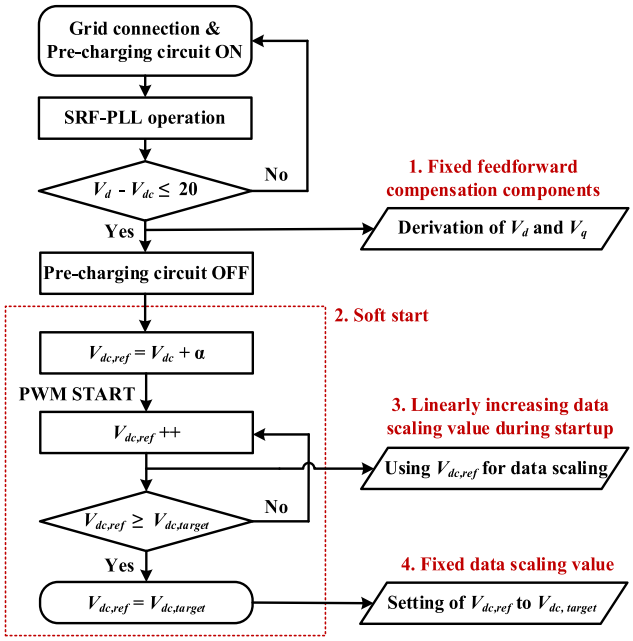


Fig. 15. Control algorithm for limiting inrush current of three-phase PFC.

frame – phase-locked loop (SRF-PLL) control. Additionally, the composition of the controller includes voltage/current control and feedforward compensation components.

However, this feedforward compensation method heavily depends on sensing performance to obtain the V_d and V_q, in addition to the $V_{\rm dc}$ information for data scaling. Therefore, when accurate sensing performance is not provided, effective inrush current limiting cannot be achieved, potentially leading to system instability and divergence. The main factors that degrade sensing performance are switching noise caused by high *dv/dt* and *di/dt*. Although this noise may not present significant issues at actual power levels, its impact on sensing circuits dealing with small signals within 5 V can be dominant. Particularly, in WBG device-based systems with high-speed switching characteristics, the impact of switching noise is greater compared to conventional systems, which necessitates considering the distortion of the feedforward compensation components.

Therefore, this article proposes the control algorithm shown in Fig. 15. All components required for feedforward compensation are derived during the precharging operation before PWM control starts, ensuring high control stability that is unaffected by switching noise. During the precharging operation, V_d and V_q are derived through SRF-PLL control based on grid voltage sensing and are input as constant values to the controller. As a result, stable feedforward components can be input to the controller without the influence of switching noise before PWM control begins. During PWM control, the feedforward components maintain the constant values (corresponding to No. 1 in Fig. 15). To prevent inrush current caused by a large error when directly applying the target reference voltage $V_{\rm dc,target}$, which is approximately 280 V higher than $V_{\rm dc}$ at startup, $V_{{\rm dc},ref}$ is defined as $V_{\rm dc}$ + α at the precharging operation OFF point (The explanation for selecting α is presented in the following paragraph.). After startup, $V_{{\rm dc},ref}$ increases linearly until it reaches $V_{\rm dc,target}$ (corresponding to No. 2 in Fig. 15). Furthermore, applying a soft start is essential to effectively suppress inrush current, but this should be accompanied by the appropriate incorporation of the previously derived feedforward components into the controller output. Thus, accurate data scaling is crucial. The data scaling value is determined by the ratio of the $V_{\rm dc}$ to the carrier peak voltage $V_{tri,\rm peak}$. However, inaccurate sensing of $V_{\rm dc}$ may lead to instability in feedforward compensation. Therefore, in this study, $V_{\rm dc}$ is set to the $V_{{\rm dc},ref}$, which is not affected by sensing accuracy, ensuring a stable controller implementation (corresponding to No. 3 in Fig. 15). For this reason, the data scaling value increases linearly as $V_{{\rm dc},ref}$ rises during startup. After $V_{{\rm dc},ref}$ is fixed at $V_{\rm dc,target}$, the data scaling value remains constant (corresponding to No. 4 in Fig. 15). As a result, using $V_{{\rm dc},ref}$ instead of $V_{\rm dc,target}$ for data scaling allows the scaling value to be influenced by the soft start during startup, effectively suppressing inrush current while maintaining a constant value after startup.

The three-phase PFC used in ac–dc converter module is required to maintain a stable dc link voltage even under no-load conditions, ensuring immediate response to load connections. Therefore, to validate the effectiveness of inrush current limitation and no-load control performance, operational verification is performed, as shown in Fig. 16(a). The PFC reaches the target $V_{\rm dc}$ under no-load conditions approximately 30 ms after startup. Subsequently, as the load is connected, the PFC begins supplying 10 kW to the load. Fig. 16(b) and (c) represents the transient response characteristics during no-load control and load connection, respectively. Fig. 16(b) confirms that the inrush current is eliminated, and the initial current at startup is approximately 10 A by applying the proposed control algorithm. Additionally, Fig. 16(c) confirms that the designed system operates stably even when a 10 kW load is connected.

Next, the reason for selecting α is explained. When α is set to zero at startup, meaning that $V_{{\rm dc},ref}$ is equal to $V_{\rm dc}$ at the precharging operation OFF point, the startup waveforms correspond to Fig. 17(a). Additionally, when $V_{{\rm dc},ref}$ is initially set to $V_{\rm dc,target}$, the startup waveforms correspond to Fig. 17(b). As a result, when α is set to zero, $V_{\rm dc}$ experiences difficulty in rising due to the low $V_{{\rm dc},ref}$, leading to an extended startup time. However, since accurate data scaling values are provided at startup when the feedforward component is applied, the initial current remains similar to that in Fig. 16. On the other hand, when $V_{{\rm dc},ref}$ is fixed at $V_{\rm dc,target}$ during startup, the startup time is observed to be similar to that shown in Fig. 16. However, inaccurate data scaling leads to an increase in the initial current to approximately 35 A. Consequently, setting $V_{{\rm dc},ref}$ slightly higher than $V_{\rm dc}$ at the precharging operation OFF point is advantageous for reducing startup time and limiting inrush current, resulting in the selection of α as 20.

B. Experimental Investigation-Based PI Gain Tuning Guidelines

This article analyzes waveform variations based on controller gains through experimental verification to provide guidelines for

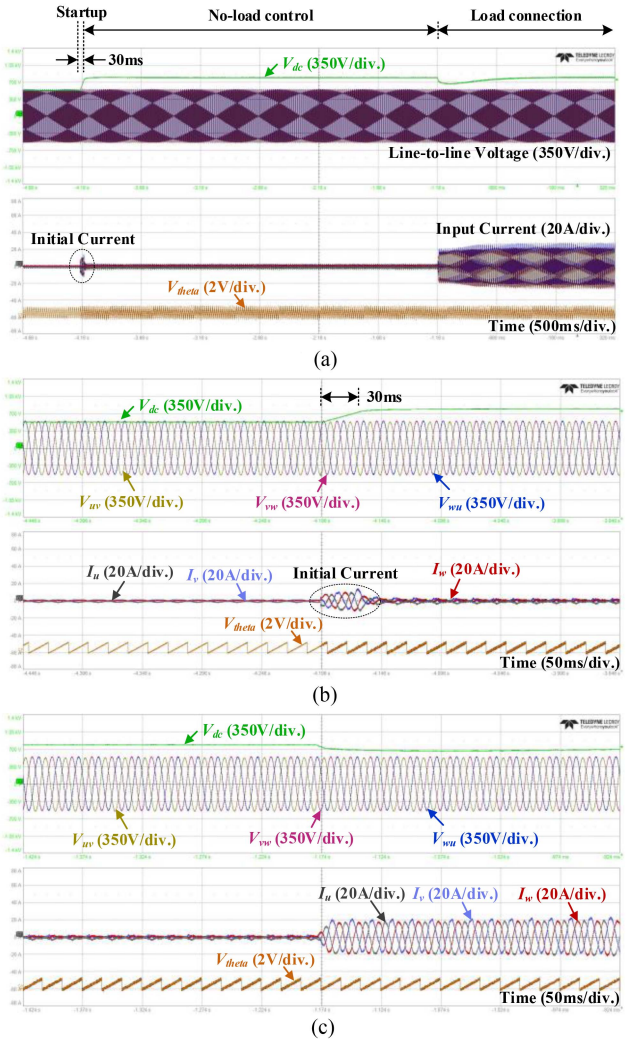


Fig. 16. Experimental waveforms of no-load startup and load connection. (a) No-load startup and load connection. (b) Transient response characteristics during no-load startup. (c) Transient response characteristics during load connection.

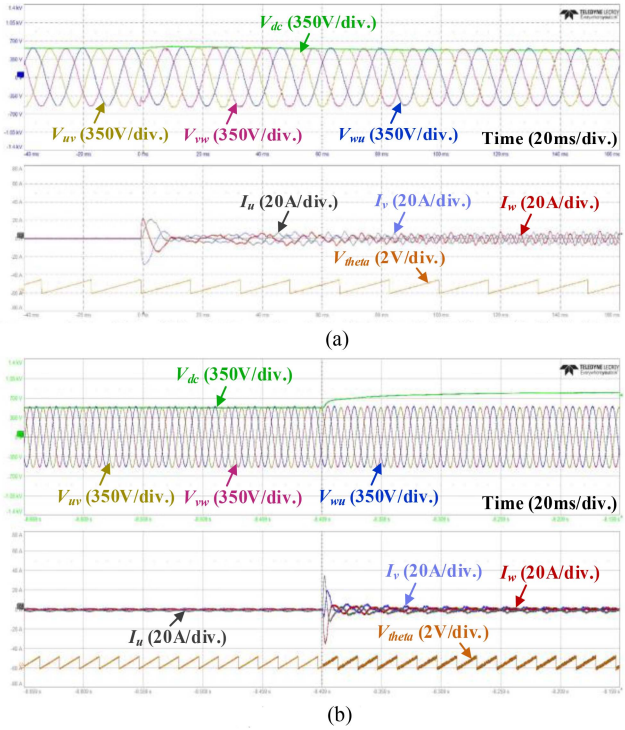


Fig. 17. Experimental waveforms of startup according to $V_{\mathrm{dc},ref}$ variation. (a) $V_{dc,ref}$ being equal to V_{dc}. (b) $V_{dc,ref}$ being equal to $V_{dc,target}$.

TABLE V
GAIN TUNNING TEST CONDITIONS

Parameters	Values	[Unit]
Line-to-line voltage V_{LL}	380	[V_{rms}]
Grid frequency f_g	60	[Hz]
Dc link voltage V_{dc}	800	[V]
Output power P_o	3 – 50	[kW]

gain tuning. As shown in Fig. 14, the three-phase PFC consists of a voltage controller, a d-axis current controller responsible for current magnitude, and a q-axis current controller responsible for current phase. Each controller is implemented using a PI controller, resulting in three pairs of PI gains in total.

System characteristics variations with respect to controller gains can be examined by categorizing them into steady-state and dynamic characteristics. First, the steady-state characteristics are compared by observing waveform variations while V_{dc} remains constant, indicating that the output of the voltage controller is in a steady state. Therefore, with the PI gains of the voltage controller fixed at 0.1 and 2, the waveform and current THD variations are analyzed by classifying the cases into three types: increasing only the PI gain of the d-axis current controller, increasing only the PI gain of the q-axis current controller, and increasing the PI gains of both current controllers. The experimental conditions are shown in Table V, and the experimental results for gain variations under an 18 kW load condition are presented in Table VI and Fig. 18. Additionally, for specific cases in which current variations are prominent in the current THD graph of Fig. 18, the corresponding waveforms are presented in Fig. 19. In Case I, where the d-axis and q-axis current controllers have small gains, a significant current imbalance is observed, as shown in Fig. 19(a). The effect of increasing only the d-axis gain while keeping the q-axis gain fixed is analyzed by evaluating current THD and waveforms. The results indicate that the current imbalance remains unresolved, while current oscillations intensify, leading to an increase in current THD. Specifically, when the d-axis P gain becomes excessively high, irregular current oscillations intensify, as shown in Fig. 19(b). Next, with the d-axis gain set to its initial value, the q-axis gain is increased to examine its effect. The results indicate that as the q-axis P gain increases, the current imbalance improves, as shown in Fig. 19(c). However, when the I gain becomes excessively high, the current THD increases, as observed in Case XI. With the q-axis gain from Case X, which exhibits the lowest current THD, the d-axis gain is further increased as in Cases XII and XIII to examine changes in current THD and waveforms. As a result, current THD slightly improves as the d-axis gain

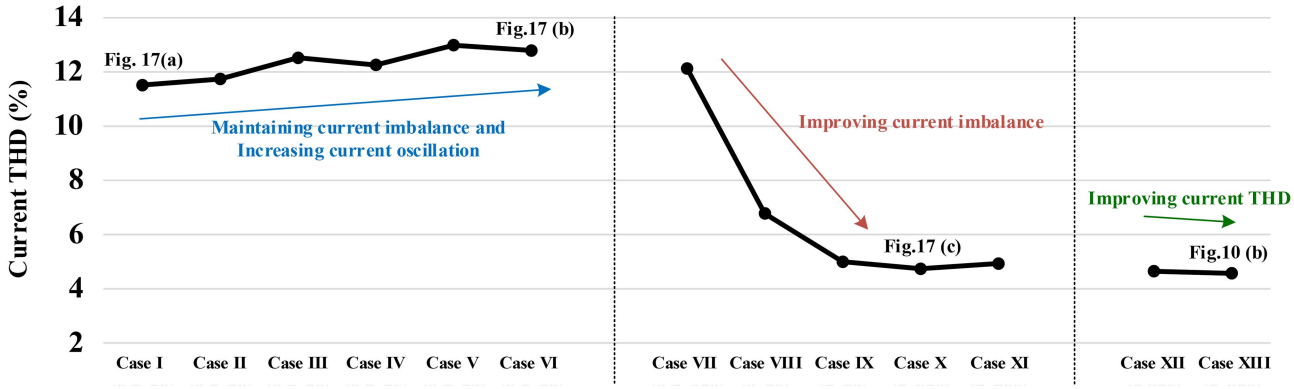


Fig. 18. Experimentally measured current THD according to gain variation under an 18 kW load condition.

TABLE VI
GAIN TUNNING TEST RESULTS AT 18 KW LOAD

Case	d-axis current (P gain, I gain)	q-axis current (P gain, I gain)	Current THD
I	(0.5, 50)	(0.5, 50)	11.51
II	(2, 50)	(0.5, 50)	11.74
III	(0.5, 200)	(0.5, 50)	12.52
IV	(2, 200)	(0.5, 50)	12.26
V	(2, 500)	(0.5, 50)	12.99
VI	(6, 200)	(0.5, 50)	12.79
VII	(0.5, 50)	(0.5, 350)	12.13
VIII	(0.5, 50)	(2, 50)	6.78
IX	(0.5, 50)	(5, 50)	4.99
X	(0.5, 50)	(5, 350)	4.74
XI	(0.5, 50)	(5, 700)	4.93
XII	(0.5, 200)	(5, 350)	4.65
XIII	(2, 200)	(5, 350)	4.57

increases. For this reason, this article selects the gain from Case XIII, and Fig. 10(b) shows the experimental waveforms with this gain applied.

Next, the current THD variation according to gain is investigated under increasing load conditions. Since previous experiments confirmed that increasing the gain of the *q*-axis current controller does not improve the waveform once the current imbalance issue is resolved, the current THD variation under different load conditions is examined only for Case X and Case XIII. In Fig. 20, the application of the gain in Case X causes the current THD to increase as the load increases. In contrast, the application of the gain in Case XIII results in a negligible change in current THD with increasing load, maintaining current THD within 5% up to an output of 50 kW. Moreover, Fig. 21 presents the experimental waveforms under 40 kW and 50 kW load conditions with Case X and Case XIII. A comparison of experimental waveforms clearly verifies the improvement in current THD achieved through the application of the gain in Case XIII. Consequently, these results indicate that even if the target current THD is achieved at an intermediate load level, current distortion may occur as the load increases, which can be mitigated by increasing the *d*-axis current gain.

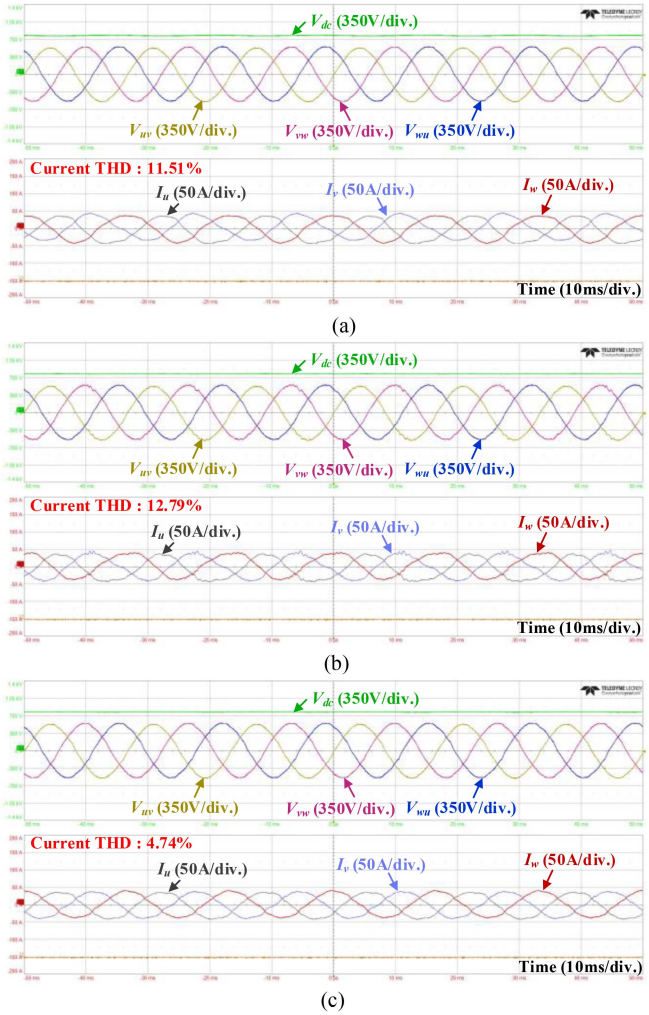


Fig. 19. Experimental waveforms according to gain variation under an 18 kW load condition. (a) Case I. (b) Case VI. (c) Case X.

Finally, the dynamic characteristics are evaluated when applying the final selected Case XIII. The dynamic characteristics exhibit noticeable changes depending on the voltage controller gain. As commonly understood, increasing the voltage controller

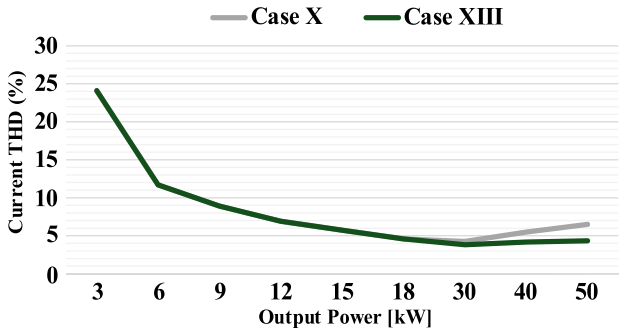


Fig. 20. Experimental waveforms according to gain variation.

gain enhances the response speed. Fig. 22 illustrates the system response characteristics during the transition from no load to an 18 kW load with the application of Case XIII. During this transition, the dc output current increases at a rate of 2 A/μs. The voltage controller is configured with the same PI gains as in the previous experiment, set to 0.1 and 2, respectively. As a result, V_{dc} requires approximately 1.28 s to recover to 800 V immediately after the 18 kW load connection. Considering that typical dc chargers are designed with a maximum charging current slew rate of 20 A/s or higher and a response time within 1 s, this result sufficiently ensures fast transient performance. Consequently, reducing the voltage controller gain only slows the response speed without causing other problems. In contrast, increasing the gain initially enhances the response speed but eventually leads to voltage controller oscillations in the steady state, resulting in current distortion, as shown in Fig. 23.

Based on the experimentally validated waveform variations according to the controller gain, the following gain tuning guidelines are proposed. First, steady-state current imbalance can be mitigated by increasing the q-axis current controller gain, while increasing the d-axis current controller gain helps reduce current distortion. After resolving the current phase imbalance through q-axis current controller gain tuning, the tuned gain remains effective regardless of load variations.

However, for the d-axis current controller gain, it is essential to verify whether current distortion occurs as the load increases. Even with the same gain, an increase in output power may lead to higher input current, which can cause current waveform distortion. This issue can be addressed by further increasing the d-axis current controller gain. Next, for the voltage controller gain, a higher value improves response speed; however, if set excessively high, it may induce current oscillations. Therefore, the voltage controller gain should be gradually increased from a low value to ensure that the target system achieves the desired response speed.

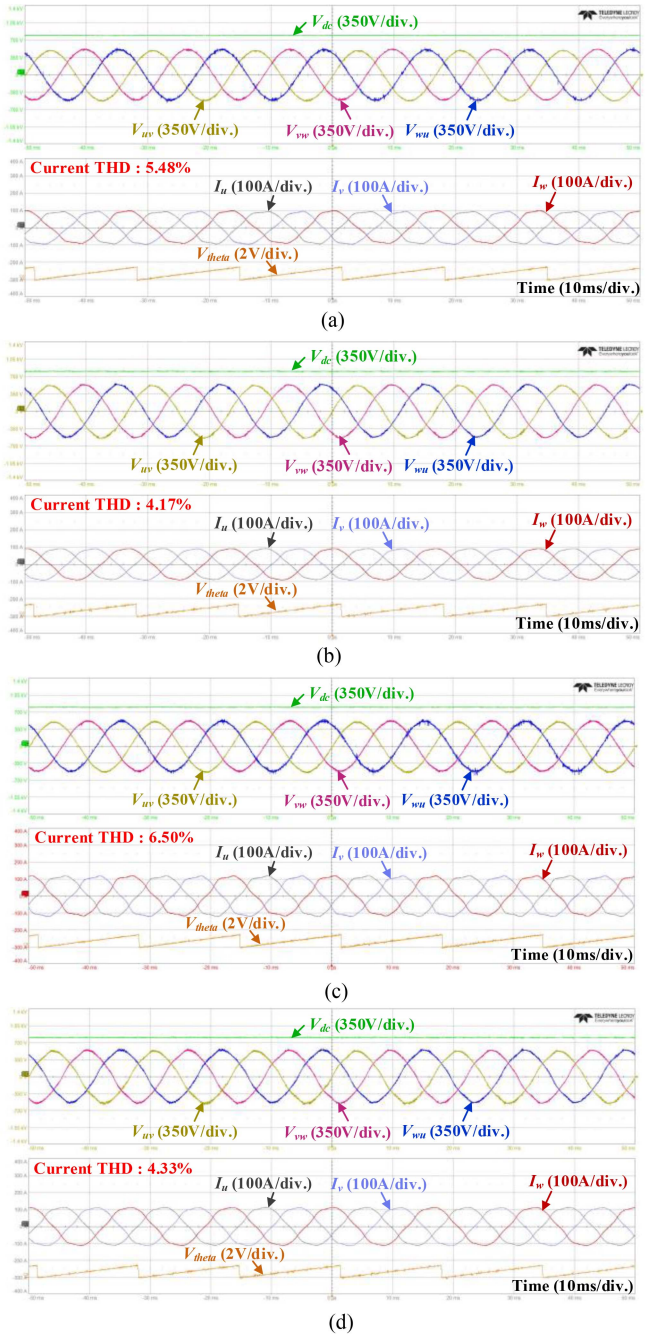


Fig. 21. Experimental waveforms according to gain variation under 40 kW and 50 kW load conditions. (a) Case X under a 40 kW load condition. (b) Case XIII under a 40 kW load condition. (c) Case X under a 50 kW load condition. (d) Case XIII under a 50 kW load condition.

IV. PFC Hardware Implementation Method

Fig. 24 presents the three-phase PFC hardware implemented in this article. The hardware is divided into two layers and follows the configuration shown in Fig. 25. The gate driver board on the upper layer receives PWM signals from the MCU and delivers them to the gates of the SiC MOSFETS on the lower layer via an isolated gate driver circuit. Additionally, Fig. 26 illustrates the PCB layout of the gate driver board and power board corresponding to one leg of the three-phase PFC, with the components used listed in Table VII. In this article, discrete type three-parallel SiC MOSFETS are utilized, so the PWM signal generated from a single gate driver is delivered to three switches. For this reason, the PCB layout from the gate driver circuit to the SiC MOSFETS is configured to achieve symmetry and

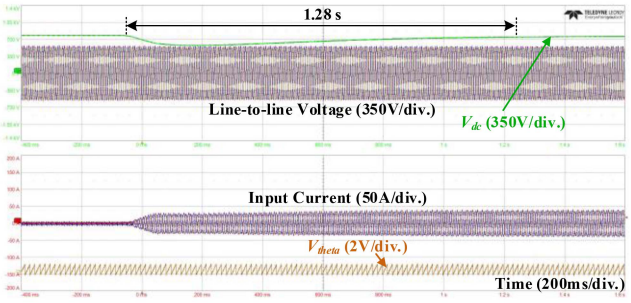


Fig. 22. Transient response characteristics under an 18 kW load connection.

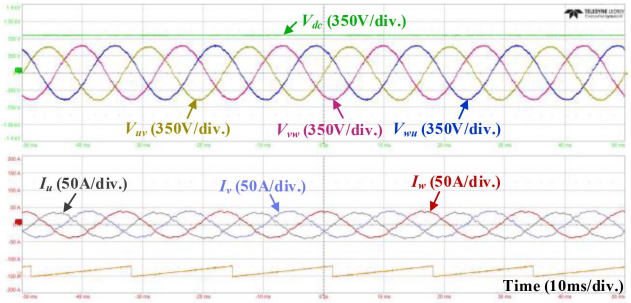


Fig. 23. Experimental waveforms of current distortion caused by the increase in voltage PI gain.

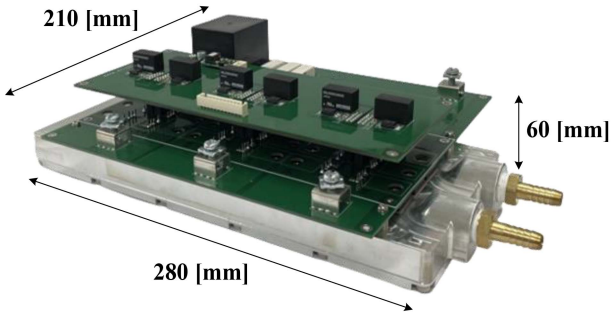


Fig. 24. Hardware implementation of three-leg switching stage in the 50 kW PFC.

TABLE VII
HARDWARE INFORMATION

Component	Model Name	Manufacturer
Isolated dc–dc converter	MGJ2D052005SC	Murata
Gate driver	1ED3123MU12HXUMA1	Infineon
Snubber capacitor	R76QN3100DQ30K	Kemet
SiC MOSFET	MSC025SMA120B4	Microchip Technology

consistency, ensuring similar parasitic effects on each switch. Moreover, as shown in Fig. 26(a), in addition to the gate resistors directly connected to the gate driver output, gate resistors are positioned immediately before the gate of each switch, as shown in Fig. 26(b). With this configuration, switching oscillation is reduced and current distribution is balanced compared to

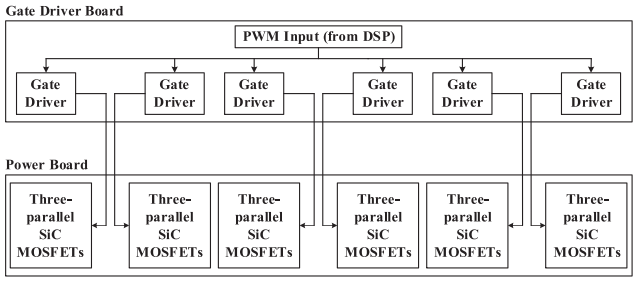
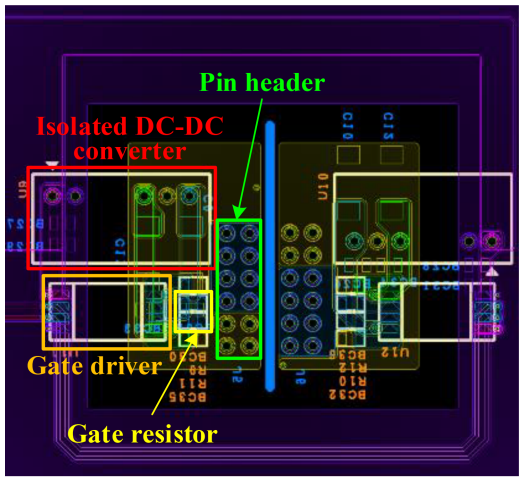
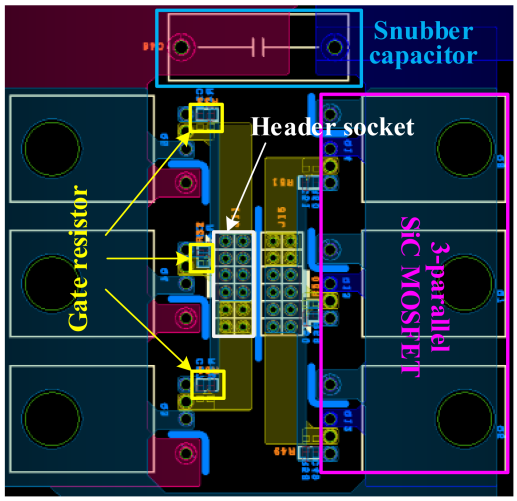


Fig. 25. Hardware configuration of three-leg switching stage.



(a)



(b)

Fig. 26. PCB layout for a single leg of a three-phase PFC. (a) Gate driver board. (b) Power board.

a configuration in which parallel-connected switches share a single gate resistor [34], [35].

Since SiC MOSFETS exhibit significant variations in internal resistance with temperature changes, the temperature of parallel-connected devices should be consistently maintained [29], [30], [31]. When a temperature imbalance occurs, the switch with the lower temperature has reduced internal resistance, leading to current concentration and potential device

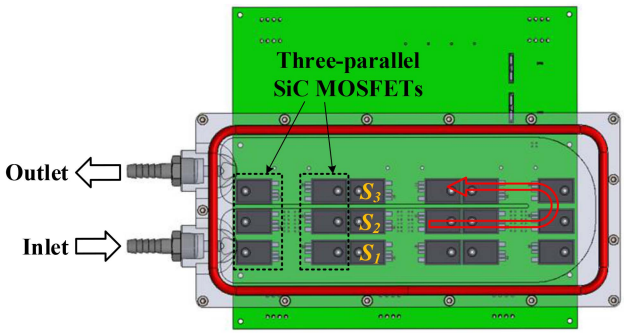


Fig. 27. Thermal dissipation path of three-parallel SiC MOSFETs.

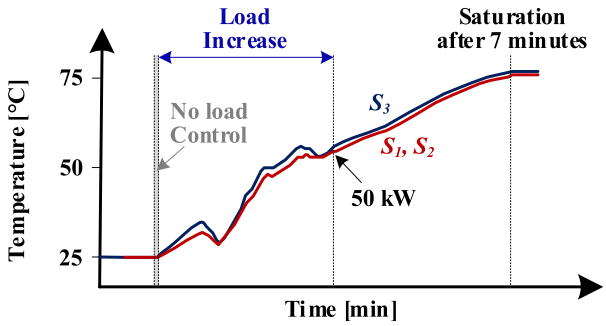


Fig. 28. Temperature measurement results in three-parallel SiC MOSFETs.

failure from exceeding the rated current. Accordingly, this article implements a liquid cooling channel, as shown in Fig. 27, to achieve thermal uniformity in the three-parallel SiC MOSFETs. Since the liquid temperature is relatively lower at the inlet, effective heat dissipation can be achieved. Therefore, two of the three parallel switches are positioned along the liquid inlet path, while the remaining switch is placed along the liquid outlet path. Consequently, as shown in Fig. 28, the temperature difference among the parallel-connected switches remains negligible under all load conditions. Moreover, under a 50 kW load condition, the switch temperature stabilizes at approximately 75 °C after operating for 7 min

$$T_{\text{case}} = T_{\text{coolant}} + P_{\text{loss}}(R_{th(c-h)} + R_{th(h-cl)}) \tag{8}$$

$$T_j = T_{\text{coolant}} + P_{\text{loss}}(R_{th(j-c)} + R_{th(c-h)} + R_{th(h-cl)}). \tag{9}$$

Next, the junction temperature estimation based on the thermal model is used to validate the proposed cooling design and assess its applicability under extreme temperature conditions. Assuming a simplified thermal model, the case temperature can be estimated based on (8). The thermal resistances $R_{th(c\text{-}h)}$ and $R_{th(h\text{-}cl)}$ represent the heat transfer from the case to the heatsink and from the heatsink to the coolant, respectively. While $R_{th(h\text{-}cl)}$ is typically specified in the heatsink datasheet, $R_{\text{th(c-h)}}$ varies between 0.3 and 0.5 °C/W depending on screw tightening torque and the contact condition of the insulating pad. To align with the experimentally measured case temperature of 75 °C, $R_{th(c\text{-}h)}$ is back-calculated. The detailed specifications of the liquid cooling system and thermal model applied in this study are summarized in Table VIII. The junction temperature T_j can be estimated using (9). The junction-to-case thermal resistance $R_{th(j\text{-}c)}$ is referenced from the datasheet of the employed SiC MOSFET. As a result, the junction temperature is estimated to range from a minimum of 84.4 °C to a maximum of 87.2 °C. Therefore, the proposed cooling system ensures that the device operates reliably within its maximum allowable junction temperature. Moreover, these results indicate that the device can operate reliably without exceeding the 175 °C junction temperature limit, even when the coolant temperature increases to around 50–60 °C. Therefore, designers considering operation under more extreme temperature conditions than those in the experimental setup of this article can refer to these results.

TABLE VIII
SPECIFICATIONS OF LIQUID COOLING SYSTEM AND THERMAL MODEL

Parameters	Value	[Unit]
Initial coolant temperature	25	[°C]
Coolant flow rate	1	[L/min]
$R_{th(c\text{-}h)}$	0.45	[°C/W]
$R_{th(h\text{-}cl)}$	0.4	[°C/W]
$R_{th(j\text{-}c)}$	0.2 - 0.26	[°C/W]
$T_{coolant}$	35	[°C]
P_{loss}	47	[W]
Maximum junction temperature	175	[°C]

V. CONCLUSION

This article presents design guidelines for the practical implementation of a 50 kW three-phase PFC converter used in dc fast charging systems. A quantitative analysis of volume, performance, cost, and efficiency for different filter types is conducted to provide selection criteria for designers. Based on the analysis results and tradeoff considerations, this article applies an *LC* filter and achieves a maximum efficiency of 98.65%. Additionally, control strategies based on feedforward compensation are proposed for stable startup, and experimental validation confirms that the initial current is limited to approximately 10 A. Moreover, a detailed analysis of waveform and current THD variations with respect to changes in the controller gain provides gain tuning guidelines. As a result, optimizing the controller gain based on the proposed guidelines ensures that the current THD remains within 5% in the primary operating region. Additionally, the PCB layout design and liquid-cooled heat dissipation structure are discussed for preventing current imbalance and achieving thermal uniformity in three-parallel SiC MOSFETs. Based on the implemented hardware, temperature measurement experiments confirm that the temperatures of the parallel-connected switches remain balanced regardless of load conditions. Consequently, under the maximum output condition, the switch temperature saturates at approximately 75 °C after 7 min of operation.

TABLE IX
DESIGN CONDITIONS OF 22 KW THREE-PHASE PFC

Parameters	Values	[Unit]
Line-to-line voltage V_{LL}	380	[V_{rms}]
Grid frequency f_g	60	[Hz]
Maximum output power, P_o	22	[kW]
Dc link voltage V_{dc}	700 – 800	[V]
Switching frequency f_{sw}	40	[kHz]
Current THD	< 5%	-
Maximum input current ripple $\Delta I_{in,max}$	10	[A]

TABLE X
DESIGN PARAMETERS OF *LC* FILTER

Parameters	Volume [cm^3]	Turns	Core material	Inductance [μH] / Capacitance [μF]
L	97	20	High flux	320
C	19	-	-	4.8

TABLE XI
HARDWARE INFORMATION

Component	Model Name	Manufacturer
Isolated dc–dc converter	MGJ2D052005SC	Murata
Gate driver	1ED3123MU12HXUMA1	Infineon
Snubber capacitor	PPB2103100KHL	Nichicon
SiC MOSFET	AIMW120R035M1H	Infineon

APPENDIX A
IMPLEMENTATION AND VALIDATION OF 22 KW THREE-PHASE PFC

In this section, a three-phase PFC is designed based on the proposed design guideline to satisfy the specifications listed in Table IX, and its performance is experimentally validated through hardware implementation. The results verify the effectiveness of the proposed guideline and further demonstrate its applicability at relatively low power levels regardless of the system capacity.

A. LC Filter Design

The design values of the *LC* filter obtained from (1) and (2), along with the hardware implementation results, are summarized in Table X. $\Delta I_{\mathrm{in,max}}$ is set to 10 A, which corresponds to 20% of $I_{\mathrm{in,max}}$, and f_c is selected as 1/10 of f_{sw}. In addition, the filter inductor is implemented using the same method described in Section II-B.

B. Hardware Implementation

The components used for the hardware implementation of the 22 kW three-phase PFC are listed in Table XI, and the corresponding results are presented in Fig. 29. Considering the current rating and efficiency, two discrete-type SiC MOSFETS are connected in parallel. The PCB layout for this configuration is implemented using the same method described in Section III, as shown in Fig. 30. However, since the current rating of the

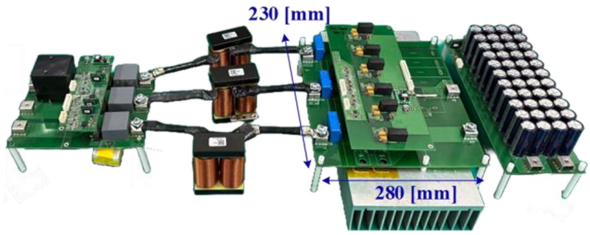
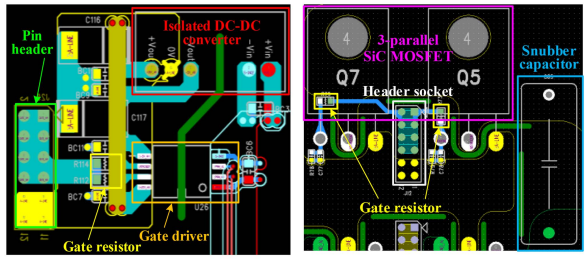


Fig. 29. Hardware implementation of 22 kW three-phase PFC.



(a) (b)

Fig. 30. PCB layout of three-phase PFC. (a) Gate driver board. (b) Power board.

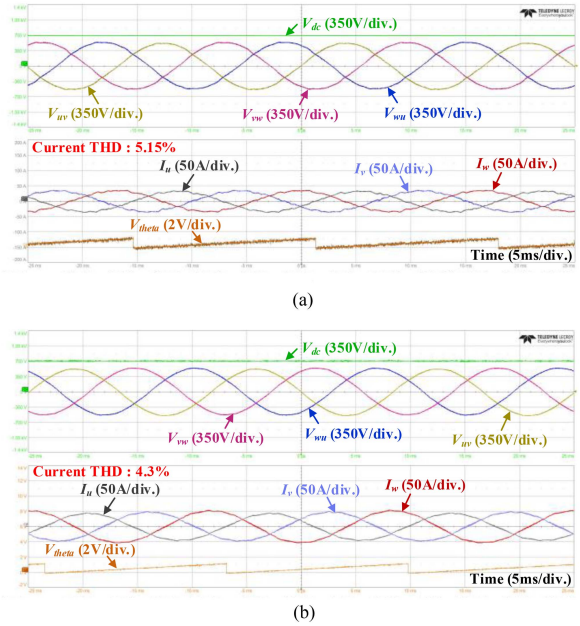


Fig. 31. Experimental waveforms at 15 kW and 22 kW under an output voltage of 700 V. (a) 15 kW. (b) 22 kW.

TABLE XII
PERFORMANCE COMPARISON OF STARTUP CONTROL

Parameters	[19], [20]	[21]	[24]	This paper	[Unit]
Line-to-line voltage	170	380	164	380	[V]
Output voltage	400	270	400	800	[V]
Line frequency	45 – 65	47 – 63	400	60	[Hz]
Initial current at startup	6	-	10	10	[A]
Startup time	60	184	3	30	[ms]

TABLE XIII
SPECIFICATION AND PERFORMANCE COMPARISON WITH EXISTING STUDIES

Parameters	[24]	[36]	[37]	[38]	[39]	[40]	[41]	[42]	[43]	[44]	[45]	This paper		[Unit]
Line-to-line voltage	400	210	200-480	480	200	400 – 480	380	400	380	400	110	380	380	[V]
Dc link voltage	650	400	400-800	800	360	750	550	650	700	200	270	800	700-800	[V]
Output power	6	2.2	5	25	4	12	10	50	50	1.6	2	50	22	[kW]
Damping method	-	-	-	Passive	-	-	-	Active	Active	Active	-	Passive		-
Filter types	*L*	*L*	*L*	*LCL*	*L*	*L*	*L*	*LCL*	*LCL*	*LCL*	Interleaved *LC*	*LC*		-
THD at full load	-	4.3%	4–25%	3.85%	-	3.5%	2.5%	2.67% (Simulated)	1.45% (Simulated)	4.52%	2.52%	4.9%	3.3–4.3%	-
Switching frequency	100	100	50	300	120	150	20	20	5	12	50	25	40	[kHz]
Switching device	Discrete SiC	Discrete SiC	SiC module	Discrete SiC	-	Discrete SiC	Discrete SiC	Discrete IGBT	Discrete IGBT	IGBT module	Discrete SiC	Three-parallel	Two-parallel	-
Peak efficiency	-	-	-	98.9% (@ 20kW)	-	98.85%	99.2% (@ 5kW)	-	-	-	96.3%	98.65% (@ 12lW)	98.75% (@ 12kW)	-
Efficiency at full load	-	-	97.8% (@ 400V)	98.7%	-		99.0%	-	-	-		97.1%	98.45% (@ 700V)	-
Cooling method	-	-	Forced-air cooling	Forced-air cooling	-	Forced-air cooling	-	-	-	Forced-air cooling	Forced-air cooling	Liquid cooling	Forced-air cooling	-

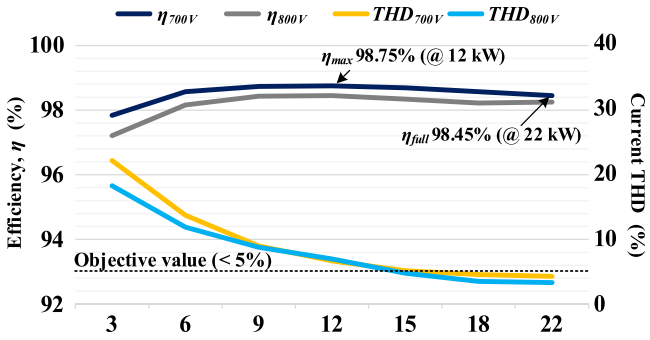


Fig. 32. Experimental results of efficiency and current THD.

22 kW system is approximately 50% lower than that of the 50 kW system designed in the main text, forced-air cooling is employed instead of liquid cooling, while still ensuring adequate thermal management.

C. Experimental Validation

Fig. 31 shows the steady-state waveforms of the designed PFC under the main operating conditions at load levels of 15 kW and 22 kW under an output voltage of 700 V. The controller is implemented based on the design method described in Section IV, and the gain parameters are also selected according to the proposed guideline. Fig. 32 presents the measured current THD and efficiency of the implemented 22 kW PFC under various load conditions. The system maintains a current THD below 5% within the main operating range and achieves a maximum efficiency of 98.75% at 12 kW, as well as a full-load efficiency of 98.45% at 22 kW.

APPENDIX B
SPECIFICATION AND PERFORMANCE COMPARISON

In Table XII, the startup performance of the proposed method is compared with that of existing studies. The results confirm that the proposed method achieves fast startup time and low initial current, even under the highest output voltage condition. In addition, Table XIII summarizes the comparison of specifications and performance between existing studies and the 50 kW and 22 kW three-phase PFCs designed in this article. The results confirm that the three-phase PFC converters developed based on the proposed design guidelines achieve competitive performance compared to previously published high-performance works. Notably, the 50 kW PFC designed in this study features the highest output power rating among the existing studies. To support this power level, a three-parallel discrete-type SiC MOSFET configuration and liquid cooling are employed. These results demonstrate the effectiveness of the proposed design guidelines and provide valuable reference for designers aiming to implement high-power systems.

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