Dual Synchronous Rotating Frame-Based Power Allocation Control of Single-Stage Multiport Inverter in Islanded Microgrids

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***Abstract*—The single-stage multiport inverter (SSMPI) is a promising configuration for islanded microgrids, eliminating the need for an intermediate dc–dc converter. However, existing control schemes are always executed under mixed reference frames, where the grid-forming control on the ac side is implemented in the rotating frame, and the power allocation control on the dc side is implemented in the stationary frame. This coupled feature, operating under the mixed reference frame, leads to excessive port power ripple and poor dynamic performance. Given this, this article proposes a dual synchronous rotating frame (DSRF)-based power allocation control strategy that achieves low port power ripple and fast dynamic response, where the control objectives on both the ac side and dc side are realized on the rotating frame. In the proposed DSRF-based strategy, the SSMPI is decoupled into dual subinverters, with each subinverter managed independently in a synchronous rotating frame. The sum of the d-axis and q-axis components for the subinverters is used for grid-forming control on the ac side, and the magnitude of d-axis and q-axis components of the subinverter is employed for power allocation control on the dc side. The range for power allocation capability of the SSMPI with the proposed DSRF-based strategy is also analyzed. Experimental results show that the port power ripple can be reduced by approximately 11.69%, and the dynamic response is significantly improved with the proposed DSRF-based strategy.**

***Index Terms*—Dual synchronous rotating frame (DSRF), microgrid, power allocation, single-stage multiport inverter (SSMPI).**

I. Introduction

In recent years, microgrids have played a crucial role in facilitating the high penetration of distributed generation resources due to their autonomous capability, smaller scales, and reliability, especially their flexible access to distributed energy sources [1], [2], [3], [4]. Among them, the islanded microgrids integrating hybrid energy sources, such as renewable energy sources (RESs) and energy storage systems (ESSs) [5], have attracted increasing attention as energy density and power density improve and smoothing power fluctuations [6], [7].

In the islanded microgrids with RESs/ESSs, power electronic converters are essential since they determine the size/weight, power/energy density, and efficiency of these systems [8]. Up to now, numerous power electronic converter topologies integrated with RESs/ESSs in the islanded microgrids are reported [9], [10]. However, these power electronic converter topologies integrated with RESs/ESSs need one [11], [12] or more extra dc–dc converters [13], such as fully active type in Fig. 1(a), semiactive type I in Fig. 1(b), and semiactive type II in Fig. 1(c). To increase power density and reduce additional costs, the single-stage multiport inverter (SSMPI), as shown in Fig. 1(d), has drawn increasing attention by enabling direct RESs/ESSs connection to ac microgrids without bulky dc–dc converters [14], [15], [16], [17], [18]. Consequently, SSMPI offers advantages of reduced cost, power loss, and component stress compared to other topologies [19], [20], [21], [22]. Despite these advantages,

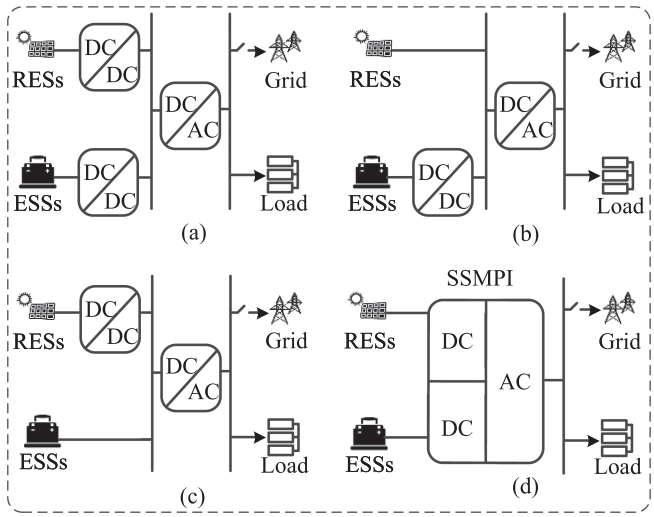

Fig. 1. Power electronic interfaces for integrating multiple sources in island microgrids. (a) Fully active type. (b) Semiactive type I. (c) Semiactive type II. (d) Single-stage multiport inverter.

Received 20 March 2025; revised 24 July 2025; accepted 25 August 2025. Date of publication 28 August 2025; date of current version 22 October 2025. This work was supported in part by the National Natural Science Foundation of China under Grant 62173067, in part by Guangdong Basic and Applied Basic Research Foundation under Grant 2024A1515010184 and Grant 2023A1515240060, in part by Guangdong Science and Technology Program under Grant 2021QN02L854, and in part by Shenzhen Science and Technology Program under Grant JCYJ20220530165001003 and Grant JCYJ20230807120006012. Recommended for publication by Associate Editor G.-S. Seo. *(Corresponding author: Dehong Zhou.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3603997.

Digital Object Identifier 10.1109/TPEL.2025.3603997

its control scheme is challenging because grid-forming control on the ac side and power allocation control on the dc side should be achieved simultaneously [23], [24].

To simultaneously achieve grid-forming control on the ac side and power allocation control on the dc side, several modulation-based strategies have been widely explored. Carrier-based discontinuous pulse width modulation strategies achieved dc-side power control by injecting zero-sequence components into modulation signals [25]. Alternatively, space vector modulation (SVM)-based strategies leveraged redundant vectors [26], [27] or zero vectors [28] to allocate dc-side power. In addition, a modified SVM method was reported in [29], where a novel virtual voltage vector was constructed to explicitly account for dc port voltage variations and regulate small voltage vectors. Although these modulation strategies effectively achieve simultaneous grid-forming and power allocation control, they suffer from cumbersome computational demands because power allocation control is indirectly regulated by adjusting the redundant voltage vector or the zero-sequence component.

Apart from modulation-based strategies, some control-based strategies have been investigated for grid-forming control and power allocation control as multiobjective control issues. Based on the mathematical models of the SSMPI, a direct duty cycle control-based strategy was conducted in [30] to simultaneously achieve power control and ac voltage control. In [31], a model predictive control strategy was developed for the NPC inverter, capable of sustaining motor drive performance even in the presence of imbalanced dc ports. A finite-control-set model predictive control strategy with flexible power allocation was investigated for the SSMPI system in [32]. Additionally, an iterative learning-based strategy was reported in [33], and ripple-free port power regulation was achieved. Although those control strategies achieved multiobjective for SSMPI effectively, they suffer from excessive port power ripple and poor dynamic response as they are executed under mixed reference frames, i.e., the grid-forming control on the ac side is with the rotating frame, while power allocation control on the dc side is with the stationary frame.

In view of this, this article proposes a dual synchronous rotating frame (DSRF)-based power allocation control strategy to achieve grid-forming control on the ac side and power allocation control on the dc side under the unified synchronous frame. In the proposed DSRF-based strategy, the SSMPI is decoupled into dual subinverters, with each subinverter managed independently in a synchronous rotating frame. The sum of the d-axis and q-axis components of the subinverter is used to synthesize the voltage reference for grid-forming control on the ac side, and the magnitudes of the d-axis and q-axis components are used to achieve power allocation control on the dc side. With the proposed DSRF, reduced port power ripple and a fast dynamic response are achieved because the power allocation is linearly and intuitively calculated in DSRF. Finally, the power allocation range between two dc ports is also analyzed in detail.

The rest of this article is organized as follows. Section II presents the configuration of SSMPI and the decoupled power model. Section III illustrates the proposed DSRF-based power allocation control strategy. The experiment results are presented in Section IV. Finally, Section V concludes this article.

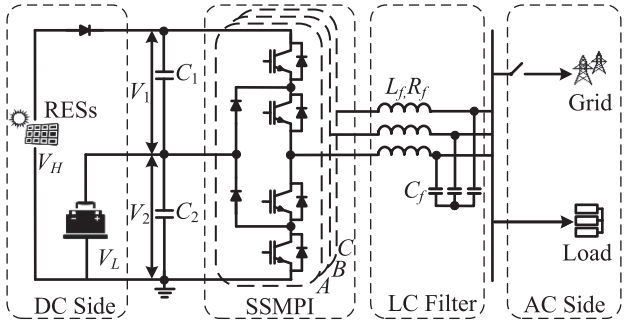

Fig. 2. Configuration of the SSMPI.

TABLE I
SWITCHING STATES AND OUTPUT VOLTAGE FOR SSMPI

Gating signals (S_{x1}, S_{x2})	Switch state S_x	Output voltage v_{xN}
(1,1)	h	V_H
(0,1)	l	V_L
(0,0)	0	0

II. MATHEMATICAL MODEL OF SSMPI CONFIGURATION

This section introduces the SSMPI configuration first. Then, the decoupled power model is presented in detail.

A. Configuration of SSMPI

The typical SSMPI configuration is depicted in Fig. 2, which is transplanted from the three-level neutral-point-clamped (3L-NPC) inverter. On the dc side, the upper dc port is connected to the unidirectional RES source, such as the PV unit, while the lower dc port is connected to the ESS source, such as the battery. In this configuration, two sources are directly connected to the insulated-gate bipolar transistor (IGBT) and diodes. The output voltages of the upper and the lower dc ports are V_H and V_L, respectively. Capacitance C_1 and C_2 on the dc side serve to stabilize the dc voltage and store or release energy, with their voltage marks as V_1 and V_2, respectively. An obvious issue of this configuration is the dc port voltage imbalance between the upper and lower dc ports due to variations in the PV environment or climate and the state of charge (SoC) of the battery.

In the SSMPI, each phase consists of four active switches, named $S_{x1}, S_{x2}, \overline{S}_{x1}, \overline{S}_{x2}, (x \in a, b, c)$, where $\overline{S}_{x1}$ and $\overline{S}_{x2}$ are complementary switching states of S_{x1} and S_{x2}, respectively. When S_{x1} and S_{x2} are turned ON, the PV unit supplies power to the ac side, and the phase output voltage is V_H. When $\overline{S}_{x1}$ and S_{x2} are turned ON, the battery delivers power to the ac side, and the phase output voltage becomes V_L. When both $\overline{S}_{x1}$ and $\overline{S}_{x2}$ are turned ON, no power is supplied, resulting in a phase output voltage of zero. Table I summarizes the corresponding switching states S_x and phase output voltages v_{xN} of the SSMPI.

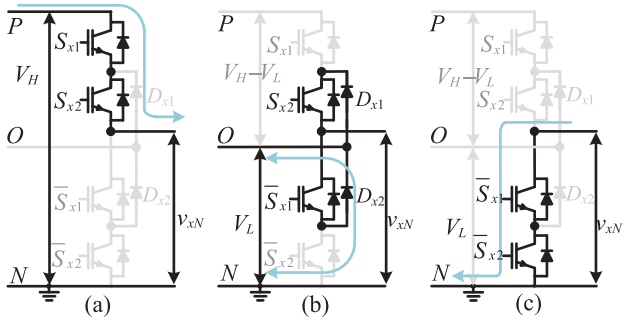

Fig. 3. Current paths of SSMPI. (a) $S_x = h$. (b) $S_x = l$. (c) $S_x = 0$.

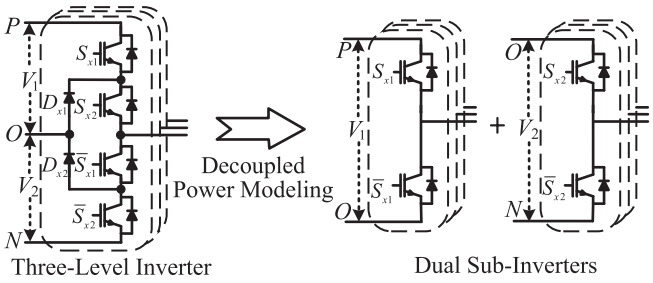

Fig. 4. Decoupled power modeling for SSMPI.

B. Decoupled Power Modeling for SSMPI

The SSMPI can be regarded as an integrated inverter formed by dual two-level voltage-source inverters with a shared ac output [34]. The feature of sharing ac output provides the SSMPI with the advanced merit of single-stage power conversion, eliminating the need for dc–dc converters. However, it also brings challenges in the controller design because the two-level voltage-source inverters are not independent, and the gating signals of (S_{x1}, S_{x2}) are not allowed to be equal to (1,0) because the current path is uncontrollable at this switching state.

In this article, the configuration of SSMPI is decoupled into dual subinverters (subinverter I and subinverter II), as shown in Fig. 4, thereby simplifying the control design procedure. In subinverter I, the PV supplies the load when S_{x1} is ON, and the equivalent dc port voltage of subinverter I is V_1, which equals $V_H - V_L$. In subinverter II, the battery supplies the load when S_{x2} is ON, and the equivalent dc port voltage of inverter II is V_2, which equals V_L. Since the sum of active power generated from dual subinverters should be equal to that of the upper and lower ports, the following can be derived:

$$P_H + P_L = P_1 + P_2 \tag{1}$$

where P_H/P_L is the power of upper/lower dc port and P_1/P_2 is the power of dual subinverter I/II.

As S_{x1} directly connects to the upper dc port, the power of the upper dc port P_H can be calculated in the decoupled dual subinverters as follows:

$$P_H = \frac{V_1 + V_2}{V_1} P_1. \tag{2}$$

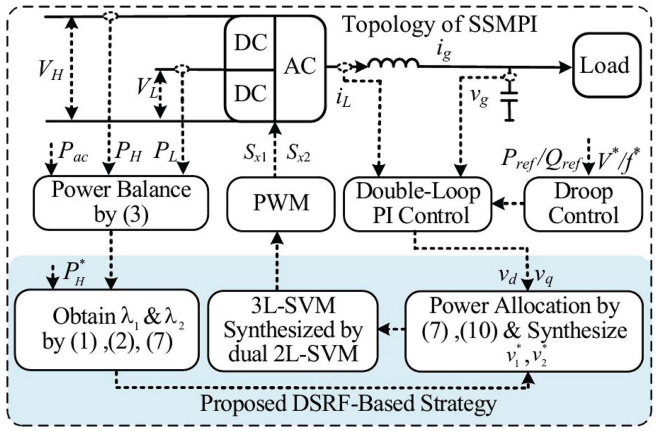

Fig. 5. Control diagram for the DSRF-based strategy.

Based on decoupled dual subinverters, the power of each subinverter is managed independently in a synchronous rotating frame. The detailed analysis will be presented in Section III.

III. Proposed Dual Synchronous Rotating Frame-Based Power Allocation Control Strategy

The proposed DSRF-based power allocation control strategy is shown in Fig. 5. The SSMPI is operated in an island microgrid mode. In this study, the double loop proportional-integral (PI) control is adopted to track rated grid voltage/frequency V^*/f^*. This method has been widely adopted in microgrid applications, and a detailed block diagram can be found in [8].

The proposed DSRF-based power allocation control strategy for the SSMPI consists of four parts: flexible power allocation control based on DSRF, grid-forming control under DSRF, modulation scheme for SSMPI under DSRF, and power allocation capability analysis. The detailed implementation process of each part is shown in the following text.

A. Flexible Power Allocation Control Based on DSRF

In the SSMPI configuration, according to the active power balance principle for SSMPI on the two dc ports and the power demanded P_{ac} on the ac side, this is demonstrated in

$$P_{ac} = P_H + P_L. \tag{3}$$

For SSMPI, P_{ac} can be calculated in the synchronous rotating frame in [35] as follows:

$$P_{ac} = \frac{3}{2}(v_d i_d + v_q i_q) \tag{4}$$

where i_d and i_q is output current i_g while v_d and v_q is reference voltage in synchronous rotating frame.

Similarly to (4), the power of subinverter I and subinverter II can be calculated in the synchronous rotating frame by

$$\begin{cases} P_1 = \frac{3}{2}(v_{d1} i_d + v_{q1} i_q) \\ P_2 = \frac{3}{2}(v_{d2} i_d + v_{q2} i_q) \end{cases} \tag{5}$$

where v_{d1}, v_{q1}, v_{d2}, and v_{q2} are voltages for the subinverters I and II, respectively.

According to (1), (3), (4), and (5), the relationship between v_d, v_{d1}, v_{d2} and v_q, v_{q1}, v_{q2} can be expressed as follows:

$$\begin{cases} v_d = v_{d1} + v_{d2} \\ v_q = v_{q1} + v_{q2}. \end{cases} \tag{6}$$

As the current is shared between SSMPI and dual subinverters, the power allocation can be diverted to regulate the voltage for dual subinverters according to (6). To achieve the flexible power allocation control on the dc side, two proportional factors, λ_1 and λ_2, are used to regulate the power of the decoupled dual subinverters as follows:

$$\begin{cases} P_1 = \lambda_1 P_{ac} \\ P_2 = \lambda_2 P_{ac}. \end{cases} \tag{7}$$

According to (1), (3), and (7), the limitation for λ_1 and λ_2 should be satisfied

$$\lambda_1 + \lambda_2 = 1. \tag{8}$$

Thus, the voltage for SSMPI and dual subinverters can be regulated as follows:

$$\begin{cases} v_{d1} + v_{q1} = \lambda_1 (v_d + v_q) \\ v_{d2} + v_{q2} = \lambda_2 (v_d + v_q). \end{cases} \tag{9}$$

By combining (2), (5), and (7), the relationship between P_H and λ_1 can be established as follows:

$$P_H = \frac{3}{2}\lambda_1 \xi (v_d i_d + v_q i_q) = \frac{3}{2}\lambda_1 \xi P_{ac} \tag{10}$$

where ξ is equal to $\frac{V_1+V_2}{V_1}$.

From the above analysis, when the reference power of the upper dc port P_H^* is given, the corresponding λ_1 can be obtained as P_{ac}, and ξ are parameters for SSMPI. The power of the lower dc port, P_L, can also be obtained by (3).

B. Grid-Forming Control Under DSRF

Regarding the grid-forming on the ac side, the reference voltage is generated by the d-axis and q-axis components of the dual subinverters. When λ_1 is achieved in (10), the corresponding v_{d1} and v_{q1} obtained as well based on (9). As specified in (6), v_{d1}, v_{q1} synthesize reference voltage v_1^* and v_{d2}, v_{q2} similarly generate reference voltage v_2^* by

$$\begin{cases} v_1^* = v_{d1} + j v_{q1} \\ v_2^* = v_{d2} + j v_{q2} \end{cases} \tag{11}$$

where the j represents imaginary units, means the q-axis lags behind the d-axis by 90°.

By combining (6) and (11), the reference voltage v^* for the SSMPI can be calculated as

$$v^* = v_1^* + v_2^*. \tag{12}$$

As indicated in (12), once the voltage references for the dual subinverters are obtained, the voltage reference v^* for grid-forming control can be synthesized. The synthesis process of v^* in the rotating reference frame is illustrated in Fig. 6.

In SSMPI, four power flow modes are considered as shown in Fig. 7. The lower dc port separately provides power for the ac side (mode I). The upper and lower dc ports are provided simultaneously for the ac side (mode II), and the upper dc port provides power separately for the ac side (mode III). The upper dc port provides power for the ac side, and the lower dc port absorbs power (mode IV). The four modes can be expressed as follows:

$$\begin{cases} P_H = 0, P_L = P_{ac} & |v_1^*| = 0, v_2^* = v^* \\ P_H < P_{ac}, P_L < P_{ac} & |v_1^*| < |v^*|, |v_2^*| < |v^*| \\ P_L = 0, P_H = P_{ac} & |v_2^*| = 0, v_1^* = v^* \\ P_H > P_{ac}, P_L < P_{ac} & |v_1^*| > |v^*|, v_2^* \cdot v^* < 0. \end{cases} \tag{13}$$

C. Modulation Scheme for SSMPI Under DSRF

In this part, the traditional modulation scheme in 3L-NPC cannot be applied to SSMPI directly as the voltage of the dc port is imbalanced, which can easily have switching dead zones. To solve this issue, dual separate two-level SVM (2L-SVM) is synthesized as a three-level SVM (3L-SVM) based on the decoupled power model in the proposed DSRF-based strategy.

The process of dual 2L-SVM synthesizing to 3L-SVM is depicted in Fig. 8. The gating signals of S_{x1} and S_{x2} are generated separately by v_1^* and v_2^*. However, the gating signals of (S_{x1}, S_{x2}) are constrained to be equal to (1,0) for the current path being uncontrollable in this switching state. To avoid the switching state of (1,0), d_{x1}/d_{x2}, the duty cycles for S_{x1}/S_{x2} should satisfied the constraint of $d_{x1} \le d_{x2}$. In this article, the duration time of zero vector (111) for subinverter I is minimized, while that for subinverter II is maximized to meet the constraint. In other words, only the zero vector (111) is employed for vector

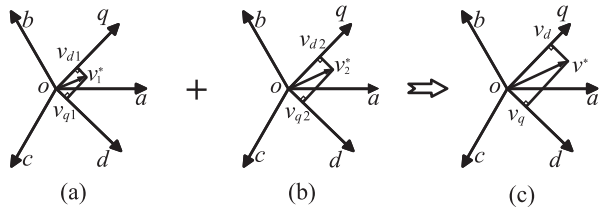

Fig. 6. Synthesis process for v^* in synchronous rotating frame. (a) Reference voltage for subinverter I. (b) Reference voltage for subinverter II. (c) Reference voltage for SSMPI.

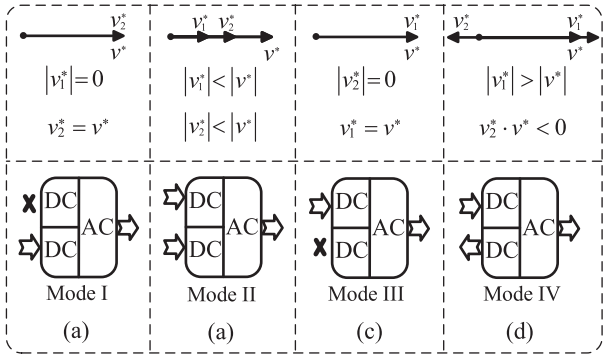

Fig. 7. Four power modes for SSMPI. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV.

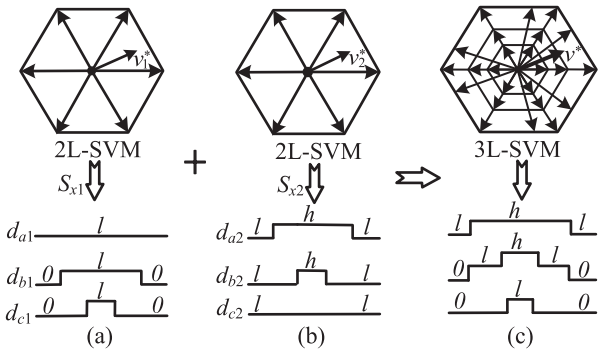

Fig. 8. Process of dual 2L-SVM synthesizing to 3L-SVM. (a) 2L-SVM for subinverter I. (b) 2L-SVM for subinverter II. (c) 3L-SVM for SSMPI.

synthesis in subinverter II, while only the zero vector (000) is employed for vector synthesis in subinverter I.

Taking sector I as an example, the desired voltage vectors of v_1^* and v_2^* are synthesized synchronously by active voltage vectors (100) and (110). The duration time for the subinverter I can be calculated as

$$\begin{cases} d_{a1} = T_1' + T_2' \\ d_{b1} = T_2' \\ d_{c1} = 0 \end{cases} \tag{14}$$

where T_1' and T_2' are the duration time for (100) and (110) of subinverter I, respectively. $d_{x1} \in [0, T_s]$, $x \in a, b, c$. The duration time for subinverter II can be calculated as

$$\begin{cases} d_{a2} = T_1'' + T_2'' + T_0'' \\ d_{b2} = T_2'' + T_0'' \\ d_{c2} = T_0'' \end{cases} \tag{15}$$

where T_1'' and T_2'' are the duration time for (100) and (110) of subinverter II, respectively. $T_0'' = T_s - T_1'' - T_2'' > 0$. $d_{x2} \in [0, T_s]$, $x \in a, b, c$. According to (14) and (15), it is obvious that $d_{a2} \geq d_{a1}$, $d_{b2} \geq d_{b1}$, and $d_{c2} \geq d_{c1}$. In this way, the constraint of $d_{x1} \leq d_{x2}$ is satisfied.

Flowchart of the proposed DSRF-based strategy is included in Fig. 9. In this proposed DSRF-based strategy, v_d and v_q are decomposed linearly for the dual subinverters by λ_1 and λ_2.

D. Power Allocation Capability Analysis

For SSMPI, complex power requirements are needed to adapt to different power modes. Given this, this part discusses the power allocation capability η, which is defined

$$\eta = \frac{P_H}{P_{ac}}. \tag{16}$$

According to (2), (4), and (5), η can be rewritten by

$$\eta = \xi \frac{(v_{d1} i_d + v_{q1} i_q)}{(v_d i_d + v_q i_q)}. \tag{17}$$

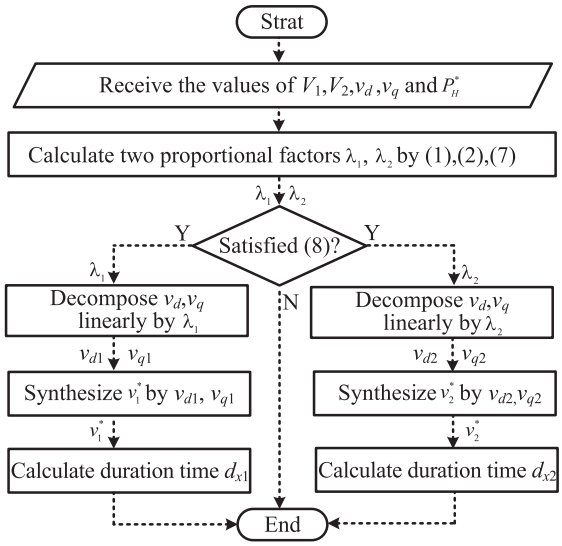

Fig. 9. Flowchart of the proposed DSRF-based strategy.

To avoid the over-modulation problem for the dual subinverters and SSMPI, v_d, v_{d1}, and v_{d2} should satisfy the following:

$$\begin{cases} 0 \leq |v_{d1}| \leq \frac{V_1}{\sqrt{3}} \\ 0 \leq |v_{d2}| \leq \frac{V_2}{\sqrt{3}} \\ 0 \leq |v_d| \leq \frac{V_1 + V_2}{\sqrt{3}}. \end{cases} \tag{18}$$

The lower border of η can be achieved in two cases as follows: in the case of $|v_{d2}|_{\max} = \frac{V_2}{\sqrt{3}} \geq |v_d|$, that means $|v_d|$ is within the output capability of the low voltage port. In this case, the following should be met:

$$\begin{cases} v_{d2} = v_d \\ v_{d1} = 0 \end{cases} \tag{19}$$

η can be obtained as

$$\eta = \xi \frac{v_{q1} i_q}{v_d i_d + v_q i_q}. \tag{20}$$

When $|v_{d2}|_{\max} = \frac{V_2}{\sqrt{3}} \leq |v_d|$, that means $|v_d|$ is beyond the output capability of the lower dc port. In this case, the following can be obtained:

$$\begin{cases} v_{d1} = |v_d| - \frac{V_2}{\sqrt{3}} \\ v_{d2} = |v_{d2}|_{\max} = \frac{V_2}{\sqrt{3}}. \end{cases} \tag{21}$$

In this case, η can be obtained as

$$\eta = \xi \frac{\sqrt{3}(v_d i_d + v_{q1} i_q) - V_2 i_d}{\sqrt{3}(v_d i_d + v_q i_q)}. \tag{22}$$

The upper border of η can be achieved in the following two cases: in the case of $|v_{d1}|_{\max} = \frac{V_1}{\sqrt{3}} \geq |v_d|$, that means $|v_d|$ is within the output capability of the high voltage port, and the following should be satisfied:

$$\begin{cases} v_{d1} = |v_d| \\ v_{d2} = 0. \end{cases} \tag{23}$$

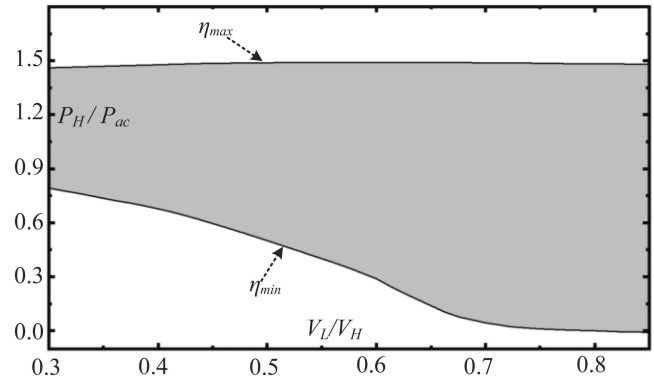

Fig. 10. Range of P_H/P_{ac} under different V_L/V_H ratio.

In this case, the upper border of η is given as

$$\eta = \xi \frac{(v_d i_d + v_{q1} i_q)}{(v_d i_d + v_q i_q)}. \tag{24}$$

In the case of $|v_{d1}|_{\max} = \frac{V_1}{\sqrt{3}} \le |v_d|$, v_d is beyond the output capability of the upper dc port, the following should be satisfied:

$$\begin{cases} v_{d1} = |v_{d1}|_{\max} = \frac{V_1}{\sqrt{3}} \\ v_{d2} = |v_d| - \frac{V_1}{\sqrt{3}}. \end{cases} \tag{25}$$

In this case, the upper border of η can be obtained as

$$\eta = \xi \frac{(V_1 i_d + \sqrt{3} v_{q1} i_q)}{\sqrt{3}(v_d i_d + v_q i_q)}. \tag{26}$$

Combining (20), (22), (24), and (26), the theoretical power allocation range can be calculated as

$$\left\{ \xi \frac{v_{q1} i_q}{v_d i_d + v_q i_q}, \xi \frac{\sqrt{3}(v_d i_d + v_{q1} i_q) - V_2 i_d}{\sqrt{3}(v_d i_d + v_q i_q)} \right\}_{\max} \le \eta \le \left\{ \xi \frac{(V_1 i_d + \sqrt{3} v_{q1} i_q)}{\sqrt{3}(v_d i_d + v_q i_q)}, \xi \frac{v_d i_d + v_{q1} i_q}{v_d i_d + v_q i_q} \right\}_{\min}. \tag{27}$$

In this article, the q-axis component is neglected as only active power is discussed, (27) can be rewritten as

$$\left\{ 0, \xi \frac{\sqrt{3} v_d - V_2}{\sqrt{3} v_d} \right\}_{\max} \le \eta \le \left\{ \xi \frac{V_1}{\sqrt{3} v_d}, \xi \right\}_{\min}. \tag{28}$$

According to (28), the power allocation of SSMPI is depicted in Fig. 10 with the modulation index equal to 0.78. From Fig. 10, when the voltage ratio V_L/V_H is set to a higher value, the lower border of power allocation capability can be equal to 0, meaning that the lower dc port can provide the load power solely without using the upper dc port.

IV. Experimental Results and Discussion

As shown in Fig. 11, the experimental setup is built to verify the effectiveness of the proposed DSRF-based strategy for SSMPI. The main experimental parameters are listed in Table II. Meanwhile, the dc side input voltages are generated by two programmable dc sources, where the lower dc source is bidirectional. A LC filter is applied to improve voltage/current quality on the ac side. The sampling frequency is set to 10 kHz, and PWM generation and analog-to-digital conversion are realized by FPGA. The SSMPI is implemented by IGBTs, and the switching frequency is also set to 10 kHz. An eight-channel oscilloscope is adopted to capture experimental variables.

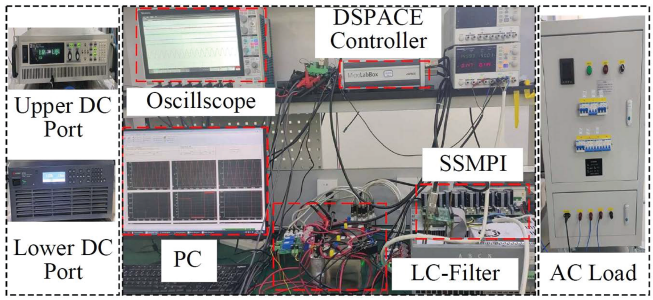

Fig. 11. Experimental setup for SSMPI.

TABLE II
Main Experimental Parameters of the Test System

Parameters	Value
HV dc port voltage	v_h = 400 V
LV dc port voltage	v_l = 160-240 V
DC side capacitance	$C_1 = C_2$ = 4920 μF
LC filter inductance	R_f/L_f = 3mH/0.4 Ω
LC filter capacitance	C_f = 10 μF
Sample time/frequency	T_s = 100μs/f_s = 10 kHz
Rated ac voltage	V_g^* = 110 V
Rated ac frequency	f_g^* = 50 Hz
Reference ac active power	P_{ac}^* = 1000 W
Reference ac reactive power	Q_{ac}^* = 0 var

A. Steady-State Performance

The effectiveness of the proposed DSRF-based power allocation control for the SSMPI is first evaluated through steady-state tests.

1) Steady-State Performance Under Imbalanced Port Voltage: To account for dc source voltage variation in practical scenarios, the proposed strategy is initially evaluated under varying voltage ratios. The steady-state performance of the proposed DSRF-based power allocation control under different voltage ratios is illustrated in Fig. 12, where V_H is fixed at 400 V, and V_L is set to 160, 200, and 240 V in Fig. 12(a), (b), and (c), respectively. The experimental results are obtained with the reference power of the upper dc port, $P_H^* = 1000$ W, and the power demand on the ac side $P_{ac} = 1000$ W. As shown, the grid-side voltage and current u_a and i_a are well-controlled, with current THD values of 3.11%, 3.07%, and 2.98%, respectively. Despite the imbalanced input voltages, the performance of the ac side remains unaffected, and the sum of v_{d1} and v_{d2} is always equal to v_d, indicating that the grid-forming control is achieved effectively.

2) Results under Different Power Demands: To verify the effectiveness of the proposed DSRF-based strategy in four modes and the capability of power allocation, the steady-state test under the different reference power of the upper dc port P_H^* is conducted in the case of the $V_H = 400$ V and $V_L = 300$ V and $P_{ac} = 1000$ W. Fig. 13(a), (b), (c), and (d) correspond to P_H^* set as 0, 700, 1000, and 1300 W, respectively. The lower dc port

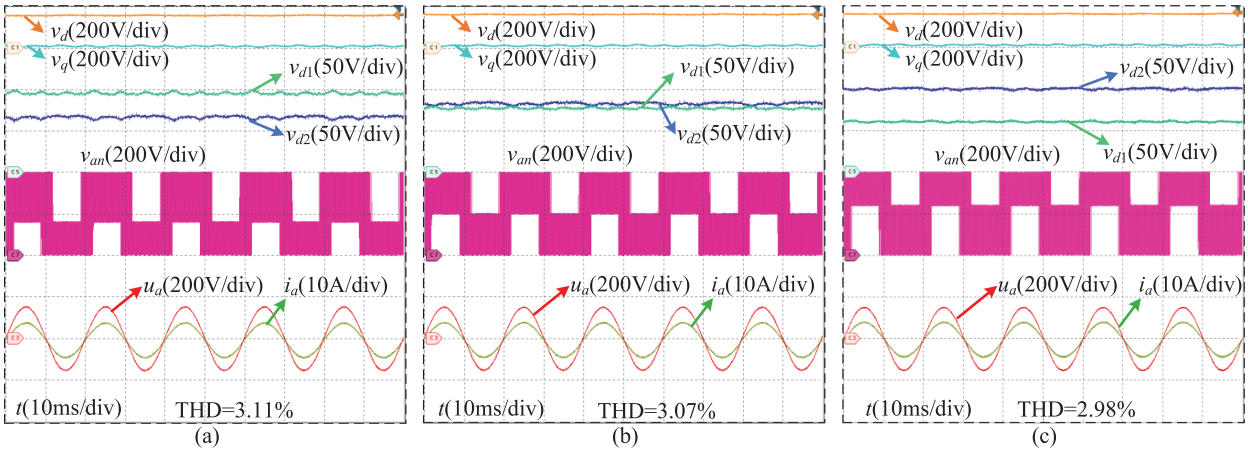

Fig. 12. Steady-state performance of the SSMPI with the proposed DSRF-based strategy under variable DC port voltages. (a) $V_L = 160$ V. (b) $V_L = 200$ V. (c) $V_L = 240$ V. Waveforms from top to bottom are d-axis of SSMPI v_d, q-axis of SSMPI v_q, d-axis subinverter I v_{d1}, d-axis of subinverter II v_{d2}, voltage of phase a v_{an}, grid-side voltage u_a, grid-side current i_a.

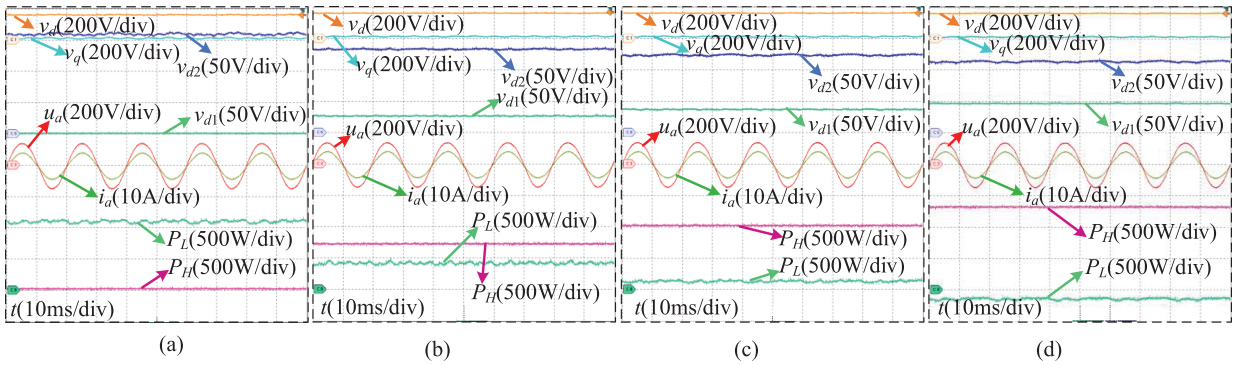

Fig. 13. Different P_H^* under imbalanced DC voltage for four modes. (a) Mode I: $P_H^* = 0$ W. (b) Mode II: $P_H^* = 700$ W. (c) Mode III: $P_H^* = 1000$ W. (d) Mode IV: $P_H^* = 1300$ W. From top to bottom, waveform is d-axis of SSMPI v_d, q-axis of SSMPI v_q, d-axis subinverter I v_{d1}, d-axis of subinverter II v_{d2}, grid-side voltage u_a, grid-side current i_a, power of upper DC port P_H, and power of lower DC port P_L, respectively.

is used to supply or absorb the remaining power. In the face of different P_H^* values, P_H can accurately track its references. In addition, the grid-side voltage/current u_a/i_a are well-controlled by control the sum of v_{d1} and v_{d2} is equal to v_d and the magnitude of v_{d1} and v_{d2} has a good adaptability when the power of dc port changed. The experiment demonstrates that the proposed DSRF-based strategy can achieve the desired power allocation for four modes in cases with varying port power demands.

B. Dynamic Performance

In addition to the steady-state performance, the dynamic performance is also present to further verify the proposed DSRF-based strategy, which is tested under both stepped changes of grid-side load and the reference power of the upper dc port.

1) Stepped Change of the Grid-Side Load: The control performance of the proposed strategy under P_{ac} steps change from 1000 to 1200 W in Fig. 14(a) and then back to 1000 W in Fig. 14(b), and change from 1000 to 750 W in Fig. 14(c) and then back to 1000 W in Fig. 14(d), with $V_H = 400$ V, $V_L = 240$ V, and $P_H^* = 1000$ W. When the load changes suddenly, P_H is regulated to P_H^*, and the lower dc port is used to release or absorb excessive power, revealing that P_H tracking can be guaranteed under grid-side load step changes. In Fig. 14, the sum of v_{d1} and v_{d2} is always equal to v_d, verifying the effectiveness of the proposed DSRF-based strategy when changing the load suddenly.

2) Stepped Change of the Reference Power of the Upper DC Port: The control performance of the reference power of the upper dc port P_H^* is tested under stepped changes from 700 to 1300 W, with $V_H = 400$ V, $V_L = 240$ V, and $P_{ac} = 1000$ W. The power reference of the upper dc port P_H^* stepped changes from 700 to 1300 W in Fig. 15(a) and then back to 700 W in Fig. 15(b). During the stepped change of P_H^*, v_d and v_q remain unchanged, and the sum of v_{d1} and v_{d2} is equal to v_d, indicating the proposed DSRF-based strategy presents good adaptability in the case of variable P_H^*. Meanwhile, with the proposed DSRF-based allocation strategy, a rapid dynamic response is achieved within two control cycles.

C. Comparison With the Existing Strategies

To highlight the benefits of the proposed DSRF-based strategy, a comparative study with existing strategies is conducted to verify the advantages of the proposed strategy features.

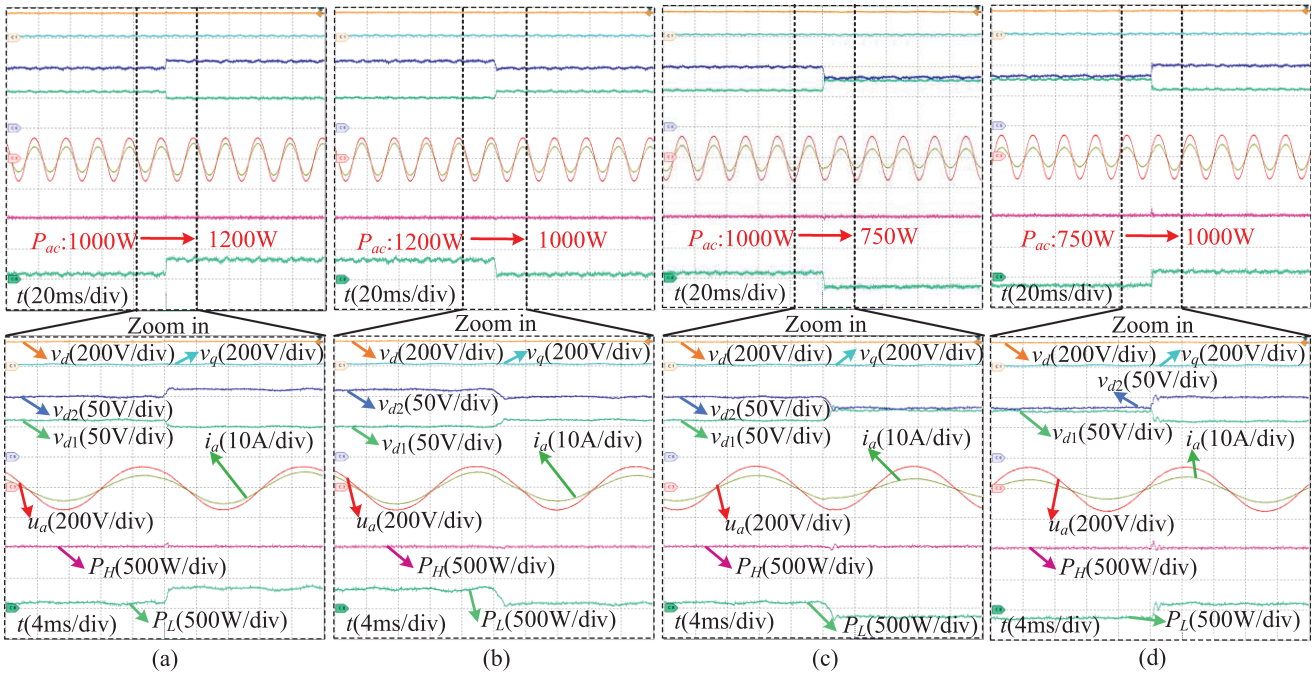

Fig. 14. Dynamic performance of SSMPI with the proposed DSRF-based strategy under grid-side load switching. (a) P_{ac} varies from 1000 to 1200 W. (b) P_{ac} varies from 1200 to 1000 W. (c) P_{ac} varies from 1000 to 750 W. (d) P_{ac} varies from 750 to 1000 W. Waveforms from top to bottom are d-axis of SSMPI v_d, q-axis of SSMPI v_q, d-axis subinverter I v_{d1}, d-axis of subinverter II v_{d2}, grid-side voltage u_a, grid-side current i_a, power of upper DC port P_H, power of lower DC port P_L.

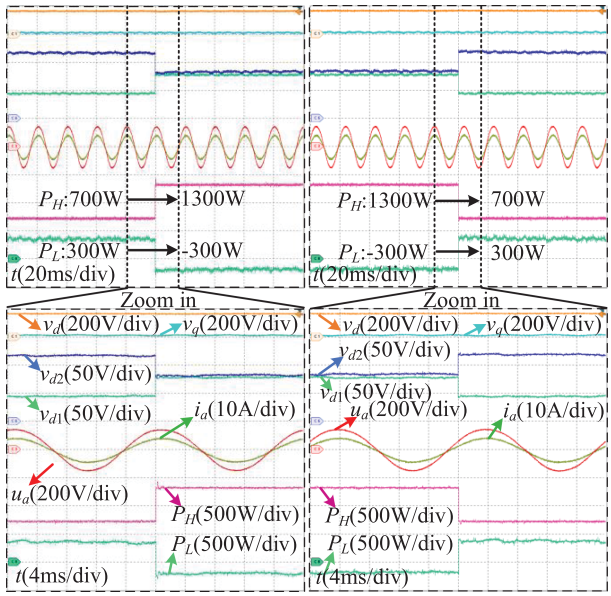

Fig. 15. Dynamic performance for SSMPI with the proposed DSRF-based strategy under variable P_H^*. P_H^* varies from 700 to 1300 W and then back to 700 W. From top to bottom, waveform is d-axis of SSMPI v_d, q-axis of SSMPI v_q, d-axis subinverter I v_{d1}, d-axis of subinverter II v_{d2}, grid-side voltage u_a, grid-side current i_a, power of upper DC port P_H, and power of lower DC port P_L, respectively.

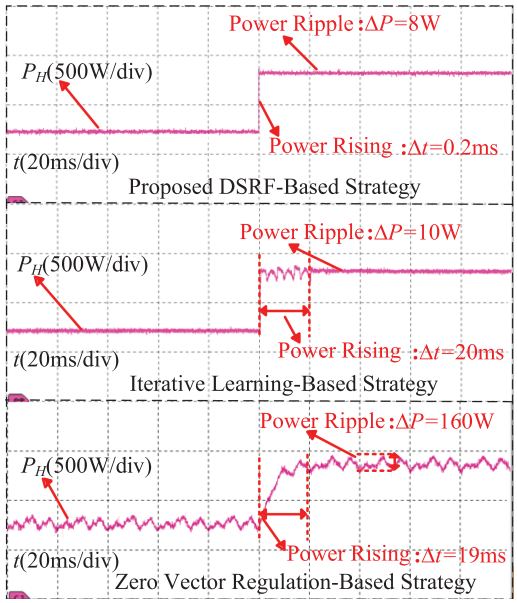

Fig. 16. Comparison on dynamic performance and port power ripple among the proposed DSRF-based strategy, iterative learning-based strategy in [33] and zero vector regulation-based strategy in [28] when the reference power of the upper DC port P_H^* rises from 700 to 1300 W.

1) Comparison on Dynamic Performance and Port Power Ripple: The comparison tests with iterative learning-based strategy in [33] and zero vector regulation-based strategy in [28] under variable P_H^* are conducted in the condition of $V_H = 400$ V, $V_L = 240$ V, and $P_{ac} = 1000$ W. As shown in Fig. 16, the power of the dc port P_H rises from 700 to 1300 W using different control strategies. As for dynamic performance, the transient time Δt for the iterative-learning-based strategy and the zero vector regulation-based strategy is 20 and 19 ms, respectively.

TABLE III
COMPARISON BETWEEN THE PROPOSED DSRF-BASED STRATEGY AND THE EXISTING STRATEGIES

Strategies	Reference frame	Power ripple	Power allocation	Power efficiency	Dynamic response
[12]	$\alpha\beta$ + dq	Small	Fixed	Low	Slow
[24]	$\alpha\beta$ + dq	Large	Flexible	High	Slow
[28]	$\alpha\beta$ + dq	Large	Flexible	High	Slow
[33]	$\alpha\beta$ + dq	Small	Flexible	High	Slow
Proposed	Both in dq	Small	Flexible	High	Fast

However, Δt for the proposed DSRF-based strategy is 0.2 ms, which is significantly improved as the power is regulated in the DSRF by the dual subinverters.

As for performance of power ripple $\widetilde{P}_r$, which is defined as follows:

$$\widetilde{P}_r = P_{H\max} - P_{H\min} \tag{29}$$

where $P_{H\max}$ and $P_{H\min}$ indicate the maximum and minimum value of the sampling power. $\widetilde{P}_r$ is 10 and 160 W for iterative learning-based and zero vector regulation-based strategies. And $\widetilde{P}_r$ is 8 W for the proposed DSRF-based strategy, which benefited from allocating the power of the dc port directly based on dual subinverters. Power ripple is reduced 11.69% when $P_H^* = 1300$ W compared with the zero vector regulation-based strategy, which demonstrates the superiority of the proposed DSRF-based strategy in suppressing the port power ripple.

2) Theoretical Comparisons with Existing Strategies: The proposed DSRF-based strategy has been evaluated against the previous methods to highlight its benefits in terms of reference frame, power ripple, power allocation, power efficiency, and dynamic response. The comparison results are presented in Table III. In [12], [24], [28], and [33], power allocation control and grid-forming control are achieved in a mixed reference frame. Power ripple is reduced in [12] and [33] by incorporating an extra dc–dc converter and an iterative learning controller, respectively. Power allocation in [24], [28], and [33] is flexible, whereas it is fixed in [12] because the power allocation control is not considered. In [12], power efficiency is lower than that of other strategies, as an extra dc–dc converter is applied. The dynamic response is slow because the model is not decoupled in [12], [24], [28], and [33].

In contrast, the proposed DSRF-based strategy decouples SSMPI in DSRF, enabling it to achieve flexible power allocation control and grid-forming control simultaneously in the dq frame. Meanwhile, the power ripple is low, and the dynamic response is fast, benefiting from the decoupled power model that regulates power intuitively and linearly. Power efficiency is high because the dc–dc converter is removed in the SSMPI configuration.

V. CONCLUSION

This article proposes a DSRF-based power allocation control strategy to achieve power allocation control on the dc side and grid-forming control on the ac side in the DSRF, thereby resolving the coupling issue caused by using mixed reference frames in existing strategies. With the proposed DSRF-based strategy, the SSMPI is decoupled into dual subinverters, and the power of each subinverter is calculated linearly and intuitively in the corresponding synchronous rotating frame. Experimental results confirmed that the proposed DSRF-based strategy reduces port power ripple by approximately 11.69% compared to the existing strategies, while also achieving fast dynamic performance. In light of these results, the SSMPI with the proposed DSRF-based strategy offers an attractive solution for achieving fast dynamic response and reduced port power ripple in islanded microgrids.

Besides, there are still several issues that should be addressed in future work, such as operating under a nonunity power factor and extending to more than two dc ports.

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