Data-Driven Design of MHz Resonant Converters for Full-Freedom Soft-Switching Optimization

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***Abstract*—Achieving soft switching is critical for MHz resonant circuits, including Class E, EF, and Φ-based resonant topologies. Traditional parameter design methods heavily rely on equation-derived analytical modeling, which is highly complex and infeasible to get direct analytical solutions. Existing approaches typically simplify the problem by constraining the model's degrees of freedom, leading to locally optimal solutions and limiting design space exploration. To address these challenges, we propose a data-driven surrogate modeling approach that eliminates the need for analytical modeling and enables direct parameter optimization for soft switching without imposing constraints on the design space. To the best of authors' knowledge, this is the first approach that allows global exploration of the full-freedom soft-switching space for resonant converters, unlocking more optimal design solutions. Inspired by the understanding of resonant converters (similarity of inverter and rectifier and resonant capacitor as the crucial soft-switching component), we proposed mirrored circuit simulation and resonant-capacitor-based parameter decouple strategies to improve data density and diversity, achieved high quality data preparation. Experimental validations across three case studies demonstrate its effectiveness. Beyond the circuits studied in this article, the proposed methodology is broadly applicable to other resonant topologies, offering a scalable framework for automated design optimization in high-frequency power electronics.**

***Index Terms*—Design automation, high-frequency converter, resonant converter, soft switching, surrogate model, tuning.**

I. Introduction

RESONANT converters work as a promising solution for multi-MHz applications due to their soft-switching ability [2], [3], [4], where the frequency-dependent switching losses is rapidly minimized by introducing zero-voltage switching (ZVS) to the power switches. Many topologies have been proposed with diverse realizations of resonant tanks to obtain various performance benefits, e.g., component stress or power output capability. Despite of the promising benefits, design of soft-switching converters face critical challenges to accurately and systematically model multiresonance operations.

1) Facing high nonlinearity, typical analytical modeling cannot settle the conflict between accuracy and equation-order complexity, leading to time-consuming derivations and approximate numerical solutions [4], [5], [6], [7], [8], [9].
2) Facing high parameter dimensions and high freedom of ZVS realization, supplementary solving conditions narrow the design freedom to a local optimum solution as they are not globally valid [6], [7].
3) Facing detuned operations caused by manufacture tolerance of capacitors and inductors [10] or more comparable parasitic circuit effects at MHz frequencies [11], such isolated workpoint solutions fail to give any insight on tuning directions [12], [13].

In summary, there is a lack of full-freedom space insight that links ZVS realizations and parameter variations together. The existing analytical models only deliver limited scope in ZVS solutions, which hinders systematical performance optimization and further tuning opportunities. These three limitations will be introduced in more details in Section II.

Addressing these limitations in analytical modeling, simulations model circuit operations in a more straightforward and accurate way [1]. However, facing the high freedom in parameter values, simulations do not inherently guarantee soft switching. Instead, collecting soft-switching samples heavily relies on mass simulations and discarding those hard-switching ones. Time-efficiency remains one of the major concerns, sample diversity, and representativeness also crucially determine the freedom of design and optimization.

Data-driven methods based on surrogate models have gained increased popularity in power electronics applications [14], [15], including reliability management [16], thermal modeling [17], and magnetics design [18]. Although a simplified model trained from feasible simulations can be used to make thousands of new soft-switching design predictions in several seconds, it is not straightforward to apply machine learning in its typical form. The training performance is greatly degraded with a coupled input parameter space or poor dataset quality from simulations. Targeting resonant topologies, transferable strategies to meaningfully decouple the input space and effectively improve dataset density and diversity are highly demanded.

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In this work, we propose a data-driven design method for MHz resonant converters. Full-freedom surrogate models are obtained as high-accuracy alternatives to traditional analytical- and simulation-models with limited freedom. We formulate the following three key contributions as follows.

1) The proposed method explores the full parameter space of design variables, including passive components values and control variables, such as frequency or duty cycle. The successful exploration of a full-freedom space that maps design variable combinations to features of soft-switching waveforms unlocks global performance analysis and optimizations.
2) We propose a systematic method to generate datasets enabling the first contribution. This is achieved by the mirrored-circuit simulation followed by the resonant-capacitor-based parameter decouple strategy, delivering more diverse and representative datasets with 70× accelerated speed and 4× reduced dimension complexity.
3) Furthermore, this data-driven-modeling methodology is transferable for resonant topologies of any class, their corresponding surrogate models enable systematical performance comparison and optimization among diverse topologies. The push-pull T-network (PPT) Class-Φ_n topology is selected in this article as an application example to present the method.

The rest of this article is organized as follows. In Section II, we introduce resonant converters and three limitations of the existing analytical modeling methods. A simulation-based design approach is presented in Section III, which partly handles the limitations but discloses its defect in preparing soft-switching datasets. Accordingly, two efficient data preparation strategies are proposed in Section IV, followed by the data-driven modeling workflow and performance comparison. Section V delivers circuit-level understanding from a fully explored soft-switching space. We design three example converters under different specifications, their experimental implementation results are presented in Section VI. Finally, Section VII concludes this article.

II. Existing Analytical-Model-Based Design Methods and Limitations

Fig. 1 summarizes the most common resonant converter topologies, including Class E, Class F, Class EF, Class Φ, and their variants, where ZVS is achieved by $v_{\rm ds}$ waveform shaping through resonant network designs. The idea of switching loss elimination rooted in shaping power-switch voltage $v_{\rm ds}$ to 0 before its current $i_{\rm d}$ starts to flow at moment $t_{\text{s-on}}$ defined by gate signals. Targeting even better switching performance, a zero $\mathrm{d}v/\mathrm{d}t$ at $t_{\text{s-on}}$ enables a lower ground noise, named zero-voltage-derivative switching (ZDS). The soft-switching conditions are defined as

$$v_{\rm ds}(t_{\text{s-on}}) = 0 \quad \text{(ZVS condition)} \tag{1}$$

$$i_{\rm d}(t_{\text{s-on}}) = 0 \text{ OR } \mathrm{d}v_{\rm ds}(t_{\text{s-on}})/\mathrm{d}t = 0 \quad \text{(ZDS condition)}. \tag{2}$$

As the most critical resonant component, C_1 is added in parallel to the power switch Q_1. When Q_1 is turned-OFF ($i_{\rm d} = 0$), current ($i_{\rm C1}$) alternately flows through the shunt capacitor. In general, $v_{\rm ds}$ is shaped by discharge of C_1, where the inductive energy can be provided by the load branch ($L_{\rm x}$, Class E/EF [2], [4], [9]), or the dc input (L_1, Class Φ [19]), or the T-branch (L_2, PPT Class Φ [5], [6]). The resonant topologies are classified into different class based on the source of the inductive power. Given the sinusoidal ac current in both wireless power transfer (WPT) [4] and RF applications [6], a filter is always present in the load branches in Fig. 1 regardless of parallel-($R_{\rm L}, L_{\rm xp}$) or series-($R_{\rm AC}, L_{\rm x}$) equivalence. Load angle ϕ defines the ratio of the real and reactive powers in the load branch

$$\tan\phi = \frac{R_{\rm L}}{\omega_{\rm s} L_{\rm xp}} = \frac{\omega_{\rm s} L_{\rm x}}{R_{\rm AC}} \tag{3}$$

where $\omega_{\rm s}$ is the angular switching frequency. Upon a successful zero-return of $v_{\rm ds}$, the duty cycle D has to be adjusted to turn-ON Q_1 immediately. Such operation minimizes the reverse conduction loss and is beneficial for efficiency [19].

Moreover, a high-order harmonic branch can be used to fine-tune $v_{\rm ds}$ shape for performance benefits, e.g., a lower voltage stress. Referring to Class EF/Φ_n topologies in Fig. 1(b)–(d), n represents the ratio of L_2C_2-branch resonance frequency normalized to the switching frequency $f_{\rm s}$, denoted as

$$n = \frac{1}{\omega_{\rm s}\sqrt{L_2 C_2}}, \quad n > 1. \tag{4}$$

It is evident that designing a soft-switching circuit under a given specification (e.g., $R_{\rm AC}, v_{\rm AC}$) has 7 degrees of freedom: we can find various $L_1, L_2, C_1, C_2, L_{\rm x}, \omega_{\rm s}, D$ combinations where diverse ZVS waveforms deliver different performance benefits, e.g., Fig. 2. Typical switch-mode analysis using explicit *V–I* equations [4], [5], [6], [8], [9], or network-impedance analysis [3], [7], [20], [21], [22] are all challenging to fully model such circuits with high-dimensional wide-range parameter selections. Next, we formulate the three limitations in detail.

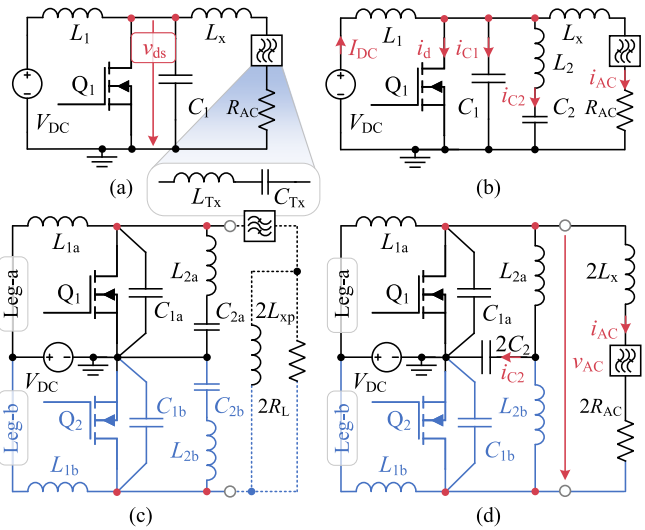


Fig. 1. Resonant circuit topologies. (a) Class E. (b) Class EF$_n$ or Φ_n. (c) Push-pull Class EF$_n$ or Φ_n (with parallel-equivalent load branch, components in push and pull legs are denoted by subscripts "$_{\rm a}$" and "$_{\rm b}$," respectively), (d) PPT Class EF$_n$ or Φ_n (with series-equivalent load branch). n defines the harmonic branch resonance, see (4).

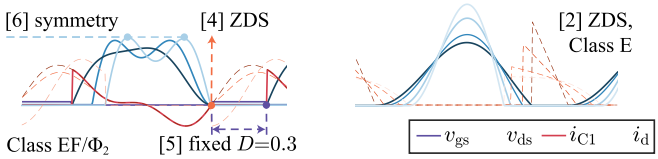


Fig. 2. Examples of diverse soft-switching waveforms from references and their corresponding supplementary conditions.

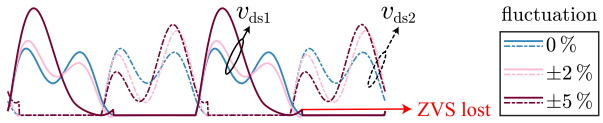


Fig. 3. v_{ds} waveforms under fluctuations of $L_{2a,b}$ and T-network tuning.

A. Limitation 1: Conflict Between Modeling Accuracy and Model Complexity

To fully describe multiresonance operations linked to all 7 dimensions, analytical models have to include much more intermediate variables, e.g., impedance matrix, harmonic current/voltage, and their derivatives and integrations.

For simplicity, the harmonic-based approaches [5], [6], [7], [20] ignore harmonic-ratios $\geq$3, leading to poor model accuracy, while time-domain analysis easily introduces 33 to 105 equations [4], [9]. Such high-order multivariable equation sets do not support analytical circuit solutions [9], even numerical solvers face challenges in assigning suitable initial search values [3], [5]. Under limited accuracy, some workpoints are more challenging to design, e.g., with high D or R_L, as the numerical solving frequently fails after long search period.

B. Limitation 2: Locally Valid Equations Fail to Describe the High Freedom of Soft-Switching Realization

Given that high variable dimension enables wide freedom in ZVS realization, e.g., Fig. 2, waveform-based approximations are mandatory to supplement analytical models to get a unique workpoint solution. For example, Gu et al. [6] focus on designs working at $D \approx 0.3$, and the work in [7] and [22] constraints the designs to operate with a symmetrical v_{ds} waveform.

Although ZVS is realized, these supplementary constraints lead to only single design solution, i.e., "local optimal." To explore ZVS designs with new features, the whole analytical modeling process has to be repeated using new workpoint-specified constrains. Facing infinite shapes of v_{ds} waveforms, such exhaustive method is impossible to explore full freedom of ZVS realization, nor to provide any scalable models for global performance optimizations.

To summarize, all existing models suffer from a limited use of the freedom in their topologies, which restricts the optimization domain. For example, Aldhaher et al. [4] introduced a design table covering two degrees of freedom (two coefficients k and q_1) still in discrete values, while limiting $D = 0.3$. Supplemented by ZDS conditions, the modeling method in [5] enabled freedom of selecting $D \in (0, 0.5)$, under a fixed T-network resonance $n = 2$.

C. Limitation 3: Lack of Overall Understanding That Links Waveform Shaping With Parameter Variations

Regardless of the design accuracy, implementation accuracy against parasitic effects is one of the major concerns that hinders a wider use of resonant converters in practical scenarios. v_{ds} waveform is highly sensitive [12], [23], e.g., Fig. 3 shows $\pm 5\,\%$ fluctuation of component values, which leads to a totally shifted workpoint or even lost ZVS.

Constrained to a single v_{ds} realization, existing analytical models cannot systematically link waveform shaping with parameter variations. In practice, converters are usually tuned by random variable sweeps in simulations [23], which heavily relies on experience, time- and computational-resources, as follows:

1) it is challenging to recreate the exact same detuned waveform in simulation;
2) wrong tuning directions easily trap the circuit in hard-switching region; and
3) the correct parameter and direction of tuning is hard to find due to the mutual coupling effects on v_{ds}-shaping among all design variables.

Design optimization is pointless if hardware implementations always operate far from the theoretical solution: However, trial-and-error tunings often end up with a shifted ZVS workpoint with totally different performance from the designed one. Nikiforidis et al. [23] have to introduce an iteration method to obtain circuit implementation parameters without need of retuning.

In conclusion, an ideal design methodology would not need a detailed analytical modeling while providing insights on performance optimization and experimental tuning. This is achieved by obtaining a full understanding that maps parameter variations to v_{ds}-shaping. Therefore, the modeling process should not be specific to particular application cases, e.g., studies based on case-by-case parasitic components. Targeting a global validity, it requires to investigate full variation freedom of all design variables and decouple their effects on v_{ds} waveform shaping. From design perspective, the method improves implementation accuracy by providing tuning guidance instead of changing circuit inherent parameter sensitivity.

III. Simulation-Based Design Approach With Huge Resource Consumption

Our previous work [1] has explored resonant converter designs based on simulation approaches. In this section, we check its performance in solving the three limitations from analytical modeling. The method is introduced based on an example of PPT Class Φ_2 converter [see Fig. 1(d)].

Facing the limited accuracy and high complexity of analytical models, straightforward circuit simulations work as perfect alternative that delivers accuracy as high as ideal circuits. To offer transferable models valid to all possible operations in a given topology, it is important to simulate the ideal circuit, working as an accurate benchmark for diverse parasitic cases.

In theory, through mass simulations by sweeping all design variables, we can overcome *limitation 2*, and explore diverse

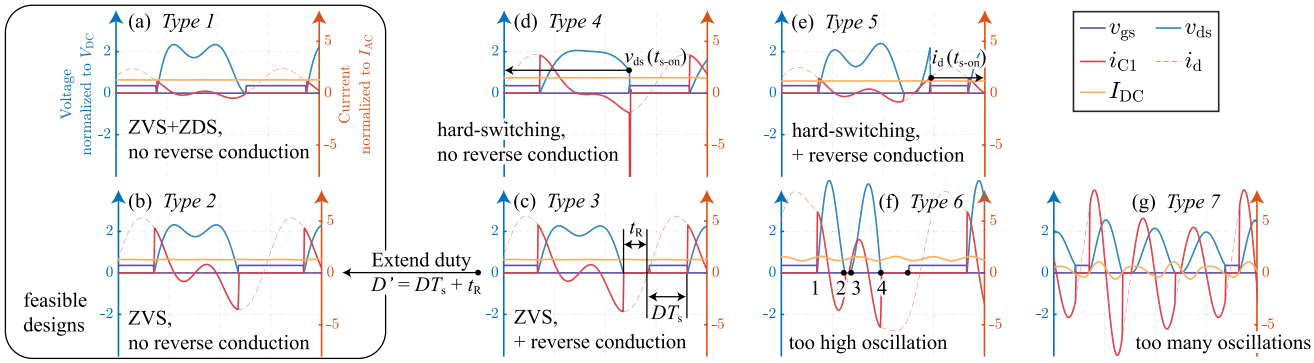


Fig. 4. Classification of seven switching types based on the power switch voltage v_{ds} and current (i_d+i_{C1}) waveforms (see Table I). The waveform-based classifications are applicable to resonant topologies of any class. Examples (a)–(g) are simulated from a PPT Class Φ_2 converter [see Fig. 1(d)] under $\phi = 0$.

TABLE I
SWITCHING TYPE CLASSIFICATION CONDITIONS†

	Type1	*Type2*	*Type3*	*Type4*	*Type5*	*Type6*	*Type7*
$v_{ds}(t_{s\text{-}on})$	0	0	0	>0	>0	0	— *
$i_d(t_{s\text{-}on})$	0	<0	≤ 0	—	>0	≤ 0	—
t_R	0	0	>0	0	>0	>0	—
Other features			*Type6*: v_{ds} zero-crossing $= 4$				
			Type7: (i_d+i_{C1}) zero-crossing > 4				

* not required, † the classification is valid to resonant topology of any class.

circuit operations in full dimensional freedom by extracting critical performance indicators from waveforms.

For the first time, we systematically analyze all resonance operations by classifying them into 7 types. Based on conditions proposed in Table I, Fig. 4 presents typical waveforms of each type, obtained from MATLAB simulations.

Type 1 describes the strictest soft-switching operation satisfies both ZVS and ZDS. *Type 2* switching only meets (1), while dv/dt at switching moment $t_{s\text{-}on}$ remains high. Both *Types 1 and 2* have no reverse conduction period, i.e., $t_R = 0$. Comparing Fig. 4(b) and (c), in *Type 3*, current flows reversely through Q_1 due to the late turn-ON signal, gives $t_R > 0$. Conduction losses can be minimized by replacing the reverse conduction with forward conduction controlled by gate signals [19], leading to *Type 2* counterparts. Thus, only *Types 1 and 2* are feasible simulations that can be used for converter design.

The remained simulations are also meaningful to provide insights into resonance behavior. They are categorized into four types based on v_{ds} waveform amplitude and its zero-return speed relative to D. *Type 4* corresponds to hard switching when v_{ds} drops too slowly to reach zero before $t_{s\text{-}on}$. In contrast, in a fast zero-return case, an excessively small D can cause a positive $(i_d + i_{C1})$ that recharges C_1 after Q_1 reverse conduction. Such positive $v_{ds}(t_{s\text{-}on})$ makes *Type 5* hard switching despite a successful zero-return. Regardless of the ZVS condition, *Type 6* is unsuitable as v_{ds} has multiple zero-returns and undesired reverse conduction, while *Type 7* designs with excessively fast oscillations are more sensitive and unstable.

Regarding *limitation 3*, we can position all simulations in a full-dimension space to map waveform shaping to parameter

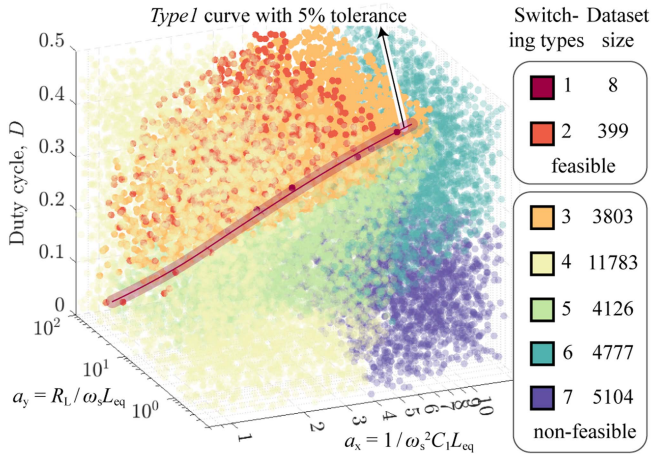


Fig. 5. Dataset size and distribution of the seven switching types. Simulation data points are created with the same example circuit used for Fig. 4.

variations. Fig. 5 presents visualized distribution regions of 7 switch-types. The space axes follows the decoupled parameters in [1], generated based on resonance relations in [5]

$$\text{axis } a_x: \ \frac{1}{\omega_s\sqrt{L_{eq}C_1}}, \quad \text{axis } a_y: \ \frac{R_L}{\omega_s L_{eq}} \tag{5}$$

where the equivalent inductance $L_{eq} = L_1 \parallel L_2$. Shunt capacitor C_1 is the sum of the internal parasitic capacitance C_{oss} and the external parallel capacitance of power switch Q_1.

To briefly analyze, Fig. 5 already indicates parameters and directions to tune an imperfect implementation to ZVS region based on waveform features, where we observe a ZVS region (*Types 1, 2, and 3*) with an upper boundary surface of *Type 2* ZVS, and a lower surface (too low D) suffers from *Type 5* reresonance. The crossing line of these two surfaces forms the boundary line of the ZVS space as well as the ZVS surface, which consists of *Type 1* designs with the strictest ZVS+ZDS conditions.

However, targeting ZVS, this typical inverter simulation is inefficient for generating *Types 1 and 2* datasets that allow either direct design or model training from it. In Fig. 5, we obtained only 399 *Type 2* and 8 quasi-*Type 1* samples out of

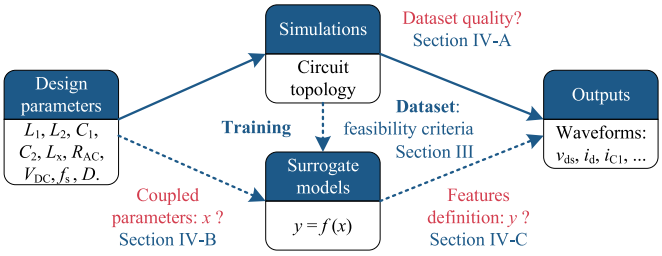


Fig. 6. Basic process of data-driven methods and its converter design application. Questions rise in input space decouple, output feature extraction, and methods to improve dataset quality will be solved in three subsections.

30 000 simulations under varied L_{eq}, C_1, D, R_L. Defined by the percentage of feasible (*Types 1 and 2*) data among the total simulation size, the sampling efficiency is only $1.34\,\%$. Preparing enough soft-switching data under this low sampling efficiency requires huge simulation size, which is challenging for time and computation resources. Nevertheless, the 8 quasi-*Type 1* samples can only be identified by expanding soft-switching tolerance in (1) and (2) to $\pm 5\,\%$ of V_{DC} and $i_{d(max)}$, suffering from reduced accuracy. *Type 2* distributions do not cover full axis ranges in Fig. 5, which also degrades model training accuracy.

Summarizing the simulation-based design method, the key limitations are as follows:

1) It is evident that accurately meeting *Type 1* conditions by mass parameter-sweep simulations is nearly impossible.
2) Moreover, targeting full exploration of resonant operations across all degrees of freedom, variations of n and ϕ are not yet introduced to simulations. The high parameter dimensionality combined with low sampling efficiency impose a heavy computational burden.
3) Both the soft-switching simulations and surrogate models trained on them will perform poorly for wide-freedom circuit design due to the low dataset quality in diversity and representativeness.

IV. Proposed Data-Driven Design Method

Facing the low number of feasible designs from simulations, surrogate models trained from representative dataset can serve as simplified alternatives to simulations or analytical models, mapping circuit parameters to critical performance. A typical data-driven modeling workflow is given in Fig. 6 [14]. However, in terms of converter development, a clear definition of the machine learning problem remains missing.

Training performance of surrogate models heavily relies on dataset quality from simulations [24], including label accuracy, data efficiency, coverage, diversity, and representativeness. To significantly enhance *Type 1* dataset in these aspects, we propose an innovative mirrored-circuit simulation in Section IV-A.

Different from conventional data-driven modeling applications [16], [17], [18] where design parameters are independent, the input parameters of resonant circuit simulations in Fig. 6 exhibit high dimensionality and strong coherence. Random parameter sweeping often results in an excessively large simulation size but low-quality datasets either confined to a small region (limited diversity) or with low data efficiency, e.g., Fig. 5. The training performance is also degraded with coherent parameters directly as input. In Section IV-B, we propose the transferrable resonant-capacitor-based decouple strategy, from which *Type 2*-data can be efficiently generated on top of a fully decoupled input space x.

Unlike simulation modeling that identify all feasible soft-switching designs by checking output waveforms v_{ds} and i_d, time-domain waveforms contain excessive data are not suitable as surrogate model prediction outputs. Building on the switching type classification in Section III, we refine the extraction of critical features from operational waveforms and redefine the output features y for model training.

The above three steps clearly address all questions in Fig. 6, providing a well-defined machine learning problem and training dataset. A detailed workflow is presented in Section IV-C to conclude this section.

A. Mirrored Circuit Simulation Method for Efficient Generation of Type 1 Samples

Under the same circuit topology, rectifiers are obtained by reversing the power flow direction of inverters, indicated as Fig. 7(a) and (b). Under the substitution theorem, inverter waveforms v_{ds}, i_d, i_{C1} exhibit a time-symmetrical relation with their rectifier counterparts v_D, i_D, i_{C1}, as shown in Fig. 7(d) and (c). Such relation allows us to gain insights into inverter operations by analyzing rectifier waveforms under circuit equivalence.

Furthermore, the use of ideal diodes with a configurable ac source makes the rectifier much more efficient in creating accurate *Type 1* simulations than inverters. Thanks to the zero reverse recovery in ideal diodes, their intrinsic zero-current turn-OFF feature results in a v_D waveform starting with $dv/dt = 0$, as shown in Fig. 7(d). Under a mirrored equivalence, such feature leads to a *Type 1* operated inverter with precise ZDS [see Fig. 7(c)]. Thus, the most critical condition, ZDS, is naturally met for all simulations due to diode operations, providing almost $100\,\%$ sampling efficiency. Moreover, input space dimension is greatly reduced since the degree of freedom related to the load branch (ϕ) and duty cycle D are now directly calculated from simulation output waveforms.

Based on the definition in (3), we make a mirrored conversion, measuring ϕ as the phase of the current leading voltage, as illustrated in Fig. 8. Similarly, inverter duty cycle D is calculated from the interval $v_D = 0$ normalized to T_s. Other ac-branch parameters are expressed as

$$|Z_{AC}| = V_{AC}/2I_{AC} \tag{6}$$

$$\text{Series:}\quad R_{AC} = Z_{AC}\cos\phi, \quad L_x = Z_{AC}\sin\phi/\omega_s \tag{7}$$

$$\text{Parallel:}\quad R_L = Z_{AC}/\cos\phi, \; L_{xp} = Z_{AC}/\sin\phi/\omega_s. \tag{8}$$

Here, $2|Z_{AC}|$ is the absolute value of the ac load impedance. The series- and parallel-equivalence refers to Fig. 1(c) and (d). Phasor relations among these variables are illustrated in Fig. 9.

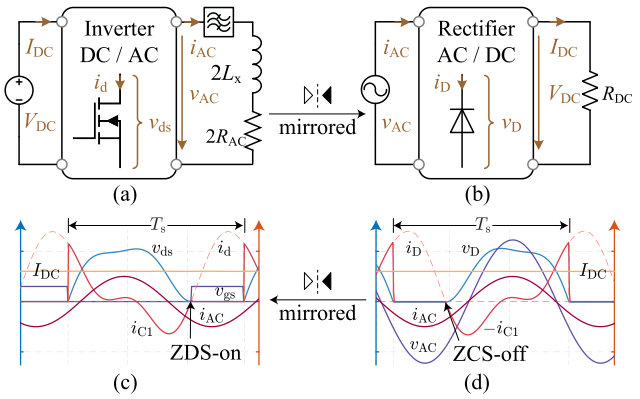


Fig. 7. Comparison between inverters and rectifiers in terms of topologies [(a) inverter, (b) rectifier] and time-domain waveforms [(c) inverter, (d) rectifier].

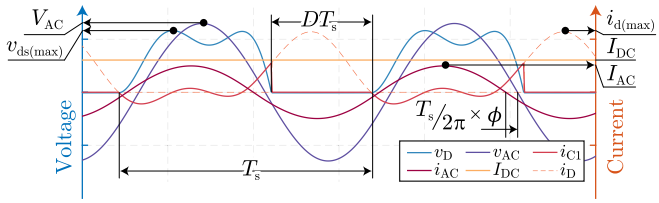


Fig. 8. Calculations based on rectifier simulation waveforms.

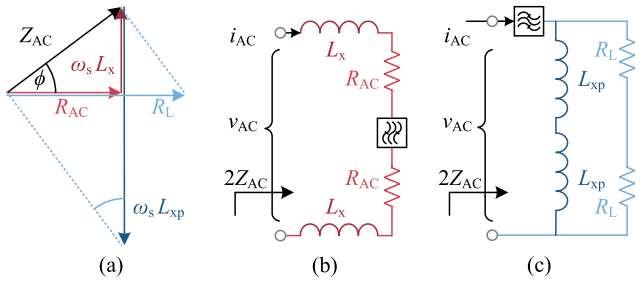


Fig. 9. (a) Vector form relation of load components and the corresponding, (b) series equivalence, and (c) parallel equivalence.

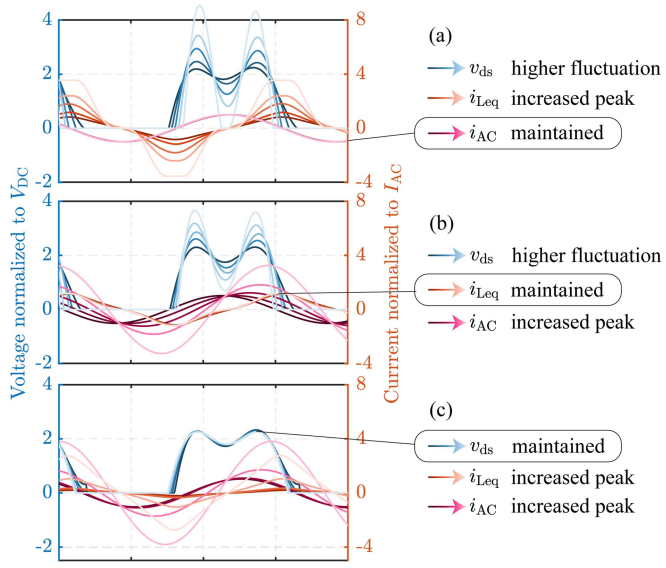


Fig. 10. Effects of decoupled parameter variation on v_{ds} waveform shaping: increasing (a) T-branch inductive power k_L with fixed k_R, k_P, (b) load-branch reactive power k_P with fixed k_R, k_L, and (c) load-branch real power k_R with fixed k_L, k_P. For a fair comparison target the same power output, current waveforms are normalized by the resistive AC current ($I_{AC}\cos\phi$).

B. Resonant-Capacitor-Based Design Space Decouple Strategy and Efficient Generation of Type 2 Samples

With higher degree of freedom included, *Type 1* designs may distribute as a 2D-surface [e.g., Fig. 11(c)] or a 3D-region in the full-freedom space rather than the 1D-curve in Fig. 5. Although *Type 1* distribution always defines the boundary between soft- and hard-switching, in practice, *Type 2* operations are more often and easier to realize due to parasitic effects. Facing *limitation 2*, we still need to explore full coverage of the *Type 1* dataset and discover *Type 2* distributions.

Although there are many ways to group resonance components $(R_L, \omega_s C_1, \omega_s L_{eq}, \omega_s L_{xp})$ and create nonoverlapping switch-type distributions (e.g., Fig. 5), we aim to find the most meaningful decouple strategy that gives the best efficiency for circuit analysis and dataset generation. The existing decouple in (5) does not reflect straightforward parameter variations, since a varied L_2 leads to changes in both a_x and a_y directions. R_L adjustment is also involved in two directions when the dimension of ϕ is directly included.

Based on the fundamental of soft-switching, discharging of C_1, we propose the resonant-capacitor-based decouple strategy. Explained by the PPT Class Φ circuit, voltage v_{ds} is denoted as in (9) shown at the bottom of this page. Here, $v_{ds1,2}$ are the push- and pull-leg outputs, v_{AC} is the fundamental component of the differential output $(v_{ds1} - v_{ds2})$, I_{DC} and i_2 are supply dc current and the nth harmonic branch C_2 current, referring to Fig. 1.

Leaving aside the complicated equation, it is evident that $\omega_s C_1$ is the major component involved with every current component inside the bracket. Under a specified load power represented by R_L, the value of C_1 defines the reactive power created for resonance. A lower freewheeling reactive power is good in terms of converter efficiency, while it is restricted by the power switch internal capacitance C_{oss}, as C_1 should be considerably higher than C_{oss} to ensure a robust operation. In contrast, soft-switching is easily reachable with higher reactive power, while it leads to smaller output capability of real power.

Following the coefficients in (9), we propose the following parameters as the design space dimensionalities:

$$\text{load-branch real power} \quad k_R = \omega_s C_1 R_L \tag{10}$$

$$v_{ds1}(\omega_s t) = \frac{1}{2}\frac{1}{\omega_s C_1}\int\left[I_{DC} - i_2 - \frac{1}{\omega_s L_{eq}}\int(v_{ds1} - v_{ds2})\mathrm{d}\omega t - \frac{v_{AC}}{R_L} - \frac{1}{\omega_s L_{xp}}\int v_{AC}\mathrm{d}\omega t\right]\mathrm{d}\omega t. \tag{9}$$

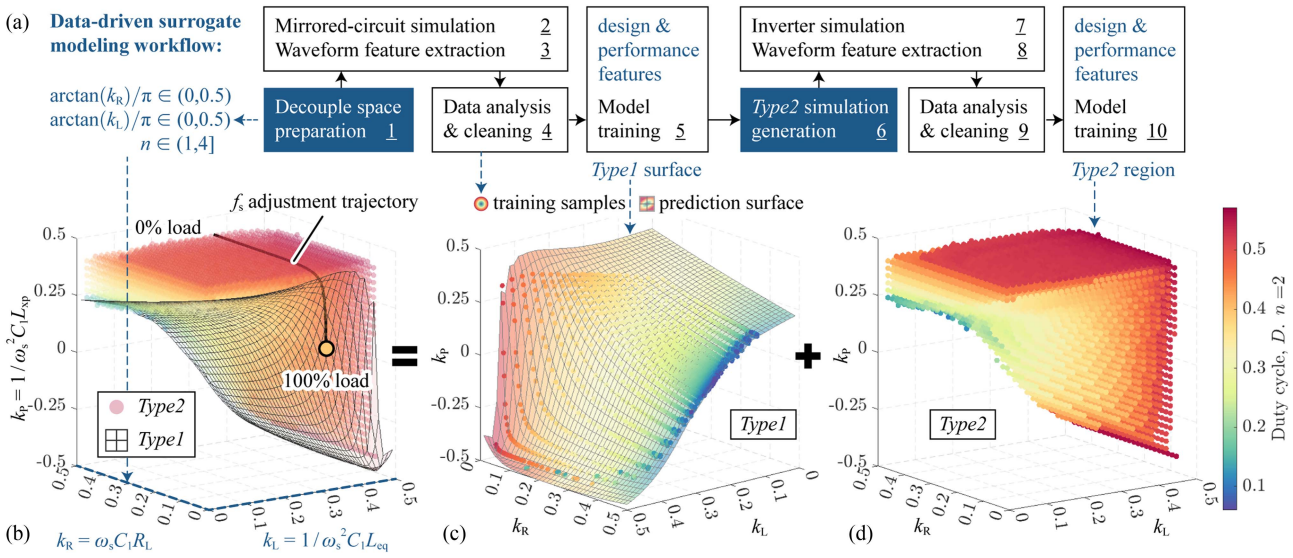


Fig. 11. (a) Conceptual outline of the proposed data-driven modeling steps. Visualization of (b) **full-freedom soft-switching design space** composed by (c) ***Type 1* surface** and (d) ***Type 2* region** above the surface, duty cycle D as color bar. Axis (a_x, a_y, a_z) describe three dimensions in scale of $\arctan(k_L, k_R, k_P)/\pi$, the last dimension of freedom $n = 2$. (b) f_s adjustment trajectory regarding load variation from 100 % to 0 % remain inside the soft-switching space (see Section V-C). (c) *Type 1:* observations of training dataset (solid dots) and new predictions from surrogate models (transparent surface). Input space $x = (k_L, k_R)$, features $y = (k_P, D)$ as z-axis and colorbar. (d) Observation of the region of *Type 2* designs distribution.

TABLE II
CIRCUIT PARAMETER DECOUPLE EXAMPLES BASED ON FIG. 1

Topology	(a) Class E	(b,c) (Push–pull) Class EF$_n$, Φ_n	(d) PPT Class EF$_n$, Φ_n
Specifications	v_{AC}, R_{AC}, P_{AC}		
DoF / dimension complexity*	$L_1, C_1, L_x, \omega_s, D, V_{DC}$	$L_1, L_2, C_1, C_2, L_x, \omega_s, D, V_{DC}$	$L_{eq}, C_1, C_2, L_x, \omega_s, D, V_{DC}$
Decouple parameters	$k_R = \omega_s C_1 R_L$ $k_L = \frac{1}{\omega_s^2 C_1 L_1}$ $k_P = \frac{1}{\omega_s^2 C_1 L_{xp}}$	$k_R = \omega_s C_1 R_L$ $k_L = \frac{1}{\omega_s^2 C_1 L_1}$ $k_P = \frac{1}{\omega_s^2 C_1 L_{xp}}$ $n = \frac{1}{\omega_s \sqrt{L_2 C_2}}$ $m = L_1/L_2$	$k_R = \omega_s C_1 R_L$ $k_L = \frac{1}{\omega_s^2 C_1 L_{eq}}$ $k_P = \frac{1}{\omega_s^2 C_1 L_{xp}}$ $n = \frac{1}{\omega_s \sqrt{L_2 C_2}}$
Reduced dimension†	k_R, k_L	k_R, k_L, n, m	k_R, k_L, n

*the initial dimension complexity = circuit degree of freedom (DoF) when applying straightforward inverter simulation.
† the reduced dimension complexity using the proposed mirrored-circuit simulation combined with the resonant-capacitor-based decouple strategy.

$$\text{T-branch inductive power} \quad k_L = \frac{1}{\omega_s^2 L_{eq} C_1} \tag{11}$$

$$\text{load-branch reactive power} \quad k_P = \frac{1}{\omega_s^2 C_1 L_{xp}} = \frac{\tan\phi}{k_R} \tag{12}$$

which fully decouple variations of load R_L, T-branch reactive power L_{eq}, and load branch reactive power ϕ.

The proposed decouple strategy is transferrable to other topologies, where decoupled parameters are found by writing the v_{ds} equation and take C_1-related coefficients. Table II lists decouple examples of all resonant topologies in Fig. 1, where we see the dimension complexity for building data-driven models are greatly reduced by 4 times with the proposed methodology: *mirrored-circuit simulation* combined with *resonant-capacitor-based decouple strategy*.

Moreover, the decoupled space (k_R, k_L, k_P) enables *independent* estimations of R_L, L_{eq}, ϕ variation effects, which successfully addresses *limitation 3*. Based on the energy to discharge C_1, *Type 1* enables the smallest inductive power for ZVS realization. Moving toward higher k_L or k_P to target more inductive power, v_{ds} returns to zero with a faster speed, while the fluctuation amplitude increases since the inductance value reduces. Therefore, there is no option to increase k_L or k_P further when a *Type 6* switching is reached.

Fig. 10(a) and (b) presents clearer waveform visualization of the above mentioned effects. We notice that increasing k_L raises the differential current i_{Leq} through L_2, while the load-branch current i_{AC} remains unchanged. In contrast, the load-branch coefficient k_P affects the phase and amplitude of i_{AC} but does not influence i_{Leq}. This confirms that the effects of k_L and k_P on waveform shaping are fully decoupled.

On the other hand, targeting more real power requires higher free-wheeling reactive power to enable soft-switching. Thus, reducing k_R in a *Type 1* design ($>100\%$ load) ends up with *Type 4* hard-switching [see Fig. 10(c)]. Toward the opposite direction, an increased k_R lowers the load percentage and does not affect the resonance. We see v_{ds} waveform remains almost the same as from the full-load until the empty load.

Based on the above discussion, we can extend coverage in the design space (k_R, k_L, k_P)—generate *Type 2* samples from the *Type 1* distribution by moving toward directions of higher k_R, k_L, or k_P. Inverter simulations with increased k_P will have higher D than its *Type 1* workpoint. Thus, the new D can be corrected based on the time period $v_{ds} = 0$.

TABLE III
COMPARISON BETWEEN THE THREE CONVERTER DESIGN METHODS

	Limitations (see Section II)	Design method based on		
		Analytical models	Simulations†	Proposed data-driven models
1	circuit analysis complexity (reflects modeling time)	100 Eq.s + numerical search	waveform feature extraction	
			7 Types	(9)
	data preparation time*	10 mins	415 mins	6 mins
	dimension complexity	7	$7 \rightarrow 5$	3
2	included dimension	1 or 0	$5 \rightarrow 3$	3
	switch-type diversity	1 v_{ds} shape	*Types 2*	*Types 1 and 2*
3	waveform tuning	trial-and-error	Fig. 5	surrogate models

* average time required for collecting 1000 soft-switching samples (6 parallel pools).
† represented by the example in Section III using (5) and Fig. 5.

C. Proposed Data-Driven Surrogate Modeling Workflow

Both proposals of the *mirrored-circuit simulation* in Section IV-A and the *resonant-capacitor-based decouple strategy* in Section IV-B are widely transferrable among resonant topologies. Thus, we redefine the problem within the machine learning framework, a conceptual outline of data-driven modeling steps is summarized in Fig. 11. Again, the full-freedom PPT class Φ_n circuit is taken as the example to demonstrate the outcome during the modeling process. A more comprehensive workflow Table V with detailed variables is shown in the Appendix.

Step 1: The workflow start with preparing a decoupled input space following the reduced dimension complexity in Table II. To obtain a widely and evenly distributed dataset that fully covers the feasible region, (a_x, a_y)-axes follow the $\arctan$ of (k_L, k_R), varying inside $(0, \pi/2)$, n serves as the third DoF.

Step 2: Combining known specification values and the defined DoF parameters, we obtain all circuit values for conducting the *mirrored-circuit simulation* (rectifier) in this step.

Steps 3 and 4: Step 3 processes simulation waveforms, delivers k_P, D, and other performance parameters. *Type 6* designs are filter out in *Step 4* and all *Type 1* data points are positioned in the decoupled coordinator. Fig. 11(c)-training samples present visualization of *Type 1* distributions under one n value.

Step 5: By training the *Type 1* dataset and mapping output $y = [k_P, D,$ other performance$]$ to inputs $x = [k_R, k_L, n]$, we obtained surrogate models that help to generate a *Type 1* surface with needed performance, i.e., Fig. 11(c)-prediction surface.

Similarly, *Steps 6–10* work on *Type2* dataset generation and surrogate model training. New inputs for inverter simulations are generated from the *Type 1* surface by maintaining values of $[k_R, k_L, n, D]$ while increasing k_P.

D. Performance Discussion of the Data-Driven Method

Reviewing the three limitations outlined in Section II, Table III summarizes and compares performance of *the proposed data-driven method incorporating data enhancement*with traditional *simulation-based*and *analytical approaches*. The proposed method significantly simplifies circuit modeling with reduced equations, sampling time, and dimensional complexity. Such benefits enable full exploitation of variations along each dimension, delivering more diverse v_{ds} shapes with less time consumption. Moreover, the waveform-based circuit analysis enables automated tuning through experimental waveform feature extraction, workpoint identification, and guided optimization toward the soft-switching region.

To be specific, the *mirrored-circuit simulation*effectively reduces input space dimension from 7 (analytical models) or 5 (simulation example in Section III) to 3. The model gets significantly simplified due to reduction of dataset size and simulation resources, which improves training accuracy. As shown in Fig. 11(c), the method identifies a complete *Type 1* soft-switching surface of inverter construction under each n value. Including all three dimensions (k_L, k_R, n) 90 000 simulations, only 3002 *Type 6* samples are infeasible, providing $96.67\,\%$ sampling efficiency compared to $8/30\,000$ from the simulation method [1]. Among various models tested in the *machine learning and deep learning toolbox—regression learner*, Gaussian process regression delivers the best training and validation accuracy, with 0.0125 and 0.0047 root-mean-squared (RMS)-errors for D and ϕ prediction models. Benefited from the well-representative training datasets (dots) in Fig. 11(c), new predictions from the surrogate models (the complete *Type 1* surface) show good consistency in terms of both D and ϕ (k_P) generation.

Furthermore, the *dataset-enrichment method from decoupled space* creates representative *Type 2* soft-switching designs, as shown in Fig. 11(d). At a given n value, e.g., $n = 2$, by filtering the 3-D space (30^3) with the *Type 1* surface in Fig. 11(c), we created 12 191 datapoints as simulation inputs, and $85\,\%$ samples among them constitute the *Type 2* space in Fig. 11(d). Notably, the *Type 1* surface does not always encompass the full variation range of k_P, yet *Type 2* designs remain feasible at these high k_P regions. Therefore, increasing k_P serves as a more thorough way to generate *Type 2* samples and ensure full coverage of the region above the *Type 1* surface.

V. CONVERTER PERFORMANCE DISCUSSION UNLOCKED BY THE FULL-FREEDOM SPACE

From the previous section, we obtained a fully explored decoupled ZVS space that maps design variables to waveform-based performance. Benefited from this full-freedom space, we are allowed us to systematically discuss circuit performance in both aspects of design and operation. During experimental implementations, although it is not possible to get the expected waveforms exactly due to the reduced accuracy from parasitics, the explored space addresses *limitation 3* by the following:

1) leaving design margin;
2) mapping parameter variation effects on related waveform features for tuning guidance.

A. Design Perspective: Targeting Type 1 Operations

The analysis in Section IV-B based on waveform comparisons in Fig. 10 already prove that *Type 1 designs represent the minimum reactive power in realizing soft-switching under a specified real power output*, outperforming their *Type 2* variants under

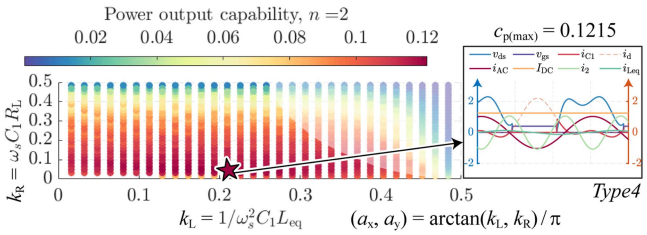


Fig. 12. Power output capability performance c_p of the $n = 2$ design space and the optimal workpoint waveforms. Transparent data points have $\phi < 0$.

k_L, k_P, k_R adjustments. Benefited from this lower limit of reactive power, efficiency is improved due to a smaller freewheeling resistive loss, and the power output capability is enhanced from a lower voltage and current stress. Thus, the design process should always target a *Type 1* operation with globally optimized performance, though practical implementation may lead to a slight shift toward *Types 2 or 4*.

Fig. 12 shows the power output capability of the *Type 1* surface (top view), $c_p = P_{AC}/[2v_{ds(max)}i_{d(max)}]$. The freedom of using an inductive load branch enables a higher $c_p = 0.125$ than with the resistive load [5]. Notably, it is possible to improve performance further by allowing a small tolerance on soft-switching, since the reactive power reduction from *Type 1* to *Type 4* enhances efficiency and power output capability, outweighing the losses from slight hard switching.

To optimize performance within *Type 1* designs, the lower k_R with a smaller capacitive power generation tends to provide higher efficiency with the same specifications, since having a higher C_1 requires more inductive power to compensate. That also explains the poor performance with a capacitive load branch under the same k_R—although it achieves *Type 1* operation, the total reactive power could be smaller by using a smaller k_L accompanied by a resistive or inductive load.

Finally, the T-network resonance number n can be used to fine-tune v_{ds} shape for performance benefits. For example, $n = 2$ gives overall minimum voltage stress, due to the complete removal of the second harmonic from voltage waveforms, which contributes to a quasi-square wave.

B. Guidance on Tuning Parameters and Directions

The decoupled space also indicates directions to tune a hard-switched implementation (locates below the *Type 1* surface) to the soft-switching region, with freedom to adjust along three directions k_R, k_L, k_P. From Fig. 12, we see that the most efficient direction is toward a smaller C_1 by lowering the energy to be discharged. However, restricted by C_{oss} of the selected power switch, it is not always possible to reduce C_1. When C_1 is close to C_{oss}, its voltage dependency may lead to a sensitive v_{ds} with a rapid increase in the voltage stress. By increasing inductive power, a reduced L_{eq} or increased L_x also help to reach soft-switching. These two approaches have different application scenarios: L_x tuning is more flexible by adjusting load-branch tuning frequency, but L_{eq} adjustment is the only option to maintain a constant voltage (CV) output, though it brings more complexities with extra T-branch tuning.

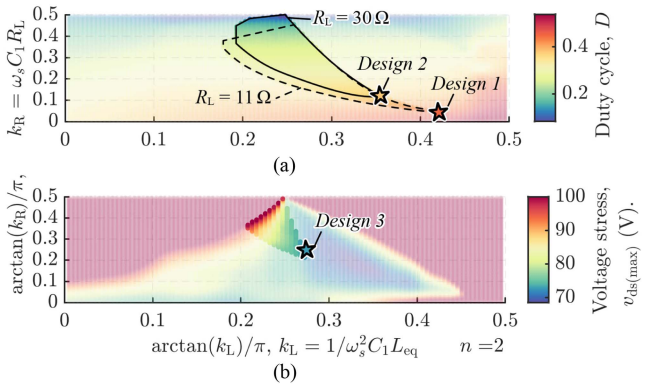


Fig. 13. Top-view of the *Type 1* surface. By applying design specifications, feasible design area are highlighted in full opacity and the optimal selection is marked by a star symbol for (a) *Designs 1 and 2*, and (b) *Design 3*.

In contrast, by moving toward higher k_R in Fig. 12, we find that tuning a *Type 2* implementation to *Type 1* is not necessarily beneficial, since an increased C_1 brings more freewheeling capacitive energy to the system. *Type 2* to *Type 1* tuning is more efficient through adjustments of L_{eq} or ϕ.

C. Operation: Effects of Controllable Parameter Variation in a Designed Converter

By observing R_L variation in Fig. 10(c) toward a higher k_R, it is evident that the class-type resonant topologies naturally provide load-independent CV at their power switch terminals $v_{ds1,2}$. The voltage gain V_{gain} is a fixed value between 1.6 and 4 depending on circuit topologies and parameter values. Unlike other switch-mode power supplies, the output voltage of resonant converters is not adjustable through the duty cycle control. Instead, D needs to be selected based on resonance operations, which is an implementation parameter rather than a controllable operation parameter. Adjustment of D either leads to a lost ZVS (toward higher values) or does not have any effect on V_{gain} (toward a lower D).

The voltage supply V_{DC} does not involve resonance operations, which has very limited effect on switching waveforms by affecting the power switch parasitic capacitance C_{oss}. Therefore, V_{DC} adjustment from a separate dc–dc converter stage can be used to control the ac voltage output.

Targeting a constant-current (CC) output feature for certain applications, e.g., a WPT system or in a battery charging scenario, the load-independent CC can be realized by adjusting load angle ϕ from operation frequency f_s. We take the series–series tuned WPT system in Fig. 14(b) as an example. Typically, the transmitter (Tx) coil L_{Tx} is tuned to a resonance at f_s by a series capacitor C_{Tx}. Different tuning frequencies ω_r can be used to obtain a load angle other than zero, following

$$\omega L_x = \omega L_{Tx} - \frac{1}{\omega C_{Tx}}, \text{ where } \omega_r^2 L_{Tx} C_{Tx} = 1. \tag{13}$$

Therefore, maintaining the same i_{AC} under a reduced resistive load power is equivalent to maintaining the same Z_{AC} with an increased ϕ. By slightly increasing the operation frequency ω

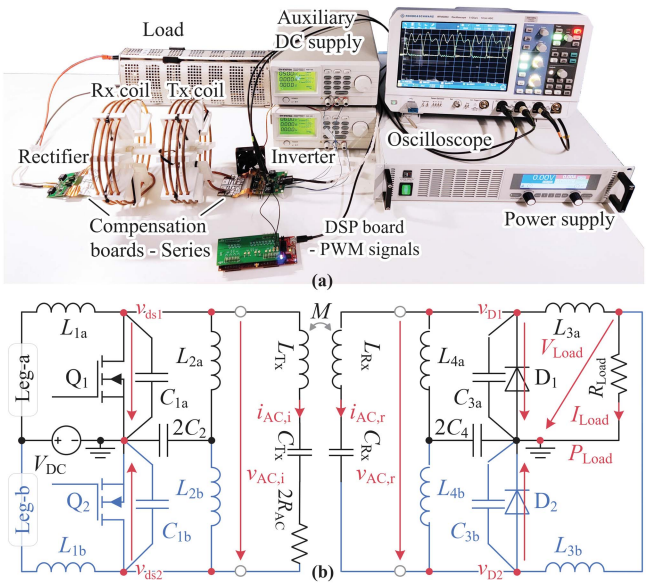


Fig. 14. WPT system (a) experiment setup and (b) equivalent circuit.

from its nominal value ω_s, k_P is obtained as

$$k_P = \left(1 - \frac{\omega_r}{\omega_s}\right) \frac{L_{Tx}}{C_1 Z_{AC}^2} \tag{14}$$

which also shifts toward a higher value. Therefore, frequency adjustment maintains i_{AC} under a reduced load power, moves the operation point toward higher k_R, k_P, with slightly dropped k_L, n. A load-variation trajectory from nominal to 0 % power is shown in Fig. 11(a). The converter secures soft switching (*Type 1* → *Type 2*) during the whole process, but exhibits increased fluctuations in v_{ds} waveforms.

D. Converter Design Examples Based on Data-Driven Models

The data-driven models obtained from *Steps 5 and 10* enable fast generation of a large number of new soft-switching designs, which supports converter design optimization. To present benefits from the wide design space coverage of the proposed method, we demonstrate how to use data-driven models for converter design on top of three different specifications in the load resistance, power levels, and output features (CC/CV). Details and the design outcomes are presented in Table IV.

1) Design 1: CV Output With a Low Nominal Resistance: We first showcase a WPT system design under the same specifications as in [5]: $f_s = 6.78$ MHz, $R_L = 11\,\Omega$, $P_{AC} = 100$ W, and CV output feature.

According to the working frequency, a possible combination of L_{eq} and C_1 is obtained from (11) as nH to μH and pF to nF, respectively. Power switches can be selected among Gallium Nitride Field-Effect Transistor (GaN-FETs) [25], e.g., *GS61004B, GS66504B, GS66508B*. Targeting a low voltage stress that enables 100V-GaN, we select $n=2$. To minimize ferrite losses especially for MHz frequency operation, we can use several nH-level air-core power inductors available on the market [10]. $L_{air} \in [33, 108, 257, 390, 430, 500]$ nH are taken as available options for L_2. The power switch output capacitance C_{oss} sets a limitation on the minimum feasible C_1. To get a robust v_{ds} waveform, we add 100 pF tolerance. ϕ is set to zero due to the requirement of CV output.

Under given design requirements, including specifications and available building components, we create the input space (k_L, k_R) and make predictions using data-driven models obtained in Step 10, Table V. By applying all filtering conditions, e.g., $L_2 \in L_{air}$, $C_1 > C_{oss} + 100$ pF, $\phi \geq 0$, $v_{ds(max)} < 100$ V, the feasible design space is obtained as Fig. 13(a) at the $R_L = 11\,\Omega$ boundary line. To pursue a high efficiency, *Design 1* is selected with the smallest feasible k_R. Corresponding waveform and parameters are given in Table IV.

2) Design 2: CV Output With a High Nominal Resistance: Under a high nominal R_L, the converter should be redesigned targeting a *Type 1* full-load operation rather than conducting reduced-power operations using the low R_L converter. While efficiency optimization under a high R_L is challenging due to the restriction from C_{oss}, it is no more a concern in the proposed method. Going through the same steps as the *Design 1* example and targeting *GS66504B* for 200 W power, modified filtering conditions $L_2 \in [L_{air}, 2L_{air}]$, $v_{ds(max)} < 650$ V provide a smaller design area surrounded by the $R_L = 30\,\Omega$ boundary in Fig. 13(a), where *Design 2* is selected based on the same rule of the optimal efficiency.

3) Design 3: CC Output With a Low Voltage Stress: Based on the understanding of parameter variation effects from Section V, CC output feature can be realized by either a high inductive load, or an adjusted frequency following load variations. The first option suffers from a low efficiency due to a high freewheeling reactive power. Here, we select a relatively small ϕ value, and realize CC using the frequency control.

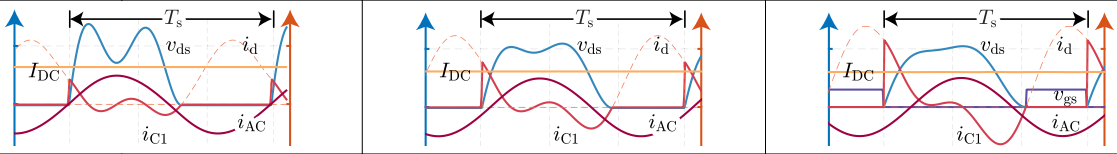
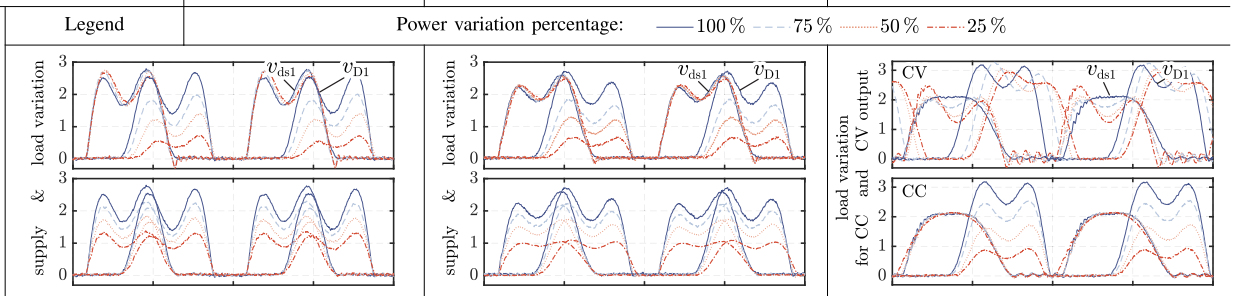
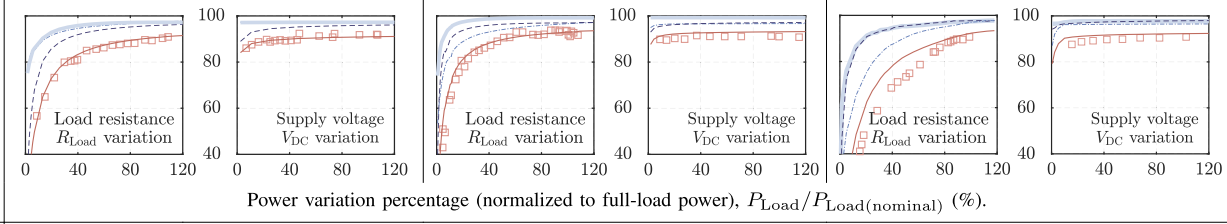
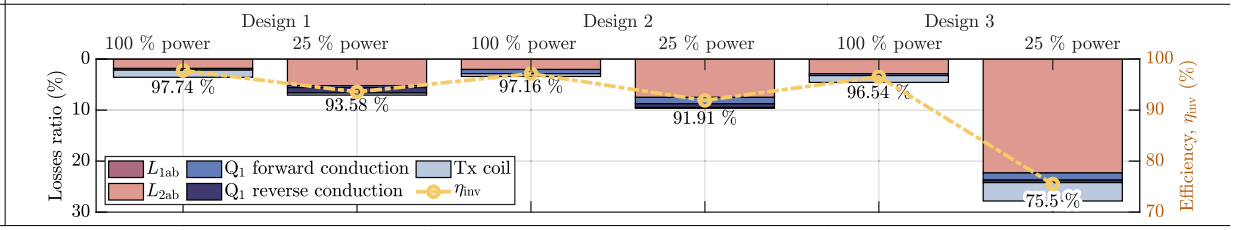
Targeting a high overall efficiency, *GS61004B* is selected due to its low on-state resistance $R_{ds(on)} = 37$ mΩ. Thus, we need to optimize toward a minimum voltage stress under the specified power output of 100 W. Fig. 13(b) is generated for $v_{ds(max)} = v_{ds(max)norm} \cdot 2\sqrt{P_{AC} R_{AC}}/\cos\phi$, where ϕ and $v_{ds(max)norm} = v_{ds(max)}/V_{AC}$ are predicted from data-driven models f_1 and f_p, obtained in Table V.

VI. Experimental Setups and Measurements

To validate the *design accuracy from data-driven-models* and *circuit-operation analysis based on the full-freedom space* in Section V, we built the WPT system in Fig. 14(a) using the three designs in Section V-D. Based on the equivalent circuit in Fig. 14(b), the entire WPT system is built since the realization of a purely resistive impedance is challenging in practice. The same labels are used for Table IV. Fig. 14(b) shows a clearer topological symmetry between the inverter and the rectifier, which are both designed with the same data-driven models. Auxiliary dc supplies are used for gate drivers, with the power consumption around 0.3 W.

For all three systems, the oscilloscope measurements of v_{ds} and v_D waveforms are presented in Table IV under 100 % to 25 % load power, obtained from variations of the load resistance R_{Load} and supply voltage V_{DC}, respectively. The experimental

TABLE IV
COMPARISON BETWEEN THREE SETS OF WPT SYSTEM IMPLEMENTATIONS

Design specifications and selected working points			
	Design 1	*Design 2*	*Design 3*
$V_{DC}, R_{AC}, R_{Load}, P_{Load}$	30 V, 11 Ω, 8.3 Ω, 100 W	65 V, 30 Ω, 21.3 Ω, 200 W	36 V, 15 Ω, 24.8 Ω, 100 W
Inverter design target	CV output, optimal efficiency		CC output, minimum voltage stress
$D, k_L, k_R, k_P, n, \phi$	0.42, 4.78, 0.115, 0, 2, 0	0.37, 2.07, 0.391, 0, 2.06, 0	0.31, 1.12, 0.89, 0.405, 2, 0.11π
Simulation curves			
Experiment implementation and measurement results			
Power switches	*GS61004B*	*GS66504B*, 650V, 15A	*GS61004B*, 100V, 30A
Rectifier diodes	*PMEG100T100E*, 10A	*C6D10065E*	*C6D10065E*, 650V, 10A
L_1, L_2, L_3, L_4 (nH)	9200, 520, 9200, 520	11300, 1074, 11300, 1074	11300, 430, 11300, 1074
C_1, C_2, C_3, C_4 (pF)	150, 530, 150, 512.2	100, 259.7, 100, 258.9	1000, 6170, 100, 258.9
Experimental waveforms * voltage normalized to V_{DC}			
Efficiency (%)			
Loss distributions			

* The experimental waveforms are measured with oscilloscope *RTM3004 Rohde & Schwarz*, taken in both formats of screenshot and data and replotted in *MATLAB*. Nominal operating frequency f_s = 6.78MHz.

v_{ds} waveforms in Table IV show good consistency with the simulation curves in the same table, confirms the implementation accuracy of our design method.

During load variation, we see that the inverter v_{ds} waveforms are almost constant against R_{Load} variations in *Designs 1 and 2*, presenting CV output characteristics. To realize a CC output inverter, which gives CV output at the system dc output, frequency adjustment has to be applied, resulting in a gradual movement of v_D waveforms during power variation. The v_{ds} waveform was designed to have flat peaks to leave enough margin for the increased fluctuation amplitude during frequency variations. At the 25 % load, the voltage stress is still 89 V, leaving 11 V margin compared to the 100 V voltage rating of *GS61004B*.

Moreover, the supply voltage variation in Table IV shows negligible effect on switching operations, i.e., v_{ds} waveforms, since V_{DC} is not included in any dimension of the full-freedom space in Fig. 11. The small change in v_{ds} shape comes from the variation of C_{oss} due to the change of voltage stress.

Finally, the end-to-end system efficiency η_{tot} is also measured for three WPT systems under power variations, shown in

TABLE V
PROPOSED SURROGATE-MODELING WORKFLOW FOR RESONANT CONVERTER DESIGN†

Steps				*Type1*	*Type2*	*Steps*	
1	Input parameter preparation	(1)	Define input space	$a_{\mathrm{x}} = \arctan(k_{\mathrm{L}})/\pi \in (0, 0.5)$, $a_{\mathrm{y}} = \arctan(k_{\mathrm{R}})/\pi \in (0, 0.5)$, $n \in (1, 4]$.		(1)	6
		(2)	Pre-processing	For rectifier simulation *, $a_{\mathrm{yr}} = \arctan(\omega_s C_1 R_{\mathrm{Load}})/\pi$	Generate 3D space $(a_{\mathrm{xi}}, a_{\mathrm{yi}}, a_{\mathrm{z1}}, D_{\mathrm{i}})$ from *Step 5*(1), where $a_{\mathrm{z1}} \in (a_{\mathrm{zi}}, 0.5)$, $a_{\mathrm{zi}} = \arctan k_{\mathrm{Pi}}/\pi = \arctan(\tan\phi_{\mathrm{i}}/k_{\mathrm{Ri}})/\pi$	(2)	
		(3)	Prepare simulation input	$V_{\mathrm{AC}}, f_{\mathrm{s}}, R_{\mathrm{Load}}, L_3, L_4, C_3, C_4$	$V_{\mathrm{DC}}, f_{\mathrm{s}}, R_{\mathrm{L}}, L_1, L_2, C_1, C_2, R_{\mathrm{AC}}, L_{\mathrm{x}}$	(3)	
2	Simulation and waveform sampling			Rectifier: $v_{\mathrm{AC}}, i_{\mathrm{AC}}, v_{\mathrm{D}}, i_{\mathrm{D}}, i_{\mathrm{C3}}, i_{\mathrm{C4}}$	Inverter: $v_{\mathrm{gs}}, v_{\mathrm{ds}}, i_{\mathrm{d}}, i_{\mathrm{C1}}, i_{\mathrm{C2}}, i_{\mathrm{AC}}$		7
3	Waveform feature extraction	(1)	Feasibility criteria	v_{ds} zero-crossings $= 2$	$v_{\mathrm{ds}}(t_{\text{s-on}}) \le 0$, and v_{ds} zero-crossings $= 2$	(1)	8
		(2)	Operation parameters	$\phi_{\mathrm{i}}, D_{\mathrm{i}}$ * see Fig. 8, Section IV-A $a_{\mathrm{yi}} = \arctan(\omega_s C_1 R_{\mathrm{L}})/\pi$, $a_{\mathrm{xi}} = a_{\mathrm{xr}}$	$D_1 =$ (time interval $v_{\mathrm{ds}} = 0)/T_{\mathrm{s}}$	(2)	
		(3)	Performance parameters	$v_{\mathrm{ds(max)}}, i_{\mathrm{d(max)}}, i_{\mathrm{d(rms)}}, i_{\mathrm{L(rms)}}, I_{\mathrm{AC}}, V_{\mathrm{gain}}, c_{\mathrm{p}}, \eta, \cdots$		(3)	
4	Exploratory data analysis and data cleaning			Filter out non-feasible samples			9
5	Model training	(1)	Design models $\boldsymbol{f_{1,2,3}}$	$\phi_{\mathrm{i}} = \boldsymbol{f_1}(a_{\mathrm{xi}}, a_{\mathrm{yi}})$, $D_{\mathrm{i}} = \boldsymbol{f_2}(a_{\mathrm{xi}}, a_{\mathrm{yi}})$	$D_1 = \boldsymbol{f_3}(a_{\mathrm{xi}}, a_{\mathrm{yi}}, a_{\mathrm{z1}})$	(1)	10
		(2)	Performance models $\boldsymbol{f_p}$	Normalized performance features $= \boldsymbol{f_p}(a_{\mathrm{x}}, a_{\mathrm{y}}, a_{\mathrm{z}}, n, D)$, $p = 4, 5, \cdots$		(2)	

† Circuit parameters used in the table refer to Fig. 14(b). * Subscript "*r*" and "*i*" denotes parameters calculated from rectifier and inverter operations, respectively.

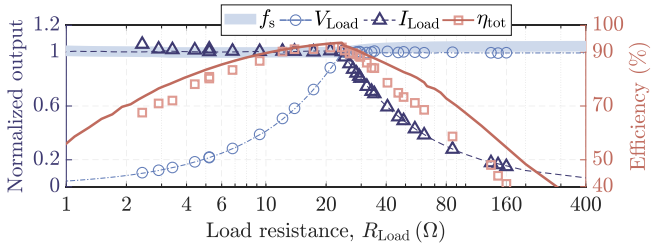


Fig. 15. CC to CV charging profile with regard to R_{Load} variation.

Table IV, and simulation results present efficiency breakdown of inverter η_{inv}, rectifier η_{rect}, and the WPT link η_{WPT}.

To compare the three systems, a loss distribution barchart is given in the last row of Table IV. *Design 1* has the lowest power switch conduction loss due to the selection of a low $R_{\mathrm{ds(on)}}$ power switch and low reactive power (i.e., the minimum feasible k_{R}). In comparison, *Design 2*, which has a high load resistance, easily realizes low Tx losses due to a lower I_{AC} current. All the full-loaded operations have zero reverse conduction loss. The L_2 power losses occupy a relatively high percentage, due to the low-quality factor $Q \approx 75$ at 6.78 MHz [10]. The loss distribution provides us a direction of efficiency optimization, which can be realized by optimizing the air-core inductors L_2 with a higher Q factor. Moreover, *Design 3* suffers from a faster efficiency drop with regard to load variations. The rapid loss increment comes partly from the high CC in Tx coil, which drops to zero at an empty load in *Designs 1 and 2* due to their CV output features. Furthermore, the lower L_2 value in *Design 3* also leads to a higher differential inductive current, following $i = \frac{1}{\omega_s L_2} \int (v_{\mathrm{ds1}} - v_{\mathrm{ds2}})$. Therefore, given the low Q-factor of L_2, *Design 3* suffers from a rapid increase in L_2 losses under the low load percentage.

Nevertheless, the *Design 3* achieves reliable CC at the inverter output, which secures a CV system output when R_{Load} increases from its nominal value. Moreover, the low nominal ϕ value also supports CC output for the WPT system, following an R_{Load} reduction from its nominal value. An f_{s} adjustment helps to fine-tune the system output and realize a stable R_{Load}-independent CV. As shown in Fig. 15, we get the full CC–CV load charging profile under R_{Load} variations, which models a battery charging scenario.

VII. CONCLUSION

Analytical modeling of resonant converters suffers from a conflict between accuracy and complexity, leading to limited design freedom and low implementation accuracy. To overcome these limitations, this article introduces a data-driven design approach that unlocks full coverage of the soft-switching parameter space and enables fast modeling and optimization. We have obtained the following conclusions.

1) Heavily relying on locally valid derivations and random numerical solving, existing analytical methods failed to deliver accurate models for wide-freedom design optimizations. The data-driven models directly trained from ideal-circuit simulation data successfully handle the accuracy concern and is free from complicated derivations, are proved to be a more accurate and transferrable replacement of traditional numerical design equations.
2) Training performance of data-driven models is highly linked to dataset quality. We propose an innovative mirrored-circuit simulation method combined with a resonant-capacitor-based decouple strategy to overcome the low accuracy and low sampling efficiency from typical parameter-sweep simulations. With significantly reduced time and computational resources, the two data enhancing methods successfully deliver highly diverse and representative samples, enabling exploration of the full-freedom design space.
3) Benefited from the outcome of data-driven modeling, the significantly widened and decoupled design space that maps design parameters to waveform shaping

performance, we get more systematical understanding of converter operations under all parameter dimensions. We identifies 7 switching types for future tuning guidance, and the designs satisfying both ZVS and ZDS are proved to be more superior in efficiency than their counterparts with only ZVS feature. The frequency-adjustment trajectory provides us an innovative view to realize CC output during inverter load adjustment.

In principle, the proposed data-driven modeling approach is transferrable to any resonant topology, provided that two key conditions are met: 1. topological symmetry between the inverter and rectifier, and 2. a capacitor parallel to the power switch enables the soft-switching. Nevertheless, it would be interesting to further investigate detailed process applicable to different resonant topologies.

It is worth noticing that the quality of dataset preparation always crucially affects the accuracy of data-driven modeling methods. In this work, we provided solutions from perspective of power electronics with two data enhancement strategies. From machine learning perspective, optimization of hyperparameter values also affects model accuracy and is worth investigating.

APPENDIX

This Appendix explains the workflow in Section IV-C with detailed parameter labels from the example circuit, full-freedom PPT Class Φ_n topology in Fig. 1(d). Illustrated by Table V, the workflow begins with modeling the *Type 1* distribution, from which new *Type 2* data are generated. These data are then used to train a comprehensive model incorporating additional output features.

A. Type 1 *Data Generation and Surrogate Model Training*

Since specifications $V_{\rm AC}, R_{\rm Load}, f_{\rm s}$ are not independently involved in the design space, we assign fix values of 50 V, 10 Ω, and 6.78 MHz, respectively. The remaining rectifier simulation inputs can be derived from (3), (4), and (10)–(12).

Next, simulations and feature extraction follow the analysis in Section IV-A. Feasible datasets consisting of inputs $(a_{\rm x}, a_{\rm y})$ and outputs, i.e., the operation parameters (ϕ, D), are then used for model training in MATLAB *Regression Learner*.

Once training is complete, we obtain *Type 1* surface models $\phi = f_1(a_{\rm x}, a_{\rm y})$ and $D = f_2(a_{\rm x}, a_{\rm y})$, serving as the foundation for circuit realization. Performance models can be deferred until *Step 10* and trained together with *Type 2* samples.

B. Type 2 *Data Generation and Surrogate Model Training*

After *Type 1* surfaces are obtained for each n value, *Type 2* designs are distributed across the space above *Type 1* surfaces. To realize full coverage, we generate new $a_{\rm z1}$ data from the predicted surface $a_{\rm zi} = f_1(a_{\rm xi}, a_{\rm yi})$. The new sampling space for a specified n is $(a_{\rm xi}, a_{\rm yi}, a_{\rm z1}, D_{\rm i})$, where $a_{\rm z1} > a_{\rm zi}$.

Similarly, we assign inverter simulation specifications $V_{\rm DC}$, $R_{\rm L}$, $f_{\rm s}$ to 50 V, 10 Ω, and 6.78 MHz. The remaining inverter building parameters can be calculated from (3) to (12).

From inverter simulations, the updated duty cycle for *Type 2* implementations is determined by normalizing the actual time interval of $v_{\rm ds}=0$ to the entire switching period $T_{\rm s}$. *Type 6* designs are considered not feasible in both simulations and should be excluded from the training dataset. Thus, the entire soft-switching space, fully covered by *Types 1 and 2* samples, is used to train a predictive model: $D = f_3(a_{\rm x}, a_{\rm y}, a_{\rm z})$.

C. Surrogate Model Training of Performance Parameters

Finally, we can analyze the circuit operating performance of both *Types 1 and 2* samples from waveform feature extractions.

Common performance metrics for converters include voltage/current stress $v_{\rm ds(max)}, i_{\rm d(max)}$, power output capability $c_{\rm p} = P_{\rm AC}/[2v_{\rm ds(max)}i_{\rm d(max)}]$, voltage gain $V_{\rm gain} = V_{\rm AC}/V_{\rm DC}$, rms current components $i_{\rm d(rms)}, i_{\rm L(rms)}$ for loss estimation, efficiency η, etc. For a fair comparison, evaluations should be conducted under the same design specifications, i.e., the output power. Accordingly, surrogate models can be trained using normalized features, e.g., current scaled to the real part of $i_{\rm AC}$ and voltage normalized to $V_{\rm DC}$.

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REFERENCES

[1] Y. Liu, Y. Zhang, J. Kyyrä, and F. Blaabjerg, "Data-based circuit design method for class Φ resonate converters," in *Proc. IEEE Des. Methodol. Conf.*, 2024, pp. 1–7.
[2] S. Kee, I. Aoki, A. Hajimiri, and D. Rutledge, "The class-E/F family of ZVS switching amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 6, pp. 1677–1690, Jun. 2003.
[3] Z. Kaczmarczyk, "High-efficiency class E, EF_2, and E/F_3 inverters," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1584–1593, Oct. 2006.
[4] S. Aldhaher, D. C. Yates, and P. D. Mitcheson, "Load-independent class E/EF inverters and rectifiers for MHz-Switching applications," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8270–8287, Oct. 2018.
[5] Y. Liu, P. Jayathurathnage, and J. Kyyrä, "A new simplified method and design guidelines for the optimization of push–pull class Φ_2 converters for wireless power transfer applications," *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 10442–10459, Aug. 2023.
[6] L. Gu, G. Zulauf, Z. Zhang, S. Chakraborty, and J. Rivas-Davila, "Push–pull class Φ_2 RF power amplifier," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10515–10531, Oct. 2020.
[7] D. Zhang et al., "Harmonic weighting and target function design strategy to minimize switch voltage stress of class Φ2 inverter," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 12289–12300, Oct. 2022.
[8] C. Cheng, Y. Zhang, X. Zheng, and W. Hua, "A full-range soft-switching class-e inverter achieving quasi-constant voltage output," *IEEE Trans. Power Electron.*, vol. 40, no. 6, pp. 7663–7667, Jun. 2025.
[9] S. Aldhaher, D. C. Yates, and P. D. Mitcheson, "Modeling and analysis of class EF and class E/F inverters with series-tuned resonant networks," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3415–3430, May 2016.
[10] Coilcraft Inc, "Square air core inductors," 2021. [Online]. Available: https://www.coilcraft.com/en-us/products/rf/air-core-inductors/square-air-core-inductors/1515sq-2222sq-2929sq/
[11] X. Zhao, C.-W. Chen, J.-S. Lai, and O. Yu, "Circuit design considerations for reducing parasitic effects on GaN-based 1-MHz high-power-density high-step-up/down isolated resonant converters," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 695–705, Jun. 2019.
[12] L. Roslaniec, A. S. Jurkov, A. A. Bastami, and D. J. Perreault, "Design of single-switch inverters for variable resistance/load modulation operation," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3200–3214, Jun. 2015.

[13] L. Lan, J. M. Arteaga, D. C. Yates, and P. D. Mitcheson, "A reflected impedance estimation technique for inductive power transfer," in *Proc. IEEE PELS Workshop Emerg. Technol. Wireless Power Transfer*, 2019, pp. 45–48.
[14] Y. Zhang, Y. Xu, and F. Blaabjerg, "Chapter 11—Surrogate models for power electronic systems applying machine learning techniques," in *Control of Power Electronic Converters and Systems*, vol. 4, F. Blaabjerg, Ed. London, U.K.: Academic, 2024, pp. 333–352.
[15] S. Zhao, F. Blaabjerg, and H. Wang, "An overview of artificial intelligence applications for power electronics," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4633–4658, Apr. 2021.
[16] L. Duchesne, E. Karangelos, and L. Wehenkel, "Recent developments in machine learning for energy systems reliability management," *Proc. IEEE*, vol. 108, no. 9, pp. 1656–1676, Sep. 2020.
[17] Y. Zhang, Z. Wang, H. Wang, and F. Blaabjerg, "Artificial intelligence-aided thermal model considering cross-coupling effects," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 9998–10002, Oct. 2020.
[18] H. Li et al., "How MagNet: Machine learning framework for modeling power magnetic material characteristics," *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 15829–15853, Dec. 2023.
[19] Z. Zhang, X.-W. Zou, Z. Dong, Y. Zhou, and X. Ren, "A 10-MHz eGaN isolated Class-Φ_2 DCX," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2029–2040, Sep. 2017.
[20] Y. Jiang, H. Li, Y. Liu, J. Liang, H. Wang, and M. Fu, "Multiconstraint design of single-switch resonant converters based on extended impedance method," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 2, pp. 1901–1912, Apr. 2023.
[21] C. Liu, Y. Guan, Y. Wang, and D. Xu, "A multi-matrix based network for multi-module parallel megahertz inverter system," *IEEE Trans. Power Electron.*, vol. 39, no. 9, pp. 11308–11317, Sep. 2024.
[22] Z. Liu, Z. Zhao, Y. Kai, Y. Lao, J. Wang, and F. Meng, "Demonstration of low DV/DT Class-Φ2 DC-DC converter with 50% duty cycle," *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 15759–15767, Dec. 2023.
[23] I. Nikiforidis, J. M. Arteaga, C. H. Kwan, N. Pucci, D. C. Yates, and P. D. Mitcheson, "Generalized multistage modeling and tuning algorithm for class EF and class Φ inverters to eliminate iterative retuning," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 12877–12900, Oct. 2022.
[24] X. Zhang et al., "An active learning framework for reliability oriented power electronics design," *IEEE Trans. Ind. Electron.*, early access. 2025, doi: 10.1109/TIE.2025.3577391.
[25] Infineon Technologies Canada Inc, "GaN transistors portfolio," 2025. [Online]. Available: https://gansystems.com/gan-transistors/

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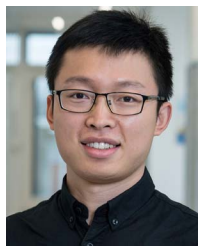

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