Letters

Current Saturation Ratio-Based Hybrid Synchronization Control of Grid-Forming Converters

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***Abstract*—Grid-forming (GFM) converters utilizing hybrid synchronization control (HSC) incorporate both power-synchronization loop (PSL)- and phase-locked loop (PLL)-based frequency components in the synchronization loop. However, existing implementations of HSC do not consider the physical current limits of GFM converters, are designed to only cater to specific types of grid disturbances, and exhibit inaccurate power setpoint tracking. In this letter, a current limit-informed HSC method is proposed to overcome these issues. The PSL and PLL components are weighted according to the current saturation ratio of the current limiter, as a proxy measure for the severity of a disturbance. In this way, the proposed method not only synergizes with current limiting control of GFM converters, but also works generally for any disturbance, which activates the current limiter. In addition, it tracks the active power setpoint accurately during unfaulted steady states, which also implies that a larger proportional gain can be used in the PLL, improving the design flexibility and dynamic performance. Experimental results demonstrate the enhanced performance of the proposed method over the PSL and existing HSC methods during grid frequency drops and voltage sags. The stability of the proposed method under weak grid conditions is also experimentally verified.**

***Index Terms*—Current limiting, grid-forming (GFM) converters, hybrid synchronization control (HSC), synchronization stability.**

I. Introduction

GRID-CONNECTED converters can generally be classified into grid-forming (GFM) and grid-following (GFL), depending on their control structures and synchronization mechanisms. GFM converters commonly utilize a power-synchronization loop (PSL) to synchronize with the grid, while GFL converters generally use a phase-locked loop (PLL) [1]. However, PSL-based GFM converters tend to lose synchronization during large disturbances when current limiting control is used, and PLL-based GFL converters exhibit poor synchronization stability in weak grids [2]. Recently, to address the limitations of each, hybrid synchronization control (HSC) methods have been proposed, which incorporate features of both GFM and GFL converters [3], [4], [5]. This is achieved by combining frequency components from both PSL and PLL in the synchronization loop.

The first proposal of HSC in [3] improves the transient stability of GFM converters by increasing the system damping compared to the conventional PSL [6]. However, the PSL and PLL components are assigned fixed weightings, which inevitably compromise the design flexibility. Adaptive weightings of the PSL and PLL components have been proposed to respond to changing external conditions. In [4], the weightings are adjusted based on the grid strength to ensure small-signal stability under varying short circuit ratios (SCRs). However, the large-signal stability is not studied, which raises doubts about its synchronization capability during large grid disturbances. The implementation in [5], henceforth, termed voltage-based HSC (V-HSC), adjusts the weightings based on the magnitude of the measured voltage at the point of common coupling (PCC). The PLL is weighted more heavily during voltage sags to improve synchronization stability. However, the performance of this method is only demonstrated during voltage sags, and the adaptive weightings take no effect during disturbances that do not alter the measured voltage magnitude (e.g., frequency drops), where the method exhibits behavior similar to the PSL. Frequency drops are also common grid disturbances of critical interest, during which GFM converters should be designed to maintain synchronization and respond appropriately [7].

One of the mechanisms of synchronization stability enhancement of HSC methods is a reduction in the equivalent active power setpoint when PLL components are incorporated [5]. However, this leads to inaccurate power setpoint tracking [6]. Furthermore, existing implementations of HSC do not consider the effects of physical current limits of GFM converters. This leaves a crucial research gap as the use of current limiters within GFM control can have profound negative impacts on synchronization stability [8]. While methods to mitigate these issues for PSL-based GFM converters have been proposed [9], [10], design

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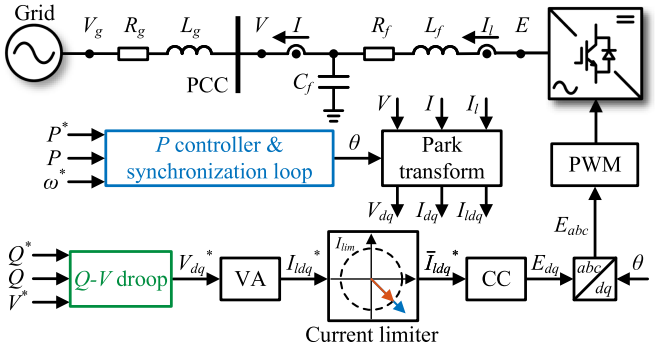

Fig. 1. Configuration of GFM converters with current limiters.

for HSC-based GFM converters with current limiters has been neglected in the literature thus far. Major limitations of existing HSC methods are summarized as follows:

1) Current limits are not considered in the design.
2) During steady states, the addition of a PLL component adjusts the equivalent active power setpoint, causing the GFM converter to exhibit inaccurate power setpoint tracking [6].
3) The adjustment of weighting factors is not designed in a systematic and intuitive way, raising concerns about the generality of such methods under different grid conditions. For example, in [5], no derivations are given to justify the chosen profile of weighting factor with respect to voltage magnitude, and the method is only verified during voltage sags.

To address these issues, this letter proposes a modified HSC method for GFM converters considering current limits, where the weightings of the PSL and PLL components are adjusted based on the current saturation ratio (CSR). In this way, not only is the HSC method adapted to coordinate with current limiters, but they also synergize by utilizing the CSR as a feedback signal to enhance synchronization stability. Compared with prior work, the main advantages of the proposed method are as follows:

1) HSC incorporating both GFM and GFL characteristics is adapted to coordinate with current limiters.
2) Accurate power setpoint tracking is achieved in steady states when the current limiter is not activated.
3) It is a general method that improves synchronization stability for all types of severe disturbances, which activate the current limiter.

II. HSC Based on Current Saturation Ratio (CSR)

Fig. 1 shows the configuration of GFM converters incorporating outer loop active and reactive power controllers cascaded with a virtual admittance (VA) [11], current limiter, and dq-decoupled proportional-integral (PI) current controller. $Q-V$ droop control is used as the reactive power controller.

The active power controller (marked blue) also provides the synchronization capability of the GFM converter by generating the internal frequency and phase angle. Fig. 2 shows the structure of the active power controller/synchronization loop of HSC-based GFM converters. $\Delta\omega_{\rm psl}$ and $\Delta\omega_{\rm pll}$ denote the frequency

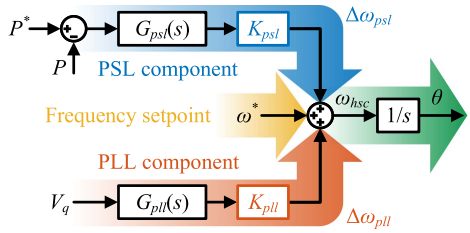

Fig. 2. Synchronization loop of HSC-based GFM converters, incorporating both PSL and PLL components.

deviations of the PSL and PLL components, respectively, which are added to the frequency setpoint ω^*. The transfer functions of the PSL and PLL are given by

$$G_{\rm psl}(s)=\frac{1}{Js+D_p}, G_{\rm pll}(s)=K_{p,\rm pll}. \tag{1}$$

Further, the outputs of these transfer functions are scaled by the weighting factors $K_{\rm psl}$ and $K_{\rm pll}$, respectively. This allows dynamic adjustment of the proportions of PSL- and PLL-based behaviors in response to changing grid conditions, particularly during disturbances. The internal angular frequency generated by HSC is given by

$$\omega_{\rm hsc}=\omega^*+\Delta\omega_{\rm psl}+\Delta\omega_{\rm pll} \tag{2}$$

where

$$\Delta\omega_{\rm psl}=K_{\rm psl}G_{\rm psl}(s)(P^*-P)=K_{\rm psl}\left(\frac{P^*-P}{Js+D_p}\right) \tag{3}$$

$$\Delta\omega_{\rm pll}=K_{\rm pll}G_{\rm pll}(s)V_q=K_{\rm pll}\left(-K_{p,\rm pll}V\sin\delta\right). \tag{4}$$

Note that δ is defined as the angle difference between the internal voltage and the PCC voltage phasors ($\delta=\theta-\theta_{\rm pcc}$).

A. Design of PSL and PLL Weightings

Using the notations in Fig. 1, the CSR is defined as

$$\sigma=\frac{\bar{I}^*_{ldq}}{I^*_{ldq}}. \tag{5}$$

This value is a measure of the amount by which the current limiter is saturating the current references produced by the VA after exceeding the maximum allowable threshold $I_{\rm lim}$. Thus, it is applicable to all disturbances during which the current limiter is activated, as a proxy measure for the severity of a disturbance. In the proposed design (termed as CSR-HSC), the PSL and PLL frequency components are weighted as

$$\begin{cases}K_{\rm psl}=\sigma\\ K_{\rm pll}=1-\sigma\end{cases} \tag{6}$$

which is intuitive as a smaller value of CSR implies a more severe disturbance, during which the PSL should be weighted less, and the PLL more, to maintain synchronization.

HSC methods produce an equivalent active power setpoint, inertia factor, and damping factor, obtained by substituting (3) and (4) into (2) and rearranging into the form of the conventional synchronous machine swing equation. Further substituting (6)

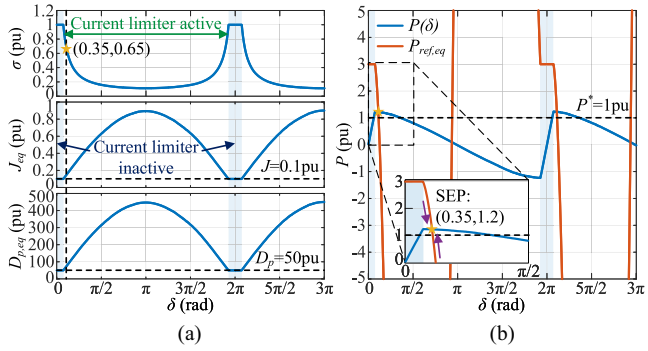

Fig. 3. Synchronization stability analysis of the proposed CSR-HSC method. (a) Plots of σ, J_{eq}, and $D_{p,\text{eq}}$ as functions of δ. (b) $P(\delta)$ and $P_{\text{ref,eq}}$ when $\Delta\omega = 0.04$ p.u.

yields

$$P^*_{\text{eq}} = P^* - \frac{(1-\sigma)D_p K_{p,\text{pll}} V \sin\delta}{\sigma} \tag{7}$$

$$J_{\text{eq}} = \frac{J}{\sigma}, \tag{8}$$

$$D_{p,\text{eq}} = \frac{D_p + (1-\sigma)JK_{p,\text{pll}} V \cos\delta}{\sigma}. \tag{9}$$

The equivalent active power setpoint should be reduced ($P^*_{\text{eq}} < P^*$) to improve synchronization stability during grid disturbances; however, during unfaulted steady states, this effect should be minimized to ensure accurate power setpoint tracking. Thus, CSR-HSC is designed to not affect the steady-state performance of GFM converters when the current limiter is not activated. That is, when $|I^*_{ldq}| \leq I_{\text{lim}}$ (which is the case during nominal unfaulted conditions), $\sigma = 1$ and $P^*_{\text{eq}} = P^*$ according to (7); therefore, accurate power setpoint tracking is achieved. Due to this fact, CSR-HSC also has more flexibility in designing the PLL proportional gain $K_{p,\text{pll}}$. Existing HSC methods must find a balance between fast frequency tracking and accurate power setpoint tracking, since a larger $K_{p,\text{pll}}$ comes at the cost of a larger active power error according to (7). This tradeoff does not need to be made for CSR-HSC.

B. Analysis of Synchronization Stability

Equations (7)–(9) demonstrate that CSR-HSC reduces the equivalent active power setpoint P^*_{eq}, and increases the equivalent inertia J_{eq} and equivalent damping $D_{p,\text{eq}}$. Increasing J_{eq} and $D_{p,\text{eq}}$ restricts the deviation of δ during disturbances to improve synchronization stability [12]. In the proposed method, the PLL components are only added when the current limiter is activated (i.e., only during severe disturbances). In Fig. 3(a), the nonshaded regions represent values of δ for which the current limiter is active, during which the equivalent parameters deviate from their nominal values to improve the transient synchronization stability. After the disturbance, the current limiter exits saturation and the equivalent parameters will automatically return to their nominal values, allowing the GFM converter to rapidly return to the prefault equilibrium.

TABLE I
IMPACTS OF DESIGN PARAMETERS ON CHARACTERISTICS OF CSR-HSC

Parameter	σ	P^*_{eq}	J_{eq}	$D_{\text{p,eq}}$	$P_{\text{ref,eq}}$
J	✗	✗	✓	✓	✓
D_p	✗	✓	✗	✓	✓
$K_{p,pll}$	✗	✓	✗	✓	✓

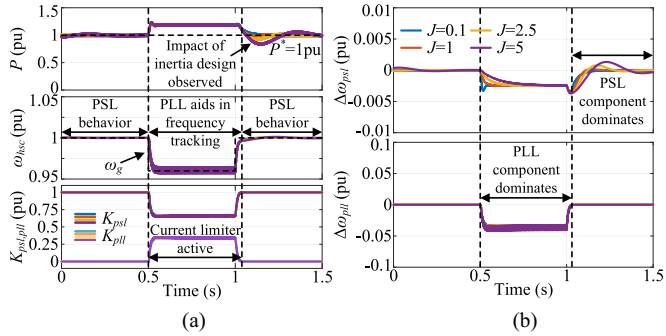

Fig. 4. Impact of inertia factor J on the transient performance of CSR-HSC. (a) Response during a grid frequency drop ($\omega_g = 0.96$ p.u.) with different values of J. (b) Frequency deviation components of the PSL and PLL.

To analyze the synchronization mechanism of the proposed CSR-HSC, Fig. 3(b) shows the $P(\delta)$ curve and a plot of the equivalent active power reference, defined as

$$P_{\text{ref,eq}} = P^*_{\text{eq}} + P_{d,\text{eq}} = P^*_{\text{eq}} + D_{p,\text{eq}}\Delta\omega \tag{10}$$

for a grid frequency drop to 0.96 per unit (p.u.) ($\Delta\omega = 0.04$ p.u.). The intersection between the two curves represents the stable equilibrium point (SEP), since for values of δ less than this point, P is lower than its reference, and δ will accelerate toward the SEP; and vice versa for values of δ greater than this point. The GFM converter will settle to the SEP once it adjusts its PSL and PLL weightings according to the CSR during the frequency disturbance. This case study is demonstrated experimentally in Section III.A.

C. Parameter Design

The main control parameters, which affect the dynamic performance of CSR-HSC, are the inertia and droop factors of the PSL (J and D_p), and the proportional gain of the PLL ($K_{p,\text{pll}}$). Table I shows the impacts of each parameter on the metrics relating to CSR-HSC. The key takeaways are as follows.

1) The PSL and PLL parameters do not impact σ, and hence do not affect the weightings of K_{psl} and K_{pll} during transients and faulted steady states.
2) All parameters impact $P_{\text{ref,eq}}$, which in turn affects the SEPs of CSR-HSC.

The droop factor D_p of the PSL should be designed in accordance with grid codes to dictate the active power response of GFM converters to frequency disturbances, and is set as 50 p.u. [13]. The inertia factor J dictates the amount of virtual inertia provided by the PSL, the design of which has been covered extensively in prior literature [7]. The difference between the conventional PSL and CSR-HSC can be analyzed through Fig. 4.

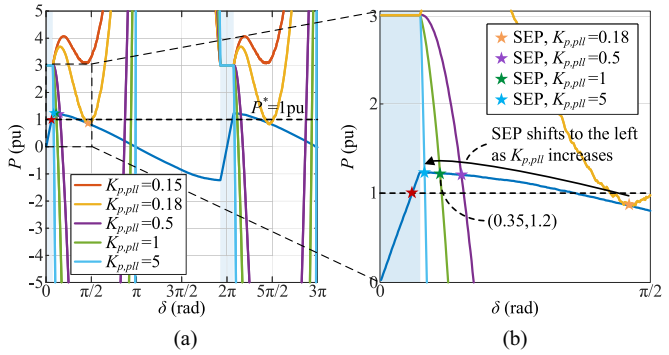

Fig. 5. Impact of $K_{p,\mathrm{pll}}$ on the SEP of CSR-HSC. (a) $P(\delta)$ and $P_{\mathrm{ref,eq}}(\delta)$ with different values of $K_{p,\mathrm{pll}}$ when $\Delta\omega = 0.04$ p.u. (b) Zoom-in plot showing SEPs.

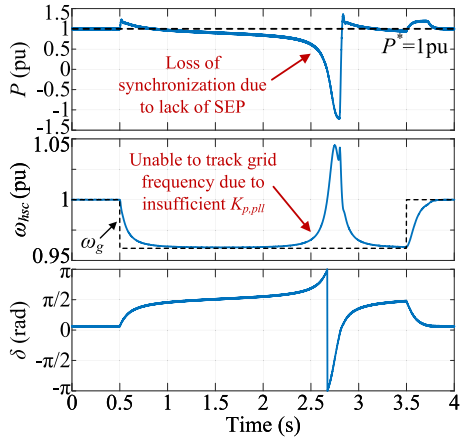

Fig. 6. Loss of synchronization of CSR-HSC due to an insufficient value of $K_{p,\mathrm{pll}} = 0.15$ rad/(V·s) causing nonexistence of SEPs during a grid frequency drop ($\omega_g = 0.96$ p.u.).

Fig. 4(a) shows the response of CSR-HSC during a grid frequency drop to 0.96 p.u. (48 Hz) for $t = 0.5 - 1$ s, with different values of J. Before the disturbance, the PLL weighting is zero since the current limiter is not saturated during nominal conditions. Dictated purely by the PSL, the GFM converter settles to a steady state with $P = P^* = 1$ p.u. and $\omega_{\mathrm{hsc}} = \omega_g = 1$ p.u. When the grid frequency drops, there is minimal difference in the response between the different J values. This is because during the disturbance, the current limiter saturates, causing the PLL weighting to increase. As observed in Fig. 4(b), the PLL frequency deviation component is more than ten times larger than the PSL frequency deviation component, and hence, the PLL dominates the frequency tracking behavior during the frequency drop. Therefore, the impact of J is negligible during this period. After the grid frequency returns to 1 p.u., the current limiter exits saturation (around $t = 1.05$ s), and the PLL weighting returns to zero. Therefore, the PSL behavior redominates, and the impact of the inertia design can be seen once again. Consistent with prior studies, larger values of J lead to slower changes in the internal frequency and reduced damping of the output power response [7]. Therefore, a small value of $J = 0.1$ p.u. is chosen to improve the postdisturbance recovery.

For the PLL, the integral gain $K_{i,\mathrm{pll}}$ is set as zero to achieve a first-order PLL. This is because a VA controller is used, which emulates a virtual impedance between the internal voltage phasor and the PCC, and thus, δ is always nonzero. Therefore, the objective of the integral gain, which is to reduce the steady-state error of $V_q = -V \sin\delta$ to zero, would conflict with the VA controller. Also, if the steady-state value of V_q is forced to zero, then $\Delta\omega_{\mathrm{pll}}$ would also converge to zero, nullifying the effect of the PLL on HSC during faulted steady states, essentially reducing it to the conventional PSL.

The proportional gain $K_{p,\mathrm{pll}}$ then becomes the only parameter to be tuned for the PLL component. $K_{p,\mathrm{pll}}$ impacts the transient performance of CSR-HSC by influencing its frequency tracking performance and steady-state operating point. A larger $K_{p,\mathrm{pll}}$ allows more accurate frequency tracking, which is particularly important during grid frequency disturbances. This also allows for faster recovery after the disturbance, as demonstrated experimentally in Section III.A. The SEP is also affected by $K_{p,\mathrm{pll}}$, as alluded to in Table I. Fig. 5(a) shows $P(\delta)$ and $P_{\mathrm{ref,eq}}(\delta)$ [as defined by (10)] for different values of $K_{p,\mathrm{pll}}$ during a grid frequency drop to 0.96 p.u. As seen when $K_{p,\mathrm{pll}} = 0.15$ rad/(V·s), $P_{\mathrm{ref,eq}}(\delta)$ has no intersection with the $P(\delta)$ curve, and therefore, no SEPs exist if $K_{p,\mathrm{pll}}$ is too small. Fig. 6 shows the response of CSR-HSC for $\omega_g = 0.96$ p.u. when $K_{p,\mathrm{pll}} = 0.15$ rad/(V·s). Since no SEP exists, the GFM converter is unable to settle at a steady-state operating point, and it loses synchronization with an ever-increasing δ since the output power P is constantly lower than the reference $P_{\mathrm{ref,eq}}$.

If $K_{p,\mathrm{pll}}$ is chosen larger than the critical value [0.18 rad/(V·s) in this case, shown by the yellow trace in Fig. 5, which just intersects the $P(\delta)$ curve], then SEPs will always exist. In fact, increasing it past this value shifts the SEP to the left, as seen in Fig. 5(b). This brings the SEP closer to the peak of the $P(\delta)$ curve, which is desirable as it means that the active power output during the frequency drop is higher, leading to improved frequency response. However, a value of $K_{p,\mathrm{pll}}$, which is too large, may lead to small-signal instability in weak grids [14]. In Section III-C, it is experimentally demonstrated that the PLL in CSR-HSC does not cause stability issues in weak grids if the parameters are tuned appropriately. Therefore, $K_{p,\mathrm{pll}}$ is chosen as 1 rad/(V·s) as a balance between transient performance and stability.

III. Experimental Validation and Comparison

An experimental setup is developed to validate the performance of GFM converters using the proposed CSR-HSC, and compare it with existing methods during different grid disturbances. The experimental prototype consists of a REGATRON TC. ACS grid simulator, a three-phase power converter, a Magna-power electronics programmable dc power supply, and a dSPACE DS1103 controller. The system and control parameters are given in Table II.

For the comparison, the methods will be labeled as follows: Method (a) is the conventional PSL; Method (b) is HSC [3]; Method (c) is V-HSC [5]; and Method (d) is the proposed CSR-HSC. $K_{p,\mathrm{pll}}$ is chosen as 0.15 rad/(V·s) for HSC and V-HSC to minimize power setpoint tracking error while still being able

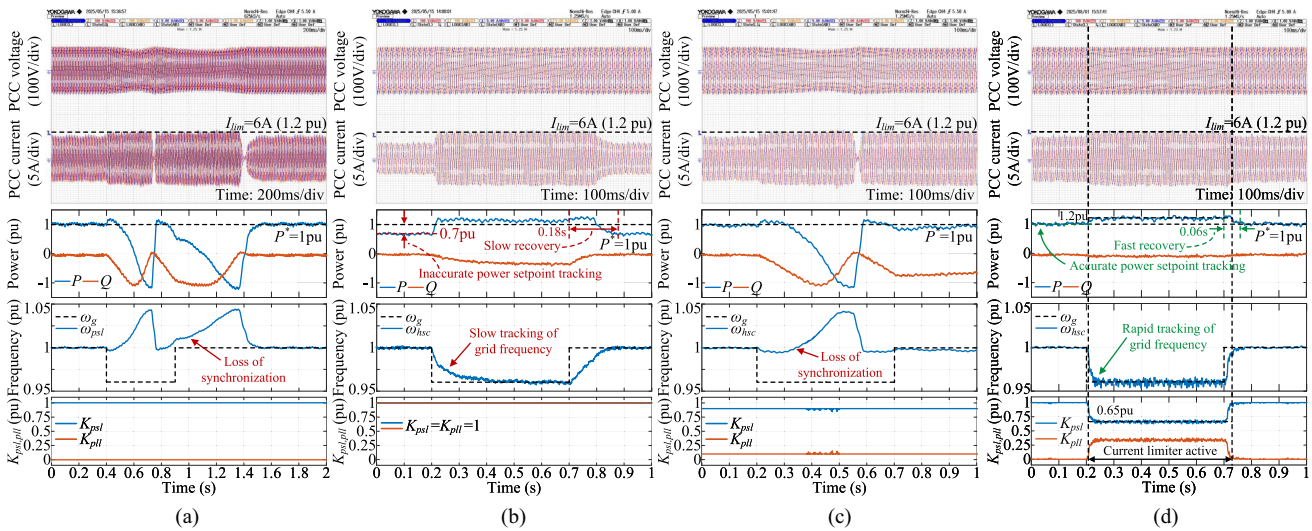

Fig. 7. Response of GFM converters during a grid frequency drop ($\omega_g = 0.96$ p.u. for 0.5 s and $P^* = 1$ p.u.). (a) With the PSL. (b) With HSC. (c) With V-HSC. (d) With the proposed CSR-HSC.

TABLE II
SYSTEM PARAMETERS

Parameter	Value	Parameter	Value
V_g (L-N, peak) (V)	100	L_f (mH)	3.44
$V_{\rm dc}$ (V)	300	R_f (mΩ)	88.7
$S_{\rm base}$ (VA)	750	C_f (μF)	4.65
$I_{\rm base}$ (peak) (A)	5	L_g (mH)	3.47
f_g (Hz)	50	R_g (mΩ)	80.9
f_s (kHz)	10	J (p.u.)	0.1
R_v (p.u.)	0.005	D_p (p.u.)	50
X_v (p.u.)	0.2	D_q (p.u.)	2
$I_{\rm lim}$ (p.u.)	1.2	$K_{p,pll}$ (rad/(V·s))	0.15–1

to track the grid frequency during frequency disturbances. For CSR-HSC, a larger value of 1 rad/(V·s) can be chosen for faster frequency tracking and improved transient performance.

A. Frequency Disturbances

Fig. 7 shows experimental results during a large grid frequency drop to 0.96 p.u. (48 Hz) for a duration of 0.5 s. Note that the instantaneous step change in frequency implies a zero-inertia grid condition, representing a worst-case scenario. This case matches the analysis in Section II.B. The results for CSR-HSC in Fig. 7(d) show $K_{\rm psl}$ settling at 0.65 p.u. [as marked in Fig. 3(a)] and P settling at 1.2 p.u. [see Fig. 3(b)] during the frequency drop. The PSL loses synchronization during the disturbance since the active power reference is unachievable due to the current limit [10]. Since the PCC voltage magnitude remains relatively unchanged during frequency disturbances, the weighting of V-HSC is ineffective and it loses synchronization similar to the PSL.

HSC and CSR-HSC both maintain synchronization. However, CSR-HSC exhibits the following advantages.

1) It tracks the active power setpoint accurately when the current limiter is not active (when $\omega_g = 1$ p.u.), while HSC only provides 0.7 p.u. of active power despite both being given the same setpoint $P^* = 1$ p.u.
2) It provides higher active power output during the disturbance, thereby enhancing its grid frequency support capability.
3) The larger $K_{p,\rm pll}$ allows closer tracking of the grid frequency, resulting in faster recovery after the frequency disturbance.

B. Voltage Sags

Fig. 8 shows experimental results during a grid voltage sag of 0.8 p.u. ($V_g = 0.2$ p.u.) for a duration of 0.5 s. The PSL loses synchronization and traverses the long recovery trajectory. HSC also loses synchronization, despite traversing the fast recovery trajectory. The internal frequency $\omega_{\rm hsc}$ cannot settle back to 1 p.u. during the fault, and therefore δ continuously increases until the fault is cleared. Note that it still exhibits the same power setpoint tracking error ($P \approx 0.7$ p.u.) during the unfaulted steady states. V-HSC and CSR-HSC exhibit comparable performance since V-HSC is designed specifically to improve synchronization during voltage sags. Both methods maintain synchronization by adjusting their PSL and PLL weightings to bring $\omega_{\rm hsc}$ back to 1 p.u. during the fault. They also provide voltage support through a reactive power output of 0.34 p.u., resulting in the PCC voltage being higher than that of the PSL and HSC, as seen in the oscilloscope traces.

C. Weak Grid Operation

In weak grids, small-signal stability of the PLL and VA becomes an important consideration. In this letter, the stability of CSR-HSC, which utilizes both, is demonstrated experimentally in weak grids. Fig. 9 shows the response of CSR-HSC during the same frequency drop as in Section III.A, under different grid strengths. The SCR is varied from 17.78 to 5.91 by adjusting the grid inductors in the experimental setup. To ensure small-signal stability in weak grids, $K_{p,\rm pll}$ is decreased according to [14], and the VA parameters are increased according to [15]. The adjusted parameters are given in Table III. Fig. 9(b) shows that the PLL

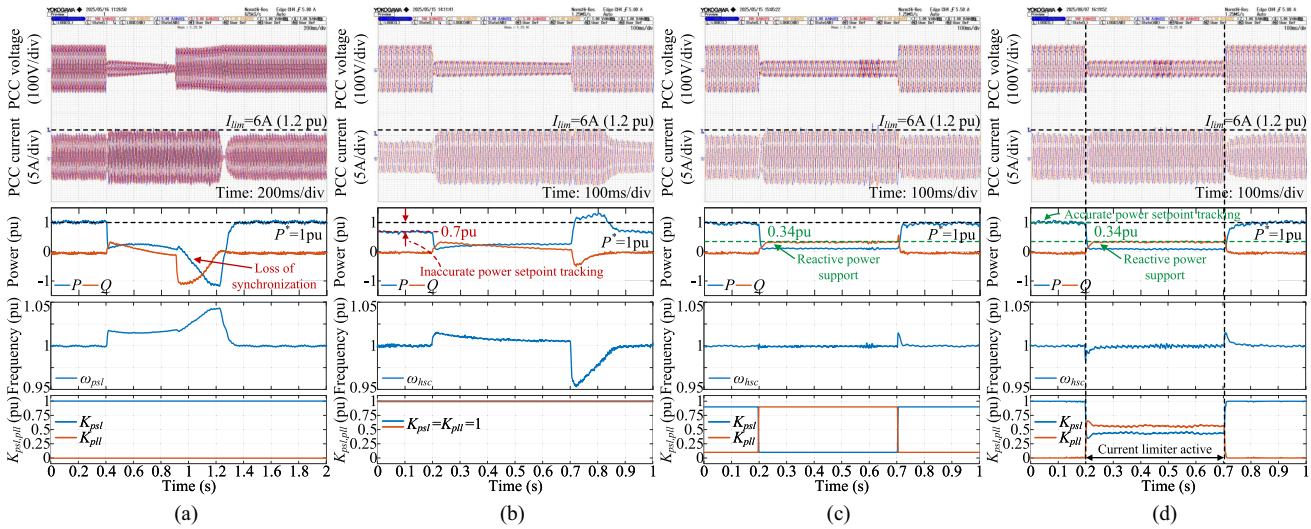

Fig. 8. Response of GFM converters during a grid voltage sag ($V_g = 0.2$ p.u. for 0.5 s, $P^* = 1$ p.u.). (a) With the PSL. (b) With HSC. (c) With V-HSC. (d) With the proposed CSR-HSC.

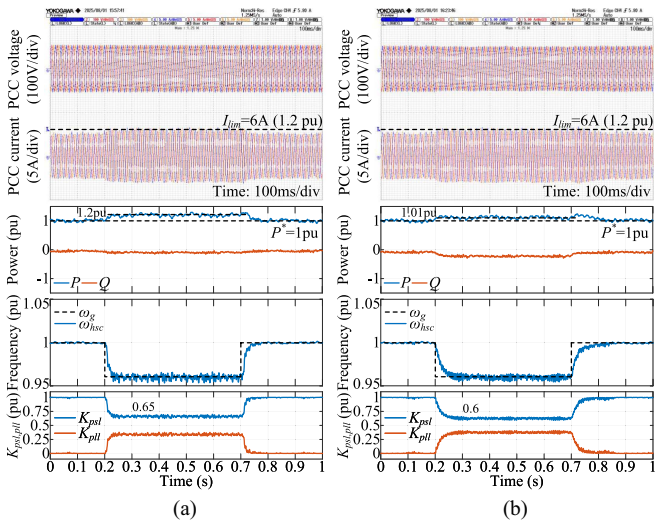

Fig. 9. Experimental validation of CSR-HSC stability under different grid strengths. A large frequency grid drop is applied ($\omega_g = 0.96$ p.u. for $t = 0.2 - 0.7$ s and $P^* = 1$ p.u.). (a) Strong grid: SCR = 17.78 ($L_g = 3.57$ mH and $R_g = 0.100\,\Omega$). (b) Weak grid: SCR = 5.91 ($L_g = 10.74$ mH and $R_g = 0.238\,\Omega$).

TABLE III
PARAMETER TUNING FOR STABILITY IN WEAK GRIDS

SCR	$K_{p,\text{pll}}$ (rad/(V·s))	R_v (p.u.)	X_v (p.u.)
17.78	1	0.005	0.2
5.91	0.5	0.01	0.4

and VA of CSR-HSC remain stable for a frequency drop of 2 Hz when SCR = 5.91 if the parameters are tuned appropriately. This grid disturbance is tested to validate the stability of both since the PLL is activated due to the current limiter saturating.

IV. CONCLUSION

This letter proposes an HSC method, which considers current limiting control of GFM converters to improve synchronization stability during large disturbances. An intuitive design is given, wherein the PSL and PLL components are weighted according to the CSR of the current limiter, as a proxy measure for the severity of a disturbance. The design of the proposed HSC method not only considers the current limiter, but also synergizes with it, whereas existing implementations of HSC do not consider the physical current limits of GFM converters. Another important advantage is the ability to realize accurate power setpoint tracking during unfaulted steady states. In addition, this allows the selection of a larger proportional gain for the PLL, resulting in closer tracking of the grid frequency and faster recovery after disturbances. The performance of the proposed CSR-HSC method and its advantages over existing methods is demonstrated with experimental results during grid frequency drops, voltage sags, and under weak grid conditions. In future work, small-signal stability-oriented design will be further investigated to consider the impact of PLL and VA parameters.

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