An Improved Four-Level Active Neutral Point Clamped Inverter With Relatively Uniform Loss Distribution

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***Abstract*—Recently, four-level inverters for low and medium voltage applications have been widely investigated thanks to their simple structure, low dv/dt, low switching loss, etc. However, the existing topologies have the disadvantage of unbalanced power loss distribution. For this reason, this article proposes an improved four-level active neutral point clamped inverter topology which is featured with low total voltage stress and uniform loss distribution under multiple operation conditions. These merits can fully utilize all power devices and expand the output capacity of the inverter. The operating principle and modulation strategy of this topology are described in detail and a comprehensive comparison with other four-level and three-level inverter topologies is analyzed. Finally, experimental results have been carried out to validate the proposed topology and its advantages in improving loss distribution.**

***Index Terms*—Four-level inverter, loss distribution, voltage balancing control.**

I. Introduction

THANKS to the development of new generation of semiconductor devices, the voltage level and capacity of new energy power generation, rail transportation, electric aircraft and other applications has been continuously increased to realize high efficiency and high power density [1], [2], [3], [4]. However, two-level inverters are not sufficient to support these applications due to the limitations of device voltage rating, power loss and heat generation, and electromagnetic interference [5]. Comparatively, multilevel inverters are good candidates due to the advantages of lower device withstanding voltage, better output waveform and lower dv/dt [6].

Recently, four-level inverters have been extensively studied. This is because that in some high-capacity applications, the device withstanding voltages of four-level inverters are more compatible with the voltage ratings of commercially available devices. For example, Airbus's E-Fan X uses a 2MW power motor and 3kV dc distribution to reduce losses and the weight of equipment [7]. As for this application, four-level inverters can partially or fully utilize 1700 V devices, while three-level inverters must use 3.3 kV devices entirely [8].

In four-level inverters, diode neutral point clamped (DNPC) and flying capacitor (FC) topologies are two classical structures, as shown in Fig. 1(a) and (b), where all active switches withstand uniform voltage stress [9], [10]. But a large number of diodes in the DNPC structure lead to higher conduction losses. Based on this, several clamped topologies that use all active devices have been proposed. Four-level π-type and double T-type (DT) inverters shown in Fig. 1(c) and (d) have been proposed in [11] and [12], respectively, but both of them suffer from the problem of switches with full voltage stress, which restricts their application in medium voltage areas. In contrast, the active neutral point clamped (ANPC) topology in Fig. 1(e) shows lower total voltage stress [13]. Therefore, it was used by Schneider Electric in the Galaxy VM uninterruptible power supply product [14]. However, in order to achieve voltage balance, the switch S_{x2} is subjected to a greater number of switching cycles and higher current stress, resulting in a seriously unbalanced loss distribution.

The topology in Fig. 1(b) has bulky FCs, one of which is subjected to two-thirds of the dc-link voltage. For the nested neutral point clamped (NNPC) topology in Fig. 1(f), both capacitors in each phase need to withstand only one-third of the dc-link voltage, which can somewhat reduce the FC size [15]. But two additional diodes are added. Ebrahimi and Karshenas [16] proposed a single FC topology overcoming this problem further, as shown in Fig. 1(g). But when the middle two voltage levels are switched, both pairs of switches must act simultaneously, and the blocking voltages of the upper and lower switches will rise directly to two-thirds of the dc-link voltage, resulting in higher switching losses. A hybrid clamped (HC) structure in Fig. 1(h) attains full uniformity of voltage stress based on eight active

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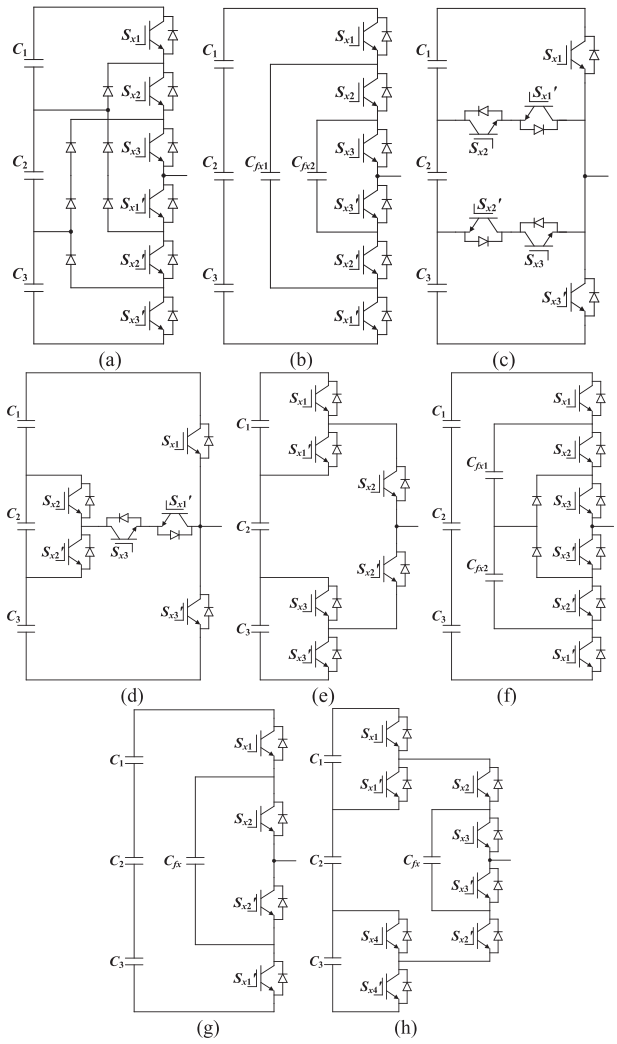

Fig. 1. Different four-level inverter topologies. (a) DNPC. (b) FC. (c) π-type. (d) DT. (e) ANPC. (f) NNPC. (g)SFC. (h) HC.

switches and one FC, which further improves the power density compared to the NNPC topology [17].

Based on the above description and analysis, the structure of the inverter is mainly measured in terms of the number of power devices and capacitors, voltage stress, cost, efficiency and power density. Several topologies consisting only of active switches have low component counts and high power density despite uneven voltage stress, making them ideal for low- and medium-voltage applications with different voltage rating devices. For these reasons, an improved ANPC (IANPC) inverter structure is proposed in this article, which is characterized by simple structure, low overall stress and uniform loss distribution. It can fully utilize the capacity of all power devices, thus increasing system capacity, switching frequency or reducing the difficulty of system thermal design.

The rest of this article is organized as follows. Section II describes the basic operating principles and characteristics of the proposed topology. Section III describes the modulation scheme and the balancing control method of the dc-link capacitor voltage. Section IV compares and analyzes the proposed topology with the existing topologies in detail. Experimental verifications have been done in Section V. Finally, Section VI concludes this article.

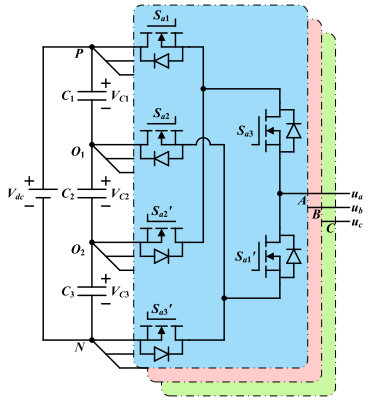

Fig. 2. The proposed inverter topology.

II. Topology and Operating Principle

The proposed four-level IANPC inverter is shown in Fig. 2. The three capacitors C_1, C_2 and C_3 at the dc-link share the input voltage $V_{\rm dc}$ evenly by series connection, and P, O_1, O_2, and N denote the four connection terminals on the dc side. Each phase consists of six active switches, where S_{x1}, S_{x2}, S_{x2}' and S_{x3}' are connected to P, O_1, O_2, and N, respectively, and S_{x3} and S_{x1}' are connected to the ac terminal. The structure of the proposed IANPC topology is a combination of three half-bridges. Although the switches of each half-bridge are not conducted complementarily, it is still possible to utilize the three half-bridge modules for developing a new four-level inverter topology.

In order to output the four voltage levels in an orderly manner, the following principles need to be observed during operation.

1) The six switches in each phase are divided into three pairs (S_{x1}, S_{x1}'), (S_{x2}, S_{x2}') and (S_{x3}, S_{x3}'). Each pair of switches operates at a complementary manner. It should be noted that S_{x1} is operated at a complementary manner with the outer switch S_{x1}', not with S_{x2}' in the same half bridge. The same is true for the other two pairs of switches.
2) When the device turns on, S_{x2} must precede S_{x1} and S_{x3} must precede S_{x2}, while the reverse order of operation occurs when the device turns off. If S_{x2} does not turn on yet and S_{x1} turns on, capacitors C_1 and C_2 will be shorted by S_{x1} and S_{x2}'.

Assuming terminal N as the ground reference, the four output voltage levels are 0, $V_{\rm dc}/3$, $2V_{\rm dc}/3$ and $V_{\rm dc}$. Based on the above principle, the different voltage levels and switching states are given in Table I, where $f(S_{xi})$ is a function that represents the (S_{xi}, S_{xi}') switching state. Specifically, $f(S_{xi})$ is 1 when S_{xi} is on and S_{xi}' is OFF, and vice versa is 0. Under the specified operation mode, only one pair of switches are actuated for all adjacent voltage levels, which ensures the minimum switching transitions.

Fig. 3 shows the current paths corresponding to different voltage levels. When the inverter outputs the voltage level $V_{\rm dc}$,

TABLE I
SWITCHING STATUS OF FOUR-LEVEL IANPC INVERTER

Voltage Level	$f(S_{x1})$	$f(S_{x2})$	$f(S_{x3})$
V_{dc}	1	1	1
$2V_{dc}/3$	0	1	1
$V_{dc}/3$	0	0	1
0	0	0	0

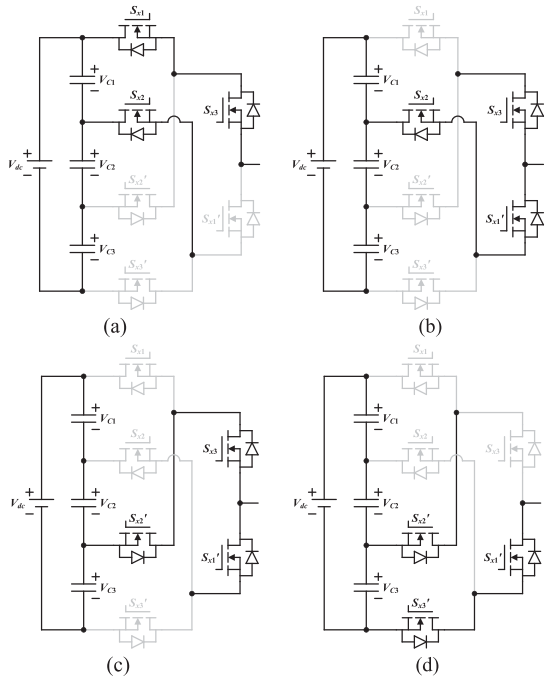

Fig. 3. Current paths of different voltage levels. (a) V_{dc}. (b) $2V_{dc}/3$. (c) $V_{dc}/3$. (d) 0.

the ac terminal is connected to terminal P through S_{x1} and S_{x3}, and S_{x2}' withstands the voltages of capacitors C_1 and C_2. At this time, S_{x2} also stays on, ensuring that the blocking voltages of both S_{x1}' and S_{x3}' are stably clamped, with S_{x1}' carrying the voltage of C_1 and S_{x3}' carrying the voltages of C_2 and C_3. Similarly, when the output voltage level is transformed to $2V_{dc}/3$, the switches S_{x1} and S_{x2}' withstand the voltages of C_1 and C_2, respectively, while the blocking voltage of S_{x3}' remains at the voltages of C_2 and C_3. Therefore, the maximum blocking voltage of the inner switches S_{x1}, S_{x2}, S_{x2}', and S_{x3}' is $2V_{dc}/3$, whereas that of the outer switches S_{x3} and S_{x3}' is only $V_{dc}/3$. However, the blocking voltage of the inner switches does not rise directly from 0 to $2V_{dc}/3$ when turning OFF, but first rises to $V_{dc}/3$. Subsequently, only if S_{x2} turns OFF does the blocking voltage of S_{x1} becomes $2V_{dc}/3$.

III. MODULATION AND CAPACITOR VOLTAGE BALANCING CONTROL

A. Modulation

The immediate problem of the proposed topology is the balancing of the capacitor voltages, and the conventional modulation method leads the intermediate capacitor to be over

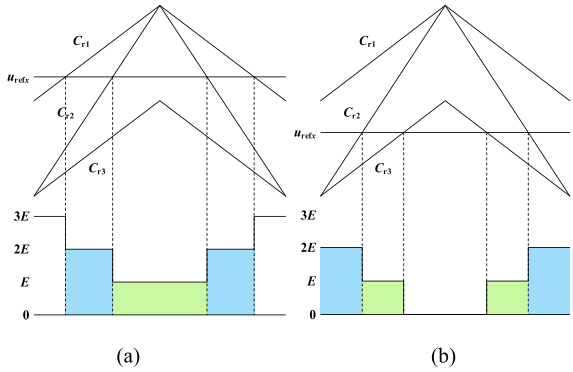

Fig. 4. Diagram of the variable carrier modulation. (a) Positive half cycle. (b) Negative half cycle.

discharged. To maintain the balancing of the capacitor voltage, variable carrier modulation in [12] is used in this article. The closed-loop balancing control of this method is simple and does not require three-phase current sampling. The reference signal of the three-phase voltage is shown in (1), where m denotes the modulation index and f_m denotes the fundamental frequency

$$\begin{cases} u_{\text{ref}a} = m * \sin(2\pi f_m t) + 1 \\ u_{\text{ref}b} = m * \sin(2\pi f_m t - 2\pi/3) + 1 \\ u_{\text{ref}c} = m * \sin(2\pi f_m t + 2\pi/3) + 1. \end{cases} \tag{1}$$

Accordingly, the output currents of the three phases are expressed as follows, where I_m is the peak current and φ is the power factor angle

$$\begin{cases} i_a = I_m * \sin(2\pi f_m t - \varphi) \\ i_b = I_m * \sin(2\pi f_m t - 2\pi/3 - \varphi) \\ i_c = I_m * \sin(2\pi f_m t + 2\pi/3 - \varphi). \end{cases} \tag{2}$$

Fig. 4 shows the modulation principle of variable carrier method. In Fig. 4, C_{r1}, C_{r2}, and C_{r3} are three triangular carriers with identical frequency and phase, which are compared with $u_{\text{ref}x}$ to generate the driving signals of S_{x1}, S_{x2}, and S_{x3}, respectively. The amplitudes of C_{r1} and C_{r3} are 1, while C_{r2} is a carrier with variable amplitude k. Fig. 4(a) illustrates the modulation waveforms during the positive half-cycle, with S_{x1} and S_{x2} acting once per switching cycle and S_{x3} remaining on at all times. The generated voltage levels are V_{dc}, $2V_{dc}/3$, and $V_{dc}/3$. During the negative half cycle, as shown in Fig. 4(b), S_{x1} no longer actuates and stays off, and S_{x3} starts to switch and outputs three voltage levels, $2V_{dc}/3$, $V_{dc}/3$, and 0. Thus, during the full cycle S_{x2} actually switches twice as many times as S_{x1} and S_{x3}.

According to Fig. 4, the duty cycles d_{x1}, d_{x2}, and d_{x3} of the switches S_{x1}, S_{x2} and S_{x3} in the one-phase circuit are shown in (3) and (4), respectively, for positive and negative half cycles

$$\begin{cases} d_{x1} = u_{\text{ref}x} - 1 \\ d_{x2} = u_{\text{ref}x}/k \\ d_{x3} = 1 \end{cases} \tag{3}$$

$$\begin{cases} d_{x1} = 0 \\ d_{x2} = u_{\text{ref}x}/k \\ d_{x3} = u_{\text{ref}x} \end{cases}. \tag{4}$$

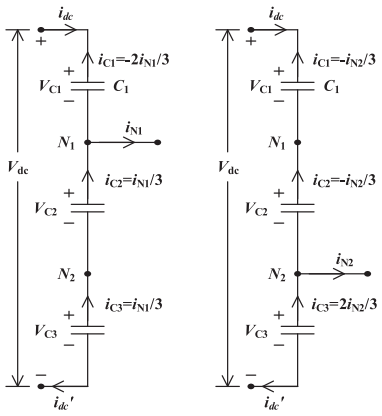

Fig. 5. Current distribution of voltage levels $2V_{\rm dc}/3$ and $V_{\rm dc}/3$.

During each switching cycle, the output voltage waveform for each phase contains two voltage levels $2V_{\rm dc}/3$ and $V_{\rm dc}/3$. For a one-phase circuit, outputting $2V_{\rm dc}/3$ discharges the intermediate capacitor C_2 if the current direction is positive, while C_2 is in the charging state when $V_{\rm dc}/3$ is output. Owing to this feature, balancing control of the capacitor voltages of four-level inverters becomes simple.

B. Capacitor Voltage Balancing Control

Under ideal conditions, the dc-link capacitor voltages can be naturally balanced at $k = 2$ without additional control [18]. The dc-link current distribution at different voltage levels is shown in Fig. 5. The average current flowing out of the two neutral points N_1 and N_2 during one switching cycle is expressed as

$$\begin{cases} i_{N1av} = \sum\limits_{x=a,b,c} (d_{x2} - d_{x1})\, i_x \\ i_{N2av} = \sum\limits_{x=a,b,c} (d_{x3} - d_{x2})\, i_x \end{cases}. \tag{5}$$

Thus, the variation of the three capacitor voltages is expressed as

$$\begin{cases} \Delta u_1 = \frac{T_s}{C}\left(\frac{2}{3} i_{N1av} + \frac{1}{3} i_{N2av}\right) \\ \Delta u_2 = -\frac{T_s}{3C}\left(i_{N1av} - i_{N2av}\right) \\ \Delta u_3 = -\frac{T_s}{C}\left(\frac{1}{3} i_{N1av} + \frac{2}{3} i_{N2av}\right) \end{cases} \tag{6}$$

where C denotes the capacitance and $T_{\rm s}$ denotes the switching period. Substituting (5) into (6), the relationship between Δu_2 and duty cycle is shown

$$\Delta u_2 = -\frac{T_s}{3C}\left(2d_{x2} - d_{x1} - d_{x3}\right) i_x. \tag{7}$$

Obviously, the middle capacitor voltage variation at $k = 2$ always remains zero during the switching cycle. From (5) and (6), the deviation of the upper and lower capacitor voltage variations is given by

$$\begin{aligned} \Delta u_{13} &= -\frac{T_s}{C}\left(i_{N1av} + i_{N2av}\right) \\ &= -\frac{T_s}{C} \sum_{x=a,b,c} \left(d_{x3} - d_{x1}\right) i_x. \end{aligned} \tag{8}$$

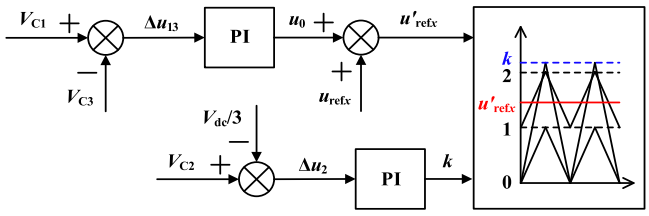

Fig. 6. Block diagram of the voltage balancing control.

The above equation shows that Δu_{13} is not zero during the switching cycle. However, during the fundamental cycle $T_{\rm m}$, since the switching frequency is much greater than the fundamental frequency, Δu_{13} can be approximated as an integral form as shown in (9). The result shows that the difference between the upper and lower capacitor voltages is zero during the fundamental period

$$\Delta u_{13} = \frac{1}{C} \sum_{x=a,b,c} \int_0^{T_m} \left(d_{x1} - d_{x3}\right) i_x dt = 0. \tag{9}$$

The analysis shows that ideally the three capacitor voltages are naturally balanced during the fundamental cycle. However, the voltage may be shifted due to factors such as high-frequency current ripple and differences in the actual capacitances. Therefore, voltage balancing requires proper closed-loop feedback control, but only a slight adjustment.

Based on (6) and (8) the sum and difference of the two neutral point currents determine the voltage balancing of the upper and lower capacitors and the voltage balancing of the middle capacitor, respectively. The middle capacitor voltage balancing can be controlled by adjusting k, and the upper and lower capacitor voltage balancing can be realized by injecting zero-sequence component.

As shown in Fig. 6, the closed-loop control of the final voltage balancing is realized based on two simple PI controllers for generating the zero-sequence voltage signal u_0 and the variable k.

The reference signal after injecting the zero-sequence component is shown in (10), and d'_{x1}, d'_{x2}, and d'_{x3} are the new duty cycles obtained from $u'_{{\rm ref}x}$

$$u\prime_{{\rm ref}x} = u_{{\rm ref}x} + u_0. \tag{10}$$

After injecting the zero-sequence voltage, the increased difference between the upper and lower capacitor voltages is defined as $\Delta u'_{13}$. Taking the case of $u_a > 0$, $u_b < 0$, $u_c > 0$ as an example, $\Delta u'_{13}$ is denoted as

$$\begin{aligned} \Delta u\prime_{13} &= \frac{T_s}{C} \sum_{x=a,b,c} \left(\left(d\prime_{x3} - d\prime_{x1}\right) - \left(d_{x3} - d_{x1}\right)\right) i_x \\ &= \frac{2u_0 i_b T_s}{C}. \end{aligned} \tag{11}$$

Further, in the case of zero-sequence voltage injection with variation of k, the increased variation of the intermediate capacitor voltage is derived by

$$\Delta u\prime_2 = \frac{T_s}{C} \sum_{x=a,b,c} \left(2d\prime_{x2} - d\prime_{x1} - d\prime_{x3}\right) i_x$$

TABLE II
VARIATION OF THE CAPACITOR VOLTAGES

	$\Delta u'_{13}$	$\Delta u'_2$
$u_a > 0, u_b < 0, u_c > 0$	$2u_0 i_b T_s/C$	$(2/k\text{-}1)1.5mI_m\cos\varphi T_s/C$
$u_a > 0, u_b < 0, u_c < 0$	$-2u_0 i_a T_s/C$	$(2/k\text{-}1)1.5mI_m\cos\varphi T_s/C$
$u_a > 0, u_b > 0, u_c < 0$	$2u_0 i_c T_s/C$	$(2/k\text{-}1)1.5mI_m\cos\varphi T_s/C$
$u_a < 0, u_b > 0, u_c < 0$	$-2u_0 i_b T_s/C$	$(2/k\text{-}1)1.5mI_m\cos\varphi T_s/C$
$u_a < 0, u_b > 0, u_c > 0$	$2u_0 i_a T_s/C$	$(2/k\text{-}1)1.5mI_m\cos\varphi T_s/C$
$u_a < 0, u_b < 0, u_c > 0$	$-2u_0 i_c T_s/C$	$(2/k\text{-}1)1.5mI_m\cos\varphi T_s/C$

$$= \frac{(2/k-1)\,1.5mI_m\cos\varphi T_s}{C}. \tag{12}$$

Equation (11) and (12) show the control of the zero-sequence component and k on the voltage balancing. The expressions for $\Delta u'_{13}$ and $\Delta u'_2$ for all cases are given in Table II. It is clear that the injection of the zero-sequence component has no effect on the balancing of the intermediate capacitor voltage, and the change of k does not affect the balancing of the upper and lower capacitor voltages, either. Therefore, the voltage balancing control is completely decoupled. The injected zero-sequence voltage is used to adjust the amount of change in the difference between the upper and lower capacitor voltages to keep them equal. Then the change of the intermediate capacitor voltage is controlled by the regulation of k to keep it at $V_{\rm dc}/3$. In this way, all three capacitor voltages are balanced at $V_{\rm dc}/3$.

IV. COMPARATIVE ANALYSIS

A. Number and Voltage Stress of Components

Table III gives the detailed comparison results of the proposed IANPC topology with other four-level topologies in terms of key components. First, the proposed IANPC, ANPC, DT, and π-type topologies have the least number of components, with each phase consisting of six active switches. In contrast, the DNPC, FC, NNPC, and HC topologies all have uniform voltage stress on the switching devices, but at the expense of an additional number of components. For one-phase circuits, the DNPC topology adds six diodes, the FC topology adds two FCs with uneven voltage stress, the NNPC adds two FCs and two diodes, and the HC topology adds two active switches and one FC. Therefore, they are more suitable for relatively higher voltages in medium voltage applications such as 3.3 kV, 4.16 kV ac, etc. This is because a larger number of components means lower reliability, increased size, and reduced power density.

Whereas, IANPC, ANPC, DT, and π-type topologies are more suitable for low and medium voltage applications as hybrid switches with different voltage ratings can be used to achieve higher power density, reliability, efficiency etc. For further comparison, the maximum blocking voltage is $V_{\rm dc}$ for DT and π-type topologies and $2V_{\rm dc}/3$ for IANPC and ANPC topologies. Moreover, the total voltage stress of the proposed topology is the same as that of the DT topology, lower than that of the π-type topology and higher than that of the ANPC topology.

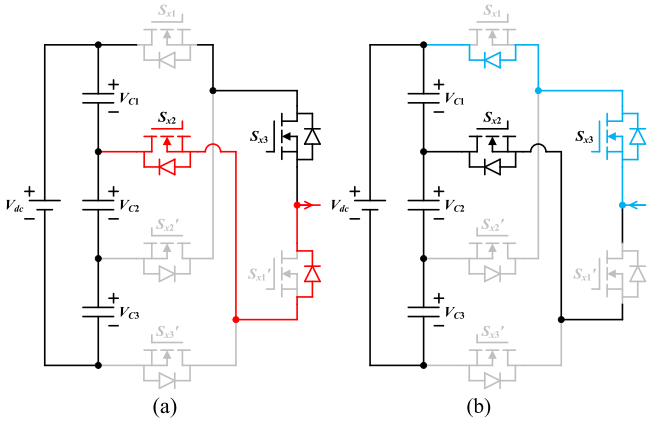

Fig. 7. Soft-switching. (a) Positive current. (b) Negative current.

However, the latter power loss analysis shows that the proposed topology has a more even loss distribution, which is beneficial to fully utilize the capacity of all switches, thus increasing the system capacity, switching frequency, or reducing the difficulty of thermal design.

In addition, the proposed topology is again compared with the three-level topology in Table IV. From the table, it is observed that the voltage stress is too high in the T-type structure. The NPC topology, despite using diodes in 1/3 of the devices, is replaced by the ANPC topology in many applications due to the loss imbalance which limits the output power. The proposed topology has the same number of devices as the three-level ANPC topology. Although 2/3 of the switches are subjected to $2V_{\rm dc}/3$, they can be used with commercially available devices of the same model, while the other 1/3 of the switches can use devices with lower voltage rating. The three-level FC structure also has the problem of large capacitor volume, and at the same time, it needs to withstand a higher $V_{\rm dc}/2$ voltage. In addition, a four-level converter has lower switching losses than a three-level converter because the switching voltage is $V_{\rm dc}/3$.

Overall, the proposed IANPC inverter has a simple structure with a small number of components and uniform loss distribution, which provides comprehensive advantages in terms of power density, efficiency, and reliability.

B. Loss Analysis

The loss of the power device consists of two parts, the switching loss and the conduction loss. First, the distribution of the switching loss depends on the magnitude and polarity of the output current during the switching action. When switching between the output voltage levels $V_{\rm dc}$ and $2V_{\rm dc}/3$ under forward current condition, the output current flows through the body diode of S_{x1}' during the dead time as shown in Fig. 7(a). Thus S_{x1}' is soft-switching and switching losses are only generated by S_{x1}. On the contrary, only S_{x1}' generates switching losses when the current flows in the reverse direction as shown in Fig. 7(b). Table V gives the switching loss distribution for different output voltage level switching with different current polarities. The switching losses all occur in the switches S_{x1}, S_{x2}, and S_{x3}

TABLE III
COMPARE OF DIFFERENT FOUR-LEVEL INVERTER TOPOLOGIES

Topologies		IANPC	ANPC[13]	DT[12]	π[11]	DNPC[9]	FC[10]	NNPC[15]	HC[17]
Number of active switches	$V_{dc}/3$	6	12	12	6	18	18	18	24
	$2V_{dc}/3$	12	6	0	6	0	0	0	0
	V_{dc}	0	0	6	6	0	0	0	0
Drivers		18	18	18	18	18	18	18	24
Number of diodes	$V_{dc}/3$	0	0	0	0	18	0	6	0
Number of flying capacitors	$V_{dc}/3$	0	0	0	0	0	3	6	3
	$2V_{dc}/3$	0	0	0	0	0	3	0	0
Total voltage stress		30	24	30	36	36	18 (27)	24 (30)	24 (27)
Maximum blocking voltage of active switches		$2V_{dc}/3$	$2V_{dc}/3$	V_{dc}	V_{dc}	$V_{dc}/3$	$V_{dc}/3$	$V_{dc}/3$	$V_{dc}/3$

Note: "(xx)" indicate the total voltage stress including the flying capacitors.

TABLE IV
COMPARISON BETWEEN THE PROPOSED TOPOLOGY AND THE THREE-LEVEL TOPOLOGIES

Topologies		IANPC	T-type	NPC	ANPC	FC
Number and blocking voltage of active switches		6*$V_{dc}/3$ 12*$2V_{dc}/3$	6*$V_{dc}/2$ 6*V_{dc}	12*$V_{dc}/2$	18*$V_{dc}/2$	12*$V_{dc}/2$
Number and blocking voltage of diodes		0	0	6*$V_{dc}/2$	0	0
Number and voltage rating of actual selected device	V_{dc}=1.2 kV	6*650 V 12*1200 V	6*1200 V 6*1700 V	12*1200 V 6*1200 V	18*1200 V	12*1200 V
	V_{dc}=3 kV	6*1700 V 12*3300 V	6*3300 V 6*4500 V	12*3300 V	18*3300 V	12*3300 V
Number and voltage stress of flying capacitors		0	0	0	0	3*$V_{dc}/2$

TABLE V
SWITCHING LOSS POSITION OF DIFFERENT CURRENT POLARITY

Voltage level	Current polarity	Switching loss position
V_{dc} and $2V_{dc}/3$	positive	S_{x1}
	negative	S_{x1}'
$2V_{dc}/3$ and $V_{dc}/3$	positive	S_{x2}
	negative	S_{x2}'
$V_{dc}/3$ and 0	positive	S_{x3}
	negative	S_{x3}'

when the current is forward. Conversely, the switching losses are generated by S_{x1}', S_{x2}' and S_{x3}' when the current is reversed.

Due to the symmetry of the circuit and the positive and negative half cycles of the modulating waveforms, the losses of the switches S_{x1} and S_{x3}' are basically the same. The losses of S_{x2} and S_{x2}', and S_{x3} and S_{x1}' are also the same. Therefore, the losses of S_{x1}, S_{x2} and S_{x3} are analysed as an example later. The temperature is ignored in the calculations as it has a small effect on the losses [19], [20]. Combining the calculations in [19] and [21], the hard-switching losses of S_{x1}, S_{x2} and S_{x3} during one fundamental cycle can be uniformly expressed as (13)

$$P_{sw} = \frac{1}{T_m} \sum e_{sw}(i_k) * \left(\frac{V_{dc}/3}{V_{ref}}\right)^{K_v} \quad 1 \le k \le N_{sw} \cap i_k \ge 0 \tag{13}$$

where e_{sw} represents the curve of total turn-ON and turn-OFF energy versus current, i_k and $V_{dc}/3$ are the current and voltage during device switching, respectively, V_{ref} is the reference voltage for the switching energy measurements in the datasheet, K_v is the constant voltage exponential correction factor, N_{sw} is the number of devices switching in the fundamental cycle, and $i_k \ge 0$ restricts (13) to only calculating the hard-switching losses of S_{x1}, $S_{x2,}$ and S_{x3}. The required parameters e_{sw}, V_{ref} and K_v are obtained from the device datasheet.

As for the conduction loss distribution of the IANPC inverter, it is simultaneously affected by the current magnitude, modulation index and power factor. Under closed-loop control, it is difficult to calculate the conduction loss because u_0 and k are unknown. However, given that the capacitor voltages are naturally balanced when $k = 2$ under ideal conditions, the fluctuation of u_0 and k is very small, so the conduction loss is calculated based on the assumption of natural voltage balance. Assuming that the on-state resistance R_{on} remains constant [22], the conduction losses of S_{x1}, S_{x2}, and S_{x3} in one fundamental cycle can be expressed as (14), (15), and (16), respectively,

$$P_{con1} = I_m^2 R_{on} \frac{m}{2\pi}\left(1 + \frac{1}{3}\cos 2\varphi\right) \tag{14}$$

$$P_{con2} = I_m^2 R_{on}\left[\frac{1}{4} - \frac{m}{2\pi}\left(1 + \frac{1}{3}\cos 2\varphi\right)\right] \tag{15}$$

$$P_{con3} = \frac{1}{4} I_m^2 R_{on}. \tag{16}$$

Based on the above results, Fig. 8 depicts the variation of the device power consumption with the regulation and power factor angle. Table VI gives the basic specifications of the devices used in the loss calculations. Fig. 8(a) shows that the closer the power factor is to 1, the higher the switching loss of S_{x1} and the lower the switching loss of S_{x3}. When the power factor is exactly 1,

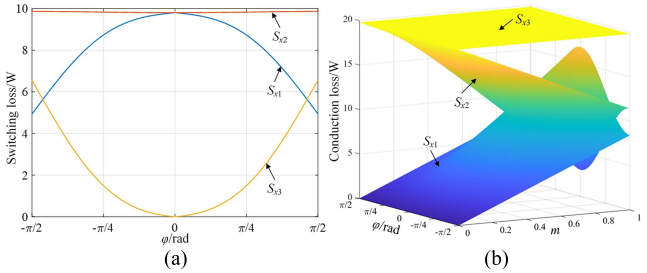

Fig. 8. Power loss analysis of devices at $V_{\rm dc} = 1200$ V, $I_m = 60$ A, and $f_s = 30$ kHz. (a) Switching loss. (b) Conduction loss.

TABLE VI
MAIN SPECIFICATIONS OF DEVICES

Device model	SCT3022AL	SCT3022KL
Drain-source voltage	650 V	1200 V
Continuous drain current	65 A @ T_c=100°C	67 A @ T_c=100°C
On-state resistance	22 mΩ @ T_{vj}=25°C 32 mΩ @ T_{vj}=150°C	22 mΩ @ T_{vj}=25°C 38 mΩ @ T_{vj}=150°C
Unit price (purchased in manufacturers standard package quantities @www.digikey.com)	35.47USD	43.48USD

the switching losses are all concentrated in S_{x1}. Note that the current flowing through S_{x3} is the sum of the currents flowing through S_{x1} and S_{x2}'. Therefore, the switch S_{x3} with the highest current stress has the minimum switching loss unless the power factor is close to 0. Since S_{x2} operates during each switching cycle, its switching losses are then independent of the power factor.

According to (14)–(16) and Fig. 8(b), the closer the power factor is to 1 and the higher the modulation index, the higher the conduction loss of the switch S_{x1}, and on the contrary the lower the conduction loss of S_{x2}. The conduction loss of S_{x3}, on the other hand, is constant and independent of modulation index and power factor.

Fig. 9(a) and (b) shows that the total losses of all switches versus the modulation index and the power factor. The total loss of the IANPC topology is slightly lower than that of the ANPC topology. The modulation index and power factor essentially do not change the total loss of all devices. The total loss depends mainly on the output current, while the regulation and power factor mainly affect the loss distribution. Fig. 9(c) and (d) demonstrates the total losses of individual switches versus the modulation index and the power factor. The maximum loss decreases in IANPC topology with increasing the modulation index. While the loss of S_{x2} in ANPC topology is independent of the modulation index and power factor and always has the maximum loss.

To show that the proposed topology is still valid at typical dc voltages and appropriate power ratings, a comparison is made based on the two conventional applications in Table VII. Case 1 is a typical voltage and power for variable frequency drive, with the power factor set to 0.9 considering the motor load. Case 2 is

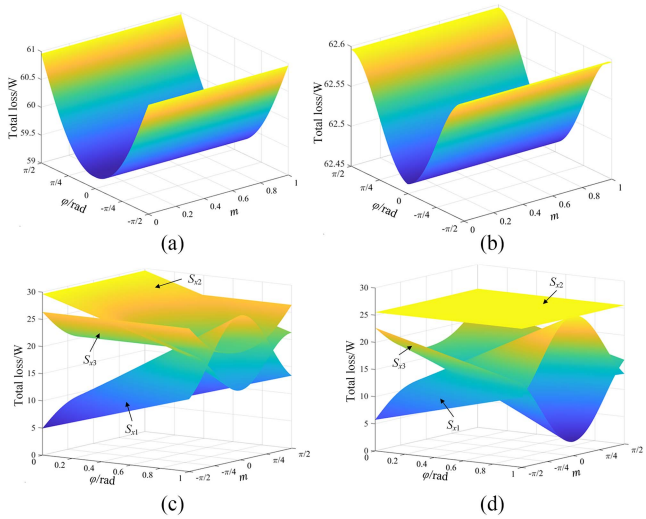

Fig. 9. Power loss comparison. (a) Total loss of S_{x1}, S_{x2}, and S_{x3} in IANPC. (b) Total loss of S_{x1}, S_{x2}, and S_{x3} in ANPC. (c) Loss distribution of IANPC. (d) Loss distribution of ANPC.

TABLE VII
TYPICAL APPLICATION CONDITIONS

	Case 1	Case 2
DC voltage	1200 Vdc	800 Vdc
AC output voltage	660 Vac	380 Vac
Output power	45k VA	25 kW
Power factor	0.9	1.0

TABLE VIII
COST COMPARISON

Topology		IANPC	ANPC
Switching device	SCT3022AL	2	4
	SCT3022KL	4	2
Total switching device cost		734.6USD	686.5USD
Inverter capacity at the same maximum device loss	Case 1	45 kVA	39.5 kVA
	Case 2	25 kW	22 kW
Cost per unit power	Case 1	16.3USD/kVA	17.4USD/kVA
	Case 2	29.4USD/kW	31.2USD/kW

a typical parameter for PV inverters, with the power factor set to 1. The dc voltage is set to the maximum voltage under full-load MPPT to evaluate the limitations imposed by maximum device losses on the system capacity.

As shown in Fig. 10, the proposed topology exhibits a more uniform loss distribution across both operating conditions and different switching frequencies. In case 1, the difference in maximum losses among individual devices is 2.7 W at 10 kHz, increasing to 5.8 W at 50 kHz. Similarly, in condition 2, this difference is 1.5 W at 10 kHz and increases to 7.5 W at 50 kHz.

Furthermore, based on the devices listed in Table VI, the costs of the IANPC and ANPC topologies under both operating conditions are compared, with the results presented in Table VIII. The

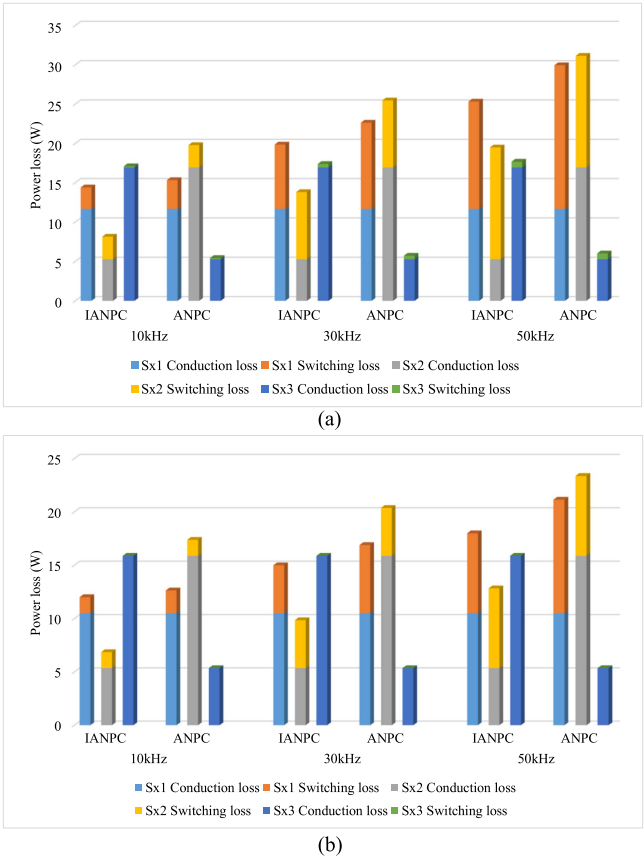

Fig. 10. Power loss distribution comparison. (a) Case 1. (b) Case 2.

total switching device cost of the proposed topology is higher than that of the ANPC topology due to its higher overall voltage stress. However, according to the loss evaluation results, when constraining the maximum device loss of the ANPC topology to match that of the IANPC topology, the IANPC inverter achieves higher capacity and power density, along with a lower cost per unit power. For example, in case one at a compromise switching frequency of 30 kHz, the proposed topology delivers an output current of 39.4 A at rated capacity with a maximum device power loss of 20 W. Under the same maximum device power dissipation constraint, the output current of the ANPC topology is limited to 34.6 A, corresponding to a capacity of 39.5 kVA.

The above analyses collectively demonstrate that the proposed topology achieves a more uniform loss distribution because of reducing the switching losses of the devices subjected to high current stress. The improved thermal balance not only increases the system capacity but also enables higher switching frequencies and reduces heatsinking requirements, thereby further enhancing its power density [22], [23].

V. Experimental Result

In order to verify the effectiveness of the proposed topology, two inverter prototypes based on IANPC topology and ANPC topology are built. The six switches of each phase are fixed on one heat sink and all heat sinks have the same size. The arrangement of the switches of the two prototypes is shown in

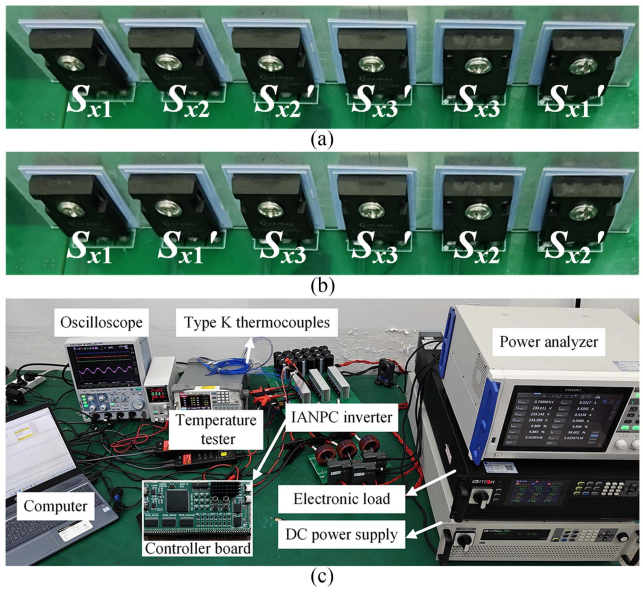

Fig. 11. Prototype of four-level IANPC inverter. (a) Switches arrangement of IANPC topology. (b) Switches arrangement of ANPC topology. (c) Test platform.

TABLE IX
Key Parameter of Prototype

Parameter		Value
DC-link voltage		750 V
DC-link capacitor		C_1=C_2=C_3=1.5 mF
Switching frequency		10 kHz
Output current		8.7 A
Line frequency		50 Hz
Switching device	$V_{dc}/3$	CI30N65SM
	$2V_{dc}/3$	CI30N120SM

Fig. 11(a) and (b), respectively, and the overall experimental platform is shown in Fig. 11(c), with the controller board and drivers located at the back of the prototype. The experimental parameter settings are given in Table IX. The prototypes are naturally cooled, and the experiments are conducted at an ambient temperature of 22 °C. The loss distribution of the inverter is measured by thermocouple measurement of the case temperature of the discrete devices when the prototype has continuously run for 20 minutes.

Fig. 12 shows the waveforms of phase C voltage, three-phase currents and dc capacitor voltages of the IANPC inverter under the operating conditions of $m = 0.9$, $\cos\varphi = 0.99$ and power of 6 kW. The phase voltages have four distinct voltage levels and the three phase currents are fine sinusoidal waveforms. The detailed amplification of the phase voltages mostly shows the orderly transitions of the four levels. The three capacitor voltages are effectively balanced at 250V, which is one-third of the dc-link voltage. The driving signals and blocking voltages of the switches S_{x1}, Sx_2, and S_{x3} are shown in Fig. 13. To balance the intermediate capacitor voltages, S_{x2} is switched twice as often

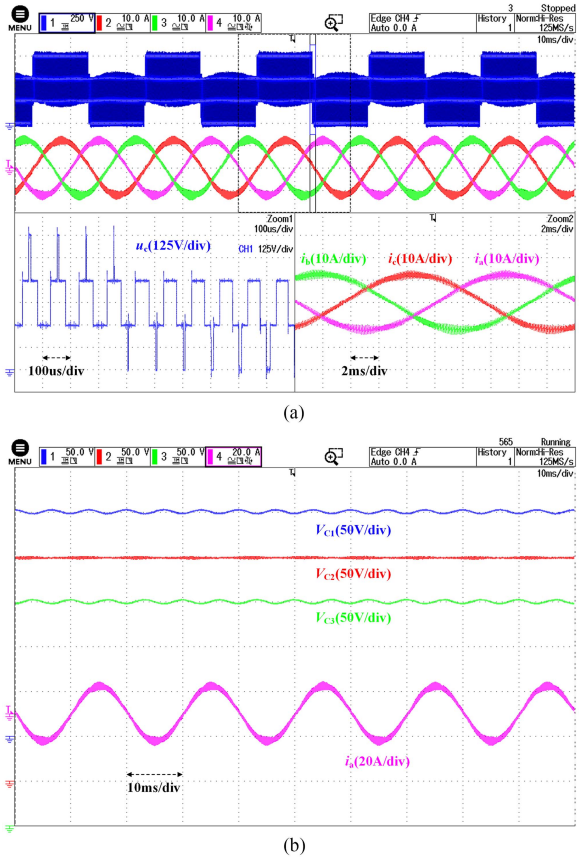

Fig. 12. Waveforms at $m = 0.9$ and $\cos\varphi = 0.99$. (a) Phase C voltage and three-phase currents. (b) Capacitor voltages.

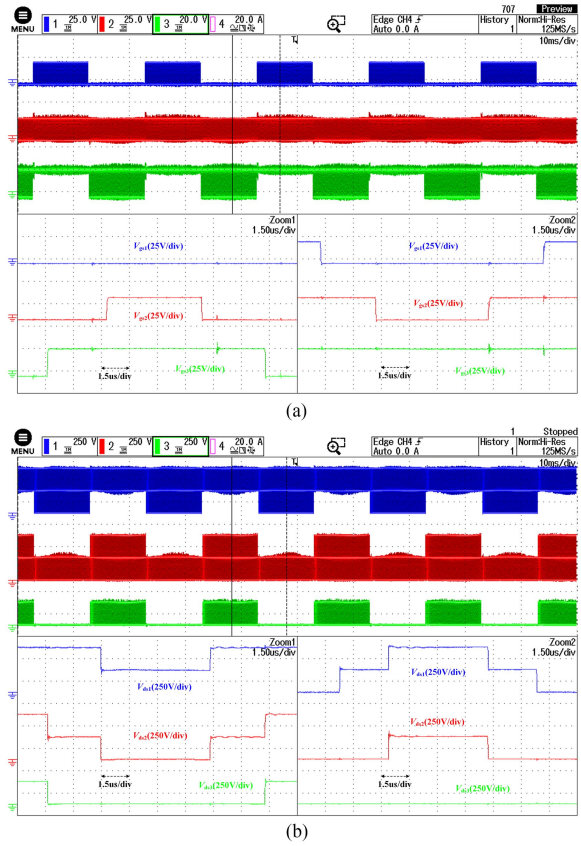

Fig. 13. Waveforms of power devices. (a) Driving signals. (b) Blocking voltages.

TABLE X
TEMPERATURE OF DEVICES

Switches	IANPC (6kW)	ANPC (6kW)	IANPC (6.6kW)
S_{x1}	52.69°C	50.23°C	57.46°C
S_{x1}'	50.90°C	48.44°C	56.99°C
S_{x2}	49.36°C	60.43°C	53.52°C
S_{x2}'	49.83°C	60.08°C	53.91°C
S_{x3}	51.30°C	49.11°C	57.41°C
S_{x3}'	52.91°C	51.09°C	58.31°C

as S_{x1} and S_{x3}. The switching voltage is $V_{\rm dc}/3$ for each action of all switches.

The measured results of the case temperature of the power devices in the proposed topology and the ANPC topology are given in Table X. From this table, it can be seen that even with the heat sink, the maximum temperature difference in the ANPC topology is still 12 °C. The temperatures of S_{x2} and S_{x2}' reach more than 60 °C.While in the proposed topology, the maximum temperature is below 53 °C and the maximum temperature difference is only 3.5 °C. Obviously it facilitates the overall lifetime of the proposed inverter, and could further extend its capacity or increase the switching frequency. To quantitatively illustrate its significance, an additional set of experiments with a 10% power

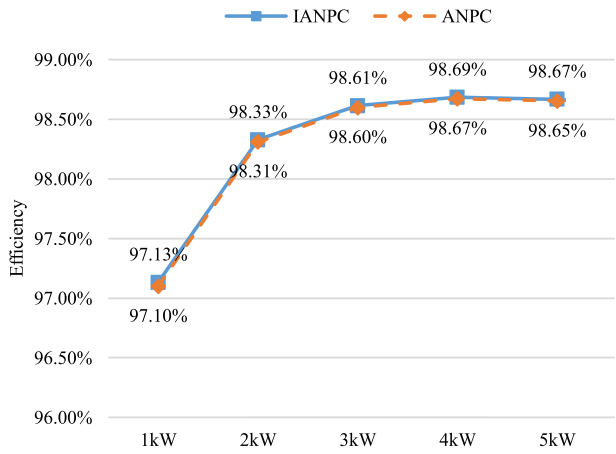

Fig. 14. Efficiency curves of IANPC and ANPC topology.

increase, i.e., 6.6 kW operating power, was performed on the IANPC topology. The testing results are also given in Table X. It can be seen that the overall temperature of the proposed topology increases after 20 minutes of steady operation at 6.6 kW, but is still lower than the maximum temperature of the ANPC topology at 6 kW.

The efficiency curves of the two prototypes are shown in Fig. 14. The results show that the efficiency of both is basically the same. The proposed IANPC topology does not lead to more

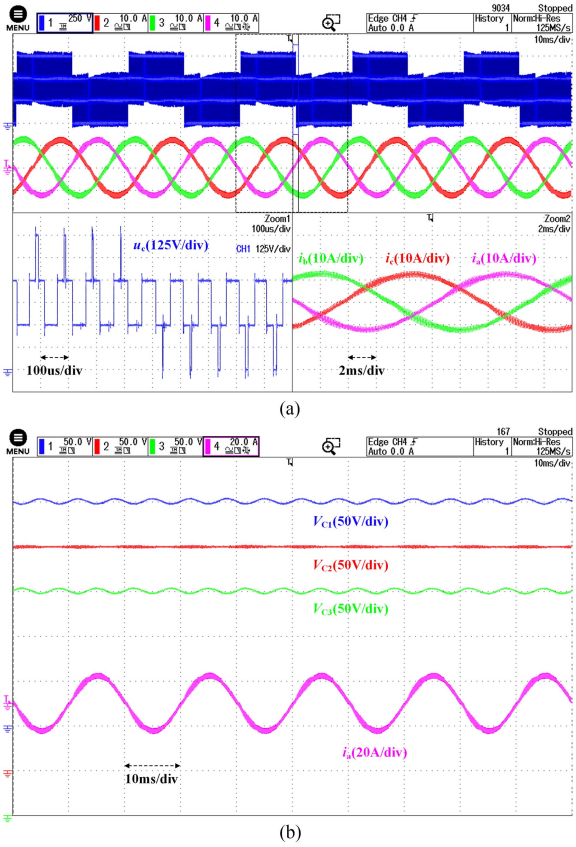

Fig. 15. Waveforms at $m = 0.9$ and $\cos\varphi = 0.6$. (a) Phase C voltage and three-phase currents. (b) Capacitor voltages.

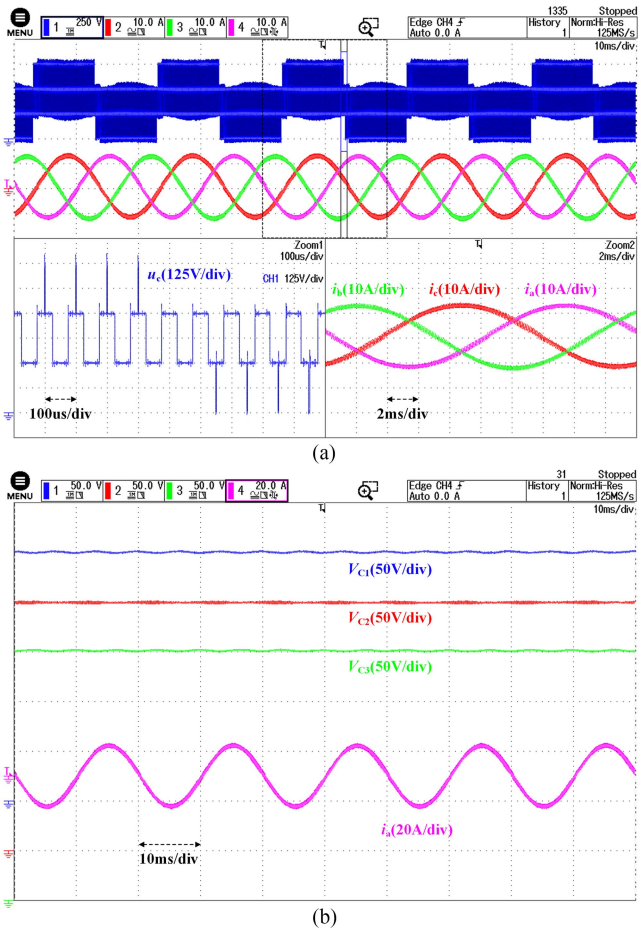

Fig. 16. Waveforms at $m = 0.3$ and $\cos\varphi = 0.99$. (a) Phase C voltage and three-phase currents. (b) Capacitor voltages.

TABLE XI
TEMPERATURE OF DEVICES

Case	Switches	IANPC	ANPC
$m = 0.9$ $\cos\varphi = 0.6$	S_{x1}	50.31℃	47.78℃
	S_{x1}'	51.52℃	48.77℃
	S_{x2}	50.62℃	60.10℃
	S_{x2}'	51.33℃	59.76℃
	S_{x3}	51.64℃	49.34℃
	S_{x3}'	50.88℃	49.64℃
$m = 0.3$ $\cos\varphi = 0.99$	S_{x1}	48.12℃	47.77℃
	S_{x1}'	51.29℃	50.00℃
	S_{x2}	51.52℃	60.13℃
	S_{x2}'	52.87℃	59.51℃
	S_{x3}	51.49℃	50.12℃
	S_{x3}'	48.59℃	48.75℃

losses though it shows slightly higher overall voltage stress than the ANPC topology.

Tests were also conducted to illustrate the performance of the proposed topology for two operating conditions with $m = 0.9$, $\cos\varphi = 0.6$ and $m = 0.3$, $\cos\varphi = 0.99$, respectively. The waveforms of phase C voltage, three-phase currents and dc capacitor voltages of the inverter are shown in Figs. 15 and 16, respectively. The dc voltages are well balanced around 250 V for both operating conditions and the waveforms of the output currents also satisfy the sinusoidal shape.

The operating temperatures for both cases are given in Table XI. Combining the results in Table X, the maximum temperature of the proposed topology is reduced by 1.3 °C and the maximum temperature difference is reduced to 1.3 °C at $m = 0.9$ and $\cos\varphi = 0.6$. For the other case with $m = 0.3$ and $\cos\varphi = 0.99$, the maximum temperature of the proposed topology remains below 53 °C, while the maximum temperature difference is 4.8 °C. The hottest devices in all three cases are S_{x3}', S_{x3}, and S_{x2}'. However, the maximum temperature of the ANPC topology remains above 60 °C for both cases, and the maximum temperature difference is slightly increased to about 12.3 °C. And the most heated device is always S_{x2}. The above results show that the proposed topology can effectively overcome the problem of loss concentration under multiple operating conditions, and reduce the maximum temperature of individual power devices.

VI. CONCLUSION

In this article, an improved four-level inverter topology is proposed that consists of six switches per phase. The total voltage stress of the proposed topology is lower compared

to other topologies without FCs and the maximum blocking voltage of the switches is $2V_{dc}/3$. Owing to the specificity of the structure that greatly reduces the switching losses of the devices subjected to the highest current stress, the proposed topology has a relatively more uniform loss distribution and hence can fully utilize the capacity of all the power devices to increase the system capacity or switching frequency. It also helps reduce the difficulty of heat dissipation and improve the lifetime. Experiments demonstrate the adaptability of the proposed inverter topology under multiple operating conditions, which effectively avoids the continuous concentration of losses and reduces the maximum temperature of the device. Therefore, it is quite attractive for low and medium voltage and large-capacity applications.

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