A Novel Variable-Level ANPC Inverter With Capacitor Voltage Reconfiguration Method for 2 kV Photovoltaic Applications

Jupeng Pang, *Student Member, IEEE*, Chao Wang, *Member, IEEE*, Mingzhe Wu, *Member, IEEE*, Kui Wang, *Senior Member, IEEE*, Zedong Zheng, *Senior Member, IEEE*, and Yongdong Li, *Senior Member, IEEE*

***Abstract*—The 2-kV photovoltaic (PV) system is widely regarded as the next evolution for megawatt-scale PV systems, enabling higher rated power. This article proposes a novel variable-level (VL) active neutral-point clamped (ANPC) inverter, capable of operating in both three- and four-level modes by incorporating a simple bypass switch *K*. To meet the 2-kV voltage grade requirement, the principle of device selection is thoroughly deduced, identifying the hybrid adoption of 1200- and 1700-V devices as an optimal solution in terms of cost and efficiency. In addition, to maximize overall efficiency across the full maximum power point tracking voltage range of PV arrays, a capacitor voltage reconfiguration strategy and a unified adaptive-level PWM method are proposed. These approaches optimize the switching voltage stress distribution between 1200- and 1700-V devices, significantly enhancing the efficiency of the proposed VL ANPC inverter. Simulation and experimental results validate that the proposed inverter, along with its modulation and control methods, offers a competitive and viable solution for 2-kV PV applications.**

***Index Terms*—Capacitor voltage control, centralized PV inverter, grid-tied inverter, multilevel inverter, 2-kV photovoltaic (PV) system.**

I. Introduction

With the urgent global demand for decarbonization and carbon neutrality, the development and deployment of renewable energy have accelerated significantly in recent years. Among various renewable sources, photovoltaic (PV) energy has emerged as one of the most promising solutions due to its scalability, sustainability, and declining cost. Particularly, megawatt (MW)-scale PV systems are gaining increasing attention as they enable high power output, low maintenance cost, excellent grid-supporting capability, and high efficiency [1], [2], making them a viable option for utility-scale clean energy generation.

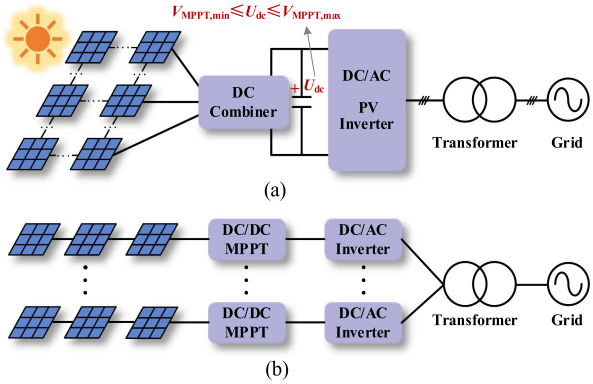

Fig. 1. Structure of PV systems. (a) Centralized PV systems with single-stage centralized PV inverters. (b) Distributed PV systems with string PV inverters.

As shown in Fig. 1, PV systems can generally be categorized into two main architectures: centralized [as shown in Fig. 1(a)] and distributed [as shown in Fig. 1(b)] structures. In distributed PV systems, multiple string inverters and high-efficiency dc–dc converters are used. These dc–dc converters facilitate voltage adaptation to maintain constant dc-link voltage of string inverters and enable maximum power point tracking (MPPT), thereby improving system flexibility and overall energy conversion efficiency under varying irradiance conditions. In contrast, centralized PV systems aggregate the output of large PV arrays through combiner boxes and connect to a centralized PV inverter. This architecture is particularly well suited and typically adopted for MW-scale applications due to its simplified structure, reduced component counts, and lower cost. Furthermore, centralized systems typically employ a single-stage PV inverter without an intermediate dc–dc stage [3], [4], [5], which contributes to higher power conversion efficiency, lower operational complexity, and greater economic viability.

To achieve better performance of PV systems, increasing the dc bus voltage has become a well-recognized trend. This can be accomplished by connecting more PV panels in series, which reduces conduction losses by lowering dc current and decreases overall cost by requiring fewer cables and combiner boxes [6]. Currently, 1500-V PV system is gradually dominating

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Jupeng Pang, Chao Wang, Kui Wang, Zedong Zheng, and Yongdong Li are with the State Key Laboratory of Power System, Department of Electrical Engineering, Tsinghua University, Beijing 100084, China (e-mail: pjp22@mails.tsinghua.edu.cn; wangchao_eea@mail.tsinghua.edu.cn; wangkui@tsinghua.edu.cn; zzd@tsinghua.edu.cn; liyd@tsinghua.edu.cn).

Mingzhe Wu is with the School of Mechanical and Electrical Engineering, China University of Mining and Technology—Beijing, Beijing 100083, China (e-mail: wmz@cumtb.edu.cn).

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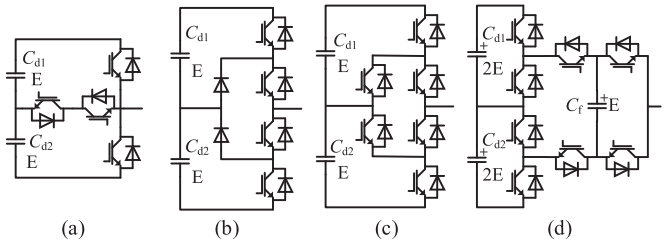

Fig. 2. Potential candidates of the topology of 2-kV PV inverter. (a) 3 L-TNPC. (b) 3 L-NPC. (c) 3 L-ANPC. (d) 5L-ANPC.

the market, outperforming the traditional 1000-V PV system [6], [7], [8]. Building on the maturity of 1500-V PV systems, 2-kV PV system is widely considered the next step for MW-scale centralized PV systems, enabling higher power ratings [7]. Indeed, engineering demonstration projects for 2-kV PV systems have already shown that adopting a 2-kV dc voltage can significantly enhance system efficiency and performance, making it a viable solution for future developments [8]. Thus, the 2-kV centralized PV inverter becomes a critical component demanding focused research in MW-scale centralized PV systems.

The PV inverter needs bearing a maximum dc-link voltage of 2 kV; however, most of the existing topologies and devices used in 1000- or 1500-V PV inverters are no longer suitable or efficient. Fig. 2 illustrates several conventional multilevel inverter topologies potentially applicable to 2-kV PV inverters. Notably, the conventional two-level inverter, which uses high-voltage devices, is excluded due to its low efficiency and high *dv*/*dt*, making it unsuitable for 2-kV PV applications. Fig. 2(a)–(c) presents common three-level (3 L) topologies, such as neutral-point clamped (NPC) [9], T-type neutral-point clamped (TNPC) [10], and active neutral-point clamped (ANPC) [11] topologies, which are used for 1500-V PV inverters. These can be adapted for 2-kV PV inverters by using 1700- or 3300-V devices. However, this adaptation can result in higher switching losses due to the higher blocking voltage and lower switching speed of devices [6], as well as higher electromagnetic interference (EMI) and *dv*/*dt*, making this approach less viable in practice. Another alternative approach from the perspective of topologies is to increase the number of voltage levels for 2-kV PV inverters, as seen in the five-level (5L) ANPC topology shown in Fig. 2(d) [12]. However, this typically requires a greater number of power devices, which leads to increased conduction losses and higher system cost.

Although there exists limited literature on newly developed inverters motivated for 2-kV PV applications [13], [14], several new grid-tied PV inverters have been proposed in recent years, which may serve as references for 2-kV PV inverters. These can be broadly divided into transformerless PV inverters (directly grid-tied) [15], [16], [17], [18], [19], [20], [21] and nonisolated inverters (grid-tied via transformers as shown in Fig. 1) [22], [23], [24]. The transformerless inverter can eliminate the bulky line-frequency transformer, improving the power density of PV systems. However, they can also result in high-frequency leakage currents, leading to safety concerns [15], [16]. To address this, PV inverters with common ground shared between PV panels and grids have been proposed to eliminate leakage currents [15], [16], [17], [18]. In addition, Anand et al. [19] present a 5L transformerless inverter with a common ground, using an extendable multilevel structure to improve power handling capabilities for centralized PV systems. However, these common-ground PV inverters are more vulnerable to faults due to a limited negative voltage output, making them unsuitable for MW-scale PV systems. The cascaded H-bridge structure, known for its modular design and ease of connection to high-voltage grids, is used in transformerless PV inverters in [20] and [21], but the leakage current between H-bridge modules should be carefully managed. As for nonisolated inverters, a three-phase structure is typically used for higher rated power and better compatibility with three-phase transformers. A 5L single-phase TNPC H-bridge inverter is proposed in [22], which can be extended into a three-phase configuration for MW-scale PV systems. Choi and Lee [23] propose a hybrid IT-Type NPC inverter with improved efficiency and reliability. Besides, Dalai et al. [24] introduce a nine-level three-phase switched capacitor inverter to boost output voltage.

In summary, most existing solutions either rely solely on high-voltage-rated devices (resulting in higher EMI and *dv*/*dt*), or adopt complex multilevel topologies (increasing system cost and complexity). Although these approaches are technically feasible, they are not well optimized for 2-kV PV systems. Therefore, a clear gap remains in the co-optimization between topology and device selection for deriving an optimal solution of 2-kV PV inverters.

Furthermore, the control of 2-kV centralized PV inverters presents another challenge. Without an extra dc–dc stage, the single-stage centralized PV inverter can achieve a compact structure and lower cost. However, it requires the inverter to simultaneously perform MPPT control and grid-connected control [25], which means that the dc-link voltage of the inverter varies with MPPT control, affecting the grid-connected operation. Moreover, the dc-link voltage of the centralized PV inverter is often lower than 2 kV due to MPPT operation [3], [4], [5], which may cause efficiency degradation due to device underutilization and diminish superiority of selected topology in the low-voltage range. For instance, a conventional 1500-V PV inverter (such as a 3 L-ANPC inverter using 1200-V devices) can actually achieve optimal efficiency when operating within a dc-link voltage range of 1500 V–1800 V. However, it cannot be used in applications requiring a maximum dc-link voltage of 2 kV. Conversely, although a 2-kV PV inverter (such as a 3 L-ANPC inverter using 1700-V devices) can operate at 2 kV, its efficiency in low-voltage range (e.g., 1500 V–1800 V) is typically lower than that of the conventional 1500-V PV inverter due to lower device utilization and increased switching losses associated with the use of high-voltage-rated devices.

Recent research on PV inverter control mainly focuses on pulsewidth modulation (PWM) techniques [26], [27], [28], [29], common-mode voltage reduction [27], [28], capacitor voltage

balancing for multilevel inverters [29], and low-frequency ripple current suppression [30]. Regarding studies on the varying dc-link voltage, Serban et al. [31] investigate the MPPT voltage range extension for 1500-V PV inverters using a voltage-reactive injection strategy to improve energy capture across a wider temperature range of PV arrays. Qin and Li [32] propose an improved space vector PWM method for 3 L PV inverters, enabling normal operation with both balanced and unbalanced dc-link capacitor voltages. However, optimizing overall efficiency of PV inverters, under varying dc-link voltages of full MPPT ranges, remains insufficiently explored research.

To address the challenge of withstanding the full 2-kV dc-link voltage and bridge the gap in the co-design of the inverter topology and device selection for optimal 2-kV PV applications, this article proposes a novel variable-level (VL) ANPC inverter. The proposed solution incorporates a capacitor voltage reconfiguration (CVR) strategy and a unified adaptive-level PWM (ALPWM) method to achieve the overall efficiency optimization across full MPPT voltage ranges. This solution offers a competitive and practical approach for 2-kV PV applications. The key contributions of this article are as follows.

1) The proposed VL ANPC inverter supports both four-level (4 L) and 3 L operation. By dynamically switching between the two modes according to the varying dc-link voltage, it ensures safe operation under the full 2-kV rating while maintaining the overall high efficiency across the entire MPPT range by minimizing switching losses.
2) Furthermore, the device selection principle of the proposed VL ANPC is analyzed in detail to ensure high voltage utilization, safe voltage margins, and cost-efficient adoption of devices, addressing the gap in the co-optimization between the topology and device selection for deriving an optimal solution of 2-kV PV inverters.
3) The proposed CVR method can reconfigure the voltage distribution across central and side dc-link capacitors, optimizing the distribution of switching voltage stresses and losses among different devices, ultimately enhancing the overall performance of the proposed 2-kV PV inverter.
4) The proposed unified ALPWM method is designed to adapt for both 4 L and 3 L operation of the proposed VL ANPC inverter, which enables the inverter to achieve high efficiency across the full range of varying dc-link voltages resulting from MPPT control. Moreover, the dynamic transition between 3 L and 4 L modulation can be implemented seamlessly by ALPWM, ensuring smooth and efficient operation.

The rest of this article is organized as follows. Section II presents the topology derivation of the VL ANPC inverter and its device selection principle. The proposed CVR strategy, unified ALPWM method, and their implementation are elaborated on in Section III. Section IV presents simulation results and efficiency comparison with other potential 2-kV PV inverters. And experimental verification is presented in Section V. Finally, Section VI concludes this article.

TABLE I
SWITCHING STATES OF THE VL ANPC TOPOLOGY

K	S_{x1}	S_{x2}	S_{x3}	S_{x1}'	S_{x2}'	S_{x3}'	V_o	State
0	0	0	0	1	1	1	0	$V1_4$
	0	0	1	1	1	0	U_{Cd3}	$V2_4$
	0	1	1	1	0	0	$U_{Cd3}+U_{Cd2}$	$V3_4$
	1	1	1	0	0	0	$U_{Cd3}+U_{Cd2}+U_{Cd1}$	$V4_4$
1 (U_{Cd2}=0)	0	0	0	1	1	1	0	$V1_3$
	0	0	1	1	1	0	U_{Cd3}	$V2_3$
	0	1	1	1	0	0	U_{Cd3}	$V3_3$
	1	1	1	0	0	0	$U_{Cd3}+U_{Cd1}$	$V4_3$

II. TOPOLOGY AND OPERATING PRINCIPLE OF THE PROPOSED VL ANPC INVERTER

A. Topology and Switching States

With MPPT operation, the practical dc-link voltage of 2-kV PV inverters is generally lower than 2000 V, as shown in Fig. 1. For example, the MPPT range of the GE Vernova FLEXINVERTER 2000 Vdc solar power station is 1277–1600 V [33]. Hence, on the one hand, the PV inverter must be capable of blocking the maximum permissible dc-link voltage of 2 kV. On the other hand, within the low-voltage range during MPPT operation, the PV inverter leaves an underutilized margin for the rated voltage of devices, which leads to a decrease in the overall efficiency of the inverter. To improve the utilization of devices and enhance the efficiency of 2-kV PV applications, the VL ANPC inverter is proposed, based on the derivation process outlined in Fig. 3.

Although there exist various topologies for 4 L ANPC inverters, all of them can be considered as different variants of the 4 L topology of the multilevel active-clamped (MAC) inverter [31], as shown in Fig. 3(a). For instance, when S_{x2}, S_{x2}', S_{x4}' and S_{x5} ($x = a, b, c$) are turned OFF, the MAC topology becomes the 4 L-ANPC topology, as shown in Fig. 3(c). In addition, the 3 L topology is also embedded within the 4 L MAC topology. The 4 L MAC topology can be degraded to the 3 L-ANPC topology by keeping S_{x1}, S_{x3}', S_{x2}, and S_{x2}' on, thus bypassing the central dc-link capacitor and forming a two-section dc link for the 3 L-ANPC inverter, as shown in Fig. 3(b). From this perspective, the 4 L MAC topology is inherently a VL topology, and the level variation can be achieved by switching S_{x2} and S_{x2}' ON/OFF simultaneously. Therefore, the switch pair S_{x2} and S_{x2}' can be replaced by a single switch K, and the redundant switches can be further disposed to improve the power density and reduce the cost of the inverter. Finally, the proposed VL ANPC inverter is obtained as shown in Fig. 3(d), which can operate in both 3 L and 4 L modes, depending on the switching state of K in parallel with C_{d2}.

The switching states and corresponding output voltages of the proposed VL ANPC inverter are presented in Table I.

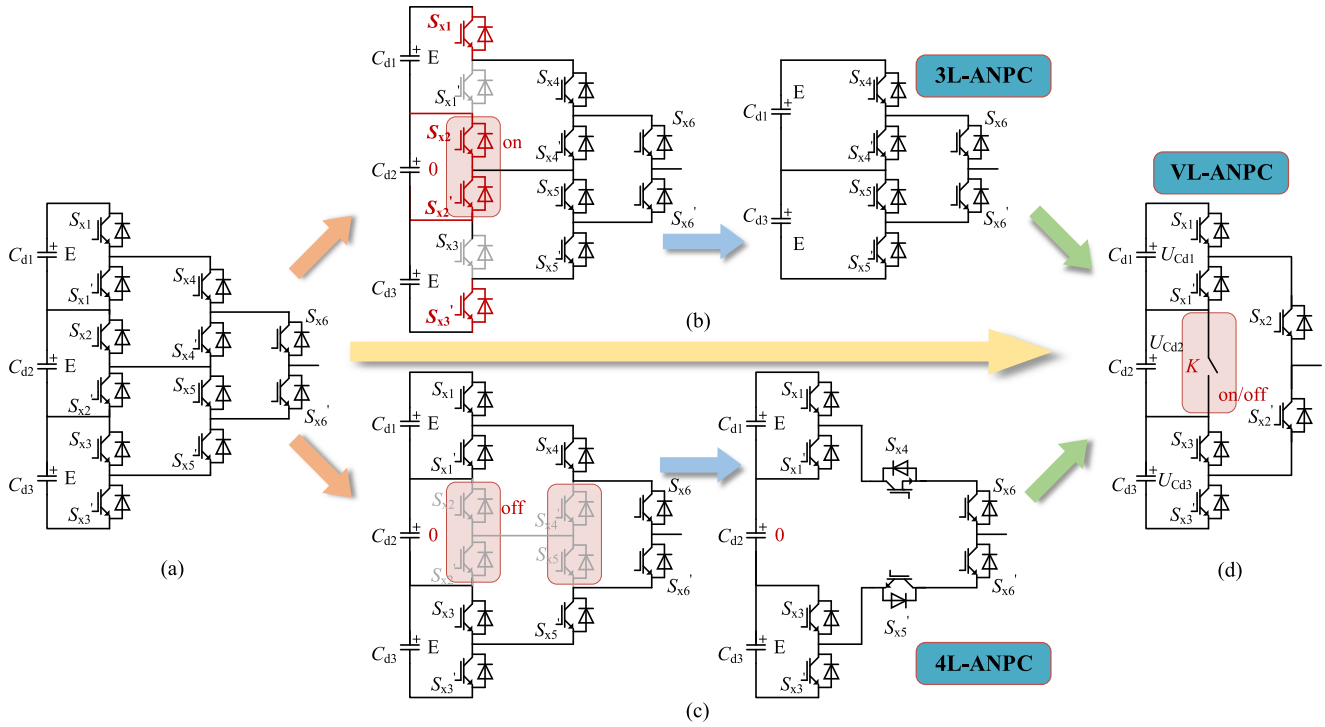

Fig. 3. (a)–(d) Derivation of the proposed VL ANPC inverter.

The introduction of switch K can bypass C_{d2} to reconfigure voltage levels as 3 L when the dc-link voltage decreases during MPPT operation. Conversely, by keeping switch K OFF, the inverter functions as a 4 L-ANPC inverter, capable of handling the high dc-link voltage required for 2-kV PV applications.

B. Principle of Device Selection

For 3 L operation of the proposed VL ANPC inverter ($K = 1$), each device shares an identical blocking voltage. However, during 4 L operation ($K = 0$), the devices S_{x2} (S_{x2}') experience higher blocking voltage compared to S_{x1} (S_{x1}') and S_{x3} (S_{x3}'). This indicates that a hybrid adoption of devices with different rated voltages can be employed to optimize the utilization of the devices' voltage ratings. The device selection principle is elaborated as follows.

As illustrated in Fig. 3(d), let the voltage of C_{di} be U_{Cdi} ($i = 1$, 2, 3). Based on Table I, the maximum blocking voltage of each switch can be derived as follows:

$$\begin{cases} V_{S_{x1},\max} = V_{S'_{x1},\max} = U_{Cd1} \\ V_{S_{x3},\max} = V_{S'_{x3},\max} = U_{Cd3} \\ V_{S_{x2},\max} = U_{Cd2} + U_{Cd3} \\ V_{S'_{x2},\max} = U_{Cd1} + U_{Cd2}. \end{cases} \tag{1}$$

Considering the symmetry of complementary switch pairs with respect to topology and their switching states, the blocking voltage is identical within each switch pair, e.g., S_{x2} and S_{x2}'. Therefore, the following equation can be established:

$$U_{Cd1} = U_{Cd3}. \tag{2}$$

Assuming that $U_{Cd1} = U_{Cd3} = U_{\text{side}}$ and $U_{Cd2} = U_{\text{mid}}$, the maximum blocking voltage of S_{x1} (S_{x1}') and S_{x3} (S_{x3}') can be derived, as shown in (3). Consequently, the 1200-V-rated devices can be selected for S_{x1} (S_{x1}') and S_{x3} (S_{x3}')

$$V_{S_{x1}/S'_{x1},\max} = V_{S_{x3}/S'_{x3},\max} = U_{\text{side}} = \frac{U_{\text{dc}} - U_{\text{mid}}}{2} \leq 1000\,\text{V}. \tag{3}$$

As for the devices S_{x2} (S_{x2}'), their blocking voltages equal the sum of U_{side} and U_{mid}, which can be expressed as follows:

$$V_{S_{x2}/S'_{x2},\max} = U_{\text{mid}} + U_{\text{side}} = 2000\,\text{V} - U_{\text{side}} \geq 1000\,\text{V}. \tag{4}$$

In practice, due to the necessary voltage safety margin to account for overshooting, U_{side} in (3) must be significantly lower than 1000 V for the 1200-V devices S_{x1} (S_{x1}') and S_{x3} (S_{x3}'), particularly under heavy-load conditions. For example, 1200-V devices typically operate with a maximum blocking voltage of 800 V, in order to enhance reliability. Consequently, the blocking voltage of S_{x2} (S_{x2}') exceeds 1000 V in such scenarios. Thus, 1200-V devices are inadequate for S_{x2} (S_{x2}'), whereas 1700-V devices are more suitable, offering sufficient voltage margin while considering device cost.

Therefore, a combination of 1200- and 1700-V devices is implemented to ensure high utilization, adequate voltage margin, and cost-efficient operation for VL ANPC inverters, as depicted in Fig. 4.

However, the two types of devices differ not only in their voltage-blocking capabilities but also in other characteristics, e.g., switching losses. With the same rated current, 1700-V devices typically exhibit higher switching losses compared with

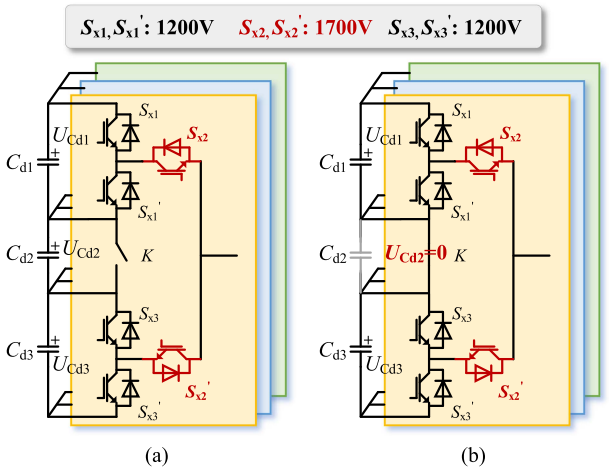

Fig. 4. VL ANPC inverter with 1200- and 1700-V devices. (a) 4L mode. (b) 3L mode. (a) 4-level with *K* open. (b) 3-level with *K* closed.

1200-V devices due to the bigger chip size and thereby larger capacitance [34]. For example, under identical switching conditions (600 V/450 A, 125 °C), the turn-ON loss of Infineon FF450R12KE7 (1200 V/450 A IGBT) is 22.16 mJ [35], while the turn-ON loss of Infineon FF450R17ME7_B11 (1700 V/450 A IGBT) is significantly higher at 58.07 mJ [36]. This demonstrates that 1700-V devices inherently have greater switching losses. Hence, to optimize the overall efficiency of the inverter, it is crucial to minimize the switching losses of 1700-V devices wherever possible.

C. Carrier-Overlapped PWM Method With Reconfigured Capacitor Voltages

Based on the aforementioned analysis, the proposed VL ANPC inverter, which adopts a combination of 1200- and 1700-V devices, particularly in the case of 4L operation, offers a more cost-efficient and low-loss solution for 2-kV PV inverters, compared to 3L schemes utilizing only 1700-V devices. Furthermore, with $U_{Cd1} = U_{Cd3} = U_{\text{side}}$ and $U_{Cd2} = U_{\text{mid}}$, it can be observed in Fig. 5 that the 1700-V devices (S_{x2}, $S_{x2}{}'$) must withstand a maximum voltage of $U_{\text{side}}+U_{\text{mid}}$. However, during switching transitions, these devices only bear the voltage of U_{mid}, which helps to reduce switching losses to some extent.

However, in the case of 4L operation, it is important to note that the traditional phase-disposition PWM (PDPWM) method cannot effectively balance the dc-link capacitor voltages across the full power factor and modulation index range [37]. To address this issue, the carrier-overlapped PWM (COPWM) method is adopted to maintain well-controlled dc-link capacitor voltages under 4L operation [38]. It should be noted that the dc-link capacitor voltages are usually divided evenly for conventional operation of multilevel inverters. And under these conditions, the COPWM method has been proven to satisfy the volt-second balance principle [38].

Nevertheless, to further reduce the switching losses of 1700-V devices S_{x2} ($S_{x2}{}'$), the switching voltage of S_{x2} ($S_{x2}{}'$) can be optimized under varying operating conditions. Therefore, a

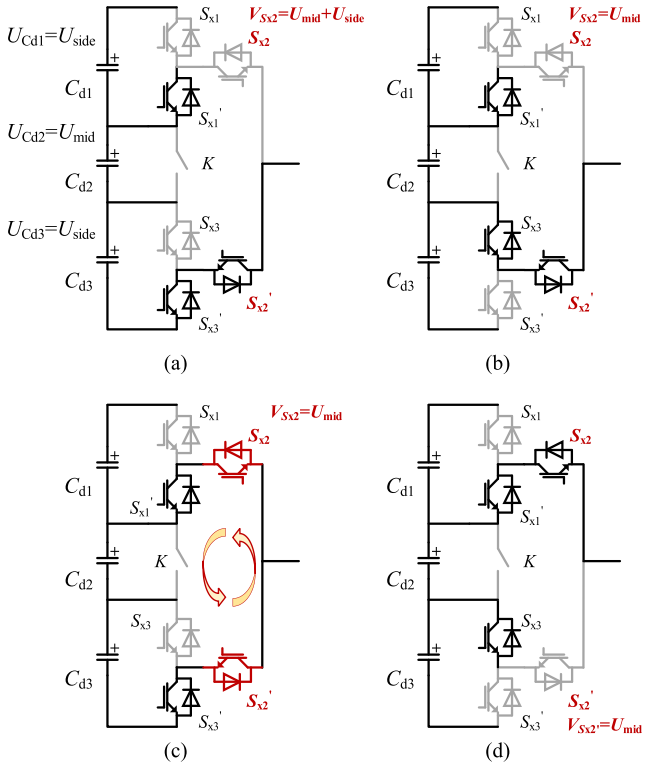

Fig. 5. Commutation transition of VL ANPC inverters under 4L operation. (a) State $V1_4$. (b) State $V2_4$. (c) State $V2_4 \rightarrow V3_4$. (d) State $V3_4$.

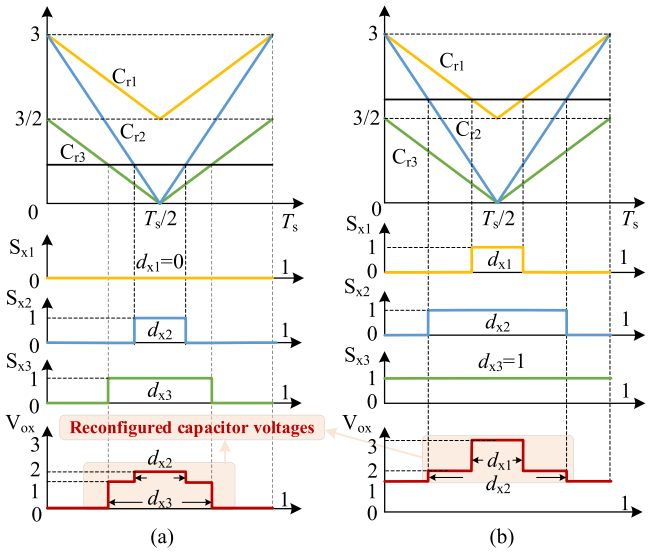

Fig. 6. Diagram of the COPWM with reconfigured capacitor voltages. (a) $0 \le u_{\text{ref}x} < 3/2$. (b) $3/2 \le u_{\text{ref}x} \le 3$. (a) $0 \le u_{\text{ref}x} \le 1.5$. (b) $1.5 \le u_{\text{ref}x} \le 3$.

COPWM method with reconfigured capacitor voltages is proposed first, as illustrated in Fig. 6. In this configuration, the three capacitor voltages are no longer equal, and the central capacitor voltage U_{mid} is intentionally reduced. Under this condition, i.e., $U_{\text{mid}} \neq U_{\text{side}}$, whether the volt–second principle is still satisfied is an important issue.

Assuming that the reference phase voltage $u_{\mathrm{ref}x}$ ranges from 0 to 3, the duty cycles of S_{x1}–S_{x3} in 4 L operation, as shown in Fig. 6(a) and (b), can be written as follows:

$$\begin{cases} d_{x1}=0 \\ d_{x2}=\frac{u_{\mathrm{ref}x}}{3} \\ d_{x3}=\frac{u_{\mathrm{ref}x}}{3} \end{cases}, \quad 0\le u_{\mathrm{ref}x}\le 1.5,$$

$$\begin{cases} d_{x1}=\frac{2(u_{\mathrm{ref}x}-1.5)}{3} \\ d_{x2}=\frac{u_{\mathrm{ref}x}}{3} \\ d_{x3}=0 \end{cases}, 1.5\le u_{\mathrm{ref}x}\le 3. \tag{5}$$

Then, the average output voltage over a carrier period with general dc-link voltages of U_{Cd1}, U_{Cd2}, and U_{Cd3} can be expressed as follows:

$$\begin{aligned} U_{ox}&=\sum_{i=1}^{3} d_{xi}U_{Cdi} \\ &=\begin{cases} \frac{U_{Cd2}+2U_{Cd3}}{3}u_{\mathrm{ref}x}, & 0\le u_{\mathrm{ref}x}\le \frac{3}{2} \\ \frac{U_{Cd2}+2U_{Cd1}}{3}u_{\mathrm{ref}x}, & \frac{3}{2}\le u_{\mathrm{ref}x}\le 3. \end{cases} \end{aligned} \tag{6}$$

To satisfy the volt–second balance principle, the output voltage U_{ox} should satisfy the following expression:

$$U_{ox}=U_{\mathrm{dc}}\cdot u_{\mathrm{ref}x}, \quad 0\le u_{\mathrm{ref}x}\le 3. \tag{7}$$

And it can be easily obtained from (6) and (7) that the COPWM method with reconfigured capacitor voltages can also satisfy volt–second balance principle as long as $U_{Cd1}=U_{Cd3}$, i.e., (2) is satisfied. This implies that the output voltage remains unaffected when the central capacitor voltage is adjusted. Therefore, it is feasible to reduce the total losses by lowering the operating voltage of the 1700-V devices S_{x2} ($S_{x2}{}'$).

III. CVR and Unified ALPWM of the VL ANPC Inverter

A. CVR Strategy

Since the central capacitor voltage does not affect the volt–second principle of COPWM, it provides a degree of freedom to modify the switching-loss distribution, thereby optimizing overall efficiency of the proposed VL ANPC inverter. Hence, to enhance inverter performance during 4 L operation, a dc-link CVR strategy is proposed. By reconfiguring the ratio between U_{side} and U_{mid} under a given overall dc-link voltage, this strategy effectively reduces switching losses and the maximum blocking voltage of the 1700-V devices.

Let the dc-link voltage be denoted as U_{dc}. The relationship between U_{side} and U_{mid} can be written as follows:

$$2U_{\mathrm{side}}+U_{\mathrm{mid}}=U_{\mathrm{dc}}. \tag{8}$$

As shown in Fig. 5, for a given dc-link voltage U_{dc}, reducing U_{mid} helps mitigate the maximum blocking voltage and switching voltage stress of 1700-V devices, thereby improving the voltage-blocking utilization of 1200-V devices. Although this may slightly increase the switching voltage stress on 1200-V devices, the additional voltage stress is shared equally between $S_{x1}(S_{x1}{}')$ and $S_{x3}(S_{x3}{}')$, meaning that the increase in switching loss is not significant. To precisely evaluate the comprehensive effects of the decreased switching voltage stress on 1700-V devices and increased switching voltage stress on 1200-V devices, we define the function of switching loss (per switching ON and OFF motion) with respect to voltage stress as g_1 for 1200-V devices and g_2 for 1700-V devices. Hence, the total average switching loss of the entire inverter per phase $P_{\mathrm{swloss,total}}$ can be described as follows, with the carrier frequency as f_c

$$\begin{aligned} P_{\mathrm{swloss,total}}&=2\left(2\cdot g_1(U_{\mathrm{side}})\cdot\frac{f_c}{2}+g_2(U_{\mathrm{mid}})\cdot f_c\right) \\ &=2f_c\cdot g_1(U_{\mathrm{side}})+2f_c\cdot g_2(U_{\mathrm{mid}}). \end{aligned} \tag{9}$$

Furthermore, considering the safe margin for voltage overshooting, the 1200- and 1700-V devices typically operate at voltages lower than their rated blocking voltage. Denote the maximum utilization rates of blocking voltage as η_1 for 1200-V devices and η_2 for 1700-V devices, and the constraint on capacitor voltages can be written as follows:

$$\begin{cases} 0\le U_{\mathrm{side}}\le 1200\eta_1 \\ 0\le U_{\mathrm{mid}}\le 1700\eta_2. \end{cases} \tag{10}$$

Therefore, for a given dc-link voltage, e.g., $U_{\mathrm{dc}}{}^*$ obtained by MPPT control, with the basis of (8)–(10), the general CVR can be modeled as

$$\begin{aligned} &\min\ P_{\mathrm{swloss,total}}=2f_c\cdot g_1\left(\frac{U_{\mathrm{dc}}^*-U_{\mathrm{mid}}}{2}\right)+2f_c\cdot g_2(U_{\mathrm{mid}}) \\ &\text{s.t.}\begin{cases} U_{\mathrm{dc}}^*-2400\cdot\eta_1\le U_{\mathrm{mid}}\le U_{\mathrm{dc}}^* \\ 0\le U_{\mathrm{mid}}\le 1700\cdot\eta_2. \end{cases} \end{aligned} \tag{11}$$

With (11), the optimized U_{mid} can be determined for CVR to minimize overall switching losses of the inverter. It should be noted that conduction losses are independent of the aforementioned CVR process, so the optimization results will directly improve the efficiency of the inverter. Although the optimization outcome of CVR depends on switching-loss characteristics of selected devices, the aforementioned modeling and formulation of CVR control is decoupled from specific device characteristics. Therefore, it demonstrates generality and adaptability of the proposed CVR strategy across different device types and manufactures.

To illustrate the proposed CVR strategy in more detail, an example is analyzed with $\eta_1=\eta_2=2/3$. And the functions g_1 and g_2 are obtained for Infineon FF450R12KE7 and FF450R17ME7_B11 from the official PLECS models, which are practiced through linear interpolation. The expressions of g_1, g_2, and $P_{\mathrm{swloss,total}}$ are as follows:

$$\begin{aligned} g_1(u)&=k_1u \\ g_2(u)&=k_2u \\ P_{\mathrm{swloss,total}}&=k_1f_cU_{\mathrm{dc}}^*+f_c(2k_2-k_1)U_{\mathrm{mid}}. \end{aligned} \tag{12}$$

It is worth noting that the linear interpolation method is widely adopted in both simulation and theoretical analysis. Under fixed-load currents, gate driver parameters, and switching speed, switching losses are usually regarded as incrementally linear with respect to switching voltage stresses, which has

been studied experimentally [39]. Hence, considering that the coefficient of 1700-V devices (k_2) is larger than the coefficient of 1200-V devices (k_1), the minimum $P_{\text{swloss,total}}$ occurs when U_{mid} is as follows:

$$U_{\text{mid}} = \begin{cases} U_{\text{dc}}^* - 2400\eta_1, & U_{\text{dc}}^* > 2400\eta_1 \quad \text{(4L mode)} \\ 0, & U_{\text{dc}}^* \le 2400\eta_1 \quad \text{(3L mode)} \end{cases}. \tag{13}$$

From (13), it is evident that the optimized operating point varies with the dc-link voltage. The operation model of the proposed VL ANPC inverter adjusts dynamically according to the relationship between $U_{\text{dc}}{}^*$ and $2U_{\text{cr}}$, where U_{cr} is the criterion for the 3L/4L selection, given by

$$U_{\text{cr}} = \frac{U_{\text{dc}}^* - U_{\text{mid}}}{2} = 1200 \cdot \eta_1. \tag{14}$$

Moreover, U_{cr} is also the maximum voltage value of 1200-V devices within consideration of safe margin, and the 1200-V devices are operating at this voltage throughout the 4L operation mode. Therefore, the proposed CVR strategy can cooperate well with the proposed VL ANPC inverter, i.e., for a given dc-link capacitor voltage; the low-switching-loss devices (1200-V devices) are optimally utilized, while the high-switching-loss devices (1700-V devices) are optimized to minimize their switching loss.

Above all, regardless of whether the MPPT result corresponds to a global or sub-MPPT condition, the MPPT algorithm of the centralized PV inverter will always output a reference dc-link voltage $U_{\text{dc}}{}^*$ [3], [4], [5]. The proposed CVR control strategy is designed to function effectively under any given $U_{\text{dc}}{}^*$, by ensuring the optimal voltage distribution across the dc-link capacitors. Therefore, the proposed CVR strategy ensures that the inverter operates at its optimal modulation level and minimal loss condition all the time, regardless of the MPPT status, which makes the method robust to different irradiance scenarios, including partial shading. As a result, the overall efficiency and cost performance of the proposed inverter are improved.

B. Unified ALPWM Method

It can be seen from (13) that once the dc-link voltage drops below a certain threshold, the VL ANPC inverter will switch to the 3L topology. In this case, the COPWM is no longer required, as the complexity of capacitor voltage balancing is significantly reduced. Even the conventional PDPWM has been shown to effectively maintain capacitor voltage balance in 3L ANPC inverters [40], thereby enabling greater flexibility in the modulation strategy to further optimize the switching losses of the 1700-V devices and improve overall system efficiency.

Therefore, a unified ALPWM method for VL operation is proposed, as shown in Fig. 7. The unified ALPWM method employs a unified carrier configuration for both 3L and 4L operation, with the only difference being the carrier wave C_{r2}. Hence, the dynamic transition between 3L and 4L modulation can be achieved seamlessly by modifying the carrier wave C_{r2}, which makes this PWM method easily implementable with a digital control system and ensures good dynamic performance of the proposed VL ANPC inverter.

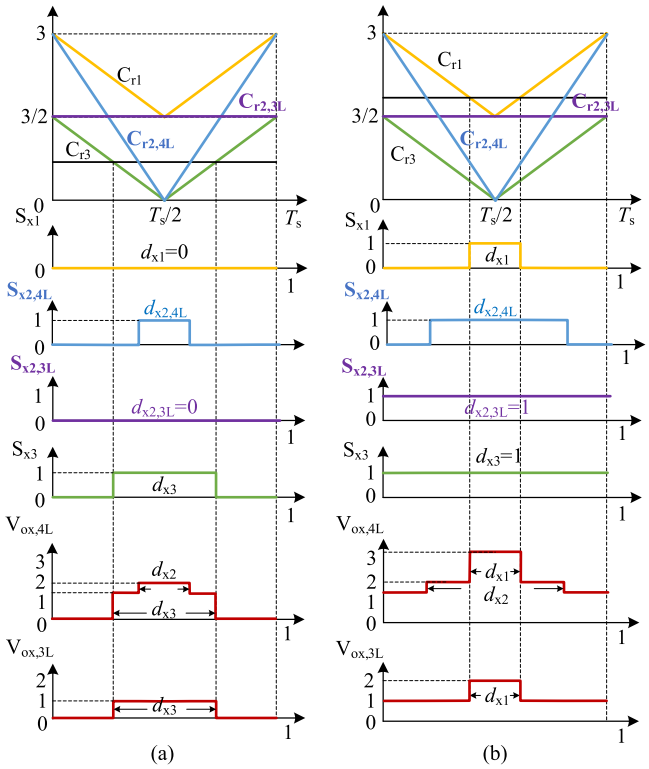

Fig. 7. Diagram of the unified ALPWM method. (a) $0 \le u_{\text{ref}x} < 3/2$. (b) $3/2 \le u_{\text{ref}x} \le 3$. (a) $0 \le u_{\text{ref}x} < 1.5$. (b) $1.5 \le u_{\text{ref}x} \le 3$.

TABLE II
VOLTAGE STRESS AND SWITCHING FREQUENCY OF DEVICES

Operation mode		$S_{x1}(S_{x1}')$	$S_{x2}(S_{x2}')$	$S_{x3}(S_{x3}')$
3L	$V_{\max}$	U_{side}	U_{side}	U_{side}
	V_{sw}		0	
	f_{sw}	$f_c/2$	f_b	$f_c/2$
4L	$V_{\max}$	U_{side}	$U_{\text{side}} + U_{\text{mid}}\,(= U_{\text{dc}} - U_{\text{side}})$	U_{side}
	V_{sw}		U_{mid} [obtained by (13)]	
	f_{sw}	$f_c/2$	f_c	$f_c/2$

f_c: carrier frequency. f_b: fundamental frequency.

In addition, the proposed ALPWM method not only enables unified configuration for 3L and 4L operation but also effectively utilizes the modulation flexibility under 3L and 4L operation, ensuring higher efficiency and more stable performance across different operating conditions. For 3L operation, the modulation for S_{x1} ($S_{x1}{}'$) and S_{x3} ($S_{x3}{}'$) remains constant, while the switch S_{x2} ($S_{x2}{}'$) transitions to line-frequency modulation, for which the switching loss of 1700-V devices can be further decreased or even eliminated due to zero switching voltage stress, according to the corresponding switching states ($V2_3$ and $V3_3$) listed in Table I. As for 4L operation, the unified ALPWM is consistent with the COPWM with CVR, with which the CVR strategy can be easily implemented.

In addition, the maximum blocking voltage ($V_{\max}$), switching voltage stress (V_{sw}), and switching frequency (f_{sw}) of each device under the proposed unified ALPWM method are shown in Table II, from which it can be observed that the switching losses

of S_{x2} (S_{x2}') are optimized in both 3 L and 4 L modes, with optimized switching frequency and reduced switching voltage stress.

Hence, with the proposed CVR strategy and the unified ALPWM method, the overall efficiency of the proposed VL ANPC inverter can be optimized, by leveraging relatively low switching losses of 1200-V devices while avoiding high switching losses of 1700-V devices.

C. Capacitor Voltage Control

With the premise of the aforementioned CVR strategy and the unified ALPWM method, another key problem is to ensure stable control of capacitor voltages at the given value. Given a certain dc-link voltage, this problem can be decoupled into maintaining the capacitor voltage balance between C_{d1} and C_{d3} and stably controlling the capacitor voltage of C_{d2}. First, for the capacitor voltage balance between C_{d1} and C_{d3}, it can be maturely achieved by the zero-sequence voltage (ZSV) injection method under both 4 L and 3 L operation [38], which is completely unaffected by the CVR strategy. On the other hand, for the stable capacitor voltage control of C_{d2}, it can also be easily achieved by adjusting the three duty cycles (d_{x1}, d_{x2}, d_{x3}) slightly to modify the neutral-point currents [38]. These capacitor voltage balancing techniques have been thoroughly analyzed in our previous work [38] and are, therefore, not the focus of this article.

D. Implementation Procedure of Proposed Methods

The overall implementation procedure of the proposed CVR strategy and the capacitor voltage control method is shown in Fig. 8.

1) *Determining $U_{\rm cr}$ based on device characteristics:* First of all, η_1, η_2, g_1, and g_2 are determined based on the characteristics of adopted devices and the hardware design of inverter, for example, the parasitic parameters of dc busbar and the performance of snubber circuit, which affect the voltage overshooting values. Then, $U_{\rm cr}$ can be solved by (11). It should be noted that $U_{\rm dc}{}^*$ in (11) is given by the MPPT dc-link voltage control, as shown in the gray box in Fig. 8, which is relatively mature studied [41], [42] and decoupled from the proposed CVR strategy and the capacitor voltage control method, thus not the key point of this article.
2) *Capacitor voltage reconfiguration:* With the solved $U_{\rm cr}$ and given $U_{\rm dc}$, the CVR strategy, as well as the principle of selection between 3 L and 4 L operation, can be modeled, e.g., (13). Hence, the switching state of K and the three reference values of capacitor voltages can be set.
3) *Unified ALPWM and capacitor voltage control:* On the basis of reference voltage generated by normal grid-connected current control [43], the proposed unified ALPWM method together with ZSV injection and duty cycle adjustment can generate driver signals for the inverter, which can ensure both reference output voltage and stable capacitor voltage control.

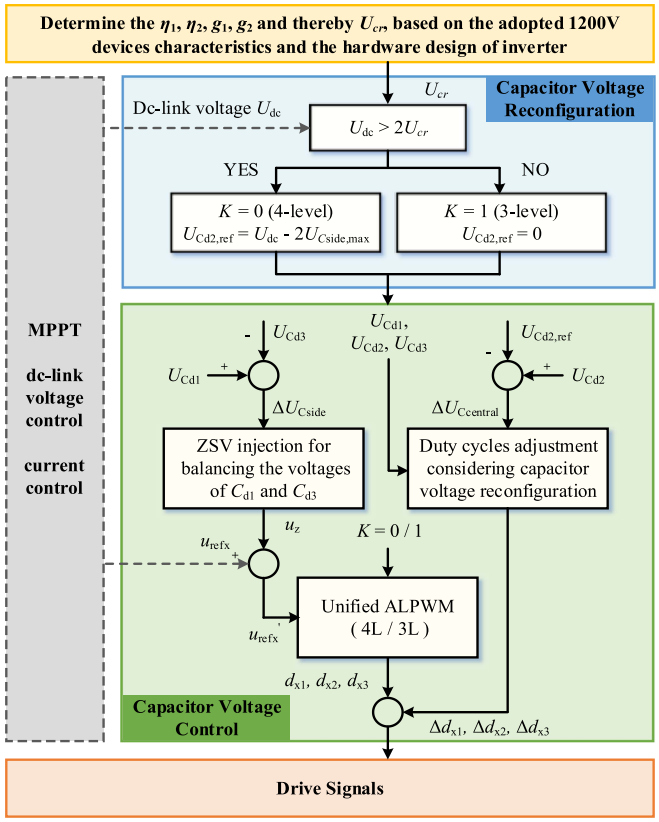

Fig. 8. Implementation procedure of proposed methods.

To sum up, the overall implementation procedure has taken into consideration the VL topology, difference in device characteristics, unified ALPWM, CVR strategy, and capacitor voltage control to improve performance of the proposed VL ANPC inverter in 2-kV PV applications under full ranges of MPPT voltage.

E. Design and Operating Consideration of Switch K

The adoption of switch K is one of the main distinctive features of the proposed VL ANPC inverter compared to conventional inverters. On the one hand, for the static characteristics, the switch K should have the maximum blocking voltage of $1700\eta_2$ according to (10), while having low ON-state resistance to ensure reliable and efficient bypassing of C_{d2} under 3 L operation. On the other hand, for the dynamic characteristics, the motion of switch K is controlled by the CVR strategy shown in the blue box of Fig. 8, which indicates that the state of switch K is mainly determined by the dc-link voltage set by MPPT control. Typically, MW-scale centralized PV plants exhibit significantly smoother short-term voltage and power fluctuations compared to small-scale distributed PV systems, reflecting a higher degree of MPPT voltage stability. Consequently, the MPPT-regulated dc-link voltage in centralized PV systems shows very limited fluctuations over short time spans [5], [44], but with an overall trend governed by gradual daily irradiance variation. This means that the transition between 3 L and 4 L operation occurs not that frequently. Even if the maximum power point varies in a

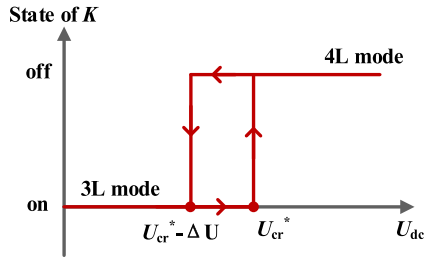

Fig. 9. Hysteresis strategy for the motion of switch K.

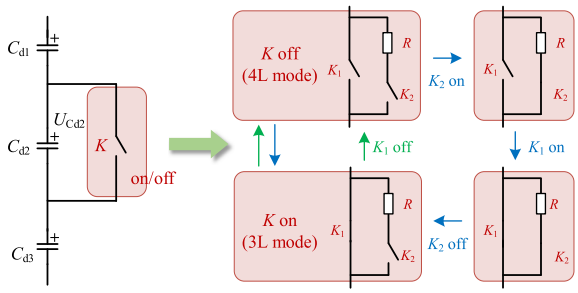

Fig. 10. Internal realization of K and its switching sequence.

short time, the according shift of dc-link voltage is within a narrow range, which may not cause the motion of switch K. Therefore, the switching frequency or speed requirement for switch K is not too high compared to semiconductor devices. Hence, with aforementioned characteristics, the switch K can be implemented by solid-state breakers or even mechanical breakers, which has good bypassing capability, high reliability, low cost, and adequate switching speed.

In addition, for the operation of switch K, to avoid producing extra arc and losses, the switching action of K should be carried out just when $U_{Cd2} = 0$ for reliability, which can be first ensured reliably by the duty cycle adjustment of capacitor voltage control with the adopted balancing control strategy [38]. Second, as mentioned earlier, in the context of centralized PV systems, the MPPT-regulated dc-link voltage varies gradually due to the smooth irradiance profile throughout the day. This slow variation allows sufficient time for the control loop to regulate U_{Cd2} before any switching action of K is triggered. Furthermore, to avoid the undesired frequent action of switch K when U_{Cd2} is fluctuating around 0, a hysteresis strategy can be adopted for the control of switch K, as shown in Fig. 9. In practice, the window width (i.e., ΔU) of the hysteresis strategy can be empirically determined based on system-level behavior and typical variation patterns observed in centralized PV systems.

Finally, to further ensure that the transition between 3 L and 4 L modes via K is both electrically secure and practically feasible with mechanical (solid-state) switches, in practical implementation, the internal realization of K can include two separate switches: K_1 (main path) and K_2 (discharge path), along with a high-resistance discharge resistor R at discharge path, as illustrated in Fig. 10.

For the OFF-state of K, both K_1 and K_2 in Fig. 10 are open (OFF), and thus, the VL ANPC inverter operates in the mode of 4 L. For the ON-state of K, only K_1 is closed (ON) to bypass the central C_{d2}, and the VL ANPC inverter operates in the mode of 3 L.

As for the transition from the 4 L mode to the 3 L mode, the capacitor voltage U_{Cd2} is first regulated to zero by the control loop. Then, switch K_2 is turned ON, placing the discharge resistor in parallel with the central capacitor C_{d2}. Since U_{Cd2} is already near zero, the discharge process takes little time. Subsequently, switch K_1 is closed to establish the main conduction path. Finally, K_2 is turned OFF under zero-current conditions, ensuring a smooth and safe transition. On the other hand, for the transition from the 3 L mode to the 4 L mode, the K_1 breaker can be directly turned OFF to cut the current path, since the current flowing through K can be transferred to C_{d2} to charge it.

This staged operation ensures that any remaining charge on the central capacitor can be safely dissipated before K is fully turned ON, mitigating potential switching transients or shoot-through concerns. Therefore, even if a minor voltage deviation exists due to unexpected errors, this hardware-level discharge mechanism can provide a second layer of safety for the proposed VL ANPC inverter.

TABLE III
SIMULATION PARAMETERS OF 2-KV PV INVERTERS

Parameter	Value	Parameter	Value
AC line voltage	800 V (RMS)	Rated current and power	230.9 A/320 kW (cosφ=1)
DC-link capacitance	C_{d1}=C_{d2}=C_{d3}=1 mF	MPPT range	1225–1850 V
Switching frequency	12 kHz	U_{cr}	800V
1200 V devices	1200 V/450 A IGBT Infineon FF450R12KE7	1700 V devices	1700 V/450 A IGBT Infineon FF450R17ME7_B11

IV. SIMULATION AND COMPARISON RESULTS

To prove the effectiveness of the proposed VL ANPC inverter, unified ALPWM method, CVR strategy, and capacitor voltage control method, a MATLAB/Simulink model is built for the simulation of 2-kV PV inverters. The detailed simulation parameters are shown in Table III, and the parameters are designed by scaling up the existing 1500-V system.

A. Simulation Results

Fig. 11 shows simulation results of capacitor voltages, phase voltage, line voltage, and phase current with $U_{dc} = 1850$ V. In such a condition, the VL ANPC inverter is operating in the 4 L mode, and 1200-V devices are operating at its maximum voltage ($U_{cr} = 800$ V). Hence, the switching voltage stress of 1700-V devices is only 250 V, which greatly reduces the switching losses. In addition, the simulation results prove that the reconfigured capacitor voltage can be well controlled with the capacitor voltage control method presented in Fig. 8. The zoom-in view of phase voltage and line voltage are also provided

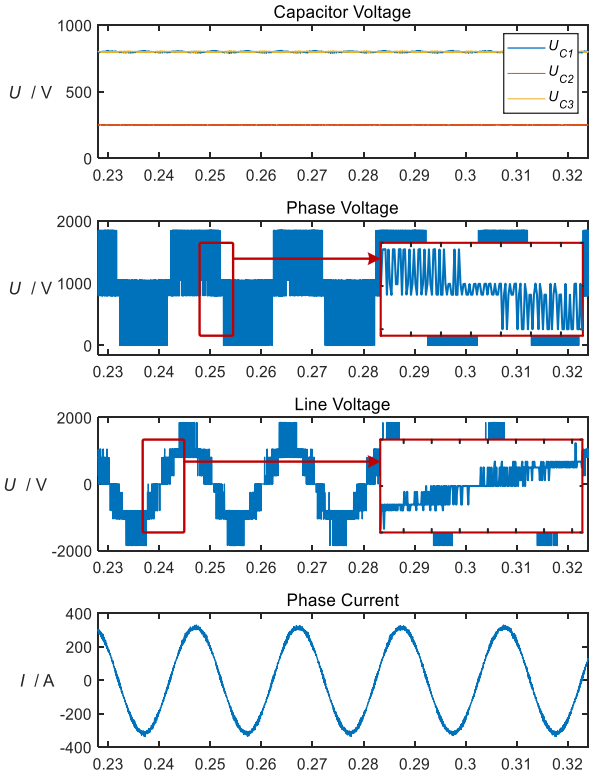

Fig. 11. Simulation results under $U_{\rm dc} = 1850$ V ($U_{C1} = U_{C3} = 800$ V, $U_{C2} = 250$ V).

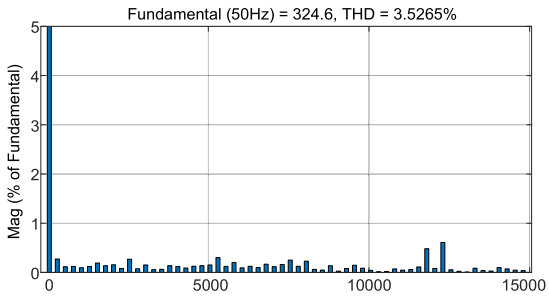

Fig. 12. Phase current harmonic spectrum results related to Fig. 11.

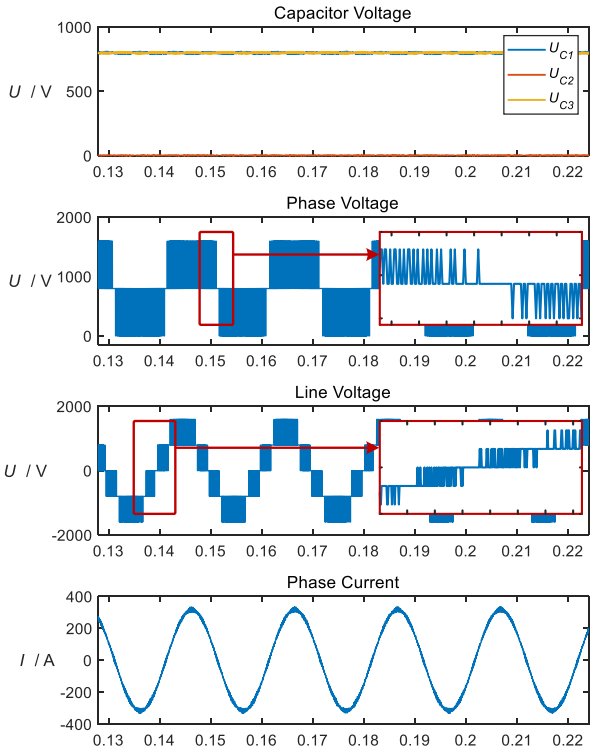

Fig. 13. Simulation results under $U_{\rm dc} = 1600$ V ($U_{C1} = U_{C3} = 800$ V, $U_{C2} = 0$ V).

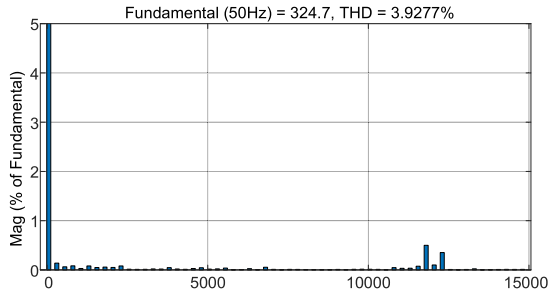

Fig. 14. Phase current harmonic spectrum results related to Fig. 13.

in Fig. 11, from which it can be seen that there exists a missed pulse and apparent level skipping (e.g., a transition from 0 level directly to 2 level) from time to time. It should be noted that this phenomenon arises not from topological limitations, but rather from the temporal modulation conflicts between power quality and capacitor balancing control, which can be addressed by implementing a minimum pulsewidth limiter to prevent such narrow pulses. Moreover, the phase current harmonic spectrum is given in Fig. 12 with total harmonic distortion (THD) of 3.5265%, which indicates that the proposed VL ANPC inverter and its control methods have a good performance of harmonics and are friendly to PV applications.

The simulation results with $U_{\rm dc} = 1600$ V are shown in Fig. 13, and the VL ANPC inverter is operating in the 3L mode with 1200-V devices bearing its maximum voltage ($U_{\rm cr} = 800$ V). In that case, the 1700-V devices switch in line frequency with much lower switching losses. The simulation results prove that the capacitor voltages can also be well controlled. Moreover, the zoom-in view of phase voltage and line voltage is also provided. It can be seen that the level skipping phenomenon is addressed by implemented a minimum pulsewidth limiter, and thus, the *dv*/*dt* performance is further improved. The according phase current harmonic spectrum is given in Fig. 14 with THD of 3.9277%.

Fig. 15 demonstrates dynamic capacitor voltage controlling effect with different reconfiguration schemes under $U_{\rm dc} = 1500$ V. $U_{\rm mid}$ is set to 500, 375, 250, 125, and 0 V, respectively, while $U_{C1} = U_{C2} = U_{\rm side} = (1500 - U_{\rm mid})/2$. The results prove that capacitor voltages can be well controlled.

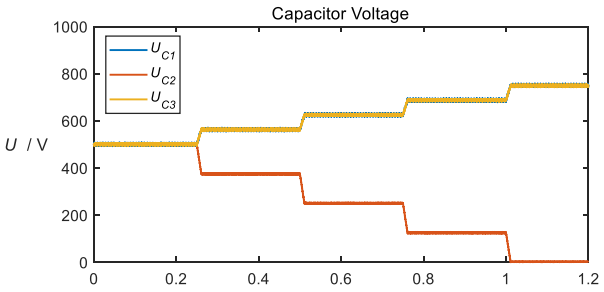

Fig. 15. Simulation verification of dynamic capacitor voltage controlling.

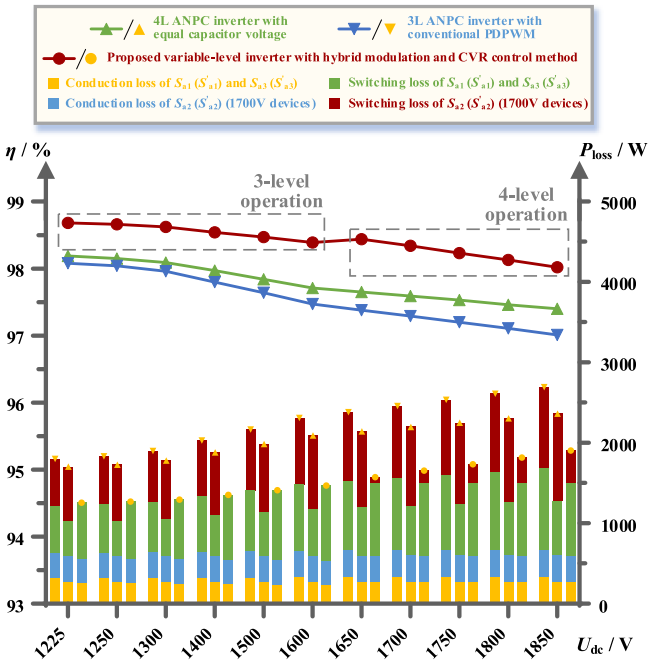

Fig. 16. Efficiency comparison results with respect to varying DC-link MPPT voltages.

B. Comparison With Other Candidates of 2-kV PV Inverters

To further prove the novelty and superiority of the proposed VL ANPC inverter, unified ALPWM, CVR strategy, and capacitor voltage control method, the efficiency comparison among candidates of 2-kV PV inverters is conducted based on the PLECS model.

The 3 L ANPC inverter (with adoption of all 1700-V devices), the 4 L ANPC inverter (with adoption of 1200- and 1700-V devices, evenly distributed capacitor voltages, and COPWM), and the proposed VL inverter (with adoption of 1200- and 1700-V devices, CVR strategy, and unified ALPWM) are compared at rated power and unity power factor, within full MPPT voltage range shown in Table III. The efficiency curves and composition of inverter losses are shown in Fig. 16.

It can be observed from Fig. 16 that, for low-voltage MPPT range (1225 V $\leq U_{\rm dc} \leq$ 1600 V), the unified ALPWM method enables 1700-V devices switching in line frequency and thereby greatly reduces the switching losses (as shown as the nearly zero red bars). On the other hand, for the high-voltage MPPT range

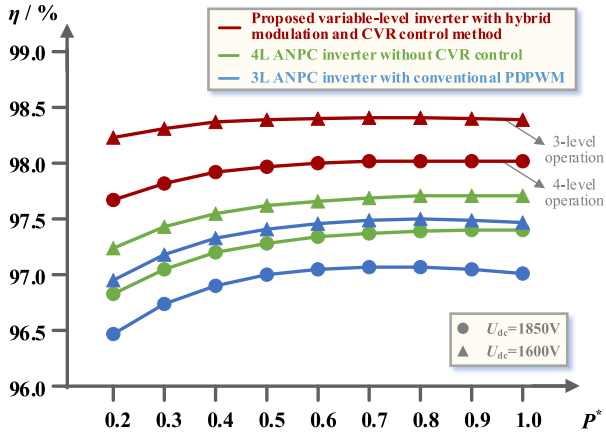

Fig. 17. Efficiency comparison results with respect to power. ($P*$ = output power/rated power).

(1600 V $< U_{\rm dc} \leq$ 1850 V), the VL ANPC inverter operates in the 4 L mode, and the proposed CVR method optimizes the switching loss distribution between 1200- and 1700-V devices, which slightly increases the switching loss of 1200-V devices but greatly decreases the switching loss of 1700-V devices (as shown as the green and red bars), finally reducing the total losses. Therefore, the overall efficiency of the proposed VL ANPC inverter is ultimately improved within full MPPT voltage range, which strengthens overall superiority of the proposed 2-kV PV inverter compared to other schemes.

In addition, the comparison is conducted at different power points, with $U_{\rm dc}$ = 1850 and 1600 V, respectively, and the results are shown in Fig. 17. The color of curves represents different candidates of 2-kV PV inverters, while the shape of data represents operating conditions with different dc-link voltages. The proposed VL inverter operates in the 3 L mode for $U_{\rm dc}$ = 1600 V and the 4 L mode for $U_{\rm dc}$ = 1850 V.

It can be seen from Figs. 16 and 17 that, regardless of the power level or $U_{\rm dc}$, the proposed VL ANPC inverter with the proposed modulation and control methods is superior to other candidates, which demonstrates the novel performance of the proposed inverter, modulation, and control methods. In particular, for the high-voltage case of $U_{\rm dc}$ = 1850 V, the proposed VL inverter operates in the 4 L mode, and the reconfigured capacitor voltages with low $U_{\rm mid}$ decrease the switching loss of 1700-V devices, for which the overall efficiency of the proposed inverter is significantly improved and stands out from other candidates, as shown by the comparison of three dotted lines in Fig. 17. Hence, among candidates of 2-kV PV inverters, the proposed inverter is competitive in terms of device count, cost, and efficiency.

V. Experimental Verification

To further verify the effectiveness of the proposed VL ANPC inverter with unified ALPWM, CVR strategy, and capacitor voltage control method, a downscaled prototype is set up, as shown in Fig. 18. The experimental parameters are shown in Table IV.

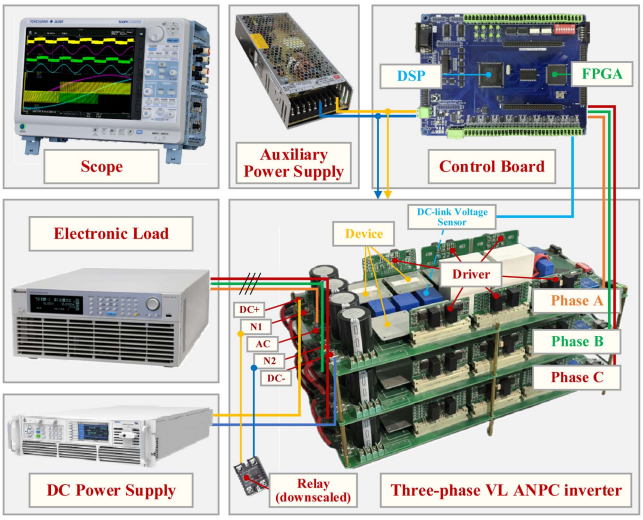

Fig. 18. Experimental prototype of the proposed VL ANPC inverter.

TABLE IV
EXPERIMENTAL PARAMETERS OF THE DOWNSCALED PROTOTYPE

Parameter	Value	Parameter	Value
DC-link voltage	120–180 V	Modulation index	0.95
Load	14 Ω + 2 mH	$C_{d1} = C_{d2} = C_{d3}$	820 uF
Switching frequency	5 kHz	U_{cr}	60 V

Fig. 19(a) shows the experimental results with dc-link voltage varying from 180 to 120 V. It can be seen that the U_{Cd1} and U_{Cd3} remain equal to U_{cr} (60 V), while U_{Cd2} decreases constantly to adapt the changing dc-link voltage, which is consistent with the implementation shown in Fig. 8.

Three zoom-in figures are also shown in Fig. 19(b)–(d) to present the waveforms of phase voltage, line voltage, phase current, and drive signals of S_{a2} and S_{a3} under three conditions. It is worth noting that the phase current values are in direct proportion to the dc-link voltage, while the modulation index stays at 0.95, which proves that the proposed unified ALPWM and the CVR strategy ensure the volt–second balance principle with $U_{Cd1} = U_{Cd3}$ and are of high effectiveness. Moreover, through the waveforms of drive signals, it can be seen that the high-voltage device S_2 has twice switching frequency compared with S_3 in 4 L operation, while switching in line frequency in 3 L operation.

Fig. 20 presents the experimental results of the dynamic transition between 4 L and 3 L operation. The adopted capacitor voltage control method ensures precise and reliable control of U_{Cd2} with little overshooting of capacitor voltages, which guarantees the safety of switching action for breaker K and steady transitions. The hysteresis strategy is also proved to keep the transition of switching action stable. In addition, the unified ALPWM method can also change smoothly, which results in almost no distortion of the phase currents. Moreover, the zoom-in view of phase voltage, phase current, and full waveforms during the CVR process is provided in Fig. 20(b). It can be observed that the *dv*/*dt*, current ripple, and mode shifting performance are all acceptable, which proves the feasibility of the proposed

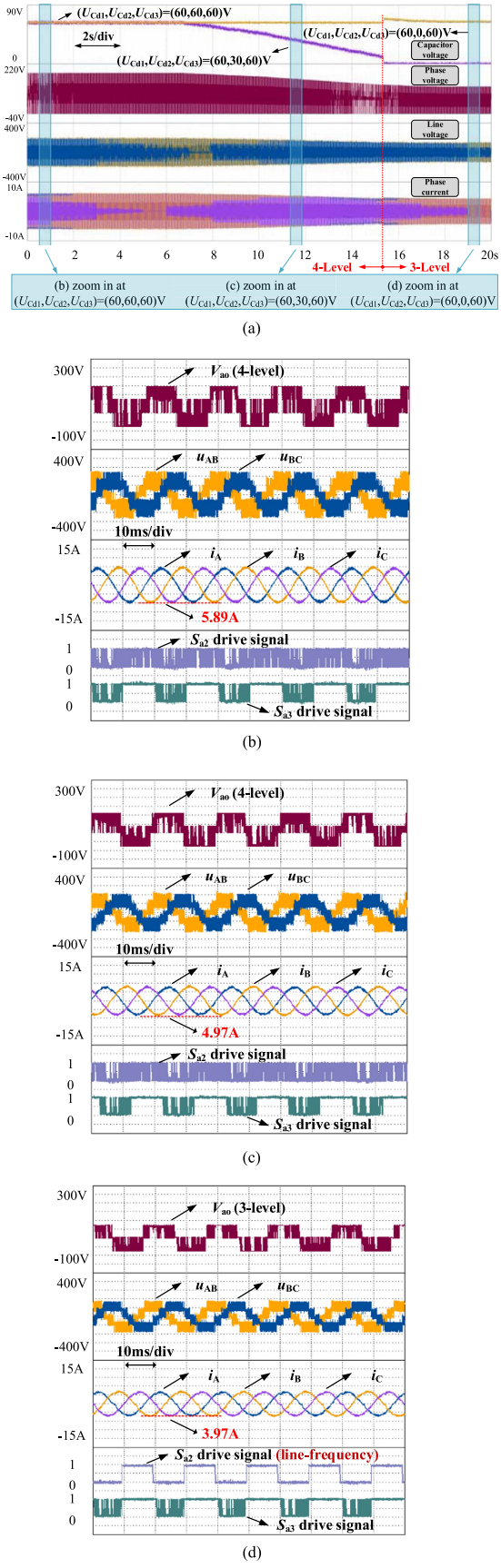

Fig. 19. Experimental results under different reconfigured capacitor voltages. (a) Full-range waveforms. (b) Zoom in at $(U_{Cd1}, U_{Cd2}, U_{Cd3}) = (60, 60, 60)$ V. (c) Zoom in at $(U_{Cd1}, U_{Cd2}, U_{Cd3}) = (60, 30, 60)$ V. (d) Zoom in at $(U_{Cd1}, U_{Cd2}, U_{Cd3}) = (60, 0, 60)$ V.

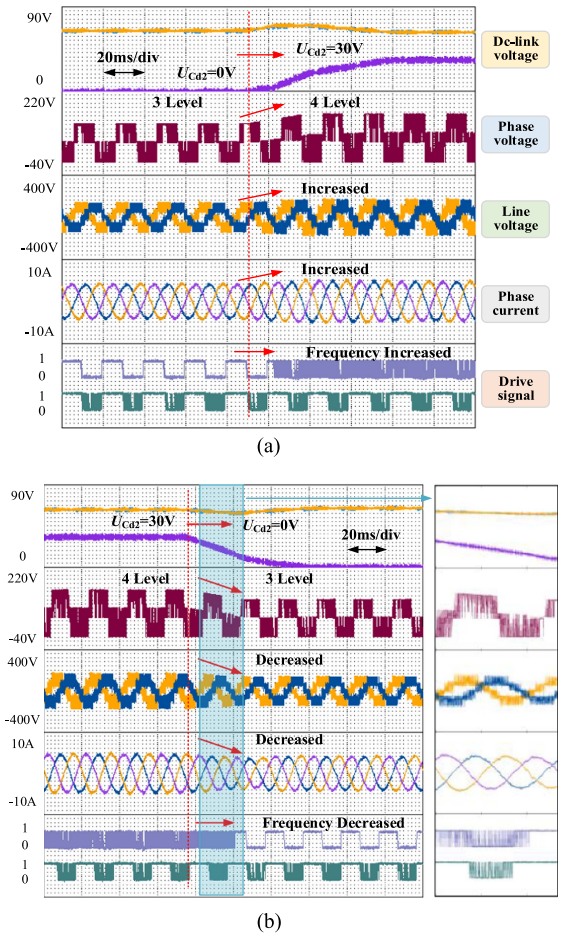

Fig. 20. Experimental results of dynamic transitions. (a) Transition from U_{dc} = 120 V to U_{dc} = 150 V. (b) Transition from U_{dc} = 150 V to U_{dc} = 120 V.

TABLE V
COMPARISON AMONG CANDIDATES OF 2-KV PV INVERTERS (SUPERIORITY: +++ > ++ > + > –)

	Device count	Cost	Efficiency
3L-TNPC	4 (1.7 kV, 3.3 kV)	+	–
3L-NPC	6(1.7 kV)	++	–
3L-ANPC	6(1.7 kV)	+	+
5L-ANPC	8(1.2 kV)	–	++
Proposed	**6(1.2 kV, 1.7 kV)**	+++	+++

The bold values highlight the advantages of proposed topology, compared to other existing topologies.

VL ANPC inverter and the effectiveness of the proposed CVR strategy.

Moreover, Table V shows the comparison among candidates of 2-kV PV inverters, in which the proposed inverter is competitive in terms of device count, cost, and efficiency.

VI. CONCLUSION

The 2-kV PV system is extensively considered the next step for MW-scale centralized PV systems with higher rated power. This article proposes a novel VL ANPC inverter with a hybrid adoption of 1200- and 1700-V devices, and the inverter consists of a breaker, for which it can operate in both 3 L and 4 L modes. A unified ALPWM method and a CVR strategy are proposed to optimize switching voltage stress distribution between 1200- and 1700-V devices, reducing switching losses and finally enhancing overall performance of the proposed VL ANPC inverter. Simulation and experimental results demonstrate the effectiveness of the proposed VL ANPC inverter as well as corresponding modulation and control strategy, proving it a competitive solution for the 2-kV PV system. Aiming to further advance the efficiency, hardware feasibility, and reliability of next-generation PV inverters, future work will focus on prototyping and resolving engineering challenges of the proposed VL ANPC inverter under 2-kV operating conditions.

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Jupeng Pang (Student Member, IEEE) was born in Shandong, China, in 2000. He received the B.S. degree in electrical engineering in 2022 from the Department of Electrical Engineering, Tsinghua University, Beijing, China, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include topology and control of multilevel converters, packaging, and application of wide-bandgap semiconductor.

Chao Wang (Member, IEEE) was born in Gansu, China, in 1993. He received the B.S. and Ph.D. degrees in electrical engineering from the Department of Electrical Engineering, Tsinghua University, Beijing, China, in 2016 and 2022, respectively.

He is currently a Postdoctoral Researcher with the Department of Electrical Engineering, Tsinghua University. His research interests include multilevel converters, renewable energy generation, and wide-bandgap semiconductors.

Mingzhe Wu (Member, IEEE) received the B.Sc. degree in electrical engineering from the China University of Mining and Technology—Beijing, Beijing, China, in 2019, and the Ph.D. degree in energy systems from the University of Alberta, Edmonton, AB, Canada, in 2023.

From 2017 to 2019, he was a Research Assistant with the Department of Electrical Engineering, Tsinghua University, Beijing, working on power system resilience and multilevel converters. He is currently a Lecturer with the Department of Electrical Engineering, China University of Mining and Technology—Beijing, Beijing. His current research interests include topology, modulation, and control of high-power converters.

Dr. Wu was the recipient of the Chinese Government Award for Outstanding Self-Financed Students Abroad in 2021.

Kui Wang (Senior Member, IEEE) was born in Hubei, China, in 1984. He received the B.S. and Ph.D. degrees in electrical engineering from the Department of Electrical Engineering, Tsinghua University, Beijing, China, in 2006 and 2011, respectively.

From 2018 to 2019, he was a Visiting Scholar with the Center for Ultra-Wide-Area Resilient Electric Energy Transmission Networks, University of Tennessee, Knoxville, TN, USA. He is currently an Associate Researcher with the Department of Electrical Engineering, Tsinghua University. His research interests include topology and control of multilevel converters, renewable energy generation, and wide-bandgap semiconductor applications.

Dr. Wang was recognized as the distinguished reviewer for IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS in 2022.

Zedong Zheng (Senior Member, IEEE) was born in born in Shandong, China, in 1980. He received the B.S. and Ph.D. degrees in electrical engineering from the Department of Electrical Engineering, Tsinghua University, Beijing, China, in 2003 and 2008, respectively.

He is currently an Associate Professor with the Department of Electrical Engineering, Tsinghua University. His current research interests include power electronics converters and high-performance motor control systems.

Yongdong Li (Senior Member, IEEE) was born in Hebei, China, in 1962. He received the B.S. degree from the Harbin Institute of Technology, Harbin, China, in 1982, and the M.S. and Ph.D. degrees from the Department of Electrical Engineering, Institute National Polytechnique de Toulouse, Toulouse, France, in 1984 and 1987, respectively, all in electrical engineering.

He was an Invited Professor with the Institute National Polytechnique de Toulouse and the Dean of the School of Electrical Engineering, Xinjiang University, Ürümqi, China. Since 1996, he has been a Professor with the Department of Electrical Engineering, Tsinghua University, Beijing, China, where he is currently the Lead Developer of the Power Electronics and Motor Control Laboratory. His current research interests include power electronics, machine control, and wind power generation.

Dr. Li is a Senior Member of the China Electrotechnique Society, the Vice President of the China Power Electronics Society, and the Vice President of the Electrical Automation Committee of China Automation Association.