# A Novel Modular DC Chopper Based on Combination of Fully and Semicontrolled Devices for Offshore Wind VSC-HVDC Transmission System

Yunqi Jing, Jianwen Zhang, *Senior Member, IEEE*, Liqian Su, Gang Shi, *Member, IEEE*, Jiajie Zang, *Member, IEEE*, Jianqiao Zhou, *Member, IEEE*, Wei Bao, and Xu Cai, *Senior Member, IEEE*

***Abstract*—Voltage source converter based high voltage dc (VSC-HVDC) transmission is widely used for grid integration of offshore wind farms. However, dc overvoltage caused by ac grid faults poses a serious threat to the system. Different dc choppers are commonly employed as energy dissipation devices to enhance the fault ride-through capabilities. This article proposes a novel hybrid dc chopper with composite submodules that combines both fully-controlled and semicontrolled devices, specifically the IGBT and thyristor. This modular hybrid dc chopper incorporates both lumped and distributed resistors, inheriting the merits of both centralized and distributed dc choppers. Meanwhile, the use of thyristors in the submodule topology enables precise power dissipation at a lower cost compared to counterparts relying solely on fully-controlled devices. A submodule modulation scheme is applied to facilitate the forced commutation of thyristors, and the operation principle and control strategies of the chopper are thoroughly investigated. Finally, a full-scale simulation model and a scaled-down experimental prototype are established to validate the chopper's operation principle and performance.**

***Index Terms*—DC chopper, fault ride through, offshore wind farms, voltage source converter based high voltage dc (VSC-HVDC).**

## NOMENCLATURE

| | |
|---|---|
| SEC | Sending end converter. |
| REC | Receiving end converter. |
| VSC-HVDC | Voltage source converter based high voltage direct current. |
| MMC | Modular multilevel converter. |
| FRT | Fault ride-through. |
| DCC | DC chopper. |
| PWM | Pulse width modulation. |
| EMI | Electromagnetic interference. |
| HBSM | Half-bridge submodule. |
| FBSM | Full-bridge submodule. |
| SM | Submodule. |
| IGBT | Insulated gate bipolar transistor. |
| TDS-DCC | Thyristor-diode-switch dc chopper |
| TDS-DCC-SM | SM of TDS-DCC in the energy dissipation valve. |
| PCC | Point of common coupling. |
| $R_{\mathrm{sm}}$ | Distributed cell resistor. |
| $T_1$ | Thyristor in a TDS-DCC-SM. |
| $T_2$ | IGBT in a TDS-DCC-SM. |
| $R$ | Lumped power dissipation resistor. |
| $L_{\mathrm{dcc}}$ | Chopper inductor. |
| $C_{\mathrm{sm}}$ | Capacitance of the SM capacitors. |
| $U_{\mathrm{dc}}$ | DC link voltage. |
| $U_{\mathrm{valve}}$ | Energy dissipation valve output voltage. |
| $U_R$ | Voltage across the lumped resistor. |
| $U_{\mathrm{sm}}$ | TDS-DCC-SM output voltage. |
| $U_{C\mathrm{sm}}$ | SM capacitor voltages. |
| $U_{CN}$ | Rated SM capacitor voltage. |
| $i_{\mathrm{chop}}$ | Chopper branch current. |
| SM-PWM | State control signal for the SM. |
| $ST1$ | Gate trigger pulse of $T_1$. |
| $ST2$ | Gate driving signal of $T_2$. |
| $i_{T1}$ | Thyristor current. |
| $u_{T2}$ | IGBT voltage. |
| $V_{AK}$ | Voltage across thyristor. |
| $t_Q$ | Duration of reverse bias across thyristor for forced commutation. |
| $t_q$ | Thyristor turn-OFF time. |
| $U_{\mathrm{dc}N}$ | Rated dc link voltage. |
| $I_{\mathrm{rated}}$ | System rated current. |
| $P_{\mathrm{rated}}$ | Rated system power of the VSC-HVDC power transmission system. |
| $I_{C\mathrm{sm,charge}}$ | Charging current of the SM capacitors. |
| $I_{C\mathrm{sm,discharge}}$ | Discharging current of the SM capacitors. |
| $C_{\mathrm{line}}$ | Parasitic capacitance of the dc cable. |
| $R_{\mathrm{line}}$ | Parasitic inductance of the dc cable. |

Received 25 March 2025; revised 3 June 2025 and 21 July 2025; accepted 28 August 2025. Date of publication 3 September 2025; date of current version 22 October 2025. This work was supported in part by the Smart Grid National Science and Technology Major Project under Grant 2025ZD0805300, in part by the Project supported by the Shanghai Foundation for Development of Science and Technology under Grant 25DZ3003300, and in part by the Shanghai Pujiang Program under Grant 23PJ1404000. Recommended for publication by Associate Editor A. Davoudi. *(Corresponding authors: Jianwen Zhang; Jiajie Zang.)*

Yunqi Jing, Jianwen Zhang, Liqian Su, Gang Shi, Jianqiao Zhou, and Xu Cai are with the Key Laboratory of Control of Power Transmission and Conversion of Ministry of Education, School of Electrical Engineering, Shanghai Jiao Tong University, Shanghai 200240, China (e-mail: jingyunqi2020@sjtu.edu.cn; icebergzjw@sjtu.edu.cn; liqiansu@sjtu.edu.cn; gangshi@sjtu.edu.cn; jianqiaozhou@sjtu.edu.cn; xucai@sjtu.edu.cn).

Jiajie Zang is with the School of Electronic and Electrical Engineering, Shanghai University of Engineering Science, Shanghai 201620, China (e-mail: jiajie_zang@sues.edu.cn).

Wei Bao is with State Grid Shanghai Municipal Electric Power Company, Shanghai 200122, China (e-mail: baow@sh.sgcc.com.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3605896.

Digital Object Identifier 10.1109/TPEL.2025.3605896

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|---|---|
| $L_{\mathrm{dc}}$ | Smoothing reactor. |
| $L_{\mathrm{SEC}}$ | Equivalent inductance of SEC. |
| $C_{\mathrm{SEC}}$ | Equivalent capacitance of SEC. |
| $R_{\mathrm{SEC}}$ | Equivalent resistance of SEC. |
| $L_{\mathrm{REC}}$ | Equivalent inductance of REC. |
| $C_{\mathrm{REC}}$ | Equivalent capacitance of REC. |
| $R_{\mathrm{REC}}$ | Equivalent resistance of REC. |
| $P_{\mathrm{dcc}}$ | Power consumed by DCC. |
| $P_R$ | Power consumed by lumped resistor. |
| $P_{\mathrm{valve}}$ | Power consumed by cell resistor. |
| $C_{eq}$ | System equivalent capacitance between the dc link. |
| $N_T$ | Number of groups where SMs act together. |
| $T_s$ | Energy dissipation valve operation period. |
| $i_{\mathrm{chop}}$ | Chopper branch current. |
| $d$ | Duty cycle of the valve control signal. |
| PWM | Energy dissipation valve control signal. |
| $k$ | Surplus power coefficient. |
| $U_{\mathrm{ac}}$ | AC side voltage of the REC. |
| $I_{\mathrm{ac}}$ | Three-phase ac side current of the REC. |
| $I_{\mathrm{dc}}$ | DC current that flows into the HVDC system through SEC. |

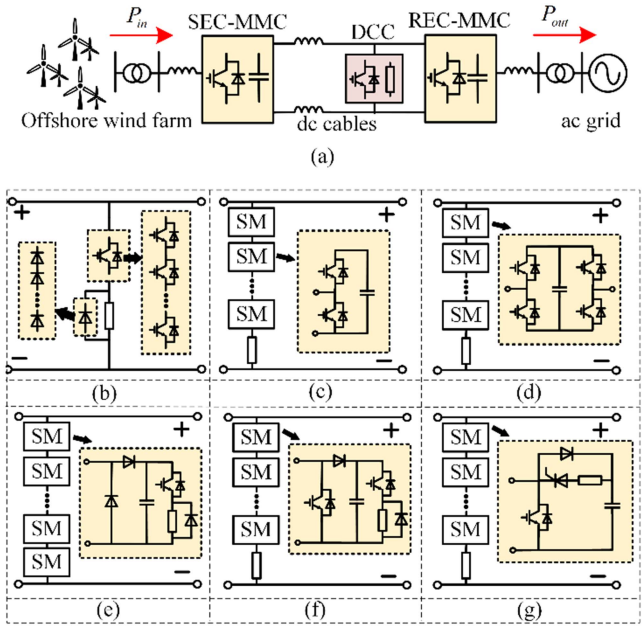


Fig. 1. Configuration of the offshore wind VSC-HVDC system and typical DCC topologies. (b) Series-connected IGBT valve. (c) Half-bridge submodule based DCC. (d) Full-bridge submodule based DCC. (e) Distributed DCC. (f) Hybrid DCC based on IGBT [11]. (g) Hybrid.

## I. Introduction

OFFSHORE wind power is widely recognized as a prospective solution to address the energy shortage caused by the depletion of traditional fossil fuels [1], [2]. For underground submarine cables, at a breakeven distance of 40/50 km, dc power transmission becomes more cost-effective than ac [3]. Consequently, VSC-HVDC has become a widely adopted technology for connecting deep-sea offshore wind farms to the onshore utility grids [4], [5]. Fig. 1(a) illustrates the configuration of an offshore wind a VSC-HVDC system for offshore wind power transmission, consisting of the wind farm, the SEC, the REC, and submarine dc cables [6], [7].

In the VSC-HVDC system, the safe operation of the devices must be ensured to meet the requirements of grid integration. During the operation of the offshore wind power transmission system, onshore ac network faults may occur at the ac side of the REC [8], resulting in an immediate reduction in the power transmission capability of the REC to the grid [3]. However, during the fault, the wind farm continues the power transmission through the SEC and the HVDC system. The surplus energy will cause a surge in the dc link voltage, posing serious risks to the system [3], [9]. As a result, the FRT capability of the VSC-HVDC system remains one of the major challenges in offshore wind power transmission.

Many solutions have been proposed to prevent overvoltage on the dc link and to achieve FRT in offshore wind power transmission systems. The existing approaches can generally be divided into two major types: applying control strategies to rapidly reduce the power generation from wind farms, or introducing dedicated circuits such as choppers to dissipate the excess energy during fault [10]. Among these, DCC are widely used in VSC-HVDC systems, since they offer a robust and quick response to the fault and can achieve reliable FRT without influencing the operation of the wind farm, allowing the transmission to be fully restored once the fault is cleared [11].

Existing DCC topologies can be classified into three main types in terms of the energy consumption resistor implementation positions: centralized, distributed, and hybrid [7]. Three typical centralized DCCs topologies are displayed in Fig. 1(b)–(d). In centralized DCCs, the surplus energy is dissipated by a lumped resistor, typically placed outside the valve hall and cooled by air. By controlling the voltage over the lumped resistor, centralized DCCs can achieve precise energy dissipation. Fig. 1(b) shows a classic topology proposed by ABB [12], featuring series-connected IGBTs controlled by pulsewidth modulation (PWM). This topology has the advantage of low cost and was applied in BorWin1 project. However, the dynamic voltage sharing of the series-connected IGBTs still hinders the device's practical application [10]. Additionally, since all IGBTs switch simultaneously, the equipment exhibits high d$v$/d$t$ and d$i$/d$t$, leading to poor EMI performance. Modular designs such as the topologies based on HBSM and FBSM shown in Fig. 1(c) and (d) have been adopted by DolWin3 project in Germany [13] and the Rudong offshore wind project in China [14], [15]. The modular structure effectively mitigates the d$v$/d$t$ and d$i$/d$t$ of the chopper [7]. Nevertheless, to maintain zero net change in the SM capacitor voltages, additional semiconductors are required, which increases the cost of the equipment [10], [16].

The distributed DCC shown in Fig. 1(e) features power dissipation resistors distributed in each SM [3], [17]. In this configuration, the SMs function as independent power units. The chopper controls the energy consumed by adjusting the number of SMs involved in power dissipation. This approach allows for smooth power dissipation adjustments. Moreover, the capacitor voltage balancing is achieved through the distributed resistors

instead of using additional SMs, which eliminates the need for extra semiconductors [10]. However, the distributed resistors integrated into SMs are placed inside the valve hall, requiring additional expensive water-cooling system and increasing the system's volume.

Hybrid DCCs offer a balance between the advantages and disadvantages of centralized and distributed DCCs. These topologies combine a lumped resistor connected in the main chopper branch with distributed resistors integrated in each SM. Fig. 1(f) [12] and Fig. 1(g) [18] display two typical hybrid DCC topologies proposed in recent studies. The modular design effectively reduces d$v$/d$t$ and d$i$/d$t$, and provides greater control flexibility [14]. The lumped resistor reduces the heat generated by the SMs inside the valve hall compared to the distributed topologies. This design makes the hybrid DCC more competitive than the other solutions to ride through the offshore wind VSC-HVDC system's fault conditions.

Notably, the existing hybrid DCC topologies still rely on a large number of pricy fully-controlled semiconductors, hindering their practical applications. To save the system's cost, a novel low-cost hybrid DCC, the TDS-DCC, is proposed in this article along with the corresponding control strategies. The TDS-DCC adopts a composite design by sharing the switches, therefore reducing the total number of semiconductors. Also, the SM design of the TDS-DCC replaces half of the fully-controlled devices with thyristors, further decreasing the initial investment of the chopper.

Nevertheless, the adopted semicontrolled devices need forced commutation. Also, the composite module design necessitates coordinated actions of the semiconductors in the SM. These factors pose challenges to the modulation of SMs and the overall control of the DCC. To overcome the challenges, a specific modulation scheme for the TDS-DCC-SM is proposed to achieve the forced commutation of the thyristors, which ensures the reliable operation of the SMs while maintaining the good performance typical of hybrid DCCs.

The rest of this article is organized as follows. Section II introduces the topology and basic operation principle of the TDS-DCC. In Section III, the modulation scheme for the chopper SMs is illustrated. Section IV presents the control strategies for the proposed topology. In Section V, a ±400 kV/1100 MW simulation model is established to verify the proposed topology and the corresponding control schemes. Additionally, the cost of the TDS-DCC is compared with those of a few existing DCC topologies in terms of semiconductor costs. Experimental results of a scaled-down prototype are presented in Section VI. Finally, Section VII concludes this article.

## II. Topology and Operation Principle of TDS-DCC

### A. Topology of the Proposed TDS-DCC

The proposed TDS-DCC branch is shown in Fig. 2, consisting of an energy dissipation valve, a lumped power dissipation resistor $R$, and a chopper inductor $L_{\rm dcc}$. This configuration helps mitigate voltage spikes induced on the dc link during chopper operation. The output voltage of the energy dissipation valve is denoted as $U_{\rm valve}$, and the dc link voltage is referred to as

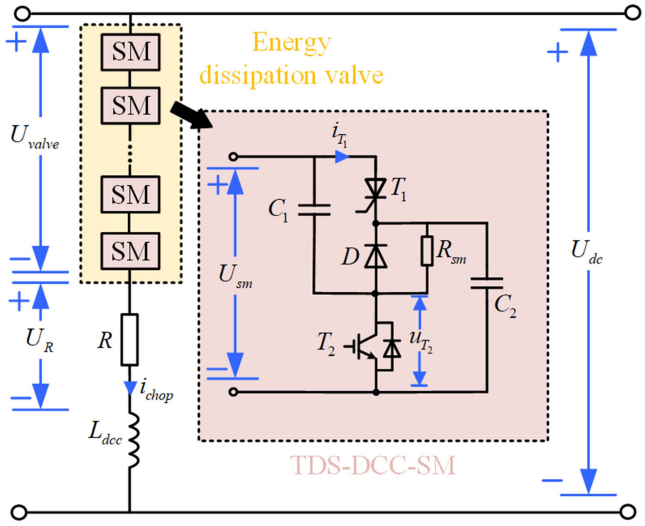


Fig. 2. Topology of proposed TDS-DCC.

$U_{\rm dc}$. The energy dissipation valve is composed of hundreds of cascaded TDS-DCC-SMs, each containing a thyristor, an IGBT with its anti-parallel diode, a diode, two storage SM capacitors, and a distributed cell resistor.

In each SM, the thyristor ($T_1$), IGBT ($T_2$), and the cell resistor ($R_{\rm sm}$) are series-connected. The switching of $T_1$ and $T_2$ controls the energy dissipated across $R_{\rm sm}$ and regulates the power stored in the SM capacitors $C_1$ and $C_2$. The freewheeling diode ($D$) is reversely placed between $T_1$ and $T_2$ in parallel with $R_{\rm sm}$, allowing the capacitors to charge from the dc link when the switches are turned OFF. Ideally, the capacitances of $C_1$ and $C_2$ are identical, i.e., $C_1 = C_2 = C_{\rm sm}$. Assuming that the capacitor voltages are well maintained around their rated value: $U_{C1} = U_{C2} = U_{CN}$, the TDS-DCC-SM will then have two output voltage levels, $U_{CN}$ and $2U_{CN}$, depending on its switching modes. In a TDS-DCC-SM, the capacitor voltages of $C_1$ and $C_2$ are regulated via $T_1$ and $T_2$, respectively.

The TDS-DCC-SM topology significantly reduces the cost of the chopper, since it requires fewer semiconductors owing to the composite module design. Compared to the SM topologies shown in Fig. 1(c), (f), and (g), the proposed topology saves 1/4 of the total switch count, where each SM can sustain twice of the voltage than the other modular counterparts by series-connecting the capacitors. As a result, the number of the SMs is halved. Additionally, the proposed topology further reduces the cost of the chopper by replacing half of the IGBTs with thyristors, which are more cost-effective than IGBTs at equivalent voltage and current ratings [19].

### B. Operation Principle of Energy Dissipation Valve

When an ac network fault takes place, the dc link voltage of the VSC-HVDC system increases rapidly due to the surplus energy generated by the offshore wind farm. To prevent equipment damage from the overvoltage issue, the TDS-DCC starts operation when $U_{\rm dc}$ reaches a predetermined threshold, for instance, 1.05 p.u. [3], [21]. During the FRT, the dc chopper dissipates the surplus energy in accordance with the reduction

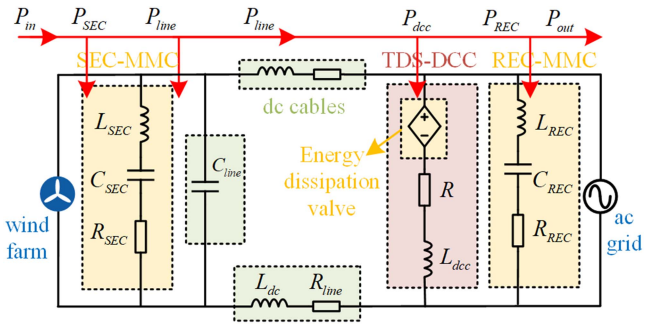


Fig. 3. Simplified model of an offshore VSC-HVDC system with a hybrid DCC installed and the power flow of the system during FRT.

of the REC output power capability to balance the power of the system.

An offshore VSC-HVDC system with a hybrid dc chopper installed at the dc side of the REC can be simplified into the equivalent circuit shown in Fig. 3. In this model, the REC and SEC are represented by two series *RLC* branches, based on the MMC dc side equivalent impedance modeling [22], [23]. During the FRT process, the energy dissipation valve of the dc chopper can be approximated as a controllable voltage source with two output voltage levels, $U_{\mathrm{dc}N}$ and $0.5U_{\mathrm{dc}N}$, by controlling the switching of the cascaded SMs. The valve is series-connected to the lumped resistor ($R$) and chopper inductor ($L_{\mathrm{dcc}}$). $C_{\mathrm{line}}$ and $R_{\mathrm{line}}$ represent parasitic parameters of the cable, and $L_{\mathrm{dc}}$ is the smoothing reactor on the dc cable.

During the FRT scenario, the power flow of the system is also shown in Fig. 3 [18], where $P_{\mathrm{in}}$ is the input power of the wind farm, and $P_{\mathrm{out}}$ is the ac power delivered to the onshore power grid. $P_{\mathrm{dcc}}$ is the power consumed by the hybrid DCC, which consists of two components: 1) the power consumed by the lumped resistor ($P_R$) and 2) the power dissipated by the distributed resistors integrated into SMs of the energy dissipation valve ($P_{\mathrm{valve}}$). Ignoring the losses and power absorbed by the MMCs, the relationship between the above quantities can be summarized as follows:

$$\begin{cases} P_{\mathrm{dcc}} + P_{C_{eq}} = P_{\mathrm{in}} - P_{\mathrm{out}} \\ P_{\mathrm{dcc}} = P_R + P_{\mathrm{valve}} \end{cases} \tag{1}$$

where $P_{Ceq}$ is the charging power of the system equivalent capacitance between the dc link ($C_{eq}$). This capacitance includes SM capacitors of the MMCs.

The TDS-DCC energy dissipation valve has two operating states. Through the coordinated switching of the cascaded SMs, the energy dissipation valve can shift these states flexibly.

*1) Blocked State:* The chopper does not affect the normal operation of the VSC-HVDC system. The output voltage of the energy dissipation valve $U_{\mathrm{valve}}$ equals the rated dc link voltage: $U_{\mathrm{valve}} = U_{\mathrm{dc}N}$. In all TDS-DCC-SMs, the thyristors and IGBTs remain blocked, and all capacitors are connected in series and charged to the rated capacitor voltage $U_{CN}$ by the dc link voltage, which can be expressed as follows:

$$U_{CN} = \frac{U_{\mathrm{dc}N}}{2N} \tag{2}$$

where $N$ is the number of SMs in the energy dissipation valve of the TDS-DCC.

*2) Power Dissipation State:* When the dc link voltage reaches the predetermined threshold, the TDS-DCC is activated and dissipates the rated active power of the HVDC power transmission system. According to (1), the powers consumed by the lumped resistor and the valve should obey the following criterion:

$$P_R + P_{\mathrm{valve}} = P_{\mathrm{rated}}. \tag{3}$$

In this state, all switches are turned ON, and all capacitors in SMs are bypassed. The chopper branch current $i_{chop}$ flows through the cell resistors and the lumped resistor, dissipating rated power of the system. The resistances of cell resistor $R_{\mathrm{sm}}$ and the lumped resistor $R$ are chosen so that the energy dissipation valve and the lumped resistor each consume half of the system rated power [7]

$$i^2{}_{chop}R = i^2{}_{chop}NR_{\mathrm{sm}} = 0.5P_{\mathrm{rated}}. \tag{4}$$

In this case, when the dc link voltage is well maintained around its rated value $U_{\mathrm{dc}N}$, $U_{\mathrm{valve}}$, and $U_R$ satisfy

$$U_{\mathrm{valve}} = U_R = 0.5U_{\mathrm{dc}N}. \tag{5}$$

Consequently, the resistances of the lumped resistor ($R$) and cell resistors ($R_{\mathrm{sm}}$) can be determined by the following equation:

$$R = NR_{\mathrm{sm}} = \frac{\left(\frac{1}{2}U_{\mathrm{dc}N}\right)^2}{P_{\mathrm{rated}}} \tag{6}$$

and the current that flows through the TDS-DCC branch in this mode can, thus, be obtained

$$i_{chop} = \frac{U_R}{R} = \frac{0.5U_{\mathrm{dc}N}}{R} = I_{\mathrm{rated}}. \tag{7}$$

In practical engineering, scenarios like a 20% reduction in the lumped resistor's value is possible. Under this circumstance, the TDS-DCC is still able to maintain the dc link voltage within a reasonable range. However, for the consistency with the existing publications, in this article, the resistance of the lumped resistor ($R$) is still determined for rated power consumption, as is shown in (6).

## III. Modulation Scheme of the TDS-DCC-SM

To achieve the switching between the *Blocked state* and the *Power dissipation state* of the energy dissipation valve, the TDS-DCC-SM output voltage $U_{\mathrm{sm}}$ should be able to switch between two levels: $U_{CN}$ and $2U_{CN}$. However, since thyristors do not have self-commutation capability, an SM modulation scheme for the proposed chopper is proposed to achieve forced commutation of the thyristors.

### A. Mode Analysis of the TDS-DCC-SM

In a TDS-DCC-SM, the capacitor voltage of $C_1$ is regulated via $T_1$, while the voltage of $C_2$ is controlled through the switching of $T_2$. A single TDS-DCC-SM has four switching modes: *OUT mode*, *transition mode A*, *IN mode*, and *transition mode B*, as is illustrated in Fig. 4(a)–(d). The current path is highlighted in

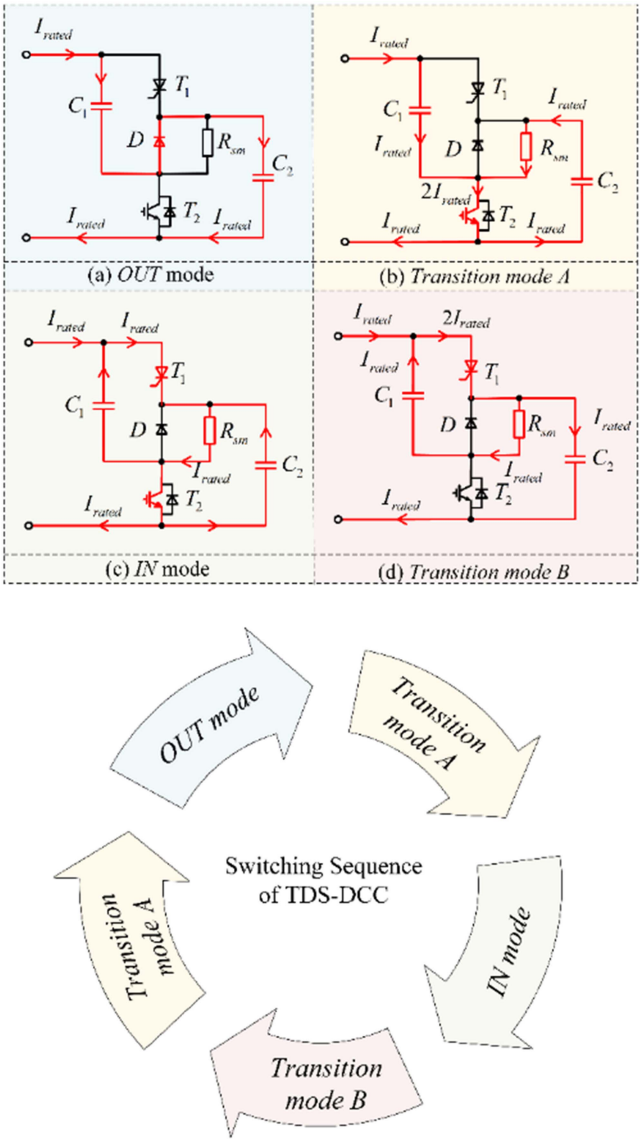


Fig. 4. Mode analysis of the TDS-DCC. (a) OUT mode of the TDS-DCC SM. (b) Transition mode A. (c) IN mode. (d) Transition mode B. (e) Switching sequence of a TDS-DCC-SM in a period during FRT process.

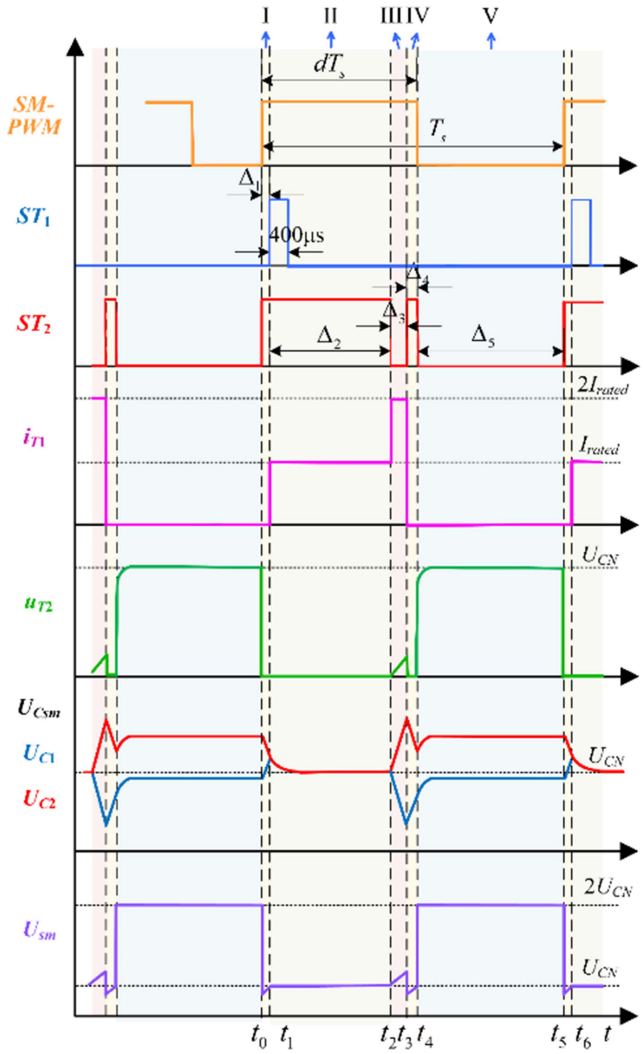


Fig. 5. Switching sequence of a TDS-DCC-SM in a period during FRT process.

red. The two transition modes are introduced to assist the forced commutation of the thyristor and enable the periodic switching of the SM output voltage between two levels. The sequence of switching modes of a TDS-DCC-SM over a valve control period during the FRT process is shown in Fig. 5. SM-PWM is the mode control signal for the single SM, whose duty cycle is $d$, while $ST_1$ and $ST_2$ are the control signals of the switches. During the operation of the chopper, $U_{C2}$ is kept greater than $U_{C1}$ via control strategies to generate a reverse bias across the thyristor for forced commutation. The switching process of a TDS-DCC-SM in a period can be divided into five subintervals.

*1) Interval I ($t_0$~$t_1$):* Before $t_0$, the SM stays in the *OUT mode*, as is shown in Fig. 4(a). Both $T_1$ and $T_2$ are OFF, and no current flows through the cell resistor $R_{\rm sm}$. $C_1$ and $C_2$ are series-connected through $D$ and are charged from the dc link. The output voltage of the SM ($U_{\rm sm}$) is $2U_{CN}$, the sum of the capacitor voltages of $C_1$ and $C_2$. At $t_0$, the *SM-PWM* changes from low to high. $T_2$ turns ON, and the SM enters *transition mode A* shown in Fig. 4(b), where $U_{C2} > U_{C1}$. During this interval, the chopper branch current $i_{chop}$ flows through $T_2$ to charge $C_1$, causing $U_{C1}$ to rise, while $C_2$ is discharged from $R_{\rm sm}$ in the module, and $U_{C2}$ decreases. The IGBT current $i_{T2}$ includes both the chopper current and the discharging current of $C_2$, which is about $2I_{\rm rated}$. In this mode, the output voltage of the SM ($U_{\rm sm}$) in this mode is equal to $U_{C1}$. During this interval, the difference between $U_{C2}$ and $U_{C1}$ ($U_{C2}$–$U_{C1}$) keeps decreasing until $t_1$, when $U_{C2}$ becomes equal to $U_{C1}$, and the thyristor becomes forward biased.

*2) Interval II ($t_1$~$t_2$):* At $t_1$, $ST_1$ is set to high level, turning on the thyristor. The SM enters the *IN mode*, where both $T_1$ and $T_2$ conduct, connecting $C_1$ and $C_2$ in parallel, which automatically balances the capacitor voltages. As can be seen from Fig. 5, in Interval II, the SM output voltage ($U_{\rm sm}$) is $U_{CN}$, which is also the voltage across $R_{\rm sm}$. $i_{chop}$ flows through $T_1$, $R_{\rm sm}$ and $T_2$ ($i_{T1}$

$= i_{chop} = I_{\text{rated}}$), and the SM participates in power dissipation. The equivalent circuit of the SM during this interval is shown in Fig. 4(c).

*3) Interval III ($t_2$∼$t_3$):* At $t_2$, $T_2$ turns OFF, and the SM enters the *Transition mode B*. At this point, the negative terminals of $C_1$ and $C_2$ are no longer at the same potential. The thyristor remains on and is unable to turn OFF independently. $C_2$ continues to be charged by $i_{chop}$, and $C_1$ is discharged from $T_1$ and $R_{\text{sm}}$, causing $U_{C2}$ to gradually exceed $U_{C1}$. The thyristor current $i_{T1}$ includes both the chopper current and the discharging current of $C_1$, which is about $2I_{\text{rated}}$. The output voltage of the module equals $U_{C2}$. The equivalent circuit of this stage is shown in Fig. 4(d).

*4) Interval IV ($t_3$∼$t_4$):* In this interval, the forced commutation of the thyristor is achieved. At $t_3$, $T_2$ turns ON again, and the SM enters the *transition mode A*. The negative terminals of the $C_1$ and $C_2$ restore equipotential condition via the IGBT. At this moment, the SM enters *transition mode A* again, and the voltage between the anode and the cathode of the thyristor, $V_{AK}$, equals $U_{C1}$–$U_{C2}$. $T_1$ is, thus, reverse biased. The thyristor commutation path goes through $C_1$ and $R_{\text{sm}}$, as is shown in Fig. 4(b). $i_{T1}$ drops to zero, and the forced commutation is achieved. In this mode, $i_{chop}$ flows through the IGBT to charge $C_1$, while $C_2$ is discharged by $R_{\text{sm}}$. The output voltage of the module equals $U_{C1}$.

*5) Interval V ($t_4$∼$t_5$):* At $t_4$, $T_2$ turns OFF again, and the SM finally enters the *OUT mode*, where $U_{C2}$ remains higher than $U_{C1}$, and the SM outputs $2U_{CN}$. The switching process is then repeated until the fault is cleared and the TDS-DCC is no longer in operation.

From the abovementioned analysis, it can be observed that in *IN mode* and the two transition modes, the TDS-DCC-SM outputs $U_{CN}$ and participates in energy dissipation. Therefore, these three modes can be grouped as the energy consumption modes. In *OUT mode*, on the other hand, the SM outputs $2U_{CN}$, and no energy is dissipated by $R_{\text{sm}}$. When all SMs of the chopper switch together between the *OUT mode* and the energy consumption modes, according to (2), the energy dissipation valve will consequently transition between the *Blocked state* and the *Power dissipation state* introduced in Section II.

### B. Timing Constraints of the SM Switching Process

The duration of each interval needs to be carefully designed to achieve the forced commutation of $T_1$. The time durations of interval I to V explained in the previous part are defined as $\Delta_1$ to $\Delta_5$. It can be observed that the thyristor forced commutation is realized in interval IV, when $T_1$ needs to be reverse biased for a duration $t_Q$ longer than the turn-OFF time $t_q$ of the thyristor [20]. However, in interval IV when the SM is in *transition mode A*, the absolute value of the thyristor voltage $V_{AK} = U_{C1}$–$U_{C2}$ gradually decreases due to the charging and discharging of the SM capacitors, as is shown in Fig. 4(b). To prevent $T_1$ from being forward biased before it commutates successfully, the duration of interval III ($\Delta_3$) should be sufficiently long to ensure that the reverse bias applied across $T_1$ ($U_{C2}$–$U_{C1}$) is adequately large when the SM enters *transition mode A*.

To establish the quantitative relationships between the voltage across $T_1$ and the durations of the intervals, the charging and discharging currents of the SM capacitors in each mode are calculated to determine the voltage variations of the SM capacitors.

When the dc link voltage is kept around $U_{\text{dc}N}$, and the capacitor voltages in all SMs stay around $U_{CN}$, in the transition modes, the SM output voltages will stabilize at $U_{CN}$, causing the valve to stay in the *Power dissipation state* and output a voltage of $0.5U_{\text{dc}N}$, as is shown in (5). In each SM, the SM capacitor charging current is the chopper branch current, while the capacitor discharging current is influenced by $R_{\text{sm}}$. According to (6), (7) and the analysis in Section II, the charging and discharging current of the capacitors can be expressed as follows:

$$\begin{cases} I_{C_{\text{sm,charge}}} = \frac{U_{\text{dc}} - U_{\text{valve}}}{R} = \frac{0.5U_{\text{dc}N}}{R} = I_{\text{rated}} \\ I_{C_{\text{sm,discharge}}} \approx \frac{U_{CN}}{R_{\text{sm}}} = I_{\text{rated}}. \end{cases} \tag{8}$$

From (8), it is known that the charging and discharging speeds of the two SM capacitors in both transition modes are almost identical, as is expressed in the following equation:

$$\frac{dU_{C_{\text{sm}}}}{dt} = \frac{I_{\text{rated}}}{C_{\text{sm}}}. \tag{9}$$

To ensure the thyristor remains reverse biased at $t_4$, the following equation should be satisfied:

$$U_{C_2}|_{t=t_4} - U_{C_1}|_{t=t_4} = 2\frac{I_{\text{rated}}}{C_{\text{sm}}}(\Delta_3 - \Delta_4). \tag{10}$$

In Interval V in Fig. 5, $U_{C2} - U_{C1}$ is stable because the SM capacitors are series-connected and charged together. As a result, $U_{C2}|_{t=t5}$–$U_{C1}|_{t=t5} = U_{C2}|_{t=t4}$–$U_{C1}|_{t=t4}$ in (10). To ensure that the thyristor is effectively turned ON in the next cycle at $t_6$ in Fig. 5, $T_1$ is supposed to be forwardly biased when the gate trigger pulse of the thyristor ($ST_1$) is given ($U_{C1}|_{t=t6}$–$U_{C2}|_{t=t6} \geq 0$). $\Delta_1$ is, thus, required to meet the following equation:

$$\begin{aligned} &U_{C_2}|_{t=t_6} - U_{C_1}|_{t=t_6} \\ &= \left(U_{C_2}|_{t=t_5} - \Delta_1 \times \frac{dU_{C_2}}{dt}\right) - \left(U_{C_1}|_{t=t_5} + \Delta_1 \times \frac{dU_{C_1}}{dt}\right) \\ &= 2\frac{I_{\text{rated}}}{C_{\text{sm}}}(\Delta_3 - \Delta_4 - \Delta_1) \leq 0. \end{aligned} \tag{11}$$

As a result, the relationships between the interval time durations can be summarized as follows:

$$\begin{cases} \Delta_4 > t_q \\ \Delta_3 > \Delta_4 \\ \Delta_1 + \Delta_4 \geq \Delta_3. \end{cases} \tag{12}$$

Let $\Delta_1 + \Delta_4 = \Delta_3$. The time durations of the five intervals are then determined as follows:

$$\begin{cases} \Delta_1 = \lambda \\ \Delta_2 = dT_s - \Delta_1 - \Delta_3 - \Delta_4 \\ \Delta_3 = t_Q + \lambda \\ \Delta_4 = t_Q \\ \Delta_5 = (1-d)T_s \end{cases} \tag{13}$$

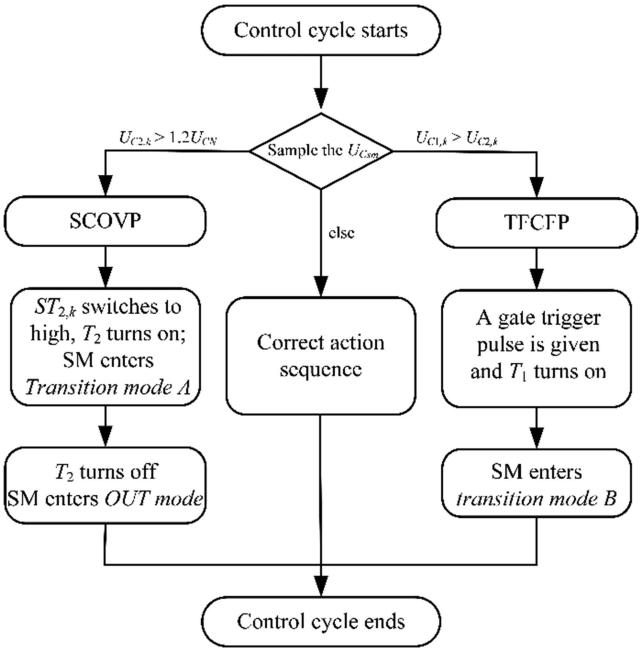


Fig. 6. Thyristor turn-OFF failure prevention strategies of TDS-DCC.

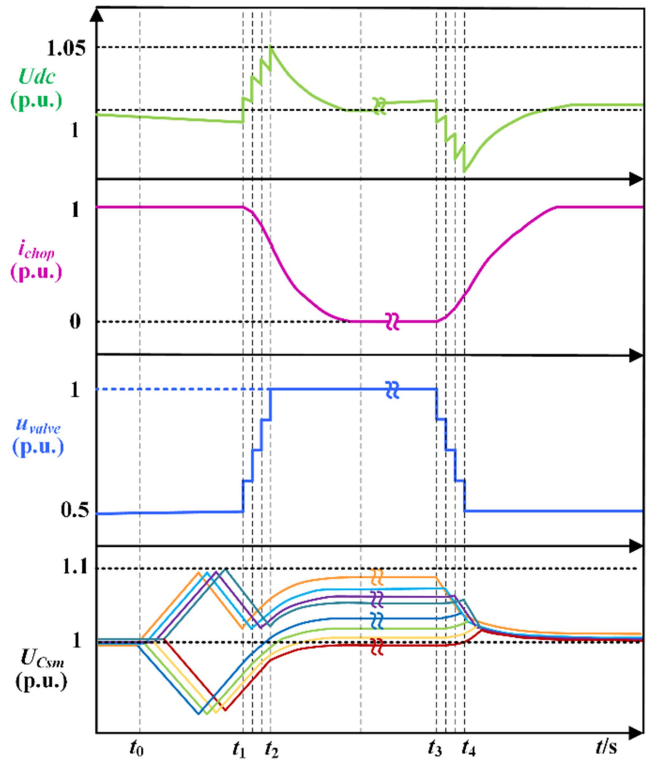


Fig. 7. Waveforms of TDS-DCC in a complete valve operation period.

where $t_Q = pt_q$, with $p$ being a constant greater than 1. $\lambda$ is a constant that influences the ripple of the SM capacitors.

The reverse recovery problem of the thyristors in the TDS-DCC has also been considered, and a thyristor forced commutation failure prevention (TFCFP) strategy along with a SM capacitor over voltage protection (SCOVP) strategy have been adopted to prevent possible thyristor shutdown failure due to insufficient commutation time. In the TDS-DCC-SM, when the thyristor is ON, turning OFF the IGBT will cause the SM to enter the *Transition mode B* shown in Fig. 4(d), where $U_{C2}$ rises and $U_{C1}$ drops. When $U_{C2} > U_{C1}$, turning ON the IGBT will reverse bias the thyristor and assists the forced commutation of $T_1$. As a result, proper switching of $T_1$ and $T_2$ can solve the possible issue of thyristor shutdown failure caused by insufficient commutation time and achieve forced commutation. The TFCFP strategy is to turn ON the thyristor when $U_{C2} < U_{C1}$ to ensure $U_{C2} \geq U_{C1}$ during the operation of the device, while the SCOVP strategy is to turn ON the IGBT when $U_{C2}$ exceeds the preset limit to prevent the over voltage of $C_2$. The flow chart of the strategies is shown in Fig. 6.

Since the action time of the thyristors are significantly shorter than the overall operational period of the energy dissipation valve, the impact of the transition modes on the valve operation can be considered negligible. Consequently, by altering the modes of the cascaded SMs, the energy dissipation valve as a whole can transition between its two operating states and regulate the dissipated power flexibly.

## IV. Control Strategies of the Proposed TDS-DCC

### A. Stepwise Power Dissipation Control

When the dc link voltage reaches the predetermined threshold (1.05 p.u.) [21], the TDS-DCC begins power dissipation. During FRT, PWM is employed to control the energy dissipation valve and regulate the amount of energy dissipated. However, applying full dc link voltage across the lumped resistor in the form of square pulses results in poor EMI performance. To reduce d$v$/d$t$ and d$i$/d$t$, a periodic trapezoidal pulse is generated as the output voltage waveform of the energy dissipation valve [3], [14]. The cascaded SMs are divided into $N_T$ groups, switching between *IN* and *OUT mode*s in separate groups rather than simultaneously. Fig. 7 shows the current and voltage waveforms of TDS-DCC over one complete valve operation period, denoted as $T_s$. In this case, $N_T$ is set to be 4 for a clearer presentation. As is shown in this figure, $U_{\text{valve}}$ is $0.5U_{\text{dc}N}$ at $t_1$, and is ramped up until it reaches $U_{\text{dc}N}$ at $t_2$ and remains constant until $t_3$. From $t_3$ to $t_4$, it is ramped down again back to $0.5U_{\text{dc}N}$. The interval $t_1 \sim t_2$ is referred to as the disengage transition stage of the energy dissipation valve, while the interval $t_3 \sim t_4$ is called the engage transition stage of the energy dissipation valve. The duration of each step in the transition stages is preset with $\delta$.

A voltage closed-loop control is employed to match the power dissipation demand and maintain the dc link voltage around its rated value, as is shown in Fig. 8 [3]. $U_{\text{dc}}$ is compared with the voltage reference of $U_{\text{dc}N}$ to generate the error signal as the input of the proportional-integral controller. The output $d$ is then passed through the modulation to generate the PWM signals that are then transferred to the sorting algorithm block for the switches [3]. $d$ represents the duty cycle of the valve control signal PWM that governs the switching of the energy dissipation valve between its two states.

The amount of power that needs to be dissipated by the chopper is defined as $kP_{\text{rated}}$ [12]. During FRT, $d$ is adjusted

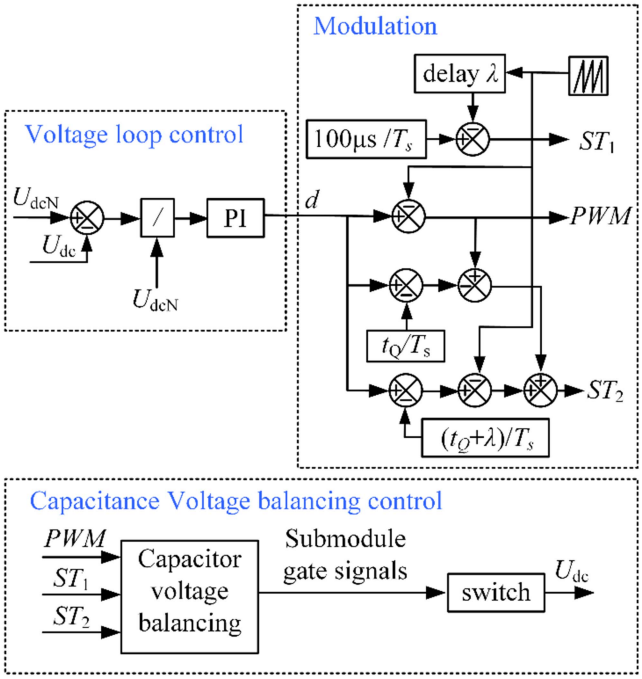


Fig. 8. Control strategies of TDS-DCC.

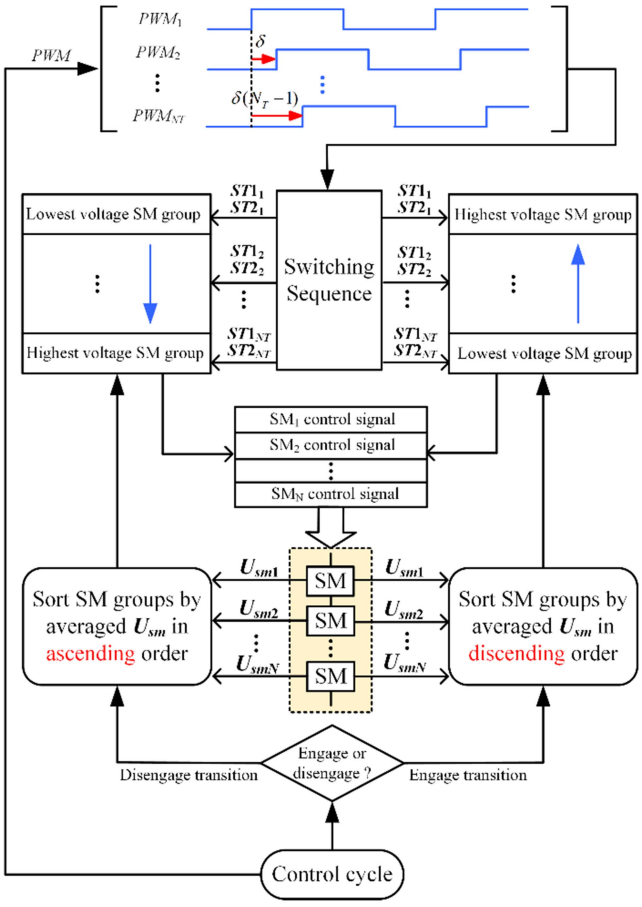


Fig. 9. Sorting algorithm of capacitor voltage balancing control process.

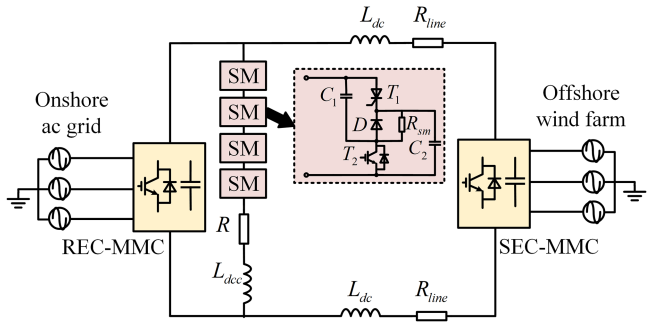


Fig. 10. Configuration of the simulation model in MATLAB/Simulink.

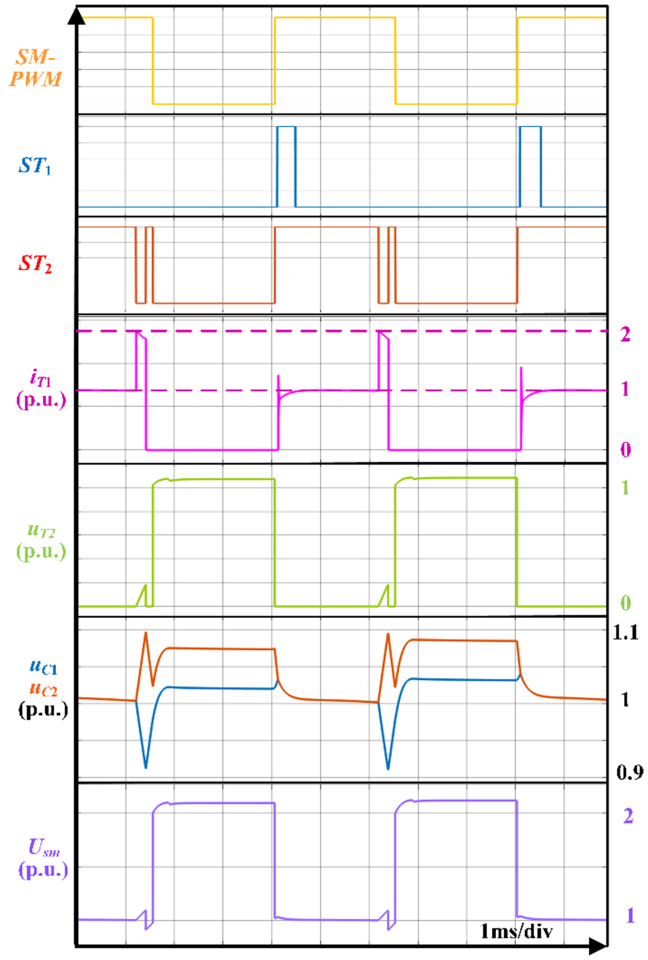


Fig. 11. Voltage and current variations of the switches and capacitors in a TDS-DCC-SM.

in proportion to $k$ to keep the dc link voltage within a tolerable range. After the ac fault is cleared, the energy dissipation valve will return to the *Blocked state*, and the TDS-DCC exits operation.

### *B. SM Capacitor Voltage Balancing Based on Sorting Algorithm*

Because of the stepwise power dissipation control, during the transition stages of the valve, part of the SMs have already entered energy consumption modes and output $U_{CN}$, while the

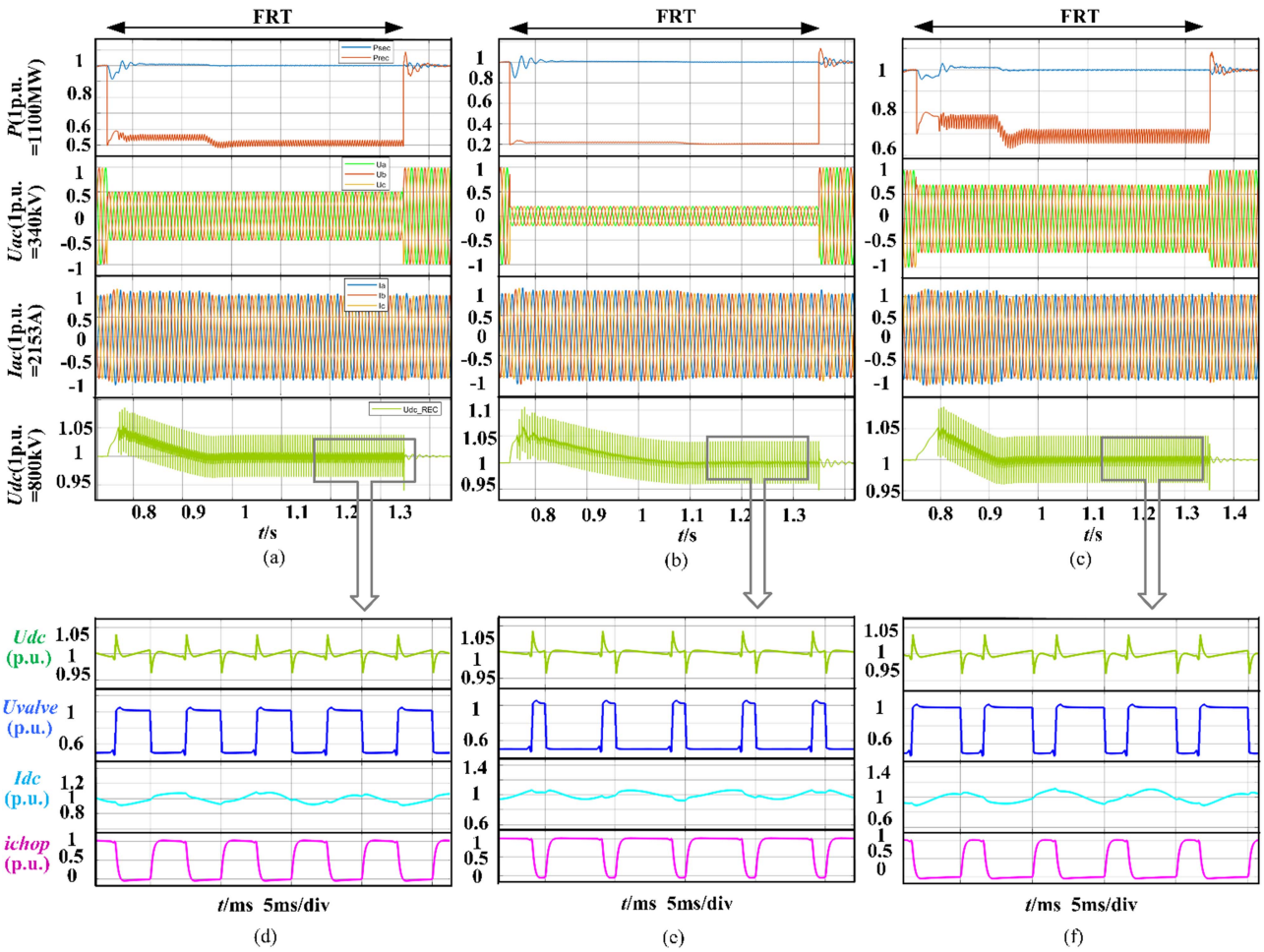


Fig. 12. Simulation results of TDS-DCC. (a) $k = 0.5$. (b) $k = 0.8$. (c) $k = 0.3$. (d) Detailed voltage and current waveforms of the chopper branch when $k = 0.5$. (e) Detailed voltage and current waveforms of the chopper branch when $k = 0.8$. (f) Detailed voltage and current waveforms of the chopper branch when $k = 0.3$.

other SMs are still blocked and output $2U_{CN}$. As a result, $U_{\text{valve}} < U_{\text{dc}}$, and current flows through the chopper branch. This chopper branch current can be estimated by the following expression:

$$i_{chop} = \frac{U_{\text{dc}} - U_{\text{valve}}}{R} \approx \frac{m}{N_T} \times \frac{NU_{CN}}{R} = \frac{mI_{\text{rated}}}{N_T} \tag{14}$$

where $m$ ($0 < m < N_T$) represents the number of groups in which the SMs have already entered the *OUT mode*s, and the number of groups where the SMs output $U_{CN}$ is ($N_T$–$m$).

According to the mode analysis in Section III, during the transition stages of the valve, the capacitors of the SMs in *OUT mode* will be charged by the branch current. In this case, different action sequences of the SM groups in stepwise control will result in unbalanced capacitor voltages across the SMs in different groups. During the disengage transition stage from $t_1$ to $t_2$, as is shown in Fig. 7, the voltage increment of a capacitor in an SM in the $i$th ($1 \le i \le N_T$) group that enters the *OUT mode* can be calculated as

$$\Delta U_{C_{\text{sm}},i} = \delta \sum_{m=N_T-i}^{1} \frac{i_{chop}}{C_{\text{sm}}}$$

$$= \frac{\delta I_{\text{rated}}}{2N_T C_{\text{sm}}}(i^2 - (2N_T + 1)i + N_T^2 + N_T) \tag{15}$$

where $C_{\text{sm}}$ is the capacitance of the SM capacitors. From (15), the following equation can be obtained:

$$\Delta U_{c_{\text{sm}},i} - \Delta U_{c_{\text{sm}},i+1} = \frac{\delta I_{\text{rated}}}{2N_T C_{\text{sm}}}(N_T - i) > 0. \tag{16}$$

The analysis of the engage transition stage is similar, as shown by the waveforms in interval $t_3 \sim t_4$ in Fig. 7. Consequently, it can be concluded that the SMs in the group that enters *OUT mode* first during disengage transition stage will experience the largest increase in SM capacitor voltages, while the group that enters *IN mode* first during engage transition stage will have the smallest increase in SM capacitor voltages.

As a result, to achieve the capacitor voltage balance of TDS-DCC-SMs in different groups, the group with SMs that outputs the lowest SM output voltage, in the valve's *Power dissipation state* will be blocked first. Additionally, SMs in the group with the highest $U_{\text{sm}}$ in the valve's *Blocked state* will first enter *IN mode*. Such an arrangement ensures that the SM group with the highest averaged SM capacitor voltages will store the least power during the transition stages of the valve operation, and the SM group with the lowest averaged SM capacitor voltages will

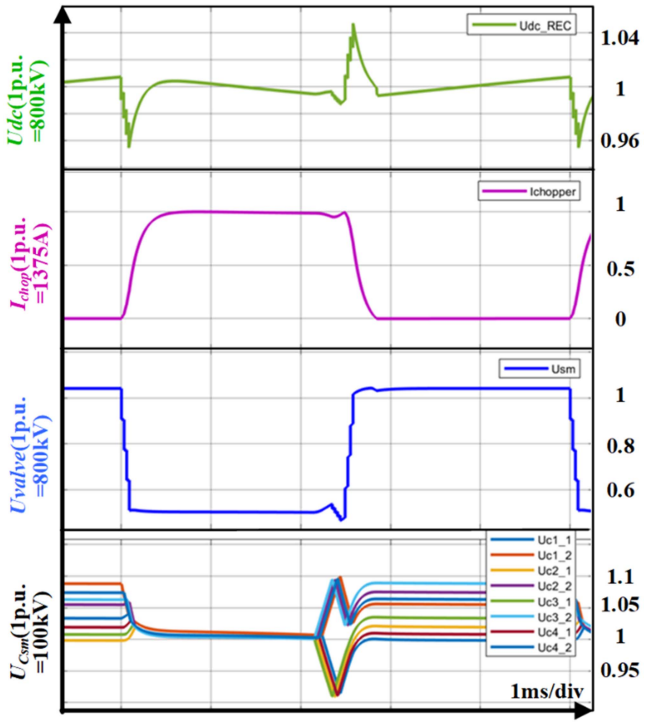


Fig. 13. Detailed simulation waveforms of TDS-DCC when k = 0.5.

store the most power during the transition stages. The procedures within each control cycle are illustrated in Fig. 9.

TABLE I
DETAILED PARAMETERS OF SIMULATION MODEL

| Parameter | Symbol | Value |
|---|---|---|
| Rated transmission power | $P_{rated}$ | 1100 MW |
| Rated dc link voltage | $U_{dcN}$ | ± 400 kV |
| Rated current | $I_{rated}$ | 1375 A |
| Smoothing reactor | $L_{dc}$ | 50 mH |
| Chopper inductor | $L_{dcc}$ | 40 mH |
| Lumped resistor | $R$ | 290.91 Ω |
| Distributed resistor | $R_{sm}$ | 1.04 Ω |
| DCC SM capacitor | $C_{sm}$ | 2 mF |
| Number of DCC SMs | $N$ | 280 |
| Number of SM groups | $N_T$ | 4 |
| Valve operation period | $T_S$ | 5 ms |

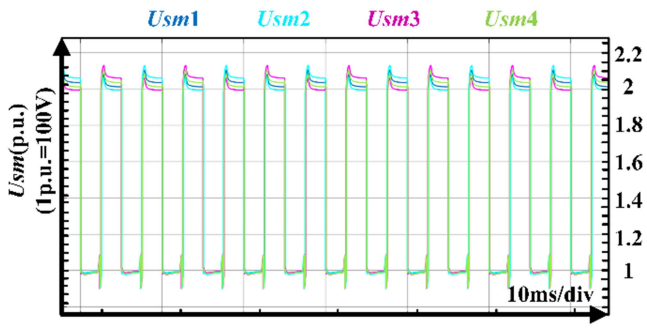


Fig. 14. Waveforms of the SM output voltages when $k = 0.5$.

## V. Simulation Validation and Cost Comparison

### A. Simulation Results

In order to verify the feasibility and effectiveness of the proposed TDS-DCC and its control strategies, a simulation model of a ±400 kV/1100 MW offshore VSC-HVDC system, based on the engineering parameters of Jiangsu Rudong offshore wind project, is established in MATLAB/Simulink environment. The configuration of the model is displayed in Fig. 10, which includes a TDS-DCC and two MMCs connected to two separate ac voltage sources. The SEC and REC of the offshore wind VSC-HVDC system are represented as the averaged models of the MMC, while the TDS-DCC is realized by a switching model. The detailed specifications of the simulation model are listed in Table I. Here, the maximum dc link voltage allowed during FRT is designed to be 1.1 p.u., and the chopper inductance is chosen to be 40 mH in accordance. The SM capacitances are set to 2 mF to limit SM capacitor voltage fluctuations limited under 1.15 p.u..

The simulation results are shown in Figs. 11–14. Fig. 11 illustrates the proposed SM modulation scheme waveforms. $ST_1$ and $ST_2$ represent the gate trigger pulse of the thyristor and the gate driving signal of the IGBT, respectively. The thyristor current, denoted as $i_{T1}$, and the voltage across the IGBT, referred to as $u_{T2}$, are also shown for a clear view of the switch actions. It can be seen that when the driving signals are given in the sequence shown in Fig. 5, $i_{T1}$ varies as the SM switches among the four modes, and the forced commutation of the thyristor is successfully achieved through coordinated actions of the IGBT.

The operation principle of the energy dissipation valve is also validated. Typical operational conditions are chosen to evaluate the performances of the proposed topology under different fault conditions. The surplus power coefficients $k = 0.3$, $k = 0.5$, and $k = 0.8$ are simulated, respectively. When $k = 0.5$, $\Delta U_{\rm dc}$ reaches the largest value [14]. The other two cases are chosen to test the FRT capability of the proposed chopper under different working conditions.

The simulation results of the FRT process when $k = 0.5$, $k = 0.8$, and $k = 0.3$ are displayed in Fig. 12. All quantities have been normalized in the simulation verification. Before the fault, the VSC-HVDC power transmission system operates normally and the TDS-DCC remains in the *Blocked state*, with all capacitors connected in series. At $t = 0.75$ s, when a three-phase short circuit fault occurs on the ac side of REC, the power transmission capability of the REC drops to (1-$k$)p.u., while $U_{\rm dc}$ rapidly increases. When $U_{\rm dc}$ reaches the predetermined threshold of 1.05 p.u., the TDS-DCC starts to operate and dissipates the excess energy, keeping the dc link voltage around the rated value. The fault lasts for 0.6 s, and after the fault is cleared at $t = 1.35$ s, the PCC voltage of REC returns to the rated value, and TDS-DCC quits operation. The maximum dc link voltage and

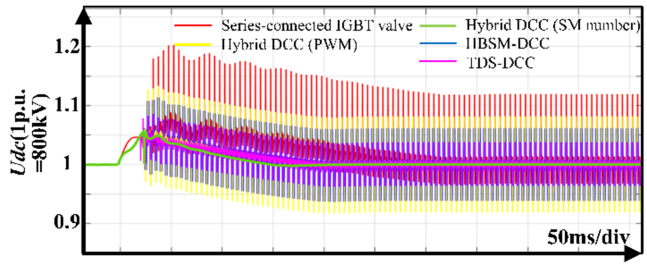


Fig. 15. DC link voltages of various DCCs.

the SM capacitor voltage fluctuations agree with the simulation model design.

According to Fig. 12(d)–(f), during FRT, the energy dissipation valve switches between the *Power dissipation state* and *Blocked state* periodically, with the operation duty cycle *d* corresponding to the surplus power coefficient *k*. When the valve is in the *Power dissipation state*, $U_{\rm valve} = 0.5U_{{\rm dc}N}$, and the voltage across the lumped resistor is also $0.5U_{{\rm dc}N}$. The chopper current equals the rated current, and TDS-DCC dissipates the rated power ($P_{\rm rated}$), causing the dc link voltage to decrease. When the valve is in the *Blocked state*, its output voltage changes to $U_{{\rm dc}N}$, and the chopper current decreases to zero. TDS-DCC dissipates no power and $U_{\rm dc}$ increases consequently. The transition stages that result from the stepwise modulation can also be observed, with $U_{\rm valve}$ rising and falling gradually in trapezoidal waves in steps. In steady state, the $U_{\rm dc}$ ripple stays within $\pm 5\%$, and the capacitor voltages are all limited under 1.15 $U_{CN}$ across all working conditions.

The SM capacitor voltage balancing strategy is also demonstrated. Fig. 13 displays the detailed waveforms of the SM capacitor voltages and the effects of the SM actions on the chopper branch voltages and currents. As can be seen from this figure, the switching of each SM will generate an induced voltage on the dc link, and the switching sequence can result in an imbalance of the capacitor voltages in different SMs. The capacitor voltage balancing strategy is thereby applied. As is shown in Fig. 13, the SM with the highest $U_{\rm sm}$ enters *IN mode* first and exits *IN mode* last, leading to a relatively balanced capacitor voltage of the SMs.

### B. Comparison With Other DCC Topologies

*1) Performance Comparison:* To compare the performance of the proposed TDS-DCC with the existing methods, the dc link voltage waveforms of several typical existing DCCs and the proposed TDS-DCC during FRT in a ±400 kV/1100 MW offshore VSC-HVDC system are presented in Fig. 15.

The concentrated DCC based on series-connected IGBT valve shown in Fig. 1(b) adopts PWM control strategy, with the IGBTs turning ON and OFF simultaneously [3]. The peak value of the $U_{\rm dc}$ can reach 1.2 p.u., and the dc link voltage ripple is about 12%. For the modular concentrated DCC based on HBSMs shown in Fig. 1(c), it employs the stepwise PWM control, with the SMs generating a periodic trapezoidal output voltage [14]. The dc link voltage ripple is about 6.2% after the $U_{\rm dc}$ stabilizes. The IGBT based hybrid DCC shown in Fig. 1(f) can either adopts

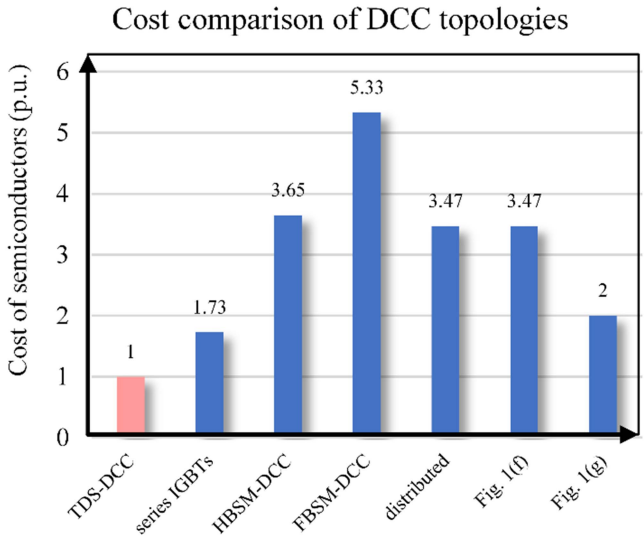


Fig. 16. Cost comparison of several existing DCCs with TDS-DCC in terms of semiconductors.

the stepwise PWM control or regulates the amount of power dissipated through changing the number of bypassed SMs [12]. From Fig. 15, it can be seen that, for the hybrid DCC, when the stepwise PWM control is adopted, the SMs are put in and cut OFF gradually in groups, and the dc link voltage ripple is about 8.2%, which is a little larger than that of the HBSM based DCC. However, when the hybrid chopper based on IGBTs regulates the power dissipation by changing the number of the SM inputs, the dc link voltage ripple is almost eliminated, since each SM functions as an independent power unit, which allows for smooth power dissipation adjustments [17].

For the proposed TDS-DCC, the peak value of $U_{\rm dc}$ is about 1.086 p.u., and the dc link voltage ripple in steady state is kept under 4%, which is between that of the HBSM based DCC and that of the IGBT based hybrid DCC controlling the number of the SM inputs. Generally, the dc link voltage ripple of the TDS-DCC is mainly determined by the inductors of the system, as is shown in (17), while $N_T$ and $\delta$ have relatively limited effects on the amplitude of the spikes

$$\Delta U_{\rm dc} = \frac{L_{\rm REC} L'_{\rm SEC} U_{{\rm dc}N}}{2(L_{\rm REC} L_{\rm dcc} + L_{\rm SEC}{}' L_{\rm dcc} + L_{\rm SEC}{}' L_{\rm REC})}. \quad (17)$$

As can be seen from (17), increasing $L_{\rm dcc}$ can mitigate the induced dc link voltage spikes. According to the engineering design of Rudong offshore wind project in China, the dc voltage spikes ($\Delta U_{\rm dc}$) in steady state should be limited under 0.05 p.u., so that peak value of the dc link voltage during the FRT process is kept under 1.1 p.u. In this article, $L_{\rm dcc}$ is selected to be 40 mH.

To conclude, the dc voltage spikes are an inherent characteristic for DCCs employing PWM control strategies, because of the changes in the SM output voltages during operation. Nevertheless, due to the composite modular design of the TDS-DCC-SMs, the dc voltage spikes of the TDS-DCC are reduced by half compared to other modular concentrated DCCs, such as the HBSM-DCC shown in Fig. 1(c).

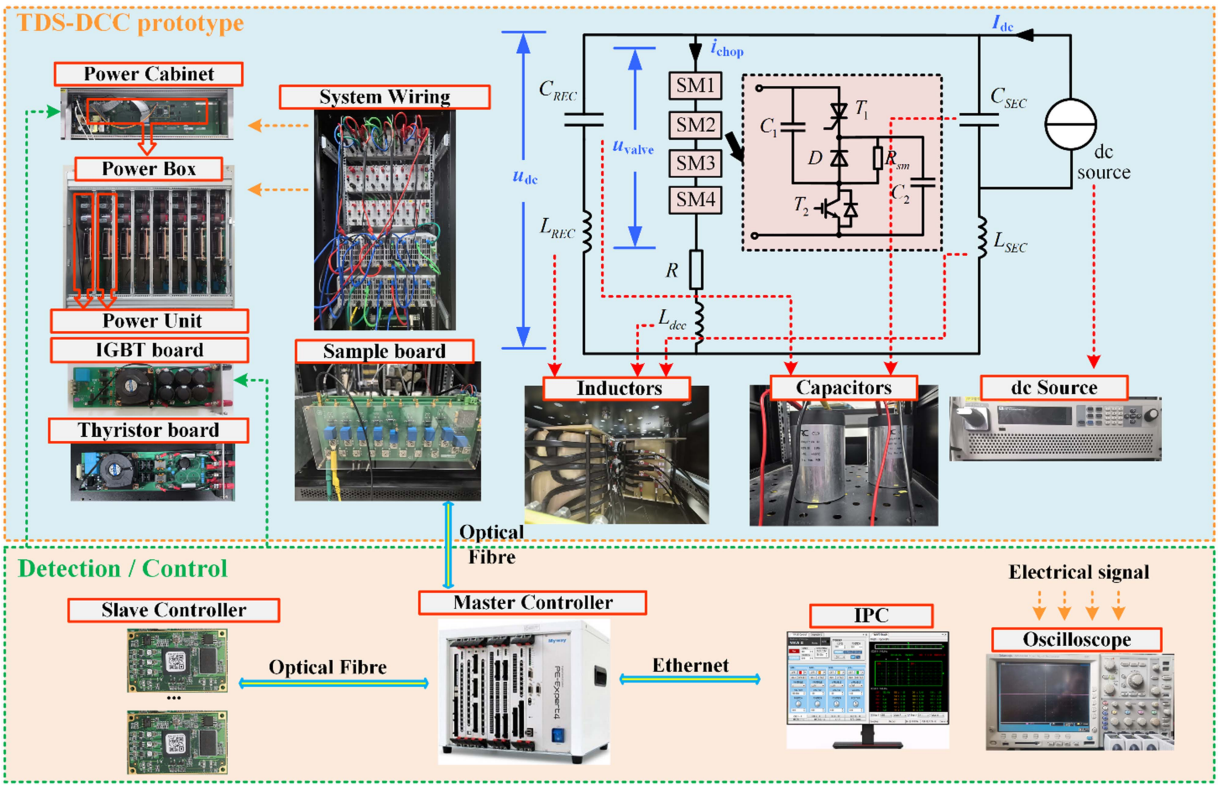


Fig. 17. Experiment prototype layout and equivalent test topology of the TDS-DCC.

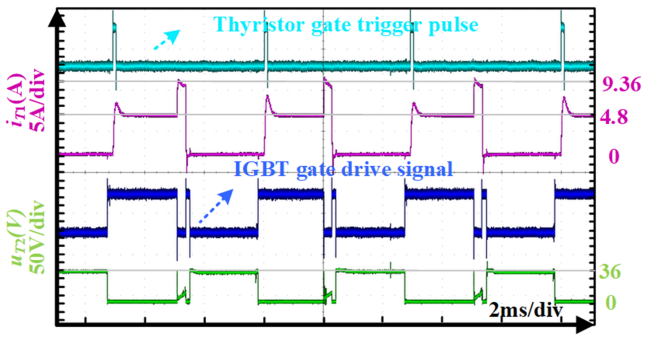


Fig. 18. Experimental waveforms of switch driving signals and voltage and current variations in a TDS-DCC-SM when $k = 0.5$.

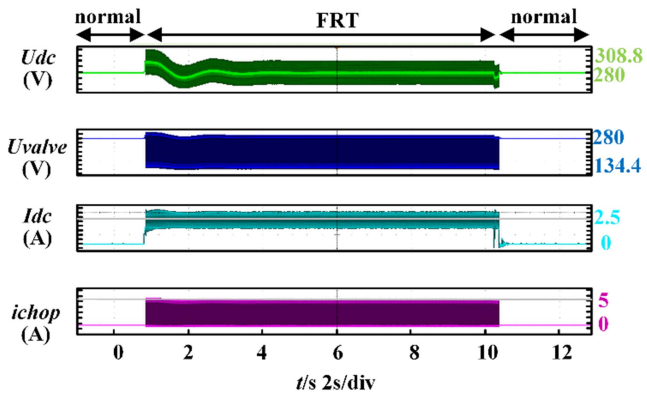


Fig. 19. Experiment waveforms of TDS-DCC during the FRT process. (a) $k = 0.5$. (b) $k = 0.8$. (c) $k = 0.3$.

*2) Cost Comparison:* Fig. 16 compares the cost of the TDS-DCC with the existing DCC topologies shown in Fig. 1 in terms of the total cost of the semiconductors. The comparison is based on the engineering parameters of a ±400 kV/1100 MW offshore VSC-HVDC system (Jiangsu Rudong offshore wind project) [19]. The types and unit prices of the selected power electronic devices are taken from the datasheets and price lists on [24] and [25]. The costs are all normalized, with the unit price of the 3.3 kV/2400 A IGBT module set as 1 p.u. ($1999.8) [26].

From the *Blocked state* analysis in Section II, the rated SM capacitor voltages for modular DCCs should meet the equation $N_C U_{CN} = U_{\mathrm{dc}\,N}$, where $N_C$ is the number of SM capacitors. In the DCC topologies shown in Fig. 1(c), (d), (e), (f), and (g), $N_C$ equals the number of SMs $N$. Unlike the traditional approaches, $N_C$ is doubled in the TDS-DCC due to the module composite design. Moreover, each SM sustains a voltage of $2U_{CN}$ since the two capacitors in a TDS-DCC-SM are series-connected during the *Blocked state*. As a result, the number of TDS-DCC-SMs is halved for the same voltage level, while the operating voltage of the semiconductors remains unchanged. For the ±400 kV VSC-HVDC system, the rated SM capacitor voltages for the modular DCCs and operating voltages of semiconductors for all DCCs are chosen as 1.5 kV, with $N_C = 560$. In this case, 3.3 kV/2400 A IGBTs, 3 kV/3003 A thyristors and 4 kV/3847 A diodes are selected for comparison.

As can be seen from Fig. 16, TDS-DCC saves at least 42% of the cost of semiconductors compared to other DCCs, thanks to its module composite design and the adoption of semicontrolled

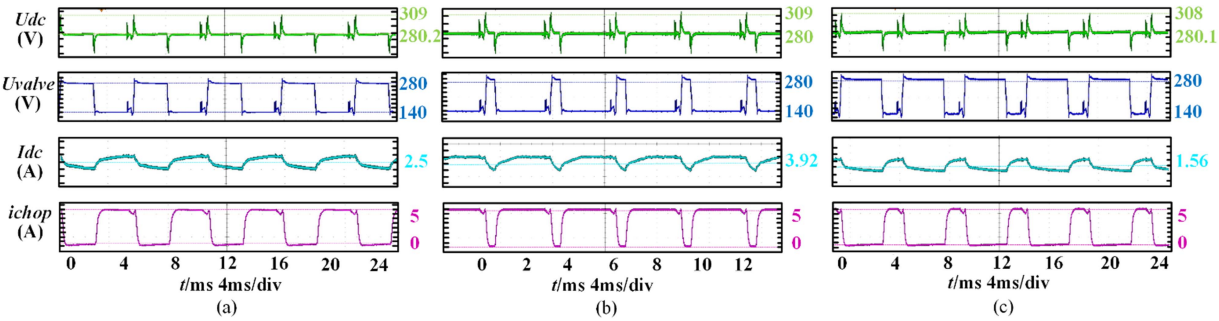


Fig. 20. Detailed experiment waveforms of the TDS-DCC in three typical cases. (a) $k = 0.5$. (b) $k = 0.8$. (c) $k = 0.3$.

TABLE II
EXPERIMENT PARAMETERS FOR TDS-DCC

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| Rated capacity | 1.4 kW | Rated dc link voltage | 280 V |
| Control frequency | 200 Hz | Rated current | 5 A |
| Lumped resistor | 28 Ω | Chopper inductance | 2 mH |
| REC inductance | 0.5 mH | SEC inductance | 10 mH |
| MMC equalized capacitance | 1.4 mF | SM capacitance | 330 $\mu$F |
| SM number | 4 | SM resistor | 7 Ω |

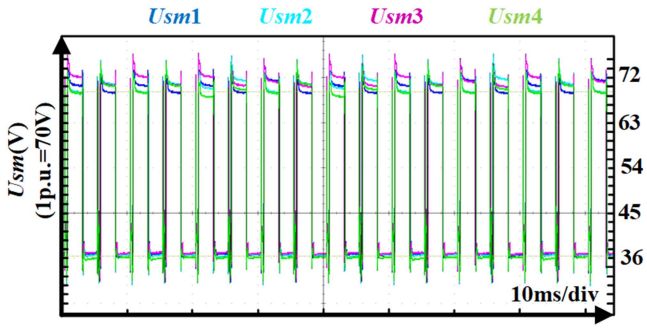


Fig. 21. Waveforms of the SM output voltages when $k = 0.5$.

devices. Given that the cost of semiconductors takes up a significant part of the total cost [19], TDS-DCC proves to be a more economical option for the offshore VSC-HVDC systems.

## VI. EXPERIMENTAL VERIFICATION

A scaled-down prototype with rated parameters of 280 V/1.4 kW is built in the laboratory to validate the effectiveness of the proposed topology and control methods. The parameters of the experimental platform are shown in Table II. Fig. 17 shows the layout of the experimental platform and the configuration of the equivalent test topology of the TDS-DCC. Similar to the simulation verification, three typical working conditions are considered in this experiment to validate the operation principles and the performance of the proposed chopper under different surplus power coefficients.

The experiment results are shown in Figs. 18–20. Fig. 18 presents the detailed experimental waveforms of the driving signals of $T_1$ and $T_2$, the thyristor current, and the voltage over the IGBT in a TDS-DCC-SM when $k = 0.5$. This figure demonstrates the successful commutation methods for the thyristors and validates the modulation scheme of the TDS-DCC-SMs introduced in Section III. During FRT, in a TDS-DCC-SM, the IGBT is turned ON first and the thyristor trigger pulse is applied with a 200 $\mu$s delay until the thyristor is forward biased. When the SM is about to enter the *OUT mode*, $T_2$ is turned OFF for 200 $\mu$s, then turned back on for 150 $\mu$s. $T_1$ is then reverse biased and completes forced commutation during the period, as shown by the thyristor current waveforms in Fig. 18, before IGBT turns OFF and the SM transits to *OUT mode*.

Fig. 19 displays the complete FRT process. At $t = 0.8$ s, the dc source switches from a voltage source to a current source to simulate a fault where REC encounters a power export failure. The dc link voltage rises following the fault, and the chopper activates immediately once $U_{\rm dc}$ exceeds the predetermined limit. The input current of the dc source is also shown in Fig. 19. During the FRT process, the power injected into the system remains around the rated power of the system (1.4 kW), and the dc link voltage stays in a safe range around the rated voltage, owing to the effective and precise power dissipation of the chopper.

Fig. 20 presents the detailed experimental waveforms of the three working conditions during FRT, respectively. The valve voltage is shaped into a trapezoidal wave with four steps, proving the correctness of the stepwise control strategy demonstrated in the previous sections. The current in the chopper branch alternates between zero and the rated current, corresponding to the periodic state changes of the energy dissipation valve.

Fig. 21 presents the output voltage of the four SMs when $k = 0.5$ to show their action sequences based on voltage sorting and validate the capacitor voltage balancing algorithm introduced in Section IV. Due to the capacitor voltage balancing strategy, SM with the lowest output voltage in the *Power dissipation state* will be blocked first during the disengage transition stage, while SM with the highest output voltage in the *Blocked state* will be the first to enter *IN mode* during the engage transition stage, keeping the capacitor voltages well-balanced in the SMs of the chopper.

## VII. CONCLUSION

This article presents a novel hybrid dc chopper topology named TDS-DCC that applies a composite module design, which halves the number of the SMs and reduces the number

of the switches by 25%. Also, the topology uses both fully-controlled and semicontrolled devices, saving at least 42% of the cost of the device in terms of the expense of the semiconductors. The topology and the operation principle of the device are deduced, and an SM modulation scheme is proposed to achieve the forced commutation of the semicontrolled devices. Moreover, the implementation of the stepwise control strategy allows the chopper to achieve precise power dissipation control and mitigates the EMI performance of the device. Additionally, to solve the capacitor voltage imbalance caused by the stepwise actions of the SMs, a voltage balancing algorithm is proposed to ensure a well-balanced energy distribution across the SMs. The full-scale simulation model and the scaled-down prototype verified the proposed operation principle as well as the control strategies. The simulation and experiment results give a possible outlook of the applications of the TDS-DCC in engineering projects.

## REFERENCES


[1] M. de Prada, L. Igualada, C. Corchero, O. Gomis-Bellmunt, and A. Sumper, "Hybrid AC-DC offshore wind power plant topology: Optimal design," *IEEE Trans. Power Syst.*, vol. 30, no. 4, pp. 1868–1876, Jul. 2015.

[2] G. Abeynayake, T. Van Acker, D. V. Hertem, and J. Liang, "Analytical model for availability assessment of large-scale offshore wind farms including their collector system," *IEEE Trans. Sustain. Energy*, vol. 12, no. 4, pp. 1974–1983, Oct. 2021.

[3] J. Maneiro, S. Tennakoon, C. Barker, and F. Hassan, "Energy diverting converter topologies for HVDC transmission systems," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, Lille, France, Sep. 2013, pp. 1–10.

[4] A. Dekka, B. Wu, R. L. Fuentes, M. Perez, and N. R. Zargari, "Evolution of topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 4, pp. 1631–1656, Dec. 2017.

[5] P. Wang, N. Deng, and X.-P. Zhang, "Droop control for a multi-line current flow controller in meshed multi-terminal HVDC grid under large DC disturbances," *IEEE Power Energy Technol. Syst. J.*, vol. 5, no. 2, pp. 35–46, Jun. 2018.

[6] X. Wang and B.-T. Ooi, "High voltage direct current transmission system based on voltage source converters," in *Proc. 21st Annu. IEEE Conf. Power Electron. Specialists*, San Antonio, TX, USA, 1990, pp. 325–332.

[7] B. Xu, X. Wang, G. Wang, Z. Ning, J. Li, and J. Zhou, "The state of art of energy consumption devices for offshore wind power system," in *Proc. Int. Conf. Power System Technol.*, Haikou, China, Dec. 2021, pp. 1510–1514.

[8] S. Cao et al., "Energy dissipation of MMC-HVDC based onshore wind power integration system with FB-DBS and DCCB," *IET Renewable Power Gener.*, vol. 14, pp. 222–230, 2020.

[9] W. Jia, X. Zhang, S. Wu, L. Qi, Y. Huang, and G. Zhao, "Energy control technology for MMC during fault ride through," in *Proc. 18th Int. Conf. AC DC Power Transmiss.*, China, 2022, pp. 678–684.

[10] Z. Li et al., "Energy diverting converter topology using unidirectional current H-bridge submodules for VSC-HVDC transmission system," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5299–5308, May 2022.

[11] S. Wu, L. Qi, M. Jin, Z. He, and X. Zhang, "An MMC with integrated energy dissipation function using thyristor-based chopper modules for the offshore wind VSC-HVDC system," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 1609–1623, Jan. 2024.

[12] B. Xu, C. Gao, J. Zhang, J. Yang, B. Xia, and Z. He, "A novel DC chopper topology for VSC-based offshore wind farm connection," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 3017–3027, Mar. 2021.

[13] A. Abdalrahman and E. Isabegovic, "DolWin1 - Challenges of connecting offshore wind farms," in *Proc. IEEE Int. Energy Conf.*, Leuven, Belgium, Apr. 2016, pp. 1–10.

[14] Y. Li, J. Xu, B. Xu, C. Gao, and T. Wen, "A power losses and thermal energy optimization method for hybrid DC chopper based on hysteresis control strategy," *IEEE Trans. Power Electron.*, vol. 40, no. 1, pp. 486–499, Jan. 2025.

[15] Z. Zhao et al., "Resonance analysis and suppression in jiangsu rudong offshore wind power flexible DC system," *Electric Power Construction*, vol. 44, no. 6, pp. 144–152, 2023.

[16] Y. Tian, Z. Zhao, and Y. Xue, "Sinusoidal modulation compensation strategy of hybrid DC chopper based on half-bridge submodules," *High Voltage Eng.*, vol. 49, no. 10, pp. 4278–4286, 2023.

[17] S. Wu, X. Zhang, Z. He, M. Jin, and L. Qi, "An economical concentrated DC chopper based on thyristors with resonant self-turn-off ability for offshore wind VSC-HVDC system," *IEEE Trans. Ind. Electron.*, vol. 71, no. 8, pp. 9951–9955, Aug. 2024.

[18] H. Yao et al., "Concentrate DC energy braking device with discharge controllable sub-module topology and its control," *High Voltage Eng.*, vol. 47, no. 8, pp. 2896–2904, 2021.

[19] S. Wu, L. Qi, X. Zhang, B. Zhang, Z. He, and M. Jin, "A novel low-cost DC chopper for offshore wind VSC-HVDC system by using thyristors instead of full-control devices," *IEEE Trans. Ind. Electron.*, vol. 71, no. 4, pp. 3639–3649, Apr. 2024.

[20] G. K. Dubet, "Classification of thyristor commutation methods," *IEEE Trans. Ind. Appl.*, vol. IA-19, no. 4, pp. 600–606, Jul. 1983.

[21] L. Yin, Q. Chen, B. Li, J. Liu, Z. Li, and Y. Liu, "A novel DC energy dissipation topology with concentrated dissipation resistor and control method for offshore wind VSC-HVDC system," *IEEE Trans. Ind. Appl.*, vol. 60, no. 2, pp. 2880–2890, Mar./Apr. 2024.

[22] X. Shi, Z. Wang, B. Liu, Y. Li, L. M. Tolbert, and F. Wang, "DC impedance modelling of a MMC-HVDC system for DC voltage ripple prediction under a single-line-to-ground fault," in *Proc. IEEE Energy Convers. Congr. Expo.*, Pittsburgh, PA, USA, 2014, pp. 5339–5346.

[23] Z. Zhang, Z. Xu, Y. Xue, and G. Tang, "DC-side harmonic currents calculation and DC-loop resonance analysis for an LCC–MMC hybrid HVDC transmission system," *IEEE Trans. Power Del.*, vol. 30, no. 2, pp. 642–651, Apr. 2015.

[24] 2025. [Online]. Available: http://www.tec.crrczic.cc/1715.html

[25] 2025. [Online]. Available: https://www.infineon.com/cms/cn/product/power/igbt/igbt-modules/

[26] 2025. [Online]. Available: https://www.digikey.com/en/products/detail/infineon-technologies/FZ2400R33HE4BPSA1/14311606?curr=usd&utm_campaign=buynow&utm_medium=aggregator&utm_source=octopart

[27] C. J. Sun, J. W. Zhang, X. Cai, and G. Shi, "Analysis and arm voltage control of isolated modular multilevel DC-DC converter with asymmetric branch impedance," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 5978–5990, Aug. 2017.

[28] S. Wu, X. Zhang, B. Zhang, and L. Qi, "A low-cost and low-ripple DC chopper with thyristors-based switch modules and flexible switching control strategy for the offshore wind VSC-HVDC system," *CSEE J. Power Energy Syst.*, to be published, doi: 10.17775/CSEEJPES.2024.01100.

[29] T. Li, B. Yuan, Y. Wang, and Y. Wu, "Optimal designation of surplus power AC chopper in new energy transmitted by VSC-HVDC system," in *Proc. IEEE 8th Conf. Energy Internet Energy Syst. Integration*, 2024, pp. 1127–1132.


**Yunqi Jing** received the B.S. degree in electrical engineering in 2024 from Shanghai Jiao Tong University, Shanghai, China, where she is currently working toward the M.S. degree in electrical engineering.

Her research interests include dc chopper and fault ride though of the VSC-HVDC system.

**Jianwen Zhang** (Senior Member, IEEE) received the B.Eng., M.Sc., and Ph.D. degrees in electrical engineering from Shanghai Jiao Tong University, Shanghai, China, in 2003, 2006, and 2014, respectively.

He is currently a Professor with Shanghai Jiao Tong University, Shanghai, China. His research interests include topology, operation, and control of power conversion systems.

**Liqian Su** received the B.Eng. and M.Sc. degrees in electrical engineering from Hohai University, Nanjing, China, in 2014 and 2016, respectively. She is currently working toward the Ph.D. degree in electrical engineering with Shanghai Jiao Tong University, Shanghai, China.

Her research interest includes the topology and control of flexible dc transmission.

**Gang Shi** (Member, IEEE) received the B.Eng., M.Sc., and Ph.D. degrees in electrical engineering from Shanghai Jiao Tong University, Shanghai, China, in 2007, 2009, and 2014, respectively.

From 2017 to 2018, he was a Research Fellow with the School of Electronic Electrical and Systems Engineering, University of Birmingham, Birmingham, U.K. He is currently an Associate Professor with Shanghai Jiao Tong University, Shanghai, China. His research interests include the operation and control of hybrid ac/dc grids.

**Jiajie Zang** (Member, IEEE) received the Ph.D. degree in mechatronic systems engineering from Simon Fraser University, Surrey, BC, Canada, in 2022.

He is currently a Lecturer with the School of Electronic and Electrical Engineering, Shanghai University of Engineering Science, Shanghai, China. His research interests include solid-state transformers, multilevel converters, and bidirectional dc–dc converters.

**Jianqiao Zhou** (Member, IEEE) received the B.Sc. degree in electric engineering from Xi'an Jiao Tong University, Xi'an, China, in 2014, and the Ph.D. degree in electrical engineering from Shanghai Jiao Tong University, Shanghai, China, in 2020.

He is currently an Associate Research Fellow with the Wind Power Research Center, Shanghai Jiao Tong University. His research interests include solid-state transformers and multiport converters.

**Wei Bao** was born in Hefei, China in 1969. He received the B.Sc. degree from Wuhan Institute of Hydraulic and Electric Engineering, Wuhan, China, in 1991, and the M.Sc. degree from Hefei Polytechnic University, Hefei, China, in 1994, all in electrical engineering.

He was Chief Engineer with the Grid Department of East China Electric Power Test and Research Institute and currently is a Chief Engineer with State Grid Shanghai Municipal Electric Power Company Electric Power Research Institute, Power Grid Center. His primary research interests include relay protection and automation of power system, power electronics, and HVDC.

Prof. Bao is a part-time Professor with the Shanghai Jiao Tong University and Shanghai Electric Power University, as well as a Standing Director of the Offshore Wind Power Grid Integration and Accommodation Subcommittee of the IEEE PES China Satellite Technical Committee - Renewable System Integration Committee.

**Xu Cai** (Senior Member, IEEE) received the B.Eng. degree from Southeast University, Nanjing, China, in 1983, and the M.Sc. and Ph.D. degrees from the China University of Mining and Technology, Xuzhou, China, in 1988 and 2000, respectively, all in electrical engineering.

In 2002, he was a Professor with Shanghai Jiao Tong University, Shanghai, China, where he has been the Director of Wind Power Research Center, since 2008. His research interests include power electronics and renewable energy exploitation and utilization.