A New Dual-Source Inverter Topology With Enhanced Modulation for Hybrid Energy Sources in Electric Vehicles Application

Javad Ebrahimi, *Senior Member, IEEE*, Hosein Ghojavand, *Student Member, IEEE*, and Suzan Eren, *Senior Member, IEEE*

***Abstract*—Hybrid energy sources in electric vehicles are a well-established approach to mitigating pollution caused by fossil fuels, thanks to their integration of batteries and ultra-capacitors. While various hybrid source inverters (HSIs) have been introduced in the literature to enable single-stage conversion, further advancements in topology and operation are still achievable. This article proposes a novel HSI structure that utilizes four shared IGBTs across three phases, complemented by a secondary two-level voltage source inverter. Compared to conventional HSIs, the proposed topology reduces the number of switches and eliminates the need for diodes. The shared-switch configuration leads to lower switching and conduction losses, enhancing overall efficiency. In addition to the new topology, a modified space vector modulation technique tailored for HSIs is introduced. This modulation strategy is applied to the proposed topology, and its performance is evaluated across multiple metrics, including junction temperature profile, efficiency, output total harmonic distortion, and switching and conduction losses. The results demonstrate significant performance improvements. Furthermore, both simulation and experimental results are presented to validate the functionality of the proposed topology and modulation scheme.**

***Index Terms*—Electric vehicle (EV), hybrid energy source, reconstructed vectors, space vector modulation (SVM), voltage source inverter (VSI).**

I. Introduction

To address concerns about fossil fuels depletion and environmental sustainability, electric vehicles (EVs) have emerged as a practical solution [1], [2], [3]. In EVs, voltage source inverters (VSIs) have been a preferred choice due to their simple design, ease of control, cost-effectiveness, and high power density. They are pivotal for converting the direct current (dc) stored in the vehicle's battery into alternating current (ac) at the specific frequency feeding the motor. However, with the rise of hybrid electric vehicles (HEVs), plug-in hybrids, and battery electric vehicles (BEVs), the demand for higher efficiency, better performance, and more advanced functionalities is growing.

For more efficient operation, a dc–dc boost converter is used in conjunction with the VSI, between the battery and the inverter. By doing this, the battery voltage can be increased to meet driving demands. A key advantage of this adjustable voltage is the expansion of high-efficiency zones for both the inverters and the electric machines (EMs). In addition, the constant torque-speed range of the EMs can be extended without requiring a higher battery voltage. However, the power density of dc–dc converters is largely influenced by the size of the indicator and as the power requirement in modern EVs is on increase, the size and weight of the dc–dc converter might undermine its advantages. Moreover, this dc–dc converter limits the power rating of the battery pack, as they are connected in series, requiring their maximum power to be matched. Consequently, extending the electric driving range by increasing battery size demands greater tradeoffs among performance, cost, and power density compared to the simpler architecture [4], [5].

A proven solution is using hybrid-source inverters (HSIs), which are already discussed in the literature [6]. Its fundamental purpose is connecting two different sources to the same ac output using a single conversion stage, allowing implementation in power-split architectures due to its source duality. Unlike conventional configuration that integrates a dc–dc in series with battery, suggested HSI connects the battery to one dc input, while the other dc-link voltage is provided by another dc source. In other words, the HSI can operate in three distinct modes during operation, supplying power to the EM with a discrete yet variable dc voltage [7]. The efficiency of the driving inverter is also expected to improve because of the single conversion stage between the battery and the EM, as well as the disconnection of the dc–dc converter from the traction system. By using Insulated Gate Bipolar Transistor (IGBT)/diode modules, the HSI can enter rectification mode and generated power can be delivered to one dc source, excluding the other. Overall, with the elimination of bulky filters typically required in dc–dc converters, HSIs achieve a higher power density [4].

For powering EVs, fuel cells, batteries, and supercapacitors are commonly used. However, to meet energy/power density and chairing requirements for EVs, not a single type of source is enough. Therefore, the industry has turned to employing two or more different types of dc sources simultaneously in

Received 24 January 2025; revised 5 April 2025; accepted 14 May 2025. Date of publication 13 August 2025; date of current version 22 October 2025. This work was supported by the Natural Sciences and Engineering Research Council of Canada (NSERC). Recommended for publication by Associate Editor D. Dah Chuan Lu. *(Corresponding author: Javad Ebrahimi.)*

The authors are with the Department of Electrical and Computer Engineering, Queen's University Kingston, ON K7L 3N6, Canada (e-mail: javad.ebrahimi@queensu.ca).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3598621.

Digital Object Identifier 10.1109/TPEL.2025.3598621

HEVs [8], [9], [10], [11]. Li-ion batteries are widely recognized as a well-developed and commercially available technology [12] and are used as the primary source of energy owing to their merits of high energy density, consistent voltage while providing power, modular design flexibility, and acceptable efficiency. These batteries, however suffer from low power density and long charging times [13], [14]. Complementing batteries' demerits, ultra-capacitors (UC) can be integrated as the secondary energy source in HSIs. UCs feature high power density, extended charge/discharge count, lower internal resistance, minimal heat loss, good reversibility for regenerative braking [15], [16], [17]. By combining the complementary features of batteries and UCs, HSIs create a more efficient and reliable power system for EV applications.

In [18], an NPC form HSI with two ports is presented. Thanks to the dual dc power sources, this converter can be effectively integrated into power-split systems, such as those utilized in the Toyota Prius [18] for industrial applications. Based on the output power requirements, the inverter can be driven by either one or both power sources. Furthermore, the use of a smaller battery pack, in contrast to the larger battery systems typically found in BEVs, reduces the volume and cost of the converter [10]. Also, HSIs are bidirectional, enabling the EM to function as a generator during regenerative braking. In this mode, HSI operates as a rectifier, directing the regenerated power back to one or both dc inputs.

Proposing new topologies for realization of HSI, Ebrahimi et al. [19] presented a single-stage HSI configuration that integrates two dc sources for EV applications. This enhanced HSI topology reduces conduction losses and improves efficiency; however, it requires a high number of switches, which increases the overall cost. Another research study, Ebrahimi and Eren [20] presented an HSI derived from a flying capacitor converter, featuring modularity for easy expansion to accommodate multiple dc voltage sources. In this topology, however, the dc voltage sources do not share a common ground, which adds complexity to industrial applications. Although HSI topologies have been extensively investigated in the literature, topologies have not reached high efficiency, and their implantation is still costly.

The circuit presented in [18] is an NPC form single-stage multiport inverter with two ports, and has generally found attraction in applications like hybrid EVs, grid-tied application, and hybrid PV-battery systems. In this configuration, different energy sources are integrated using only one energy conversion stage. As illustrated in Fig. 1(a), two energy sources, namely V_{DC_1} and V_{DC_2} are connected to high and low dc terminals of the inverter while ac terminal is only connected to the motor. It is also possible to increase the input ports to employ more sources. With proper modulation technique, flexible power distribution, and multiple operation modes are achieved. Despite the advantages highlighted in [18], this approach is not exempt from certain limitations, which impact its overall efficiency. In each phase, the presence of high number of switches and diodes increases the cost of circuit implementation, particularly as the number of dc ports increases. In addition, high number of switches can lead to increased conduction losses, subsequently reducing efficiency. Higher losses in semiconductor devices will lead to an

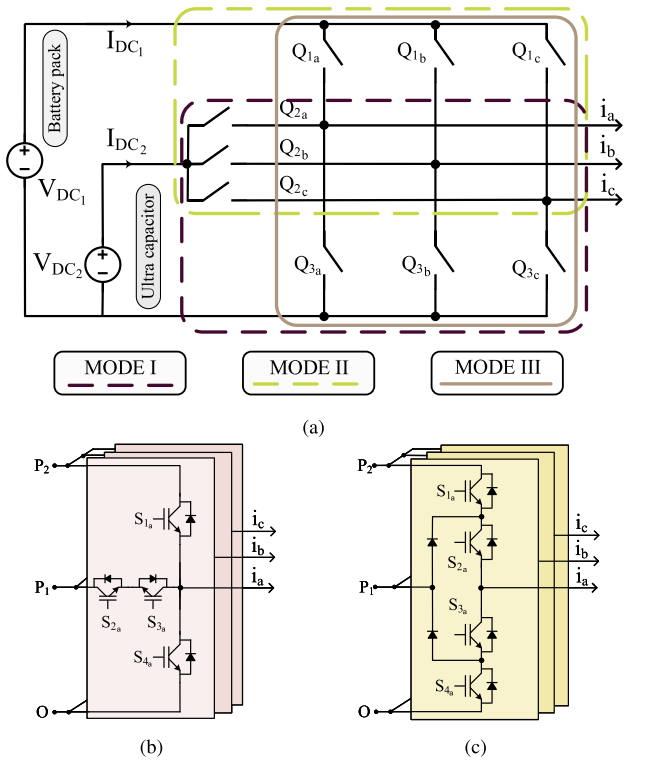


Fig. 1. (a) Schematic of a hybrid battery-UC inverter [10]. (b) Realization of the HSI based on a T-Type topology. (c) Realization of the HSI based on an NPC topology.

increase in their thermal junction temperature, shortening their operational lifespan and lowering their reliability [21], [22].

Similar to all other HSIs, Dorn-Gomba et al. [18] required a proper modulation technique. Common modulation techniques, such as pulsewidth modulation (PWM) and space vector modulation (SVM) are broadly advanced for voltage control and harmonic reduction [23], [24]. Advanced modulation techniques, such as zero-sequence component injection PWM and reconstructed level-based SVM, have been proposed to address specific challenges in multilevel converters, such as capacitor voltage balancing and power loss equalization. Despite their effectiveness, they are primarily designed for classic two-level and multilevel inverters with equal voltage steps while HSIs need higher degrees of flexibility due to their unique configuration and different operating modes.

The modified carrier-based PWM with injected specific zero-sequence components are introduced in [25], [26], and [27]. In [28], modified space vector PWM strategy via constructing a new virtual voltage vector is presented. For extending the linear modulation range and suppress extra harmonics of current and voltage, in [29], a discontinuous space vector PWM scheme is used. Even with the satisfactory performance, generation of reference voltage vectors is still complex and requires heavy computations. In addition, they are mainly focused on working under unbalanced voltage sources.

A decoupling model of power allocation of dc links is developed in [30], and in [31], the duty cycles are directly solved with mathematical equations. However, they are specifically proposed for microgrid and PV applications. One study presents

a two-stage modulation scheme aimed at maximizing the output power of one dc source by minimizing the power processed through the dc–dc converter [32]. In [31], a three-dimensional vector multimapping is presented for power split between sources in an HSI. However, these methods introduce additional complexity and increases system delays, and are mainly meant to provide flexible power distribution between sources.

With classic modulation proposed for classic topology in [18], three regions are defined, where in each of them inverter is supplied with a constant dc voltage. This modulation is simple and easy to implement, but output voltage total harmonic distortion (THD) and total conduction loss are still high and could be further mitigated. Also, with classic modulation power loss distribution is highly uneven. Beside, in each region a set of switches are ON or OFF while the other two are switched. This switching combination leads to unequal loss distribution between switches, creating different thermal profile in each switch and necessity of choosing switches with different maximum thermal tolerances.

In this article, a novel single-stage HSI topology featuring reduced switch count and elimination of diodes is proposed and designed specifically for hybrid source applications. This new topology leverages shared switches between the three phases, resulting in a significant reduction in overall conduction losses and an enhanced efficiency. In addition, the total number of semiconductor devices is reduced from 18 to 10, contributing to a substantial reduction in both cost and complexity. Furthermore, a new reconstructed SVM technique has been developed for both the proposed and classic topologies, specifically tailored for HSIs. This modulation scheme increases the number of regions in each sector to nine, optimizing the performance of the HSI across various operational parameters. By employing this advanced modulation strategy, several advantages are achieved, including reduced THD in the output voltages, lower switching losses, improved thermal management of the junction temperatures, and overall increased efficiency. This topology and modulation technique collectively offers a practical solution for improving the performance and cost-effectiveness of HSIs in EV applications.

The rest of this article is organized as follows. Classic topology and modulation for hybrid EVs are presented in Section II. In Section III, the proposed topology with classic modulation (PTCM) is introduced. Furthermore, in Section IV, proposed modulation is introduced for both classic and proposed topology. A comprehensive comparison among the PTCM, the proposed topology with the proposed modulation (PTPM) and the classic topology with classic modulation from different aspects is made in Section V. Simulation and experimental results are presented in Sections VI and VII, respectively. Finally, Section VIII concludes this article.

II. Classic Topology for HSIs and Its Modulation

A. Classic HSI Topology

A schematic of a hybrid battery-UC inverter and its realization based on the T-Type topology and the NPC topology is presented in Fig. 1. Although these topologies, T-Type and NPC, are schematically similar in many ways, they have key differences. In HSI, the high-voltage port is connected to the primary source, and the low-voltage port connects to the secondary source. Unlike classic structures, the HSI lacks a neutral point and does not have a neutral point connecting the upper and lower switches of each leg. As a result, each input capacitor is equal to the respective voltage source, unlike three-level inverters where it is typically half of that voltage. In this way, modulation and control strategies from traditional inverters cannot be directly applied to HSI and require new approaches. In addition, since the dc–dc converter can be bypassed in some scenarios and secondary voltage source is directly connected to the inverter, single stage converter can be enabled in this topology. For the rest of this article, we refer to NPC HSI topology, Fig. 1(c), as the classic topology of HSIs.

In each phase of the classic HSI, there are four active switches: S_{1_x}, S_{2_x}, S_{3_x}, and S_{4_x} (where x represents each of the three phases a, b, c), along with two diodes. The switches S_{3_x} and S_{4_x} operate in complementary manner to S_{1_x} and S_{2_x}, respectively. With different gate signals, the power path between the sources can be altered. When S_{1_x} and S_{2_x} are activated and S_{3_x} and S_{4_x} are OFF, power is delivered to the motor from the primary source, resulting in a phase-to-neutral output voltage of V_{DC_1}. Conversely, when S_{2_x} and S_{3_x} are ON and S_{1_x} and S_{4_x} are OFF, power is drawn from the secondary source, and output phase voltage is equal to V_{DC_2}. When S_{x_3} and S_{x_4} are turned-ON while S_{x_1} and S_{x_2} are OFF, neither voltage sources power the inverter, and the output phase voltage becomes 0. These three switching states for each phase are represented as $S_x \in \{0,1,2\}$. It is noteworthy that the switching state here not only determines the output voltage level but also selects, which voltage source is in the power path. Although this topology is simple to design and implement, the use of a large number of semiconductor devices reduces its cost-effectiveness. This limitation is significantly addressed by the novel topology proposed in Section III.

B. Classic Modulation Scheme

SVM offers an alternative to the carrier-based modulation techniques and they are employed commonly in three-phase VSIs. Although both methods aim to convert a modulation signal or vector into switching signals for the inverter, the SVM operates in the Clarke reference frame ($\alpha\beta$) instead of the frame abc [33], [34].

The classic SVM diagram for HSIs, Fig. 2, is segmented into three distinct hexagons based on the amplitude of the dc-link voltage. In this diagram, the projection of the three-phase reference voltages onto the $\alpha-\beta$ plane creates a vector known as the reference voltage vector $\mathbf{V_{ref}}$, which has constant magnitude and rotates counterclockwise. The reference vector can fall into any of three regions: Mode I, Mode II, or Mode III, and is constructed using two other vectors located at the vertices of the larger triangle it resides in.

Through implementation of classic SVM on the HSI of Fig. 1, only two different voltage levels are used during each operating mode. Despite availability of two voltage sources, the HSI functions similarly to three separate two-level inverters. In other

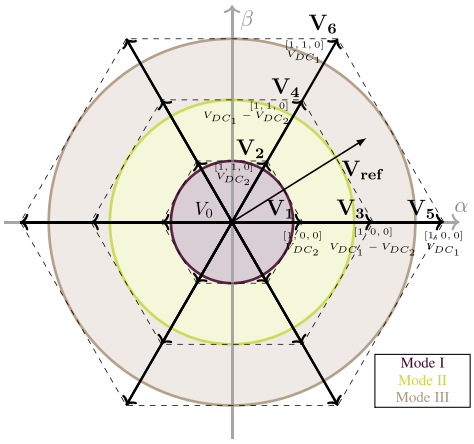


Fig. 2. Classic SVM modulation technique diagram for HSI.

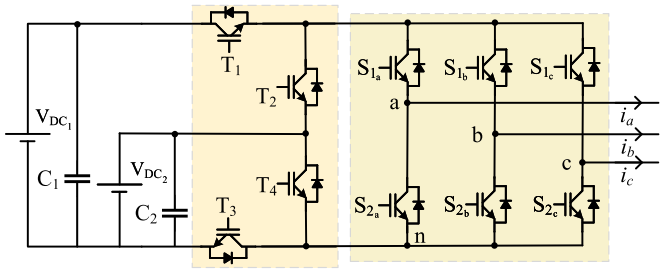


Fig. 3. Schematic of proposed HSI topology with four shared switches.

words, The larger hexagon shown in Fig. 2 represents SVM diagram of a two-level inverter with higher dc-link voltage (V_{DC_1}) than the smaller hexagon (V_{DC_2}), not a different set of vectors. In Sector I, for example, when the reference vector is within the smallest circle, the inverter should apply the $\mathbf{V_1}$, $\mathbf{V_2}$, and zero vectors. The modulator then selects dwell times based on the angle and amplitude of the reference vector. If the motor demands more power, the reference vector's magnitude increases and its location moves to the outer circle, where $\mathbf{V_5}$, $\mathbf{V_6}$, and the zero vector are used to synthesize the reference vector. Note that the only difference between $\mathbf{V_1}$, $\mathbf{V_3}$, and $\mathbf{V_5}$ is their dc-link voltage value (V_{DC_2}, V_{DC_1}–V_{DC_2}, and V_{DC_1}), and all of them are represented by [1 0 0]. Once the duty ratio for each vector is calculated, vectors need to be arranged appropriately to fulfill a certain criteria, such as minimizing the switching frequency.

The classic modulation scheme proposed for HSIs is simple to implement and easy to understand. Despite its effectiveness, there is still room for further improvement. By introducing a new modulation scheme specifically designed for HSIs, as presented in Section IV, several advantages can be achieved, including reduced conduction and switching losses, improved efficiency, and better thermal junction distribution among semiconductor devices.

TABLE I
SWITCHING STATES OF PROPOSED TOPOLOGY IN EACH MODE

Mode	States of switches							Line-to-line voltage		
	T_1	T_2	T_3	T_4	S_{1_a}	S_{1_b}	S_{1_c}	V_{AB}	V_{BC}	V_{CA}
I	0	1	1	0	1	1	1	0	0	0
	0	1	1	0	1	1	0	0	V_{DC_2}	$-V_{\mathrm{DC}_2}$
	0	1	1	0	1	0	1	V_{DC_2}	$-V_{\mathrm{DC}_2}$	0
	0	1	1	0	1	0	0	V_{DC_2}	0	$-V_{\mathrm{DC}_2}$
	0	1	1	0	0	1	1	$-V_{\mathrm{DC}_2}$	0	V_{DC_2}
	0	1	1	0	0	1	0	$-V_{\mathrm{DC}_2}$	V_{DC_2}	0
	0	1	1	0	0	0	1	0	$-V_{\mathrm{DC}_2}$	V_{DC_2}
	0	1	1	0	0	0	0	0	0	0
II	1	0	0	1	1	1	1	0	0	0
	1	0	0	1	1	1	0	0	V_{dif}	$-V_{dif}$
	1	0	0	1	1	0	1	V_{dif}	$-V_{dif}$	0
	1	0	0	1	1	0	0	V_{dif}	0	$-V_{dif}$
	1	0	0	1	0	1	1	$-V_{dif}$	0	V_{dif}
	1	0	0	1	0	1	0	$-V_{dif}$	V_{dif}	0
	1	0	0	1	0	0	1	0	$-V_{dif}$	V_{dif}
	1	0	0	1	0	0	0	0	0	0
III	1	0	1	0	1	1	1	0	0	0
	1	0	1	0	1	1	0	0	V_{DC_1}	$-V_{\mathrm{DC}_1}$
	1	0	1	0	1	0	1	V_{DC_1}	$-V_{\mathrm{DC}_1}$	0
	1	0	1	0	1	0	0	V_{DC_1}	0	$-V_{\mathrm{DC}_1}$
	1	0	1	0	0	1	1	$-V_{\mathrm{DC}_1}$	0	V_{DC_1}
	1	0	1	0	0	1	0	$-V_{\mathrm{DC}_1}$	V_{DC_1}	0
	1	0	1	0	0	0	1	0	$-V_{\mathrm{DC}_1}$	V_{DC_1}
	1	0	1	0	0	0	0	0	0	0

* V_{DC_1} and V_{DC_2} represent the dc source voltages in the topology.
** V_{dif} indicates $V_{\mathrm{DC}_1} - V_{\mathrm{DC}_2}$.

III. PROPOSED TOPOLOGY FOR HSIS

In this article, a new structure is presented, which not only reduces the switch count of classic HSI topology, but also offers great advantages in terms of conduction and switching loss, efficiency, junction temperature profiles, and THD. In this topology a set of switches. T_1, T_2, T_3, and T_4 are shared among all the phases, providing the input voltage source for a two-level three phase inverter. The two-level inverter is basically consists of six switches: S_{1_x} and S_{2_x}, where $x \in \{a, b, c\}$. Unlike classic topology with 12 IGBTs, 4in each phase with 2 diodes, in proposed topology, number of switches is reduced to 10. In Fig. 3, proposed topology circuit is presented, using two distinct voltage sources, V_{DC_1} and V_{DC_2}. V_{DC_1} is the output of battery package, and the secondary source is an UC. Like other similar topologies, a key constraint is $V_{\mathrm{DC}_1} > V_{\mathrm{DC}_2}$; otherwise, there will be uncontrolled current flow from V_{DC_2} to V_{DC_1} through the body diodes.

In Table I, different switching states of converter for different modes are presented. For example, if the reference vector is located within Mode II, turn-ON signals for T_1 and T_4 are sent, and T_2 and T_3 remain OFF. With these signals, inverter enters Mode II and V_{DC_1} powers upper side of inverter in all the phases and V_{DC_2} is connected to the lower side voltage and dc-link voltage is equal to V_{DC_1}–V_{DC_2}.

As can be seen, shared switches (T_1, T_2, T_3, and T_4) among all phases are switched-ON and -OFF with output phase voltage frequency while switches in each phase are turned-ON and OFF

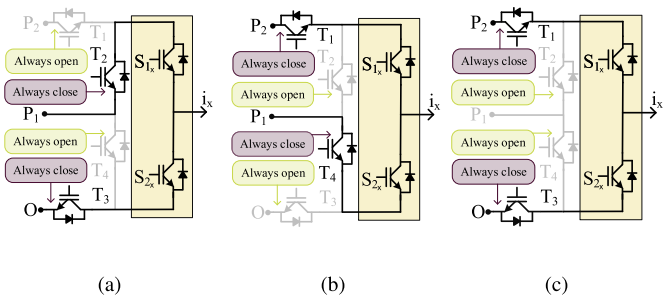


Fig. 4. Simplified schematic of proposed topology in (a) Mode I, (b) Mode II, and (c) Mode III.

TABLE II
COMPARISON OF SWITCHING DEVICES UTILIZED IN CLASSIC AND PROPOSED TOPOLOGY

	Topology for HSI		
	NPC topology	T-type topology	Proposed topology
Number of high-frequency devices	12	12	6
Number of diodes	6	0	0
Total number of switching devices	18	12	10
Loss balance of switching devices	weak	weak	good

with sampling frequency. Fig. 4 visually illustrates switching states of shared switches in each mode. In Mode I, T_2 and T_3 are turned and remained ON to provide dc-link voltage equal to V_{DC_2} to the inverter, and based on the classic modulation, S_{1_x} and S_{2_x} are switched in a complementary manner. As long as the inverter is in the first mode of operation, switching combination of T_1, T_2, T_3, and T_4 does not change. In Mode III, switches T_1 and T_3 will be ON, and the dc-link voltage will be equal to V_{DC_1}.

The classic NPC form, T-type form topologies and the proposed topology are compared in Table II in terms of the number of switching devices and their capability for loss distribution. The proposed topology includes 6 high-switching elements, with two switches per phase. In contrast, the classic topologies uses four switches per phase, totaling 12 switches overall. In addition, the classic NPC form topology requires two diodes per phase, while in the proposed topology, all diodes have been eliminated. A general observation reveals that the total number of switching components in the proposed topology is almost halved, reducing from 18 to 10. In addition, loss balance of switching devices in classic topologies is weak as switching state of two switches does not change and the others are switched ON and OFF. In addition, the total power loss is more evenly distributed among the switches in the proposed topology. Thanks to single conversion stage, the architecture shown in Fig. 3 is cost-effective, easy to manufacture, and requires simple control

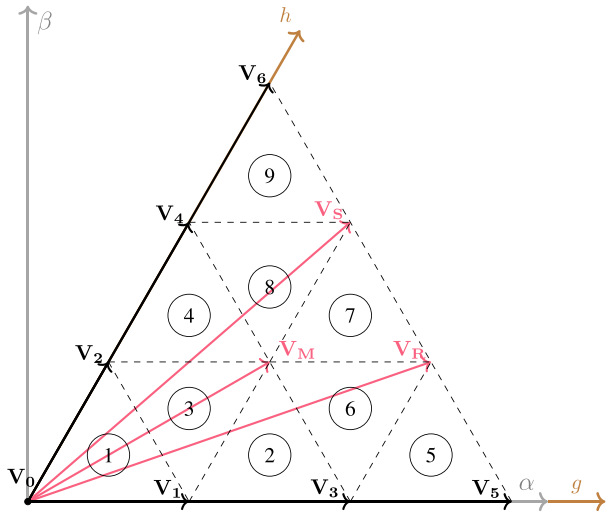


Fig. 5. First sector of the SVM diagram for the proposed modulation scheme with newly defined voltage vectors and regions.

of the switching devices. In addition, VSI topology has been extensively studied and widely used in the industry over the past decades, making it a mature, robust, and reliable solution. Since the currents drawn from dc sources is pulsating, a capacitor is connected in parallel with each dc source. These capacitors are essential to attenuate ripple current, reduce electromagnetic interference emission, and suppress voltage spikes caused by leakage inductance and switching operations [35].

In Section V, the classic and proposed topologies are compared in greater detail, beyond switch count. The proposed topology provides lower conduction losses due to its shared switches. In addition, distributing the switching frequency among the inverter IGBTs significantly reduces switching losses.

IV. PROPOSED MODULATION SCHEME

As discussed in previous section, online computations for region identification, vector selection, and level dwelling time calculation is not complex in classic modulation, but it has some demerits in many terms. The primary issue is the high switching frequency of IGBTs in all phases, which results in high junction temperatures. Switching and conduction losses contribute significantly to the total losses, and with high turn-ON and turn-OFF frequencies, managing the junction temperature becomes challenging. This issue can also lead to material and performance degradation and reduced reliability, often necessitating the use of oversize heat sinks for heat dissipation. In addition, switching and conduction losses affect efficiency across all topologies. To address these challenges, this section proposes a new SVM-based modulation scheme designed to enhance the performance of HSIs.

In this technique, a new set of vectors are defined, as illustrated in Fig. 5. Unlike classic SVM modulation with only 6 active

vectors to synthesize the reference vector, in proposed modulation there are three new reconstructed vectors. Introduced new vectors, $\mathbf{V_M}$, $\mathbf{V_R}$, and $\mathbf{V_S}$, are generated by applying two other vectors to the inverter for specific time intervals. For example, $\mathbf{V_S}$, positioned on the side of the largest hexagon, is produced by applying $\mathbf{V_6}$ and $\mathbf{V_5}$ for one-third and two-thirds of the switching period, respectively. Conversely, the vector combination for $\mathbf{V_R}$ is reversed. In addition, $\mathbf{V_M}$, located at the center of gravity of sector I, is generated by applying $\mathbf{V_3}$ and $\mathbf{V_4}$ for equal times. Equation for new reconstructed vectors are given in the following equation:

$$\begin{aligned}\mathbf{V_M} &= \frac{\mathbf{V_3}}{2} + \frac{\mathbf{V_4}}{2}\\ \mathbf{V_R} &= \frac{2\mathbf{V_5}}{3} + \frac{\mathbf{V_6}}{3}\\ \mathbf{V_S} &= \frac{\mathbf{V_5}}{3} + \frac{2\mathbf{V_6}}{3}.\end{aligned} \tag{1}$$

It might seem that proposed modulation is similar to virtual vectors, which is already in the literature. Where they are produced by applying different voltage levels from the same voltage source divided by a number of capacitors. In this technique, the voltage steps are inherently equal. However, in the proposed modulation, the reconstructed vectors are generated using different voltage sources, which can have varying values, making the voltage steps not essentially equal. In proposed modulation $\mathbf{V_2}$, $\mathbf{V_4}$, and $\mathbf{V_6}$ are all represented with the same switching pattern, [1,1,0], and their difference is in their input voltage source, V_{DC_2}, $V_{\mathrm{DC}_1} - V_{\mathrm{DC}_2}$, and V_{DC_1}, respectively. Fig. 5 is drawn under the assumption that $V_{\mathrm{DC}_1} = 3V_{\mathrm{DC}_2}$. This assumption ensures symmetrical SVM plane, simplifying its implementation. However, in cases where V_{DC_1} differs from V_{DC_2} (e.g., $V_{\mathrm{DC}_1} > 3V_{\mathrm{DC}_2}$ or $V_{\mathrm{DC}_1} < 3V_{\mathrm{DC}_2}$), the topology remains functional, but the space vector plane becomes asymmetrical.

Proposed modulation provides better accuracy in reference vector synthesize as primary vectors are much closer to each other and create tight regions. This is much more noticeable specially when modulation index increases to its upper limit, in Mode III. This feature illustrates itself in output voltage THD. In general, the closer primary vectors are, better THD performance is achieved both in phase and line voltage. A key feature of the proposed topology is its ability to continue operating even if one of the sources fails. In such a scenario, power can be solely provided by the remaining source, and the topology functions as a classic VSI with standard SVM. For instance, in the event of V_{DC_2} failure, switches T_1 and T_3 remain ON, connecting V_{DC_1} to a standard six-switch VSI configuration. This ensures uninterrupted system operation. When V_{DC_1} fails, only V_{DC_2} is connected to the dc link, and the inverter operates as a six-switch VSI. However, it cannot generate reference vectors in Modes II and III, similar to other modulation methods. Also, by employing proposed modulation scheme switching frequency is drastically reduced, which represents itself in efficiency of the converter. These two great features are explained in details in Section V, comparing it with classic modulation. In the following section, we examine the implementation process of this modulation, which has two steps: 1) region identification and 2) duty cycle calculation.

A. Region Identification

Projection of three-phase reference voltages (V_{an}, V_{bn}, and V_{cn}) into the $\alpha-\beta$ plane is a vector called reference voltage vector $\mathbf{V_{ref}}$, defined in (2) and (3)

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \tag{2}$$

$$\begin{aligned}|\mathbf{V_{ref}}| &= \sqrt{V_\alpha^2 + V_\beta^2}\\ \angle\mathbf{V_{ref}} &= \theta = \tan^{-1}(V_\beta/V_\alpha)\end{aligned} \tag{3}$$

where $|\mathbf{V_{ref}}|$ and $\angle\mathbf{V_{ref}}$ represent the magnitude and angle of the reference vector, respectively. The parameter θ_1 is the angle between the transferred reference vector into the sector I and the α-axis and is calculated as follows:

$$\theta_1 = f\mathrm{mod}\left(\theta + \pi, \frac{\pi}{3}\right) \tag{4}$$

where $f\mathrm{mod}(a, b)$ is a function that computes the remainder of the division operation $\frac{a}{b}$.

To identify the region for $\mathbf{V_{ref}}$, it should be projected on the axes of $\frac{\pi}{3}$ coordinate system and its components are calculated in the following equation:

$$\begin{aligned}V_{\mathrm{ref}_{(g)}} &= 2\left(|\mathbf{V_{ref}}|\cos\theta_1 - \frac{|\mathbf{V_{ref}}|}{\sqrt{3}}\sin\theta_1\right)\\ V_{\mathrm{ref}_{(h)}} &= 4\frac{|\mathbf{V_{ref}}|}{\sqrt{3}}\sin\theta_1.\end{aligned} \tag{5}$$

g is in the direction of $\mathbf{V_1}$ and h is in the direction of vector $\mathbf{V_2}$. Looking at Fig. 5, SVM diagram is made up of 9 regions in the form of equilateral triangles, which are divided into two categories: triangles with one side on the ground (upright equilateral triangle) and triangles with one vertex on the ground (inverted equilateral triangle).

If tip of the reference vector is situated within an upright equilateral triangle, such as region 2, defined by vertices A, B, and C, then their coordinates are calculated in the following equation:

$$\begin{aligned}&l_g = \mathrm{floor}(V_{\mathrm{ref}_{(g)}}), l_h = \mathrm{floor}(V_{\mathrm{ref}_{(h)}})\\ &(V_{A_{(g)}}, (V_{A_{(h)}}) = (l_g, l_h)\\ &(V_{B_{(g)}}, (V_{B_{(h)}}) = (l_g + 1, l_h)\\ &(V_{C_{(g)}}, (V_{C_{(h)}}) = (l_g, l_h + 1)\end{aligned} \tag{6}$$

where floor(.) is a lower rounded integer function.

Otherwise, reference vector is located in an inverted equilateral triangle, like region 8, V_A, V_B, and V_C are expressed in the

following equation:

$$(V_{A_{(g)}}, (V_{A_{(h)}}) = (l_g + 1, l_h + 1)$$
$$(V_{B_{(g)}}, (V_{B_{(h)}}) = (l_g + 1, l_h)$$
$$(V_{C_{(g)}}, (V_{C_{(h)}}) = (l_g, l_h + 1). \quad (7)$$

B. Duty Cycle Calculation

$\mathbf{V_{ref}}$ is composed of three nearest vectors, and ON-time duration of these vectors are calculated:

$$\mathbf{V_A}D_A + \mathbf{V_B}D_B + \mathbf{V_C}D_C = \mathbf{V_{ref}}T_s$$
$$D_A + D_B + D_C = 1. \quad (8)$$

After decomposing (8) into two equation of V_g and V_h axis, following equations are deduced:

$$V_{A_{(g)}}D_A + V_{B_{(g)}}D_B + V_{C_{(g)}}D_C = V_{\text{ref}_{(g)}}T_s$$
$$V_{A_{(h)}}D_A + V_{B_{(h)}}D_B + V_{C_{(h)}}D_C = V_{\text{ref}_{(h)}}T_s$$
$$D_A + D_B + D_C = 1. \quad (9)$$

By substituting V_g and V_h axis into $\boldsymbol{V_A}$, $\boldsymbol{V_B}$, and $\boldsymbol{V_C}$, the duty cycles are calculated as

$$D_B = (V_{\text{ref}_{(g)}} - V_{A_{(g)}})$$
$$D_C = (V_{\text{ref}_{(h)}} - V_{A_{(h)}})$$
$$D_A = 1 - (D_B + D_C) \quad (10)$$

for upright equilateral triangles, region 1, 2, 4, 5, 7, 8.

But if $\mathbf{V_{ref}}$ is located in an inverted equilateral triangle like, region 3, 6, and 9, the duty cycles of $\boldsymbol{V_A}$, $\boldsymbol{V_B}$, and V_C are calculated as follows:

$$D_B = (V_{A_{(h)}} - V_{\text{ref}_{(h)}})$$
$$D_C = (V_{A_{(g)}} - V_{\text{ref}_{(g)}})$$
$$D_A = 1 - (D_B + D_C). \quad (11)$$

When initial space vectors for generating $\mathbf{V_{ref}}$ and their duty ratios are determined, it is time to find final space vectors as are provided in Table III. For a reference vector located in region 3, The duty ratios D_1, D_2, and D_M are calculated using (7), because region 3 is an inverted equilateral triangle. Then, the duty ratios of final space vectors, $\mathbf{V_1}$, $\mathbf{V_2}$, $\mathbf{V_3}$, and $\mathbf{V_4}$, are calculated according to Table III

$$D_{V_1} = D_1\ ,\ D_{V_2} = D_2$$
$$D_{V_3} = \frac{D_M}{2}\ ,\ D_{V_4} = \frac{D_M}{2}. \quad (12)$$

It is important to note that the proposed modulation technique can be directly applied to T-type, NPC, and ANPC topologies with minimal modifications. The key steps-such as new vector definitions, redefined space vector regions, and switching sequence design-are independent of the topology. The only difference lies in how the switching states are determined for each topology to generate the required voltage vectors.

TABLE III
DUTY CYCLE CALCULATION OF VECTORS FOR DIFFERENT REGIONS

Region	Initial Space vectors ($\mathbf{V_A}, \mathbf{V_B}, \mathbf{V_C}$)	Space vectors utilized to generate $\mathbf{V_{ref}}$	Duty cycle calculation
1	$\mathbf{V_0}$, $\mathbf{V_1}$, $\mathbf{V_2}$	$\mathbf{V_0}$, $\mathbf{V_1}$, $\mathbf{V_2}$	$D_{V_0} = D_0$ $D_{V_1} = D_1$ $D_{V_2} = D_2$
2	$\mathbf{V_1}$, $\mathbf{V_3}$, $\mathbf{V_M}$	$\mathbf{V_1}$, $\mathbf{V_3}$, $\mathbf{V_4}$	$D_{V_1} = D_1$ $D_{V_3} = D_3 + \frac{D_M}{2}$ $D_{V_4} = \frac{D_M}{2}$
3	$\mathbf{V_1}$, $\mathbf{V_M}$, $\mathbf{V_2}$	$\mathbf{V_1}$, $\mathbf{V_2}$ $\mathbf{V_3}$, $\mathbf{V_4}$	$D_{V_1} = D_1$ $D_{V_2} = D_2$ $D_{V_3} = \frac{D_M}{2}$ $D_{V_3} = \frac{D_M}{2}$
4	$\mathbf{V_2}$, $\mathbf{V_M}$, $\mathbf{V_4}$	$\mathbf{V_2}$, $\mathbf{V_3}$, $\mathbf{V_4}$	$D_{V_2} = D_2$ $D_{V_3} = \frac{D_M}{2}$ $D_{V_4} = D_4 + \frac{D_M}{2}$
5	$\mathbf{V_3}$, $\mathbf{V_5}$, $\mathbf{V_R}$	$\mathbf{V_3}$, $\mathbf{V_5}$, $\mathbf{V_6}$	$D_{V_3} = D_3$ $D_{V_5} = D_5 + \frac{2D_R}{3}$ $D_{V_6} = \frac{D_R}{3}$
6	$\mathbf{V_3}$, $\mathbf{V_R}$, $\mathbf{V_M}$	$\mathbf{V_3}$, $\mathbf{V_4}$ $\mathbf{V_5}$, $\mathbf{V_6}$	$D_{V_3} = D_3 + \frac{D_M}{2}$ $D_{V_4} = \frac{D_M}{2}$ $D_{V_5} = \frac{2D_R}{3}$ $D_{V_6} = \frac{D_R}{3}$
7	$\mathbf{V_M}$, $\mathbf{V_R}$, $\mathbf{V_S}$	$\mathbf{V_3}$, $\mathbf{V_4}$ $\mathbf{V_5}$, $\mathbf{V_6}$	$D_{V_3} = \frac{D_M}{2}$ $D_{V_4} = \frac{D_M}{2}$ $D_{V_5} = \frac{2D_R}{3} + \frac{D_S}{3}$ $D_{V_6} = \frac{D_R}{3} + \frac{2D_S}{3}$
8	$\mathbf{V_M}$, $\mathbf{V_S}$, $\mathbf{V_4}$	$\mathbf{V_3}$, $\mathbf{V_4}$ $\mathbf{V_5}$, $\mathbf{V_6}$	$D_{V_3} = \frac{D_M}{2}$ $D_{V_4} = D_4 + \frac{D_M}{2}$ $D_{V_5} = \frac{D_S}{3}$ $D_{V_6} = \frac{2D_S}{3}$
9	$\mathbf{V_4}$, $\mathbf{V_S}$, $\mathbf{V_6}$	$\mathbf{V_4}$, $\mathbf{V_5}$, $\mathbf{V_6}$	$D_{V_4} = D_4$ $D_{V_5} = \frac{D_S}{3}$ $D_{V_6} = D_6 + \frac{2D_S}{3}$

V. COMPARISON

In this section, a detailed comparison is performed among [18], PTCM, and PTPM, examining various parameters, such as switching frequency, conduction and switching losses, efficiency, and thermal performance. These comparisons demonstrate how the proposed topology and modulation scheme improve the overall performance of the HSI. The simulation parameters are listed in Table IV.

A. Losses

1) Conduction Loss: The proposed topology can be compared with the classic topology in terms of conduction loss. One key advantage of the proposed topology is its ability to reduce conduction loss compared to the classic topology. This improvement is particularly pronounced at low modulation indices,

TABLE IV
SIMULATION PARAMETERS FOR PROPOSED HSI

Parameter name		Value
Input voltages	V_{DC_1}	400 V
	V_{DC_2}	$\frac{400}{3}$ V
Output Voltage	Frequency	60 Hz
	Power Factor	0.9
Load	Resistor	0.52 Ω
	Inductor	0.78 mH
IGBT	Model	SKM400GB066D
	Voltage rating	600 V
	Current rating	600 A
Diode	Model	ISL9R3060G2
	Voltage rating	600 V
	Current rating	600 A
Sampling frequency		20 kHz
Case temperature		100 °C

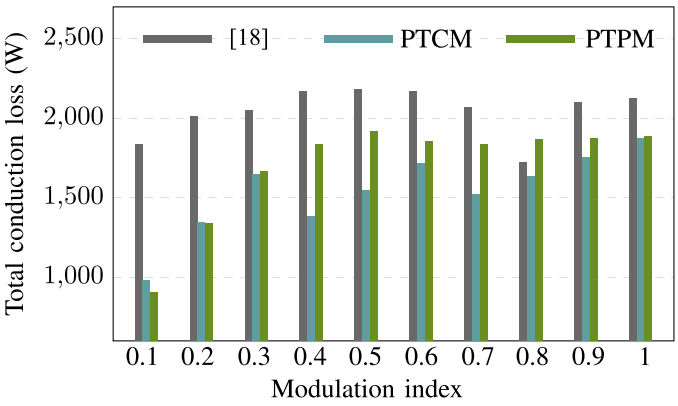


Fig. 6. Comparison of total conduction losses between the topology in [18], the PTCM, and the PTPM scheme.

where all phase currents flow through the front switches and only two switches are employed per phase. In other words, although the conduction loss in the front switches remains relatively high, the reduced total number of IGBTs leads to lower overall conduction loss.

In Fig. 6, a clear disparity is shown in Mode I at $M = 0.2$. The conduction loss in the classic modulation is approximately 1850 W, whereas the proposed topology (both with and without the proposed modulation) remains near 900 W. A similar trend appears in Mode II, where the classic topology wastes more than 2100 W in IGBT conduction loss. However, when the proposed modulation is applied to the proposed topology, the conduction loss exceeds that of the proposed topology under classic modulation.

In Mode III, the conduction loss in the classic topology increases with the modulation index, reaching 2100 W. In contrast, PTCM and PTPM maintain relatively consistent losses below 1800 W.

In summary, the proposed topology exhibits significantly better performance across all modes compared to the classic

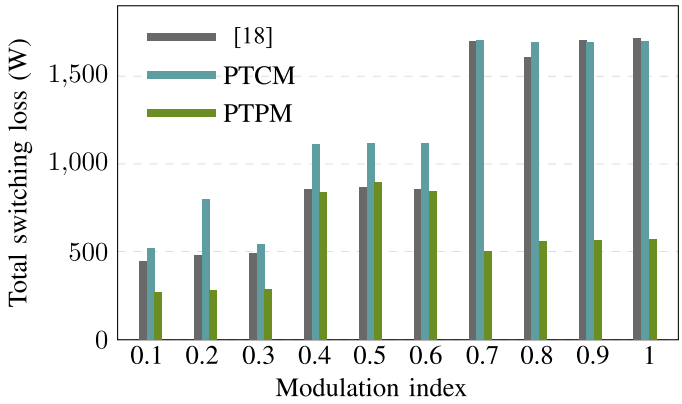


Fig. 7. Comparison of total switching losses between the topology in [18], the PTCM, and the PTPM scheme.

structure in terms of conduction losses. However, when the proposed modulation is applied to the proposed topology, conduction losses in the switches increase. This tradeoff is justified by the substantial reduction in switching losses, underscoring the superiority of the proposed modulation.

2) Switching Loss: Great advantage of applying proposed modulation is reducing switching frequency of leg switches (S_{1_x} and S_{2_x}); Therefore, if proposed modulation is applied on proposed topology, switching loss is reduced considerably across the entire range of modulation index, more notable in Mode III where new regions are defined in SVM diagram.

In Fig. 7, switching loss in [18] continues fairly unchanged in Modes I, II, and III, around 480 W, 860 W, and 2000 W, respectively. This switching loss is always greater in PTCM than PTPM, while switching loss of front IGBTs is zero in PTCM, and it goes up to 1120 W and 1700 W in Mode II and III. In PTPM, switching loss of front IGBTs (T_1, T_2, T_3, T_4) is not negligible as they turned-ON and OFF with sampling frequency, but switching loss of S_{1_x} and S_{2_x} is dropped significantly, which results in low switching loss compared to PTCM. In Fig. 7 for proposed topology with proposed modulation, switching loss in Mode III is halved compared to Mode II.

B. Switching Frequency

When evaluating switching frequency, two important factors must be evaluated: 1) the average switching frequency 2) the distribution of switching frequency among the switches. Table V compares the switching frequency of switches and its distribution in the classic and proposed modulation techniques when applied on proposed topology across different operating modes. In classic modulation, in each mode switching state of shared switches does not changed. As previously stated and visually depicted in Fig. 4. These transistors remain either ON or OFF, with no change in their switching state. But switching frequency of leg switches is equal to sampling frequency (f_{smp}). It is evident that switching frequency is distributed highly uneven between all the semiconductors in classic modulation, which leads to uneven heat dissipation. Using the proposed modulation method, part of the switching required to generate the output voltage

TABLE V
COMPARISON OF SWITCHING FREQUENCY BETWEEN CLASSIC AND PROPOSED MODULATION APPLIED ON PROPOSED TOPOLOGY

Operating Mode	Switching frequency $f_{S_{1_x}}, f_{S_{2_x}}$ $f_{T_1}, f_{T_2}, f_{T_3}, f_{T_4}$ $x \in \{a, b, c\}$	
	Classic	Proposed
Mode I	f_{smp},f_{smp}	f_{smp},f_{smp}
	0, 0, 0, 0	0, 0, 0, 0
Mode II	f_{smp},f_{smp}	$\frac{1}{3}f_{smp}$,$\frac{1}{3}f_{smp}$
	0, 0, 0, 0	f_{smp}, f_{smp}, f_{smp}, f_{smp}
Mode III	f_{smp},f_{smp}	$\frac{1}{3}f_{smp}$,$\frac{1}{3}f_{smp}$
	0, 0, 0, 0	0, 0, f_{smp}, f_{smp}

f_{smp} : Sampling frequency

TABLE VI
COMPARISON OF EFFICIENCY BETWEEN THE TOPOLOGY IN [18], THE PTCM, AND THE PROPOSED TOPOLOGY WITH THE NEW MODULATION SCHEME, PTPM

Mode	M	Efficiency (%)		
		[18]	PTCM	PTPM
I	0.1	83.3	93.0	94.8
	0.2	90.9	94.1	95.1
	0.3	93.77	94.7	95.3
II	0.4	94.5	96.3	95.1
	0.5	95.6	96.5	95.9
	0.6	96.3	96.7	96.7
III	0.7	96.1	97.1	97.5
	0.8	96.9	97.2	97.7
	0.9	96.9	97.3	97.9
	1.0	97.2	97.3	98.2

is transferred to the shared switches, reducing the switching frequency of the switches in each leg. For example, in Mode II, the switching frequency of switches S_{1x} and S_{2x} will be one-third of the sampling frequency, while switches T_1, T_2, T_3, and T_4 are now turned-ON and OFF. The same pattern is observed in Mode III, significantly reducing the switching losses in the proposed modulation method. In this mode, T_3, T_4 are switched with sampling frequency while T_1 and T_2 are always ON and OFF, respectively.

C. Efficiency

Total losses in the classic topology, PTCM, and PTPM are reflected in their respective efficiencies, as shown in Table VI.

In Mode I, the efficiency difference between the classic method and the proposed methods is particularly significant. For example, at $M = 0.2$, the efficiencies are 90.9%, 94.1%, and 95.1% for the classic topology, PTCM, and PTPM, respectively. This trend continues in Mode II, where the proposed methods maintain higher efficiencies compared to the classic method. Similarly, in Mode III, the PTPM method achieves an efficiency of 98.2% at full load, demonstrating its superior performance.

D. Junction Temperature Profiles

The proposed topology outperforms the classic topology in several aspects, most notably through reduced conduction loss. This improvement is evident in both the system efficiency and IGBT temperatures. However, directly comparing IGBT temperatures between the classic and proposed topologies is neither rational nor fair due to their differing semiconductor counts (18 versus 10, respectively). In addition, the absence of diodes in the proposed topology makes any comparison inherently biased in its favor. Therefore, this section focuses on comparing the IGBT junction temperatures within the proposed topology itself, both with and without the proposed modulation scheme.

Since the summation of all phase currents flows through the shared switches based on the Mode function, the junction temperatures of T_1, T_2, T_3, and T_4 are expected to be higher than those of the leg switches, both with and without the proposed modulation. By applying the proposed modulation, the junction temperature of the shared switches increases, but that of S_{1_x} and S_{2_x} is significantly reduced. As these switches exist in each phase, the proposed modulation leads to better efficiency and thermal performance.

To obtain thermal results in Fig. 8, the power losses from the simulation are fed into a thermal model to estimate the junction temperature T_j of each power device. In this analysis, the case temperature T_C is set to 100 °C. The thermal model used is based on a widely accepted Foster RC network, which models the transient thermal impedance of the device [36]. This model effectively calculates temperature variations during dynamic switching events in PSIM software.

In Mode I, both modulations perform very similar. For $M = 0.2$, in Table VII, thermal junction temperature of T_2 and T_3 in both modulations is around 125 °C and 130 °C, respectively, and does not fluctuates considerably as they are always on in this mode. Conversely, T_1 and T_4 are always kept turned-OFF in Mode I. Therefore, their junction temperature is equal to case temperature. The temperature profiles of switches S_{1_x} and S_{2_x} are very similar in both modulation methods. Both switches exhibit average temperatures of 125 °C and 130 °C, respectively, with a peak-to-peak temperature variation of approximately 7 °C. As it was expected, since reference vector is located in region 1in both modulation schemes, no distinguished difference can be observed in the switches thermal profile. The simulated temperatures of these switches are shown in Fig. 8(a) and (d) for the classic and proposed modulations, respectively.

In Mode II, maximum temperature between shared IGBTs in classic modulation is 131.4 °C, and peak temperature of S_{1_x} and S_{2_x} is 146 °C with an average value of 141 °C. However, in the proposed method, the thermal distribution among the shared switches is more uniform, and junction temperature of S_{1_x} and S_{2_x} are much less than classic modulation, settling at 124.4 °C. Note that S_{1_x} and S_{2_x} represent six switches across the three phases of the inverter, and their reduced temperatures are significantly more critical compared to switches T_1, T_2, T_3, T_4. As shown in Fig. 8(b), the shared switches maintain a constant temperature. However, since the shared switches are periodically

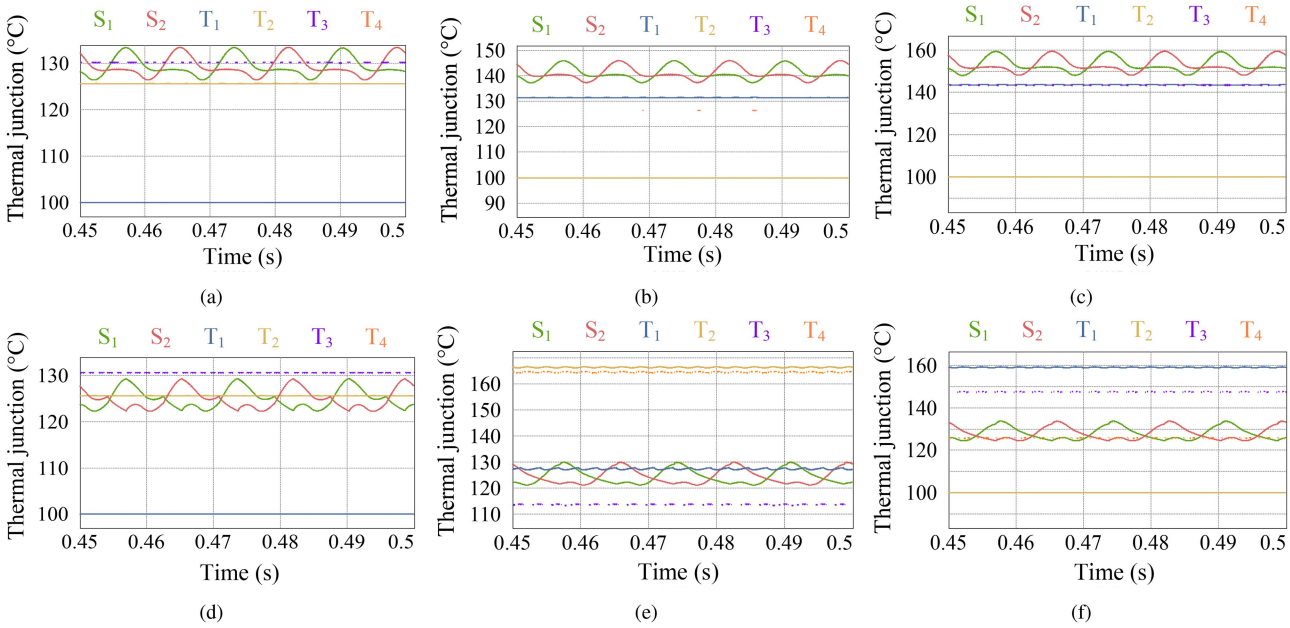


Fig. 8. Simulated thermal junction temperature of switches using (a) classic modulation-$M = 0.2$, (b) classic modulation-$M = 0.4$, (c) classic modulation-$M = 1$ and (d) proposed modulation-$M = 0.2$, (e) proposed modulation-$M = 0.4$, and (f) proposed modulation-$M = 1$.

turned-ON and OFF, a small fluctuation can be observed in their waveform [see Fig. 8(e)].

For $M = 1$, in Mode III, proposed modulation performs significantly better. Junction temperature of T_1 and T_4 increases only 13 °C and 48 °C, but that of T_3 drops from 143.6 °C to 126.5 °C. Also, for S_{1_x} and S_{2_x}, junction temperatures decline from 159.6 °C to 134.1 °C. The thermal junction temperature for shared switches are presented in Fig. 8(c) and (f). It is noteworthy to mention again that S_{1_x} and S_{2_x} represent 6 switches, since each has a phase consisting of two, and their junction temperature drop holds greater significance compared to shared switches.

E. Total Harmonic Distortion

Different types of topologies has no effect on the output voltage THD. In this way both classic modulation and PTCM perform similarly, as illustrated in Table VIII for different modulation indices. In Mode I, [18], PTCM and PTPM perform the same and their line voltage THD increases as modulation index increases. Moving from $M = 0.3$ to $M = 0.4$ For PTCM, line voltage THD jumps from 67.7% to 110%, however, PTPM performs considerably better with a drop of 7% from 67.7% to 60%. In Mode II, as modulation index grows, THD is expected to decrease because reference vector gets closer to primary active vectors, however proposed modulation outperforms classic modulation. Moving to Mode III, a big jump happens for classic modulation from 66.27% to 92.6%, but for proposed modulation reported line voltage THD decreases from 55.7% to 49% and continues fairly unchanged around 50%. Overall, with employing proposed modulation great enhancement is observable in inverter's performance as maximum line voltage in PTCM reaches peak of 110%, but that of PTPM does not exceed 67.7%.

It is worth mentioning that we set $V_{\mathrm{DC}_1} = 400$ and $V_{\mathrm{DC}_2} = \frac{400}{3}$ here, and the SVM diagram plane is symmetrical. In an asymmetrical plane, the THD values in all modes may vary but still outperform those of classic modulation. Generally, smaller regions result in lower THD.

VI. Simulation Results

This section presents simulation results of the HSI using both classic and proposed modulation techniques. The simulations were conducted in the PSIM software. The simulated system is evaluated at three modulation indices, each corresponding to a different mode of operation.

Fig. 9 presents the simulation waveforms in Mode I ($M = 0.2$) including phase-to-neutral voltages, line-to-line voltages, and load currents. The associated results of the classic and the proposed modulations are in Fig. 9(a) and (b), respectively. In both cases, the phase voltages exhibit two levels, whereas the line-to-line voltages demonstrate three levels. Both modulation techniques utilize only the voltage source V_{DC_1} in Mode I and the dc-link voltage is equal to V_{DC_1} and kept constant. As it is seen, line-to-line voltage are exactly the same and none of the modulation techniques stands out as superior in Mode I.

Fig. 10 shows the simulated waveforms when modulation index is increased to 0.4. In the classic modulation method [see Fig. 10(a)], the dc-link voltage is fixed at $V_{\mathrm{DC}_1} - V_{\mathrm{DC}_2}$, and the phase voltage exhibits only two levels. Consequently, the line-to-line voltage displays three distinct levels. In contrast, the proposed modulation technique [see Fig. 10(b)] adjusts the

TABLE VII
COMPARISON BETWEEN JUNCTION TEMPERATURE OF SWITCHES IN PTCM, AND PROPOSED TOPOLOGY WITH PROPOSED MODULATION, PTPM

M	Modulation	Switch	Junction temperature		
			Maximum	Average	Peak-peak
0.2 - Mode I	Classic	T_1	100	100	0
		T_2	125.6	125.6	0
		T_3	130.3	130.3	0
		T_4	100	100	0
		S_{1_x}	133.5	129.4	7.3
		S_{2_x}	133.5	129.4	7.3
	Proposed	T_1	100	100	0
		T_2	125.6	125.6	0
		T_3	130.6	130.6	0
		T_4	100	100	0
		S_{1_x}	129.4	124.9	7
		S_{2_x}	129.4	124.9	7
0.4 - Mode II	Classic	T_1	131.4	131.4	0
		T_2	100	100	0
		T_3	100	100	0
		T_4	126.4	126.4	0
		S_{1_x}	146	141	9
		S_{2_x}	146	141	9
	Proposed	T_1	127.7	127.3	1
		T_2	166.8	166.4	1
		T_3	114.3	113.6	1
		T_4	165.3	164.6	1
		S_{1_x}	130.1	124.4	8.6
		S_{2_x}	130.1	124.4	8.6
1- Mode III	Classic	T_1	143.6	143.6	0
		T_2	100	100	0
		T_3	143.6	143.6	0
		T_4	100	100	0
		S_{1_x}	159.6	152.9	11.8
		S_{2_x}	159.6	152.9	11.8
	Proposed	T_1	159.7	159.2	1
		T_2	100	100	0
		T_3	148.1	147.6	1
		T_4	126.5	126	1
		S_{1_x}	134.1	128	9.8
		S_{2_x}	134.1	128	9.8

Case temperature = 100 °C

dc-link voltage based on the selected vectors, resulting in a waveform with three and five voltage levels in phase and line-to-line voltages, respectively. In comparison with current waveforms in Mode I, current amplitude increased proportionally with the modulation index, as a constant resistive-inductive load is utilized.

For Mode III (see Fig. 11), waveforms for classic and proposed modulation are presented in Fig. 11(a) and (b), respectively. As explained in previous sections, the dc-link voltage is fixed at V_{DC_1} for mode III in the classic modulation and only V_{DC_1} is connected to the inverter and V_{DC_2} is disconnected. In this way, phase voltage can have only two values in classic modulation; however, in proposed modulation, waveforms have three voltage values, resulting in better THD. The same pattern can be seen for line-to-line voltages having five level.

TABLE VIII
COMPARISON BETWEEN RESULTED THD IN PHASE VOLTAGE AND LINE VOLTAGE USING TOPOLOGY IN [18], PTCM AND PROPOSED MODULATION (PTPM)

Mode	M	Phase voltage THD (%)			Line voltage THD (%)		
		[18]	PTCM	PTPM	[18]	PTCM	PTPM
I	0.1	28.8	28.8	28.8	21.2	21.2	21.2
	0.2	16	16	16	11.4	11.4	11.4
	0.3	92.2	92.2	92.2	67.7	67.7	67.7
II	0.4	152	152	84	110	110	60
	0.5	118.2	118.2	83.2	86	86	61.7
	0.6	90.4	90.4	66.3	66.2	66.27	55.7
III	0.7	127.2	127.2	68.6	92.6	92.6	49
	0.8	105.2	105.2	72	78.4	78.4	51.9
	0.9	93.6	93.6	72	65	65	51.5
	1.0	71.8	71.8	65.3	53.2	53.2	48.5

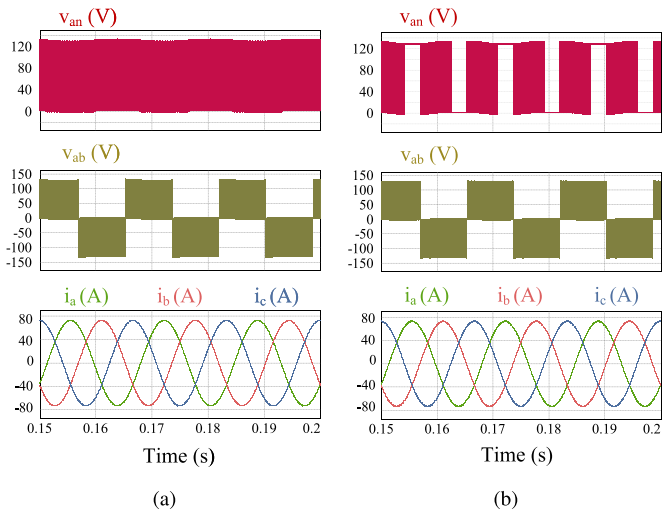


Fig. 9. Simulation waveforms of HSI for $M = 0.2$ with (a) classic modulation and (b) proposed modulation.

VII. EXPERIMENTAL RESULTS

Experimental tests were performed on a low-power prototype of HSI using the proposed modulation technique. The experimental setup, as shown in Fig. 12, was used to measure the performance of the system under different modulation indices to evaluate its practicality. The parameters of the converter are given in Table IX. A digital signal processor is utilized to execute

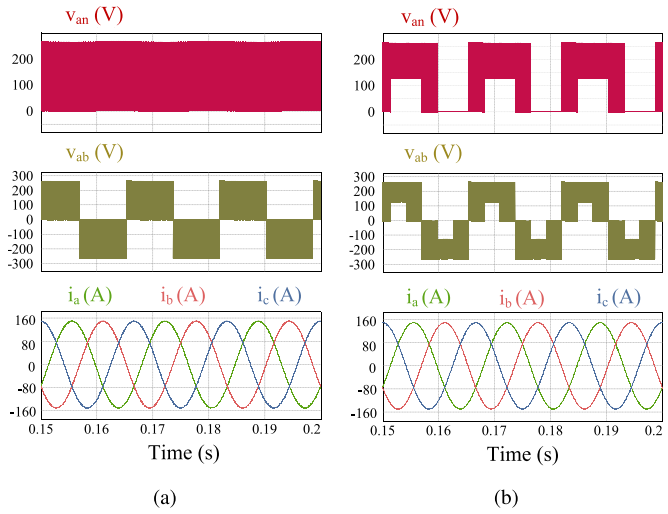


Fig. 10. Simulation waveforms of HSI for $M = 0.4$ with (a) classic modulation and (b) proposed modulation.

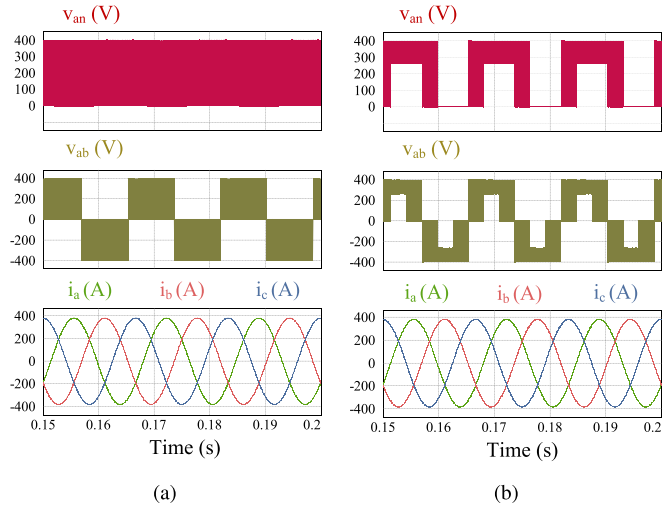


Fig. 11. Simulation waveforms of HSI for $M = 1$ with (a) classic modulation and (b) proposed modulation.

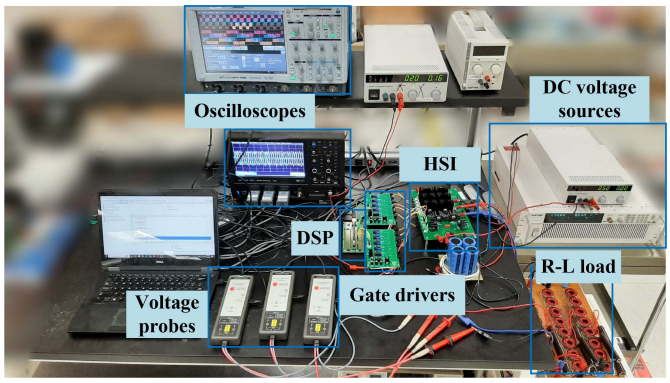


Fig. 12. Experimental scaled-down laboratory setup for the proposed topology and modulation scheme.

TABLE IX
EXPERIMENTAL PARAMETERS FOR PROPOSED HSI

System parameter	Value
Switching devices	MOSFET IRF740
Current and voltage ratings of switches	10 A, 400 V
DC source voltage (V_{DC_1})	225 V
DC source voltage (V_{DC_2})	75 V
DSP	TMS320F28335
Sampling frequency	10 kHz
Output voltage frequency	60 Hz
Load-Resistive, Inductive (R_L, L_L)	25 Ω, 30 mH

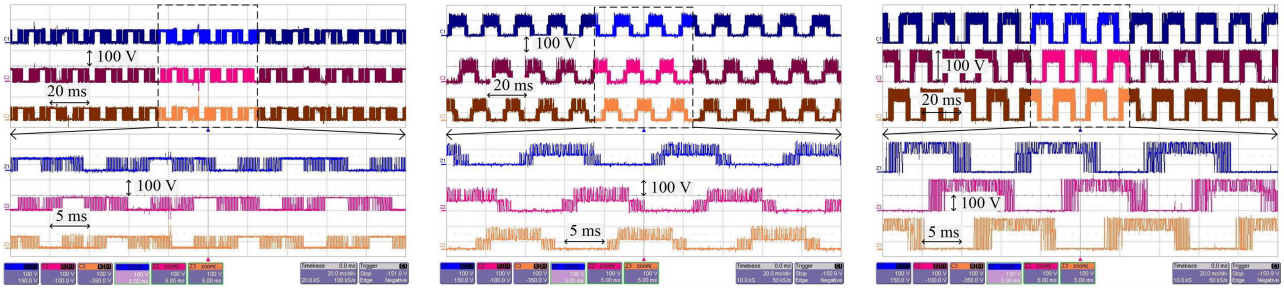
the proposed modulation scheme and generate switches' gate signals. The amplitude of the input dc voltages are 225 V and 75 V, because this served only as a proof-of-concept demonstration.

The experimental results at different modulation indexes are shown in Figs. 13–16, and each of these figures is divided into four parts, representing the phase voltages, line-to-line voltages, load currents, and the fast Fourier transform (FFT) applied to the line-to-line voltages.

Figs. 13(a), 14(a), 15(a), and 16(a) show the measured waveforms when the modulation index is set to 0.2. As shown in Fig. 13(a), the phase-to-neutral voltage waveforms exhibit two levels with a peak-to-peak amplitude of V_{DC_1}. Also, the bottom of the figure provides a zoomed-in view of the waveforms. In Fig. 14(a), the line-to-line voltage has a peak-to-peak value of 150 V ($2V_{\mathrm{DC}_1}$) at fundamental frequency of 60 Hz. As the load is balanced, the phase currents in Fig. 16(a) have the same peak-to-peak value of 3 A and phase shifted 120°. Applying the FFT to the line voltages in Fig. 15(a) reveals that the first harmonic band appears at the sampling frequency, and the next sideband harmonics of the output voltage is at 20 kHz. Since the converter operates in Mode I, the proposed modulation does not show considerable differences compared to the classic modulation.

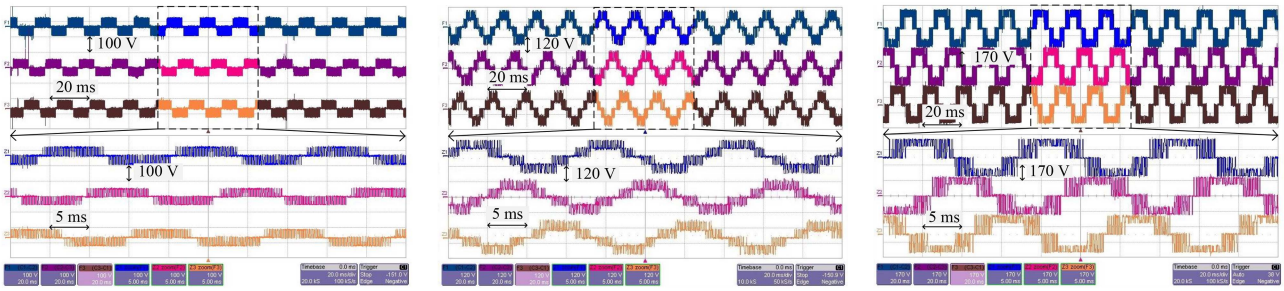
Experimental measured waveforms in Mode II are presented in Figs. 13(b), 14(b), 15(b), and 16(b) when modulation index is equal to 0.45. The phase-to-neutral voltage waveforms exhibit three levels equal to 0 V, 75 V, and 150 V (V_{DC_2}, V_{DC_1}–V_{DC_2}). Also, in line-to-line voltage five different voltage levels can be seen as expected in Fig. 14(b). With a zoomed-in part in Fig. 16(b), three phase currents are symmetrical and balanced, and in Fig. 15(b), the sideband harmonics of the line voltages are centered around the sampling frequency of 10 kHz and its multiplications.

The performance of the proposed topology and modulation scheme for $M = 0.95$ is evaluated in Figs. 13(c), 14(c), 15(c), and 16(c). By employing both V_{DC_1} and V_{DC_2}, phase voltage has three voltage levels of 0, $V_{\mathrm{DC}_1} - V_{\mathrm{DC}_2}$, and V_{DC_1}, in Fig. 13(c). Consequently, line-to-line voltage has five voltage levels and shows great enhancement over classic modulation in terms of THD, switching and conduction loss [see Fig. 14(c)]. Looking



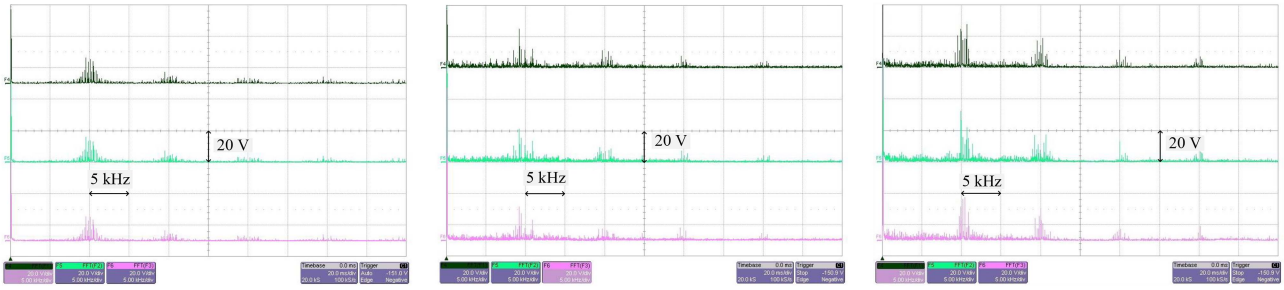
(a) (b) (c)

Fig. 13. Experimental results of phase-to-neutral voltages of the HSI with proposed modulation in (a) Mode I ($M = 0.2$), (b) Mode II ($M = 0.45$), and (c) Mode III ($M = 0.95$).



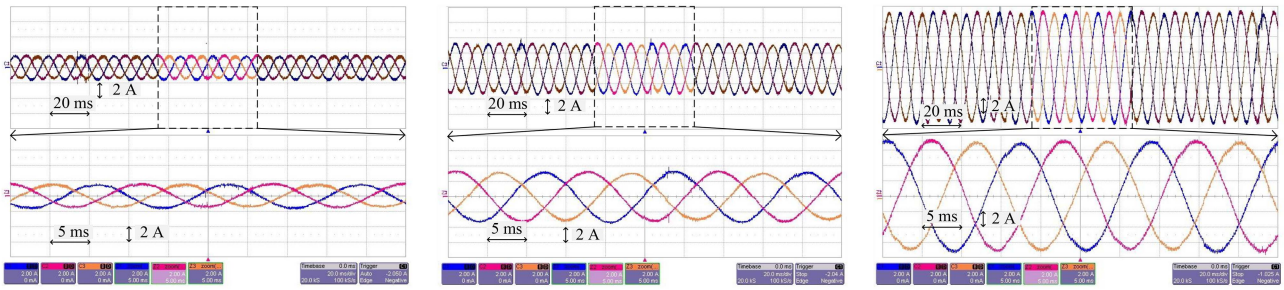
(a) (b) (c)

Fig. 14. Experimental results of line-to-line voltages of the HSI with proposed modulation in (a) Mode I ($M = 0.2$), (b) Mode II ($M = 0.45$), and (c) Mode III ($M = 0.95$).



(a) (b) (c)

Fig. 15. Experimental results of line voltages FFT of the HSI with proposed modulation in (a) Mode I ($M = 0.2$), (b) Mode II ($M = 0.45$), and (c) Mode III ($M = 0.95$).



(a) (b) (c)

Fig. 16. Experimental results of phase currents of the HSI with proposed modulation in (a) Mode I ($M = 0.2$), (b) Mode II ($M = 0.45$), and (c) Mode III ($M = 0.95$).

at Fig. 16(c), phase current are well balanced and symmetrical with a peak-to-peak value of 14.4 A.

Overall, the proposed modulation in modes II and III utilizes more voltage levels, resulting in an improved THD profile as observed in the FFT spectrum. As expected, the experimental and simulation results validate and complement each other, demonstrating complete consistency.

VIII. Conclusion

In this article, a new topology is introduced for HSIs with a better performance in different aspects. The main feature of the proposed structure is reduced semiconductor devices, which results in significant decrease in conduction loss and therefore great improvement in efficiency. The proposed topology employs only 10 semiconductor devices, which is nearly half the number required by conventional topologies, making it significantly more cost-efficient. In addition, the proposed solution is compared to classic topology in terms of junction temperature of IGBTs and proposed represented better thermal distribution. Moreover, this article introduces an enhanced modulation technique utilizing reconstructed vectors, which significantly improves THD, reduces the switching frequency of IGBTs, and enhances the overall efficiency of the inverter. To validate functionality of proposed topology and modulation scheme, simulation tests are performed and results show the effectiveness of the proposed solutions. Finally, a scaled-down laboratory prototype of the HSI is designed and tested in the laboratory to verify operation of the proposed HSI topology and modulation technique.

References

[1] J. Reimers, L. Dorn-Gomba, C. Mak, and A. Emadi, "Automotive traction inverters: Current status and future trends," *IEEE Trans. Veh. Technol.*, vol. 68, no. 4, pp. 3337–3350, Apr. 2019.

[2] S. J. Rind, Y. Ren, Y. Hu, J. Wang, and L. Jiang, "Configurations and control of traction motors for electric vehicles: A review," *Chin. J. Elect. Eng.*, vol. 3, no. 3, pp. 1–17, 2017.

[3] Z. Amjadi and S. S. Williamson, "Power-electronics-based solutions for plug-in hybrid electric vehicle energy storage and management systems," *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 608–616, Feb. 2010.

[4] U. Drive, "Electrical and electronics technical team roadmap," *Partnership Plan, Roadmaps, Other Documents*, 2017.

[5] J. O. Estima and A. J. M. Cardoso, "Efficiency analysis of drive train topologies applied to electric/hybrid vehicles," *IEEE Trans. Veh. Technol.*, vol. 61, no. 3, pp. 1021–1031, Mar. 2012.

[6] Z. Huang, D. Zhou, L. Wang, Z. Shen, and Y. Li, "A review of single-stage multiport inverters for multisource applications," *IEEE Trans. Power Electron.*, vol. 38, no. 5, pp. 6566–6584, May 2023.

[7] W. Deng, Y. Zhao, and J. Wu, "Energy efficiency improvement via bus voltage control of inverter for electric vehicles," *IEEE Trans. Veh. Technol.*, vol. 66, no. 2, pp. 1063–1073, Feb. 2017.

[8] S. Verma et al., "A comprehensive review on energy storage in hybrid electric vehicle," *J. Traffic Transp. Eng. (English Edition)*, vol. 8, no. 5, pp. 621–637, 2021.

[9] M. Ehsani, K. V. Singh, H. O. Bansal, and R. T. Mehrjardi, "State of the art and trends in electric and hybrid electric vehicles," *Proc. IEEE*, vol. 109, no. 6, pp. 967–984, Jun. 2021.

[10] L. Dorn-Gomba, P. Magne, B. Danen, and A. Emadi, "On the concept of the multi-source inverter for hybrid electric vehicle powertrains," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7376–7386, Sep. 2018.

[11] J. Cao and A. Emadi, "A new battery/ultracapacitor hybrid energy storage system for electric, hybrid, and plug-in hybrid electric vehicles," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 122–132, Jan. 2012.

[12] B. K. Bose, "Global energy scenario and impact of power electronics in 21st century," *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2638–2651, Jul. 2013.

[13] S. Hajiaghasi, A. Salemnia, and M. Hamzeh, "Hybrid energy storage system for microgrids applications: A review," *J. Energy Storage*, vol. 21, pp. 543–570, 2019.

[14] E. Chemali, M. Preindl, P. Malysz, and A. Emadi, "Electrochemical and electrostatic energy storage and management systems for electric drive vehicles: State-of-the-art review and future trends," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 1117–1134, Sep. 2016.

[15] P. Bhattacharyya, S. Ghorai, S. Sen, and S. K. Giri, "A flexible non-isolated multiport converter to integrate battery and ultracapacitor for electric vehicle applications," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 70, no. 3, pp. 1044–1048, Mar. 2023.

[16] H. Rezaei, S. E. Abdollahi, S. Abdollahi, and S. Filizadeh, "Energy management strategies of battery-ultracapacitor hybrid storage systems for electric vehicles: Review, challenges, and future trends," *J. Energy Storage*, vol. 53, 2022, Art. no. 105045.

[17] J. Sun, B. Luo, and H. Li, "A review on the conventional capacitors, supercapacitors, and emerging hybrid ion capacitors: Past, present, and future," *Adv. Energy Sustainability Res.*, vol. 3, no. 6, 2022, Art. no. 2100191.

[18] L. Dorn-Gomba, J. Guo, and A. Emadi, "Multi-source inverter for power-split hybrid electric powertrains," *IEEE Trans. Veh. Technol.*, vol. 68, no. 7, pp. 6481–6494, Jul. 2019.

[19] J. Ebrahimi, O. Salari, S. Eren, K. Hashtrudi-Zaad, A. Bakhshai, and P. Jain, "Efficiency improved multi-source inverter for hybrid energy storage systems in electric vehicle application," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1982–1997, Feb. 2022.

[20] J. Ebrahimi and S. Eren, "A multi-source DC/AC converter for integrated hybrid energy storage systems," *IEEE Trans. Energy Convers.*, vol. 37, no. 4, pp. 2298–2309, Dec. 2022.

[21] A. Akbari, J. Ebrahimi, and A. Bakhshai, "Single- and multiswitch fault-tolerant inverter topology with preserved output power and extreme learning machine fault detector," *IEEE Trans. Power Electron.*, vol. 39, no. 10, pp. 13177–13198, Oct. 2024.

[22] J. Ebrahimi, A. Akbari, S. Eren, and A. Bakhshai, "A single-phase seven-level nested switched-capacitor converter with enhancing lifetime and reducing size of flying capacitors," *IEEE Trans. Power Electron.*, vol. 40, no. 7, pp. 9234–9248, Jul. 2025.

[23] J. Ebrahimi, S. Shahnooshi, S. Eren, and A. Bakhshai, "A modulation scheme based on virtual voltage levels for capacitor voltage balancing of the four-level diode clamped converter," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 4727–4744, Apr. 2023.

[24] J. Ebrahimi, S. Shahnooshi, S. Eren, H. Karshenas, and A. Bakhshai, "Optimized switching frequency voltage balancing schemes for flying capacitor based multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 70, no. 11, pp. 10775–10788, Nov. 2023.

[25] P. Zhang et al., "A carrier-based discontinuous PWM method for a five-level flying capacitor rectifier with unbalanced DC-link voltages," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 10384–10398, Sep. 2022.

[26] J. Wang, H. Wu, T. Yang, L. Zhang, and Y. Xing, "Bidirectional three-phase DC–AC converter with embedded dc–dc converter and carrier-based PWM strategy for wide voltage range applications," *IEEE Trans. Ind. Electron.*, vol. 66, no. 6, pp. 4144–4155, Jun. 2019.

[27] P. Zhang et al., "A zero-sequence component injection PWM scheme for three-level neutral point clamped rectifiers with unbalanced DC-link voltages," *IEEE Trans. Ind. Electron.* vol. 71, no. 6, pp. 5420–5430, Jun. 2024.

[28] C. Qin and X. Li, "Improved virtual space vector modulation scheme for the reduced switch count three-level inverter with balanced and unbalanced neutral-point voltage conditions," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 2092–2104, Feb. 2023.

[29] Q. Yan, L. Xiao, H. Chen, X. Yuan, H. Xu, and R. Zhao, "An analytical discontinuous space-vector PWM for three-level inverters with unbalanced DC-link voltages," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 7718–7728, Jul. 2022.

[30] L. Liu, D. Zhou, J. Zou, and W. Wang, "Decoupled modeling and wide-range power distribution strategy for the multisource inverter in microgrids," *IEEE Trans. Power Electron.*, vol. 38, no. 10, pp. 12078–12090, Oct. 2024.

[31] L. Liu, D. Zhou, J. Zou, Z. Shen, and X. Fu, "Direct duty cycle control-based power allocation strategy for single-stage multiport inverter in islanded microgrid," *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 14956–14967, Dec. 2023.

[32] D. Zhou, J. Wang, N. Hou, Y. Li, and J. Zou, "Dual-port inverters with internal DC–DC conversion for adjustable DC-link voltage operation of electric vehicles," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6917–6928, Jun. 2021.
[33] J. Ebrahimi, H. Karshenas, S. Eren, and A. Bakhshai, "A fast-decoupled space vector modulation scheme for flying capacitor-based multilevel converters," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 14539–14549, Dec. 2021.
[34] J. Ebrahimi and H. Karshenas, "A new modulation scheme for a four-level single flying capacitor converter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 3, pp. 1860–1870, Mar. 2021.
[35] H. Wen, W. Xiao, X. Wen, and P. Armstrong, "Analysis and evaluation of DC-link capacitors for high-power-density electric vehicle drive systems," *IEEE Trans. Veh. Technol.*, vol. 61, no. 7, pp. 2950–2964, Sep. 2012.
[36] C. Zhan, L. Zhu, W. Wang, Y. Zhang, S. Ji, and F. Iannuzzo, "Multidimensional mission-profile-based lifetime estimation approach for IGBT modules in MMC–HVDC application considering bidirectional power transfer," *IEEE Trans. Ind. Electron.*, vol. 70, no. 7, pp. 7290–7300, Jul. 2023.

Javad Ebrahimi (Senior Member, IEEE) received the Ph.D. degree in power electronics from the Isfahan University of Technology, Isfahan, Iran, in 2017.

From 2017 to 2019, he was an R&D Director with Behrad Consulting Engineers Company, Isfahan, Iran, where he collaborated with utilities and industries and was actively engaged in research on power electronics and power systems. From 2019 to 2023, he was a Postdoctoral Fellow with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada. Since 2023, he has been a Principal Research Associate with Queen's University. His research interests include topology design, modulation, and control of power electronic converters, multilevel converters, electric vehicles, and the application of power electronics in power systems.

Hosein Ghojavand (Student Member, IEEE) was born in Isfahan, Iran, in 1998. He received the B.Sc. degree in electrical engineering in 2020 and the M.Sc. degree in power electronics in 2023 from the Isfahan University of Technology, Isfahan, Iran. He is currently working toward the Ph.D. degree in electrical engineering, with a focus on topology designs and advanced modulation techniques for multisource inverters, with Queen's University, Kingston, ON, Canada.

His master's research focused on dc–dc converters, high-step-down applications, and gate-drive techniques.

Suzan Eren (Senior Member, IEEE) received the B.Sc. (with first-class Hons.), M.Sc., and Ph.D. degrees in electrical engineering from Queen's University, Kingston, ON, Canada, in 2006, 2008, and 2013, respectively.

She is currently an Assistant Professor with the Department of Electrical and Computer Engineering, Queen's University, and a Member of the Centre for Energy and Power Electronics Research (ePOWER). Her industrial experience includes collaboration with SPARQ Systems in developing their highly efficient solar microinverter. She is the author of 70 peer-reviewed papers, and the holder of 14 issued and pending U.S. patents. Her research interests include the application of power electronics to micro-grids, renewable energy, electric vehicles, and energy storage.

Dr. Eren was an Associate Editor for IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN INDUSTRIAL ELECTRONICS and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. She is the Kingston Section Chair of the Institute of Electrical and Electronics Engineers (IEEE), and Co-Founder of IEEE Women in Engineering (WIE) Affinity Group, Kingston.