A High Efficiency Hybrid Modular Multilevel Converter With a SiC Device-Based External Shaping Module

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***Abstract*—In order to improve the waveform quality and efficiency of medium voltage modular multilevel converter (MMC), a hybrid MMC (HMMC) topology with an external shaping module is proposed. Each arm of the HMMC consists of N half-bridge submodules (HSMs) based on Si insulated gate bipolar transistor (IGBT), while a full-bridge submodule (FSM) based on silicon carbide (SiC) MOSFET on the ac side. Furthermore, a $2N+1$ level hybrid modulation strategy is proposed for this topology. The HSMs operate in the low-frequency state to output the staircase wave voltage, while the FSM operates in the high-frequency state to reduce the harmonics of the output voltage. It makes full use of the advantages of low ON-state loss of Si devices and low switching loss of SiC devices. Additionally, the energy fluctuation of the HMMC submodules is analyzed in detail, and a voltage balancing scheme is proposed. In the end, the feasibility and effectiveness of the proposed topology and modulation method are validated by simulation and experimental studies on a single-phase HMMC. Moreover, the comparison of cost and loss between HMMC and existing MMCs proves that the proposed HMMC can better balance the device cost and operating loss.**

***Index Terms*—Efficiency optimization, hybrid modular multilevel converter (MMC), hybrid modulation, Si IGBT, SiC MOSFET, voltage balancing.**

I. Introduction

MODULAR multilevel converters (MMCs), with advantages such as high modularity and reliability, are widely applied in medium voltage (MV) or high voltage scenarios, such as dc transmission, offshore renewable energy integration, solid-state transformer, and motor drives [1], [2], [3]. However, in MV applications, due to the limited number of MMC submodules, improving the waveform quality will result in high switching losses, especially in areas with demand for high equivalent switching frequency [4], [5], [6]. Therefore, in order to minimize the operating loss of MV MMC while optimizing the output waveform quality, the current research focuses on improving the performance of MV MMC by optimizing the modulation scheme and integrating wide bandgap semiconductor devices.

In terms of modulation methods for MMC, carrier phase-shifted pulsewidth modulation (CPS-PWM) and nearest level modulation (NLM) stand out as widely adopted methods [7], [8], [9]. The application of the CPS-PWM method can effectively reduce the output low-order harmonic content in MV MMC. However, the CPS-PWM requires complex voltage balancing control and circulating current suppression algorithm, resulting in a high device switching frequency and considerable operational losses [10]. The NLM is characterized by its simplicity in operation and low switching frequency. However, in the case of a small number of submodules, the step approximation error generated by NLM cannot be ignored, resulting in poor output waveform quality [11]. In order to improve the performance of the NLM method in MV MMC, a new rounding function is proposed in [12] and [13], which increases the level number of output voltage from $N+1$ to $2N+1$, thereby reducing the voltage harmonics in MMC. In comparison to CPS-PWM, there is a significant low-order harmonic content in the above improved NLM due to the lack of modulation accuracy. Therefore, the nearest level PWM (NL-PWM) method is proposed in [10], [14], [15], [16], which redistributes the switching pulse and introduces a high-frequency PWM waveform based on NLM. The hybrid modulation strategy exhibits lower harmonic content than NLM and CPS-PWM. However, some modules execute high-frequency switch actions, posing a challenge to enhance the operational efficiency of the device further, although unnecessary switching actions are avoided to reduce the switching frequency of NL-PWM in [15] and [16].

At present, high switching frequency is a trend for reducing volume and improving waveform quality in MV MMC

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applications [17], [18]. With the widespread wide bandgap semiconductor devices such as SiC MOSFET, the superior switching characteristics of SiC MOSFET can further reduce the operating loss of MMC while maintaining good waveform quality [19], [20], [21]. However, the market price of SiC MOSFET for commercial applications is about five times higher than that of Si IGBT [22], [23], [24]. Therefore, the high cost restricts the application of SiC MOSFET, especially in MMC with a large number of devices. In [25], [26], [27], [28], and [29], various topologies of integrated Si and SiC devices have been proposed to avoid the disadvantage of high cost of SiC devices and achieve the trade-off between efficiency and cost. Dahmen et al. [25] proposed a capacitor-switching MMC module in which SiC MOSFETs are connected in series in the module's capacitor branch, taking advantage of the fast recovery characteristics of SiC diodes to reduce the switching losses of Si IGBT. In [26], various hybrid configurations of Si IGBT and SiC MOSFET in MMC half-bridge submodule (HSM) are analyzed, and their cost and efficiency are comprehensively discussed. In addition, a full-bridge submodule (FSM) with a hybrid configuration of Si IGBT and SiC MOSFET is proposed in [27], which fixes the high-frequency switching action on SiC MOSFET to reduce the switching loss. Dahmen et al. [25], Camurça and Liserre [26], and Yin et al. [27] explored the internal hybrid utilization of Si and SiC devices within MMC submodule, offering an improvement in device efficiency. However, owing to the substantial number of modules needed for MMC, the cost of configuring SiC devices for all modules is relatively high. Therefore, the proposed topology in [28] replaced a Si HSM with a SiC FSM in each arm, and fix the high-frequency PWM waveform of NL-PWM to the SiC submodule. Compared with the SiC-based MMC, the proposed topology has both high efficiency and low cost. Based on [28], the topology proposed in [29] replaces one Si half-bridge module with two SiC full-bridge modules, increasing the level of output voltage to $2N+1$. However, the symmetrical structure of the MMC arm leads to a doubling of the number of SiC MOSFET normal and redundant modules. Therefore, the MMC configuration scheme of Si and SiC submodules needs to be further optimized and improved. A hybrid MMC (HMMC) topology with cascaded FSMs in the ac side is presented in [30] and [31] mainly to shape the output voltage and cut off the dc fault current. Compared with the traditional MMC, the switching frequency of the main power unit is relatively low, which results the main power unit loss lower. However, the FSMs with a minimum number of $0.5N$ each phase needs to be configured in the ac side each phase to achieve capacitor voltage balance and harmonic elimination of the main power unit. Due to the large number of the FSMs and the high frequency operation required for the shaping function, the overall operation loss of the device is still high.

Based on the above problems, a novel HMMC based on Si and SiC devices is proposed. The main contributions can be summarized as follows.

1) The only one FSM based on SiC MOSFET is inserted in the HMMC ac side, which has fewer SiC modules than the existing scheme [29].
2) A hybrid modulation method has been proposed that utilizes a single SiC FSM to achieve an output of $2N+1$ voltage levels with good output waveform quality.
3) The energy fluctuation mechanism of the FSM in HMMC is analyzed, and a specific voltage balancing strategy for the proposed HMMC is given.
4) Compared with the existing MMCs, the tradeoff between the efficiency and cost of HMMC is further optimized.

The rest of this article is organized as follows. In Section II, the HMMC topology based on Si and SiC devices is introduced. Besides, the working principle of the HMMC is analyzed and a hybrid modulation strategy is proposed to fix the high-frequency switching to SiC MOSFET. In Section III, the energy fluctuation of FSM capacitor voltage is quantitatively analyzed, and the capacitor voltage balance scheme of HMMC is elaborated. The simulation and experimental verifications are presented in Section IV. Furthermore, the operating losses and equipment costs of the existing MMC topologies and the proposed HMMC topology under different operating conditions are compared in Section V. Finally, Section VI concludes this article.

II. Topology and Operation Principle of the HMMC

A. Traditional MMC and NLM Method

With N submodules configured in the upper and lower arms of the traditional MMC, the level number of output voltage generated by the NLM is $N+1$ [11], and the expression for the reference value of the arm output voltage is as follows:

$$\begin{cases} u_{\mathrm{up},r} = \frac{U_{\mathrm{dc}}}{2} - u_{ao,r} \\ u_{\mathrm{low},r} = \frac{U_{\mathrm{dc}}}{2} + u_{ao,r} \end{cases} \tag{1}$$

$$u_{ao,r} = \frac{mU_{\mathrm{dc}}}{2}\sin(\omega t) \tag{2}$$

where $u_{\mathrm{up},\ r}$ and $u_{\mathrm{low},\ r}$ are the reference values of the upper and lower arm voltages, respectively. $u_{\mathrm{ao},r}$ and m are the reference values of MMC output voltage and the modulation index, respectively.

The upper and lower arm voltage and the number of inserted submodules are expressed as follows:

$$\begin{cases} u_{\mathrm{step},u} = N_p U_c \\ u_{\mathrm{step,l}} = N_n U_c \end{cases} \tag{3}$$

$$\begin{cases} N_p = \mathrm{round}\left(\frac{0.5U_{\mathrm{dc}} - u_{ao,r}}{U_c}\right) \\ N_n = \mathrm{round}\left(\frac{0.5U_{\mathrm{dc}} + u_{ao,r}}{U_c}\right) \end{cases} \tag{4}$$

where round(x), U_c, $u_{\mathrm{step},\,u,}$ and $u_{\mathrm{step,l}}$ are the function of rounding the nearest integer, the capacitor voltage of the submodules, output voltages of the upper arm and output voltages of the lower arm, respectively.

Ignoring the arm inductance voltage, the phase voltage and the dc link voltage can be expressed as follows:

$$u_{\mathrm{step}} = \frac{1}{2}(u_{\mathrm{step,l}} - u_{\mathrm{step},u}) \tag{5}$$

$$U_{\mathrm{dc}} = u_{\mathrm{step},u} + u_{\mathrm{step,l}}. \tag{6}$$

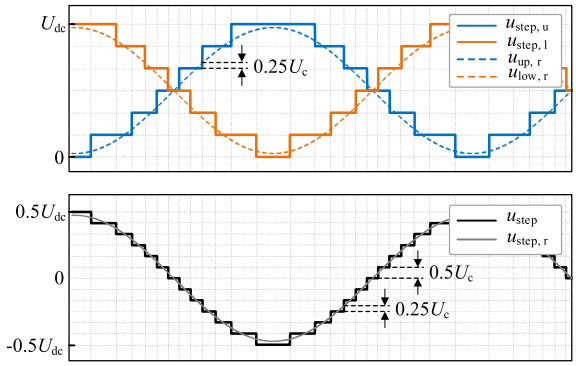

Fig. 1. Schematic diagram of $2N+1$ level NLM modulation.

According to (3), (4), and (5), each voltage level of the upper and lower arm voltages is U_c, and the error between the output voltage of the ac side and the reference value is limited to within $0.5U_c$.

To further improve the quality of the NLM output waveform, an improved NLM capable of producing $2N+1$ levels is proposed in [12], [13], as shown in Fig. 1. The number of inserted submodules in the upper and lower bridge arms is expressed as follows:

$$\begin{cases} N_p{}' = \text{round}\left(\frac{0.5U_{dc}-u_{ao,r}}{U_c} + y\right) \\ N_n{}' = \text{round}\left(\frac{0.5U_{dc}+u_{ao,r}}{U_c} + y\right) \end{cases} \tag{7}$$

where $N_p{}'$ and $N_p{}'$ represent the modified number of inserted submodules in the upper and lower arms, and y is a small offset of the reference signals. According to [13], the optimal value of offset y is ± 0.25.

According to (3), (5), and (7), the deviation between the u_{step} and the $u_{ao,r}$ is reduced to less than $0.25U_c$. However, there are still significant low-order harmonics in the MV MMC output staircase voltage.

B. Proposed HMMC and Hybrid Modulation Method

To further realize the comprehensive optimization of efficiency and cost, a novel HMMC topology based on Si IGBT and SiC MOSFET is proposed, as shown in Fig. 2.

Each phase of the HMMC contains $2N$ HSMs and an FSM. The HSM is composed of Si IGBT devices, while the FSM is composed of SiC MOSFET devices. L, C_H and C_F are the arm inductance, the capacitance value of HSM and the capacitance value of FSM, respectively. u_{jo} ($j = a, b, c$) and i_j are the output voltages and currents of the HMMC, respectively.

Based on the HMMC topology, a hybrid modulation method is proposed, as is shown in Fig. 3. The HSMs adopt the improved NLM method to generate a staircase wave voltage u_{step} with a $2N+1$ level. To eliminate the low-order harmonics of u_{step}, FSM is defined as an external shaping module to further shapes the output voltage generated by HSMs.

The reference value for the FSM output voltage $u_{\text{PWM},r}$ is expressed as follows:

$$u_{\text{PWM},r} = u_{ao,r} - u_{\text{step}}. \tag{8}$$

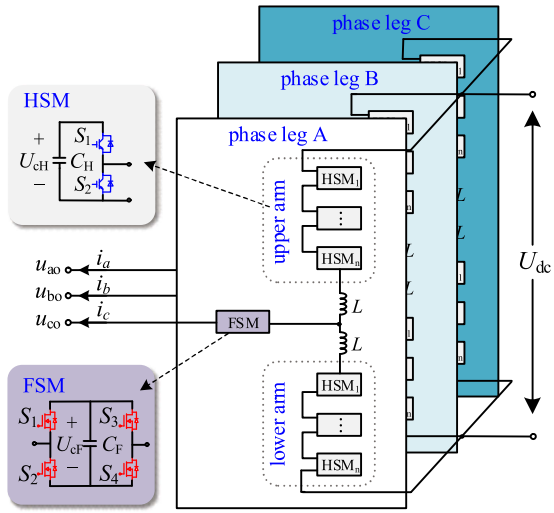

Fig. 2. Topology diagram of the HMMC.

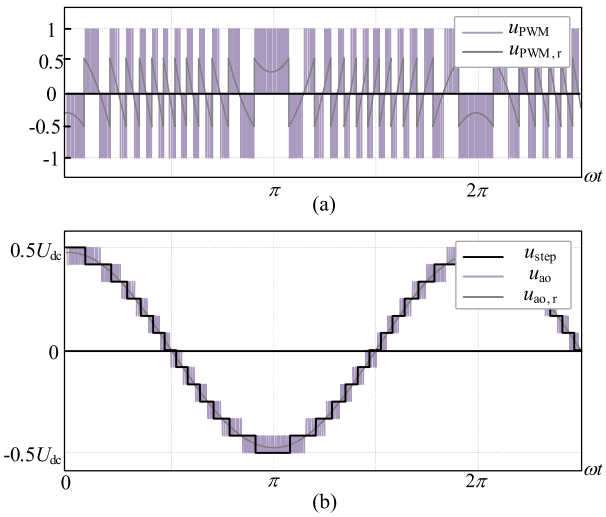

Fig. 3. Schematic diagram of the HMMC modulation. (a) Schematic diagram of FSM modulation. (b) HMMC ac side output voltage.

The FSM employs unipolar PWM to generate PWM waveform with 0 and $\pm U_{cF}$ voltage levels, as is shown in Fig. 3(a). To minimize the harmonic content of the output voltage, the reference value of FSM capacitor voltage is set to a single voltage step in u_{step}, which can be express as

$$U_{cF} = 0.5U_{cH}. \tag{9}$$

According to (9), the capacitor voltage in FSM is only half of that in HSM. Therefore, the blocking voltage requirement of SiC MOSFET device in FSM is reduced, facilitating the selection of existing commercialized components.

The FSM voltage and the HSM voltage are superimposed as the output voltage of the HMMC, as shown in Fig. 3(b). The proposed HMMC hybrid modulation optimally leverages the advantages of low switching losses in SiC MOSFET devices by maintaining the high-frequency PWM waveform in the FSM, which improves the quality of the output waveform and reduces

the overall device switching losses. Additionally, compared to the traditional MMC based on all-SiC devices, HMMC contains only one low-voltage SiC FSM in each phase, significantly reducing the cost of the converter.

III. Voltage Balancing Strategy for HMMC

Due to the implementation of a hybrid modulation strategy in HMMC, a discrepancy arises in the output voltages between HSM and FSM, rendering existing voltage balance strategies unsuitable. In this section, the energy fluctuation in FSM capacitors will be analyzed, and voltage balancing strategies for both FSM and HSM will be proposed.

A. Analysis of Energy Fluctuation in FSM Capacitor

Taking the FSM of phase A as an example, the output voltage and current in HMMC are expressed as follows:

$$\begin{cases} u_{ao} = U_m \sin(\omega t) \\ i_a = I_m \sin(\omega t + \varphi) \end{cases} \tag{10}$$

where I_m, U_m, and φ are the amplitude of the output current, amplitude of the output voltage and the power factor angle, respectively.

According to (5), (6), (7), and (8), the FSM output voltage $u_{\mathrm{PWM},r}$ is expressed as follows:

$$u_{\mathrm{PWM},r} = U_m \sin(\omega t) - \frac{U_c}{2}\left[\begin{array}{c}\mathrm{round}\left(\frac{N}{2} + \frac{U_m}{U_c}\sin(\omega t) + y\right) - \\ \mathrm{round}\left(\frac{N}{2} - \frac{U_m}{U_c}\sin(\omega t) + y\right)\end{array}\right]. \tag{11}$$

According to (10) and (11), the energy fluctuation ΔE in the FSM capacitor can be calculated by

$$\Delta E = \int_0^t i_a \cdot u_{\mathrm{PWM},r} dt. \tag{12}$$

Setting the modulation index m to 1, the number of HSMs to 8 and offset y to 0.25, the relationship between the energy fluctuation of the FSM capacitor with time and the power factor angle can be obtained from (12), as shown in Fig. 4.

When the active power flows through the HMMC, the FSM absorbs the active power from the HMMC dc bus, resulting in a continuous increase in the dc-side capacitor voltage of the submodule, making it challenging to achieve voltage balance.

B. Voltage Balancing Strategy for FSM Capacitor

To stabilize the FSM capacitor voltage around the reference value, the maximum fluctuation threshold is set ΔU. The maximum and minimum threshold voltages U_{cmax}, U_{cmin} for the FSM capacitor are represented as follows:

$$\begin{cases} U_{\mathrm{cmax}} = 0.5U_{\mathrm{cave}} + \Delta U \\ U_{\mathrm{cmin}} = 0.5U_{\mathrm{cave}} - \Delta U \end{cases} \tag{13}$$

where U_{cave} represents the average value of the HSM capacitor voltage.

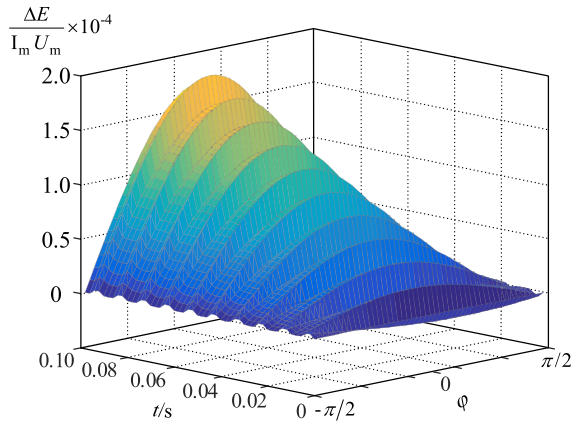

Fig. 4. FSM energy fluctuation trend chart.

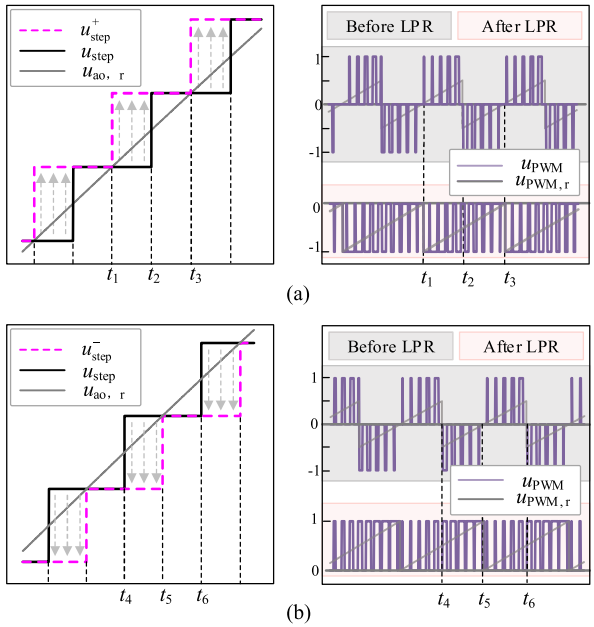

Fig. 5. Voltage balance principle of FSM. (a) Mode 1. (b) Mode 2.

The polarity of the FSM output voltage includes 0, $+U_{cF}$, and -U_{cF}, as shown in Fig. 3. Within a fundamental frequency modulation cycle, the trend of FSM capacitor voltage variation depends on the direction of the HMMC output current and the polarity of FSM output voltage. A specific voltage balance control scheme called level polarity reversal (LPR) is proposed to maintain FSM voltage balance. When the capacitor voltage exceeds the set threshold voltage, the direction of the output current and the voltage offset trend of FSM are detected. Further, it is judged whether the polarity of the output voltage is reversed to modify the charging and discharging time of the capacitor.

The LPR voltage balancing strategy can be specifically divided into mode 1 and mode 2, as shown in Fig. 5(a) and (b), respectively.

1) *LPR Process in Mode 1:* The transition process of the PWM waveform from a positive pulse to a negative pulse

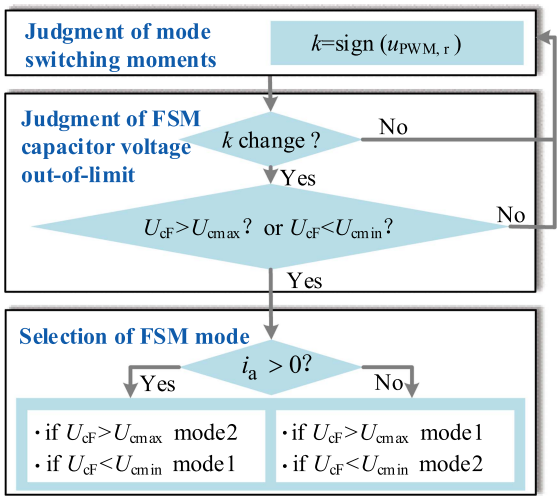

Fig. 6. FSM voltage balancing control schematic diagram.

in the FSM output. When $u_{\text{step}} < u_{ao,r}$ and $u_{\text{PWM},\ r} > 0$ (during t_1 to t_2), the FSM outputs a positive PWM waveform. To flip the FSM output PWM waveform, u_{step} is increased by a level platform of $0.5U_c$. The modified voltage u^+_{step} is expressed as follows:

$$u^+_{\text{step}} = u_{\text{step}} + 0.5U_c. \tag{14}$$

After the modification, $u^+_{\text{step}} > u_{ao,\ r}$, $u_{\text{PWM},\ r} < 0$, and FSM outputs a negative PWM waveform. When $u_{\text{step}} > u_{ao,\ r}$ and $u_{\text{PWM},\ r} < 0$ (during t_2 to t_3), and FSM outputs a negative PWM waveform without flipping. After the LPR is activated in mode 1, the state of the FSM capacitor has changed from alternating between charging and discharging to constantly discharging during t_1 to t_3, resulting in an increase in capacitor voltage.

1) *LPR Process in Mode 2:* The transition process of the PWM waveform from negative pulse to positive pulse in the FSM output. When $u_{\text{step}} > u_{ao,\ r}$ and $u_{\text{PWM},\ r} < 0$ (during t_4 to t_5), the FSM outputs a negative PWM waveform. To flip the FSM output PWM waveform, u_{step} is decreased by a level platform of $0.5U_c$. The modified step voltage u^-_{step} is expressed as follows:

$$u^-_{\text{step}} = u_{\text{step}} - 0.5U_c. \tag{15}$$

After the modification, $u_{\text{step}} < u_{ao,\ r}$, $u_{\text{PWM},\ r} > 0$, and FSM outputs a positive PWM waveform. When $u_{\text{step}} < u_{ao,\ r}$ and $u_{\text{PWM},\ r} > 0$ (during t_5 to t_6), and FSM outputs a positive PWM waveform without the need for a level change. After the LPR is activated in mode 2, the state of FSM capacitor has changed from alternating between charging and discharging to constantly discharging during t_4 to t_6, resulting in a decrease in capacitor voltage.

In summary, the two levels reversal modes in the proposed LPR scheme can freely control the charged and discharged states of the FSM capacitor.

The FSM voltage balancing control schematic is shown in Fig. 6. To reduce the switching frequency, the LPR control are activated only at the zero-crossing point of $u_{\text{PWM},\ r}$ instead of during the control cycle or PWM cycle. In addition, the FSM capacitor voltage can be controlled by modifying the threshold voltage in (13). When the capacitor voltage exceeds the threshold, the changing trend of the capacitor voltage is further judged by combining the polarity of the output current i_a and the FSM output level. Subsequently, the actual value of the FSM capacitor voltage is compared with the control value to determine the mode of the LPR.

C. Voltage Balancing Strategy for HSM Capacitor

Affected by the LPR control of FSM, the HSMs needs to change the number of voltage levels in u_{step} to meet the output level reversal of FSM. Considering the LPR transformation, the arm output voltage can be represented as follows:

$$u^+_{\text{step}} = \frac{1}{2}U_c(N'_n - N'_p) + \frac{1}{2}U_c. \tag{16}$$

The expression in (16) can be transformed into the following two cases:

$$u^+_{\text{step}} = \frac{1}{2}U_c\left[(N'_n + 1) - N'_p\right] \tag{17}$$

$$u^+_{\text{step}} = \frac{1}{2}U_c\left[N'_n - (N'_p - 1)\right]. \tag{18}$$

According to (17) and (18), either inserting a bypassed HSM into the lower arm or bypassing a previously inserted HSM from the upper arm can generate the action of increasing u^+_{step} by one level step.

Similar to the construction principle of u^+_{step}, u^-_{step} can also be transformed into the following two cases:

$$u^-_{\text{step}} = \frac{1}{2}U_c\left[(N'_n - 1) - N'_p\right] \tag{19}$$

$$u^-_{\text{step}} = \frac{1}{2}U_c\left[N'_n - (N'_p + 1)\right]. \tag{20}$$

According to (19) and (20), either bypassing a previously inserted submodule from the lower arm or inserting a bypassed submodule to the bridge arm can generate the action of reducing u^-_{step} by one level step.

In the traditional NLM, the arm voltage u_{arm} is matched to the dc link voltage U_{dc} of MMC, expressed as follows:

$$u_{\text{arm}} = u_{\text{step},u} + u_{\text{step,l}} \tag{21}$$

$$U_{\text{dc}} = u_{\text{arm}} - 2L\frac{di_{\text{cir}}}{dt} \tag{22}$$

where i_{cir} is the circulating current. However, the fluctuation in the number of inserted HSMs will affect the i_{cir}. The equivalent circuit of circulating current in HMMC is shown in Fig. 7. u_{arm} and u_L are the sum of voltages generated by the inserted HSMs and the voltage across the arm inductor, respectively.

Depending on the magnitude of the arm voltage u_{arm}, two cases can be distinguished.

1) When $u_{\text{arm}} > U_{\text{dc}}$, $u_L > 0$ and i_{cir} increases in the reference direction, as shown in Fig. 7(a). Therefore, additional submodules are inserted in the arm. After an additional HSM is inserted, the inductor voltage is expressed as

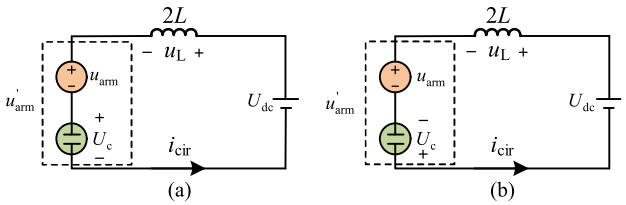

Fig. 7. Cycling current equivalent circuit of the HMMC. (a) $u_{\rm arm} > U_{\rm dc}$. (b) $u_{\rm arm} < U_{\rm dc}$.

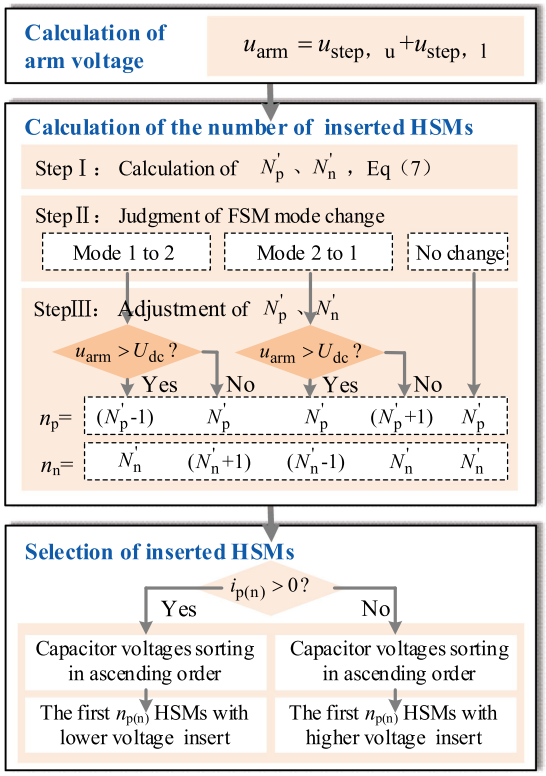

Fig. 8. HSM capacitor voltage control schematic diagram.

follows:

$$|u_{\rm L}| = |U_{\rm dc} - u'_{\rm arm}| < |U_{\rm dc} - u_{\rm arm}|. \tag{23}$$

According to (23), the voltage across the arm inductor is decreased.

1) When $u_{\rm arm} > U_{\rm dc}$, $u_L < 0$ and $i_{\rm cir}$ decreases in the reference direction, as shown in Fig. 7(b). Therefore, a previously inserted HSM needs to be bypassed in the arm (equivalent to inserting a voltage source of $-U_c$). After a previously inserted HSM is bypassed, the inductor voltage is expressed as follows.

$$|u_L| = |u'_{\rm arm} - U_{\rm dc}| < |u_{\rm arm} - U_{\rm dc}|. \tag{24}$$

According to (24), the voltage across the arm inductor is decreased.

To achieve the dynamic balance of the arm voltage and dc link voltage of HMMC in (22), the proposed HSM voltage balances scheme is analyzed in detail, as shown in Fig. 8.

TABLE I
SIMULATION PARAMETERS

Parameters	Value
Rated DC Voltage	10 kV
Power rating	1.5 MW
Number of HSMs per arm	8
Number of FSM	1
Modulation Index	0.95
Equivalent frequency	20 kHz
Bridge Inductance	10 mH
DC Capacitance of HSM	3300 μF
DC Capacitance of FSM	3300 μF

Combined with the FSM mode changes in Fig. 6, the arm voltage is compared with the dc-link voltage of the HMMC to determine the appropriate total number of submodules inserted in the upper arm (n_p) and lower arm (n_n). Then, the capacitor voltage value of HSMS is arranged in ascending or descending order according to the arm current i_p or i_n. to determine the inserted HSMs.

D. Circulating Current Control for the HMMC

The circulating current in HMMC is caused by the instantaneous voltage mismatch between the arm and the dc bus, so the current only circulates through arms of each phase leg, and do not appear at the output. According to (23) and (24), the total number of inserted HSMs is closely related to the size of the circulating current, so it is necessary to reasonably control the variation of inserted HSM caused by the FSM operation module. Considering the influence mechanism of the operating mode change of FSM on the number of inserted HSMs, the circulating current suppression method with deadbeat control proposed in [32] can be adopted to suppress the circulating current of the HMMC.

IV. SIMULATION AND EXPERIMENTAL RESULTS

With the detailed discussion of the HMMC topology and modulation mentioned above, the HMMC simulation model and experiment prototype were built to achieve the verification.

A. Simulation Results

Based on the MATLAB/Simulink platform, the model of the single-phase HMMC system is developed, and the model parameters are given in Table I.

The HMMC output voltage simulation results depicted in Fig. 9. Each arm is equipped with 8 HSMs, and the number of output levels on the ac side can reach 17. Due to the change of the LPR mode, the number of inserted HSMs needs to be adjusted inside the upper or lower arm, and the HSMs output a 17-level staircase voltage with irregular changes. In addition, the switching frequency of the FSM is much higher than that of HSM (e.g., upper arm $\rm HSM_1$).

Fig. 10 shows the number of upper and lower arm HSMs calculated by (7) ($N_p{}'$ and $N_n{}'$) and the number adjusted by the voltage balancing strategy (n_p and n_n).

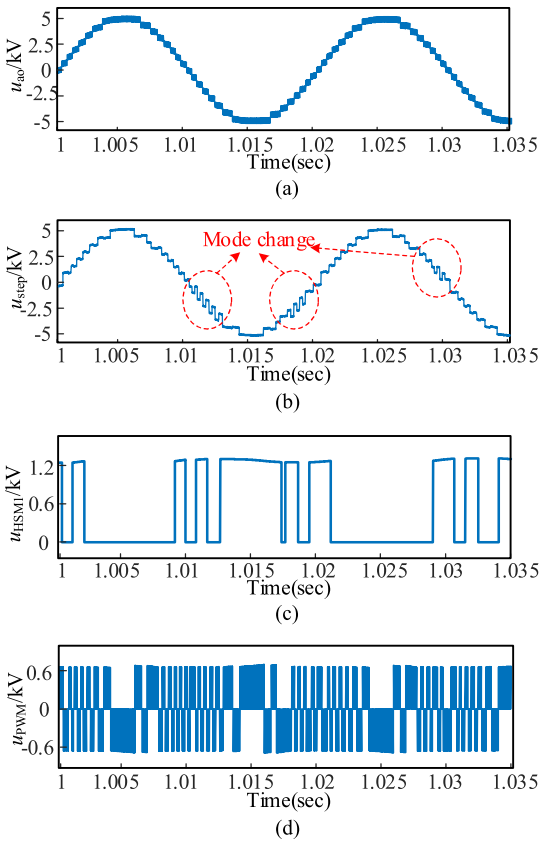

Fig. 9. Simulation results of HMMC voltage. (a) Output voltage of the HMMC. (b) Output voltage of the HSMs. (c) Output voltage of the HSM_1. (d) Output voltage of the FSM.

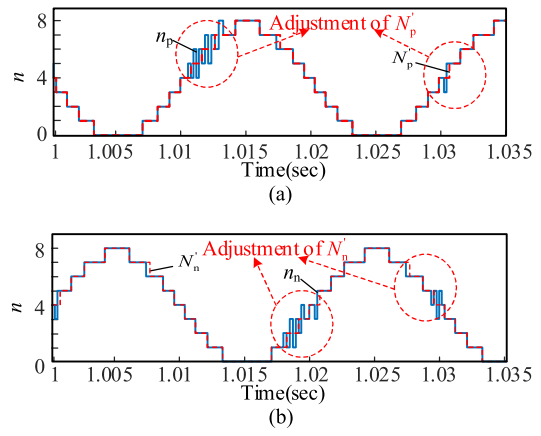

Fig. 10. Simulation results of the number of HSMs inserted in the HMMC. (a) Upper arm. (b) Lower arm.

The simulation waveform of the capacitor voltage of HMMC submodules is shown in Fig. 11. The FSM capacitor voltage and the HSM capacitor voltage fluctuate around 1250 and 625, respectively, which verifies the effectiveness of the proposed voltage balancing strategy.

To verify the dynamic characteristics of the proposed HMMC, the transient dynamics simulations under the varying modulation index and power factor are conducted separately, as shown in Figs. 12 and 13. The HMMC output voltage, output current,

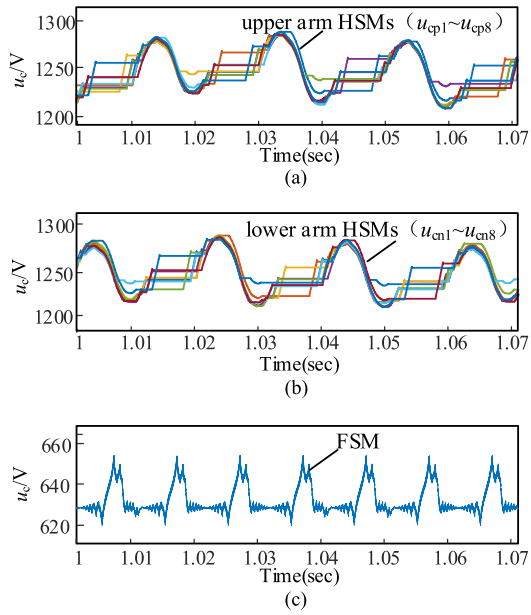

Fig. 11. Simulation results of the capacitor voltage of the HMMC submodules. (a) HSMs in the upper arm. (b) HSMs in the lower arm. (c) FSM.

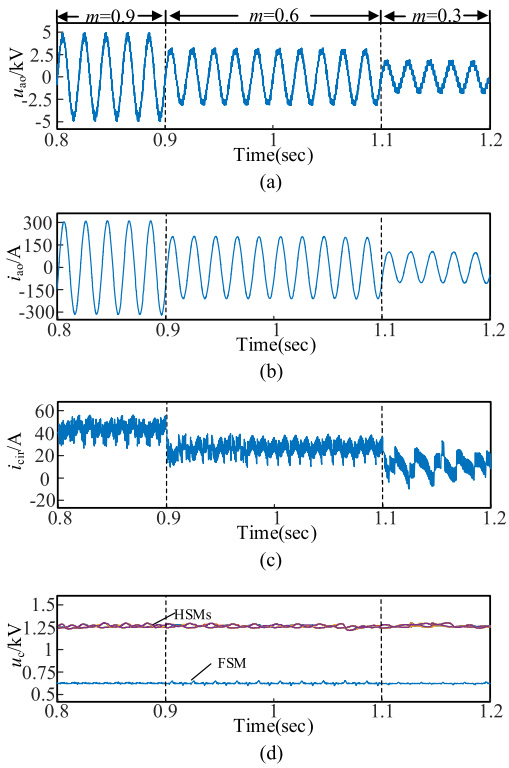

Fig. 12. Transient characteristics under the modulation index change from 0.9 to 0.3. (a) Output voltage. (b) Output current. (c) Circulating current. (c) Capacitor voltage of HSMs and FSM.

circulating current and capacitor voltage are shown in the figure from top to bottom. The initial parameters of the simulations are consistent with Table I, except for the dynamic parameters. The transient dynamics under the modulation index from 0.9 to 0.3 is demonstrated in Fig. 12. The transient dynamics under the power factor changes from 0 to 1 are shown in Fig. 13. The provided

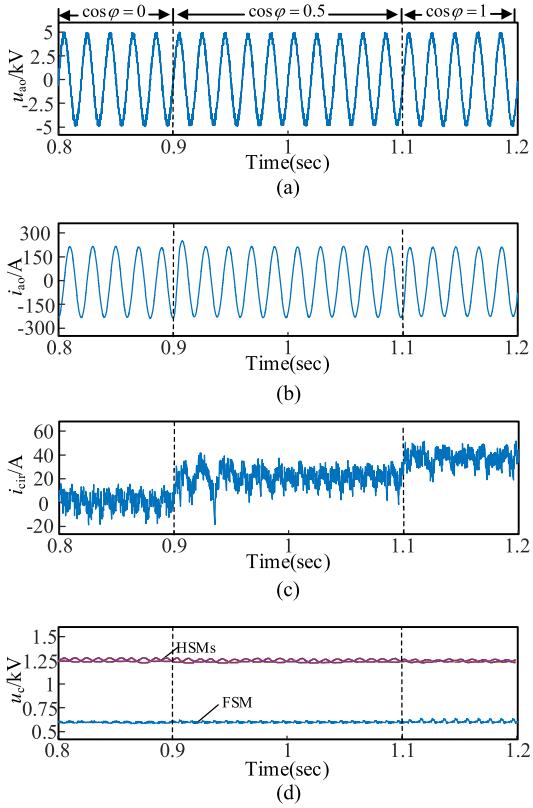

Fig. 13. Transient characteristics under the power factor change from 0 to 1. (a) Output voltage. (b) Output current. (c) Circulating current (d) Capacitor voltage of HSMs and FSM.

TABLE II
EXPERIMENT PARAMETERS

Parameters	Value
Rated DC Voltage	400 V
Number of HSMs per arm	4
Number of FSM	1
Modulation Index	0.95
Load resistance	30 Ω
Equivalent frequency	20 kHz
Bridge Inductance	5 mH
DC Capacitance of HSM	2400 μF
DC Capacitance of FSM	2400 μF

simulation results are in Figs. 12 and 13 demonstrate that the proposed voltage balance method can retained the converter stable during disturbances.

B. Experimental Results

In order to verify the effectiveness of the proposed topology and voltage balancing strategy of HMMC, an HMMC prototype with 4 HSMs per arm was built and the electrical parameters are given in Table II. The single-phase HMMC system is presented in Fig. 14.

The experimental results of output voltage for the HMMC system are shown in Fig. 15. The HMMC output voltage u_{ao} is a nine-level voltage superimposed by the FSM output voltage

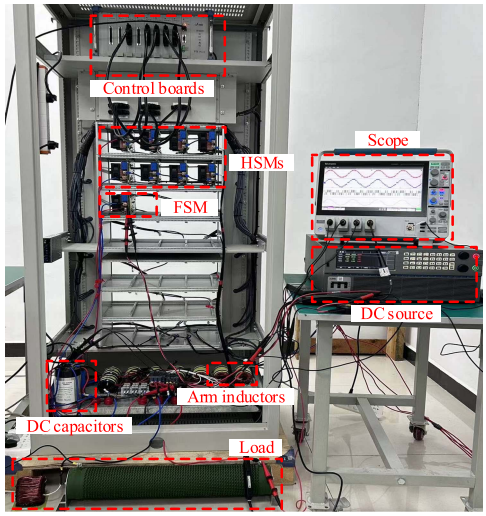

Fig. 14. Picture of the single-phase HMMC prototype.

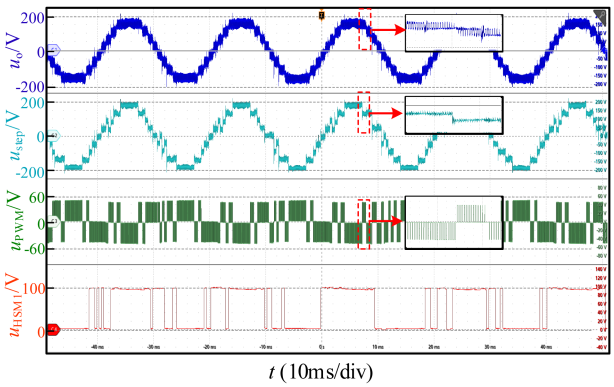

Fig. 15. Experiment results of HMMC voltage.

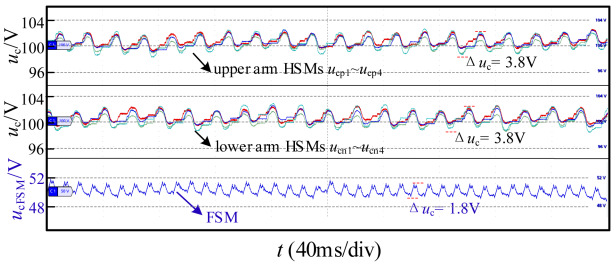

Fig. 16. Experiment results of the capacitor voltage of the HMMC submodules.

u_{PWM} and HSMs output voltage u_{step}. Among them, each HSM adopts NLM to output a 2-level square wave voltage with low switching frequency (e.g., upper arm HSM_1). The FSM adopts PWM to output positive or negative 20 kHz pulse voltage u_{PWM}.

The experimental waveform of the capacitor voltage of the HMMC submodule is shown in Fig. 16. The capacitor voltage u_{cp1} and u_{cn1} of the upper and lower arm HSM (e.g., upper and lower arm HSM_1) can be stabilized to about 100 V, with the voltage fluctuation is 3.8 V. The FSM capacitor voltage u_{cFSM}

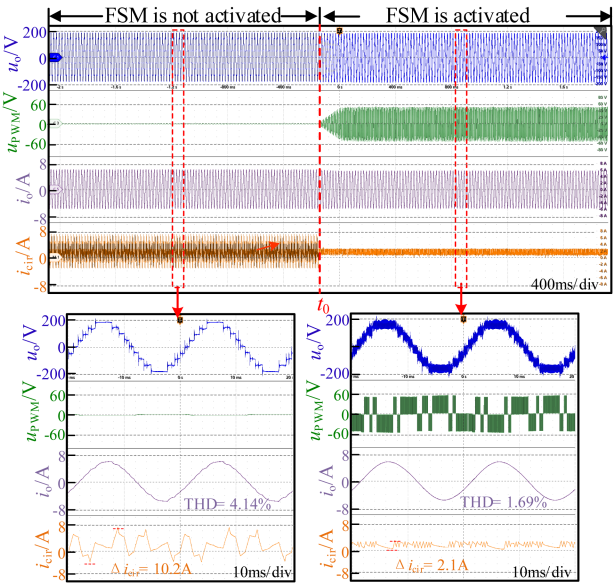

Fig. 17. Experiment results of the HMMC with and without FSM.

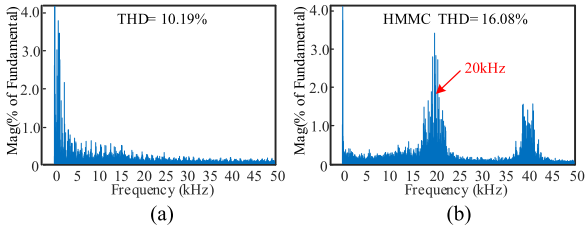

Fig. 18. Spectrum of output voltage. (a) Without FSM. (b) With FSM.

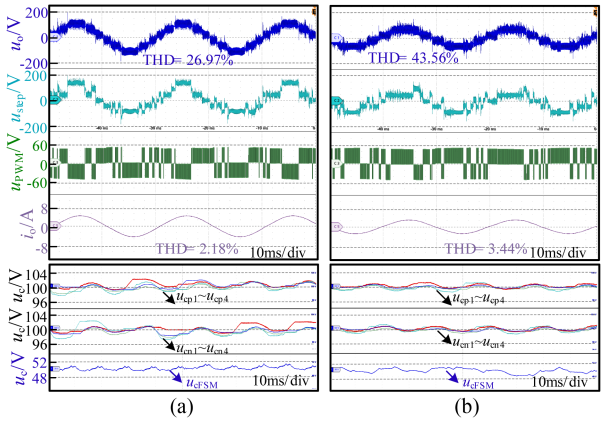

Fig. 19. Experiment results with different modulation index. (a) $m = 0.6$. (b) $m = 0.4$.

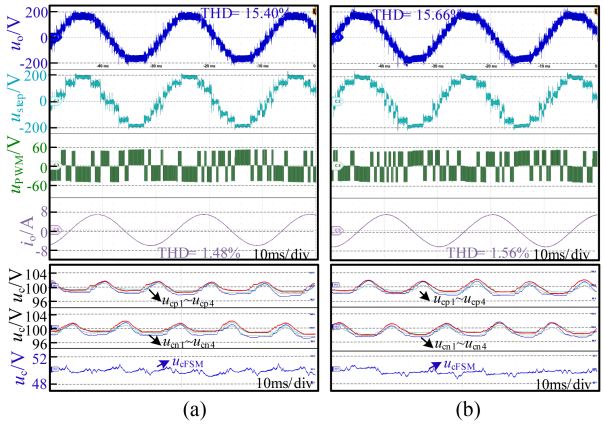

Fig. 20. Experiment results with different power factor. (a) $\cos\varphi = 0.5$. (b) $\cos\varphi = 0$.

can be stabilized to about 50 V, and the voltage fluctuation is 1.8 V.

In addition, to verify the effect of FSM on the quality improvement of HMMC output waveform, the experiments of HMMC with and without FSM are carried out, as shown in Figs. 17 and 18. After the FSM is activated, the THD of i_o in the HMMC decreases from 4.14% to 1.69%, and the circulating current $i_{\rm cir}$ of HMMC is reduced by 79%. The spectrum comparison of output voltage in HMMC with and without FSM are shown in Fig. 18. As can be seen from the output voltage spectrums, there are notable low-order voltage harmonics when the FSM is not activated. While the lowest harmonic clusters location equals to the equivalent switching frequency (20 kHz) when the FSM is activated, so the output current becomes smoother. In addition, although the output voltage with high-order harmonics may lead to high frequency noise, the EMI noise generated in HMMC is effectively suppressed by the EMI filter in practical engineering [33]. Since only one FSM per phase in HMMC operates at high switching frequency, there are fewer EMI noise sources caused by high *dv/dt* compared to the traditional MMC design.

For evaluating the voltage balancing scheme for the HMMC, the experiment under the different modulation index and power factor are conducted separately. Figs. 19 and 20 presents the experimental results of the output voltage of HMMC $u_{\rm ao}$, output voltage of HSMs $u_{\rm step}$, output voltage of FSM $u_{\rm FSM}$, output current of HMMC i_o, capacitor voltage of HSM and FSM, respectively. In Fig. 19, as the modulation index decreases from 0.6 to 0.4, the output level of HMMC decreases from 7 to 5, and the low-order harmonic content of the output voltage increases, so the THD of i_o is increased from 2.18% to 3.44%. In Fig. 20. the power factor changes from 0.5 to 0, and the THD of u_o and i_o remain unchanged. The capacitor voltage of HSMs and FSM can be stabilized at the reference value under all operating conditions, as shown in Figs. 19 and 20.

It is noted that the experimental results are consistent with the theoretical analysis, and validate the proposed hybrid modulation and voltage balancing control scheme of HMMC.

V. Comparison of Losses and Costs

A. Cost Comparison

The cost of active devices is compared among the full Si IGBT device MMC (Si MMC), the full SiC MOSFET device MMC (SiC MMC), the topology proposed in [29], and the HMMC. The dc-bus voltage for all four topologies is 10 kV and the device cost are shown in Table III. The Si MMC, SiC MMC, and the HMMC have eight HSMs in each arm, while the topology proposed

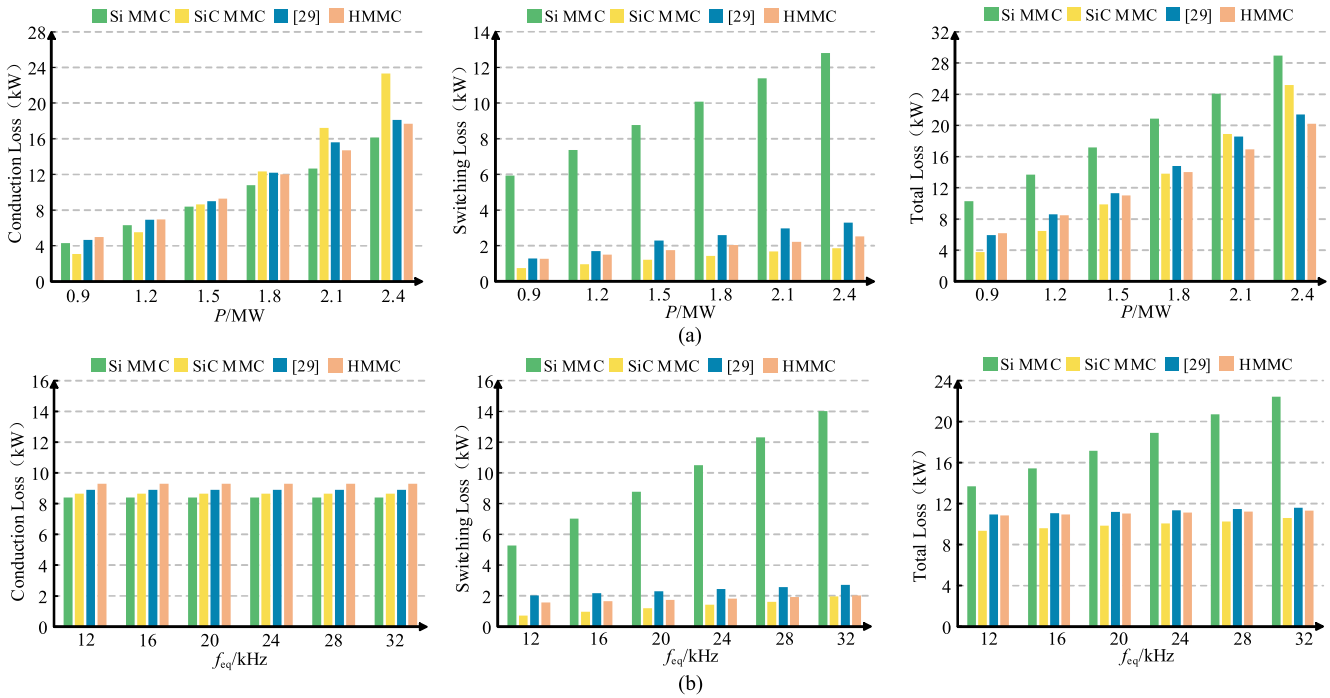

Fig. 21. Loss comparison of different topologies. (a) At different powers ($Tj = 100$ °C, $f = 20$ kHz). (b) At different equivalent switching frequencies ($Tj = 100$ °C, $P = 1.5$ MW).

TABLE III
COST COMPARISON OF DIFFERENT TOPOLOGIES

Topology	Si MMC	SiC MMC	[29]	HMMC
Si IGBT(1.7kV)	FF300R17KE4P			
Price/Quantity	$125/48	\	$125/42	$125/48
SiC MOSFET(1.2kV)	CAS300M12BM2			
Price/Quantity	\	\	$855/24	$855/6
SiC MOSFET(1.7kV)	CAS300M17BM2			
Price/Quantity	\	$996/48	\	\
Total cost	$6000	$47808	$25770	$11130

in [29] has seven HSMs. The selected Si IGBT device model is Infineon's FF300R17KE4P, while the chosen SiC MOSFET models are Cree's CAS300M17BM2 and CAS300M12BM2. According to Table III, the cost of SiC MMC is approximately 7.9 times that of Si MMC. The three-phase topology proposed in [29], adopting 12 expensive SiC FSMs, has a total cost about 4.2 times that of Si MMC. In contrast, the cost of proposed HMMC is reduced by 76.7% compared with SiC MMC, and 56.8% compared with the topology proposed in [29].

B. Loss Comparison

To validate the superiority of the HMMC topology in terms of losses, a comparative analysis of losses is conducted using the MATLAB/Simulink and PLECS co-simulation platform. The Si MMC, SiC MMC, the topology proposed in [29] and HMMC are subjected to this analysis. The selected device models for each topology are presented in Table III, and the simulation parameters are given in Table I.

The comparative results of losses for the four topologies are presented in Fig. 21. In Fig. 21(a), the loss data for the four topologies are compared under various transmission power. For Si MMC, both switching and conduction losses increase with the growth of load power. Due to the lower switching losses of SiC MOSFET, SiC MMC exhibits lower overall losses. However, as the transmission power increases, the conduction losses of SiC MOSFET rapidly rise. The HMMC concentrate high-frequency switching actions on SiC MOSFET devices, leading to lower total losses. For instance, under the rated power condition of $P = 1.5$ MW, HMMC reduces losses by 35.6% compared to Si MMC.

Fig. 21(b) displays the power losses of the four topologies under different equivalent switching frequencies. Conduction losses of the converter remain constant across all frequency levels since they are independent of the switching frequency. Due to the use of SiC MOSFET devices, SiC MMC exhibits a low switching loss, which increases slowly with increasing frequency, while the switching loss of Si MMC increases sharply. The characteristics of switching losses for HMMC are akin to SiC MMC, with total losses gradually increasing as the switching frequency rises. The advantage of low loss of the HMMC becomes more obvious at higher equivalent switching frequency. For example, under the equivalent switching frequency of $f_{\mathrm{eq}} = 32$ kHz, the HMMC reduces the loss by 49.5% compared with Si MMC.

The comparative results of losses for the HMMC with and without FSM are presented in Fig. 22. Fig. 22(a) shows the loss of HMMC under different transmission power. With the increase of transmission power, the operating loss of HMMC with and without FSM both increases. Since the NLM is adopted

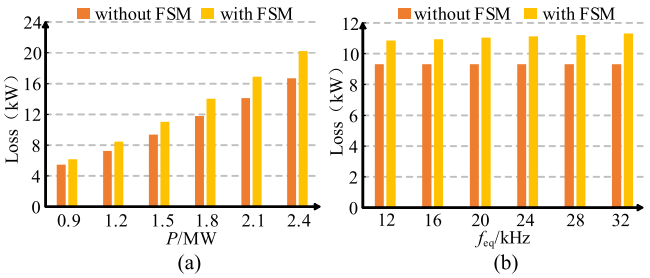

Fig. 22. Loss comparison of the HMMC with and without FSM. (a) At different powers ($Tj = 100$ °C, $f = 20$ kHz). (b) At different equivalent switching frequencies ($Tj = 100$ °C, $P = 1.5$ MW).

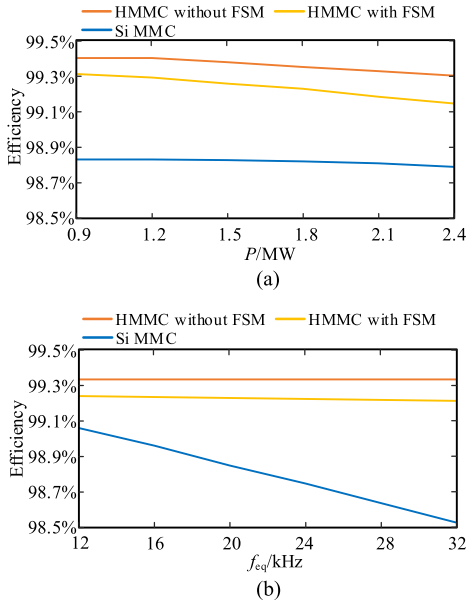

Fig. 23. Efficiency comparison. (a) At different powers ($Tj = 100$ °C, $f = 20$ kHz). (b) At different equivalent switching frequencies ($Tj = 100$ °C, $P = 1.5$ MW).

by HMMC without FSM, the HMMC without FSM has low switching loss but poor waveform quality, which is not suitable for MV application with few submodules. The switching and conduction loss of the FSM are generated after the FSM is put into operation. Therefore, during the operating condition of HMMC with FSM, the operating loss of HMMC is slightly greater than without FSM. For instance, under the rated power condition of $P = 1.5$ MW, the total loss of HMMC with FSM is 15.5% higher than that without FSM.

Fig. 22(b) shows the power loss of HMMC at different equivalent switching frequency. Since the NLM is adopted during the operation of HMMC without FSM, so its loss is independent of equivalent switching frequency and remains basically unchanged. Because the switching loss of FSM increases with the equivalent switching frequency, the total loss of HMMC with FSM increases slowly with increasing frequency. Under the equivalent switching frequency of $f_{eq} = 32$ kHz, the loss of HMMC with FSM is 17.5% higher than that without FSM.

The conversion efficiency of HMMC with and without FSM, and traditional Si MMC are compared in Fig. 23. As shown in the Fig. 23(a), when HMMC operates with the external shaping FSM, the system efficiency will be slightly reduced than that without FSM, due to additional switching and conduction loss of the external FSM. Compared with the traditional Si MMC, the Si IGBT in the proposed HMMC runs at the low switching frequency, so the efficiency of HMMC with and without FSM is higher than that of Si MMC. In addition, since most of the switching actions are concentrated on the FSM based on SiC MOSFET, the efficiency of HMMC with FSM module decreases slightly as the equivalent switching frequency increases, as shown in Fig. 23(b). Besides, the HMMC with and without FSM features higher efficiency than Si MMC when frequency increases.

VI. Conclusion

This article introduces a cost-effective, high-efficiency HMMC that integrates a SiC FSM in the ac side of each phase in the conventional Si MMC, thereby reducing the operating loss and improving the quality of voltage waveform. Additionally, a voltage balancing scheme is introduced for the HMMC. The main contributions and innovations are as follows.

1) Only one SiC FSM is added to each phase in the proposed HMMC topology. Compared with Si MMC and SiC MMC, the tradeoff between efficiency and cost is optimized.
2) The proposed hybrid modulation method fixes high-frequency components of the output voltage on SiC MOSFET devices and low-frequency components on Si IGBT devices, which reduces overall losses in HMMC and diminishes the voltage stress on SiC MOSFET devices.
3) The proposed voltage balancing scheme effectively controls the stability of FSM and HSM capacitor voltages.

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