A High-Frequency Isolated AC–AC Converter With Independently Controlled Bipolar Buck–Boost Dual Outputs

Hafiz Furqan Ahmed, *Member, IEEE*, Mohsin Jamil, *Senior Member, IEEE*, Talal Alharbi, *Senior Member, IEEE*, and Omar Al Zaabi, *Member, IEEE*

***Abstract*—In this article, a new topology of a single-phase high-frequency isolated bipolar buck–boost ac–ac converter is proposed for application as a three-phase flexible ac-link (FACL) converter. The proposed converter comprises one input and two output ac ports, requiring only three discrete converters to implement a three-phase FACL converter with flexible magnitude and phase control. All three ports are electrically isolated through a three-winding high-frequency transformer, replacing the bulky and lossy power-frequency transformer used in existing FACL converters. Both output ac ports are decoupled in terms of voltage polarity and magnitude and can provide symmetric noninverting and inverting buck–boost outputs, improving voltage magnitude and phase control and reducing design complexity. Salient features of the proposed converter include the suppression of input and output harmonics through second-order harmonic filters and bidirectional operation with inductive load support. The topology is implemented with standard full-bridge inverter modules, simplifying the implementation and commutation process. A dedicated switching strategy is developed for various operational scenarios required in FACL applications. The proposed switching strategy allows current sharing among primary-side switches during high-current stress intervals, relieving current stress and conduction losses. Detailed analysis of the proposed topology is provided, including component stresses and ripples, comparisons, and simulation results. Finally, hardware results from a laboratory-scale converter are presented to verify the advantages of the proposed topology.**

***Index Terms*—AC–AC power conversion, dual-outputs, flexible ac link (FACL) converter, high-frequency isolation, inverting and noninverting outputs, voltage compensation.**

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Hafiz Furqan Ahmed is with the Department of Electrical Engineering, National Sun Yat-sen University, Kaohsiung 80424, Taiwan (e-mail: hfahmed@mail.ee.nsysu.edu).

Mohsin Jamil is with the Department of Engineering, Brock University, St. Catharines, ON L2S 3A1, Canada (e-mail: mjamil@brocku.ca).

Talal Alharbi is with the Department of Electrical Engineering, College of Engineering, Qassim University, Buraydah 52531, Saudi Arabia (e-mail: atalal@qu.edu.sa).

Omar Al Zaabi is with the Advanced Power and Energy Center, Department of Electrical Engineering and Computer Science, Khalifa University, Abu Dhabi 127788, United Arab Emirates (e-mail: omar.alzaabi@ku.ac.ae).

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I. Introduction

THE power grid is evolving from a centrally controlled, isolated radial system into a complex network of interconnected grids, integrating distributed generation, and accommodating variable loads. However, transmission lines linking these networks face power flow constraints, leading to uneven loading, asymmetric stresses on grid assets, and underutilized infrastructure. Unregulated renewable power generation, dynamic switching states, and grid faults further contribute to continuous voltage violations, increasing the risk of equipment failure and grid instability [1], [2], [3].

AC–AC power converters are crucial for regulating power flow and voltage, enhancing grid flexibility and stability [4]. Traditional methods often rely on back-to-back ac–dc–ac converters with a dc link [5], [6]. However, large dc-link electrolytic capacitors increase system weight, costs, failure rates, and reduce lifespan [6], [7].

Recent attention has shifted to direct PWM ac–ac converters due to their single-stage conversion, absence of dc-link capacitors, simple operation, and smaller footprint. Basic ac–ac converters [8], derived from dc–dc designs by incorporating bidirectional ac switches, have limitations such as a restricted voltage transfer ratio and unipolar operation, limiting their role to as full-load voltage regulators [9]. Impedance-network [10] and unified [11] ac–ac converters offer bipolar outputs for series voltage regulation but are constrained by noninverting operation ranges and discontinuous input currents. Additionally, the lack of a natural freewheeling inductor path in these designs results in commutation issues, reduced reliability, and the need for extra components or complex controls for safe operation. Advancements in bipolar ac–ac converters include conventional inverter phase-leg-based designs for continuous input/output currents [12], dual-buck phase-leg-based reliable converters [13], and nondifferential ac-chopper converters [14], [15]. However, these converters can provide output phase shifts of zero or 180°, restricting their ability to address voltage sag or swell without phase jumps.

In a three-phase ac system, the flexible ac link (FACL) converter concept is developed to generate output voltage with adjustable amplitude and phase using single-phase direct ac–ac converters [16], [17], [18], [19]. Earlier FACL converters used unipolar ac choppers [16], [17], limiting their output phase-shift

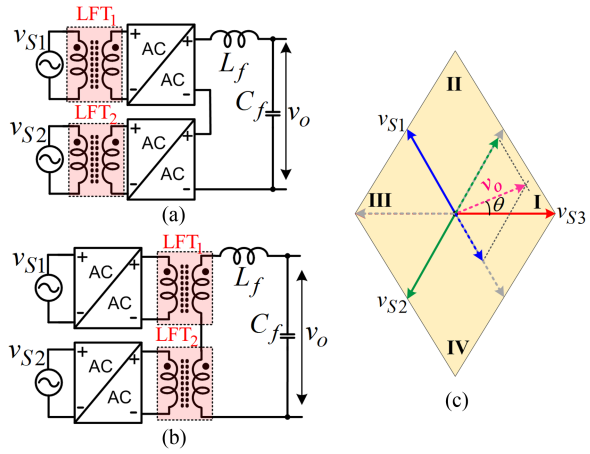


Fig. 1. Configurations of single-phase output FACL in [18]. (a) Low-frequency transformers are set at the input side. (b) Low-frequency transformers are set at the output side. (c) Voltage synthesis principle.

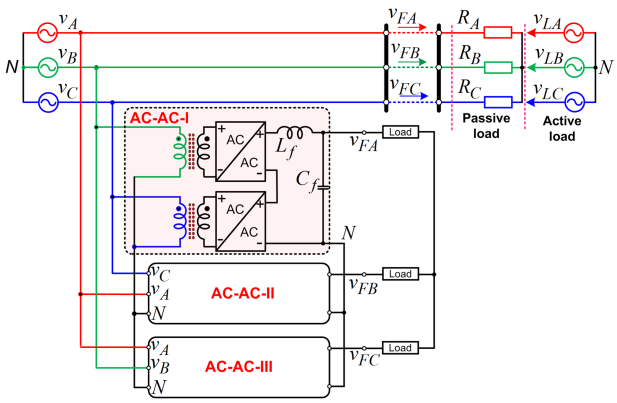


Fig. 2. Three-phase FACL converter configuration of [18] for various applications.

control within a single quadrant. A recent improved FACL converter is developed [18] based on bipolar ac–ac converters [14], enabling the output phase-shift control in all four quadrants. Fig. 1 illustrates two possible single-phase FACL converter configurations [18] based on low-frequency transformers (LFTs) set at the input [see Fig. 1(a)] or output [see Fig. 1(b)] sides. It comprises of two ac–ac converters feeding from two phase-lines v_{S1}, v_{S2} using line-frequency transformers $\mathrm{LFT}_1, \mathrm{LFT}_2$ and their outputs are connected in series to provide single-phase output v_o. Fig. 1(c) shows the vector diagram of output voltage v_o synthesis from two inputs v_{S1}, v_{S2} which can fall in any of four quadrants with 360-degree rotation and confined within the diamond region.

Fig. 2 depicts the three-phase FACL converter configuration of [18], which can be used to directly supply three-phase loads, or inject three-phase voltages (v_{FA}, v_{FB}, and v_{FC}) in series with input line voltages (v_A, v_B, and v_C) to compensate for voltage disturbances with phase jumps for passive loads, or control the power flow when an active load is connected. The FACL configuration in [18] involves six ac–ac converters for three-phase output, increasing component count, cost, and complexity. Additionally, it utilizes buck-type ac choppers, leading to voltage limitations and increased total harmonic distortion (THD) in input current. A new four-leg dual-output bipolar ac–ac converter is proposed [19] for FACL application, reducing discrete converters count to only three. However, it faces efficiency and operational limitations due to voltage gain constraints, resulting in increased stress on devices and passive component ripples. A recently developed, highly efficient dual-output bipolar ac–ac converter [20] overcomes the operational limitations of [19] by offering an extended voltage gain range, reduced voltage/current stresses and ripples, and lower power losses. However, it requires more semiconductor switches compared to [19]. Importantly, the described bipolar ac–ac converters [18], [19], [20] are non-isolated, and therefore, they must use a large number of line frequency transformers (6 LFTs for a three-phase system) for electrical isolation in application as FACL, as shown in Fig. 1. These low-frequency transformers add significant weight and volume due to their low-frequency operation (50 or 60 Hz) and suffer from high power losses, high starting in-rush currents, and dc magnetic flux bias [21].

Voltage-mode and current-mode high-frequency transformer (HFT) isolated ac–ac converters are proposed in [22] and [23], but they offer only unipolar voltage gain with discontinuous input currents. Impedance-source-based HFT-isolated bipolar buck–boost ac–ac converters [24], [25] lack noninverting buck voltage capability and require a large passive component count. A basic HFT-isolated buck matrix converter with sixteen active switches is proposed in [26], featuring a complex commutation process. A reduced-switch buck-type HFT-isolated matrix converter [27] requires an external input *LC* filter, lacks voltage boost operation, and exhibits asymmetric bipolar operation with high current stresses on switching devices. New symmetric bipolar ac–ac converter designs, integrating rectifier, and inverter stages with the dual-active bridge converter, are introduced in [28] and [29] using HFT isolation. However, they necessitate large electrolytic capacitors with constant dc-link voltages, which are redundant in FACL applications, thereby increasing circuit cost and size. A bridge-type HFT-isolated bipolar buck–boost ac–ac converter was developed in [30]; however, it employs a large number of high-frequency switches. However, I has a large number of high-frequency switches. The study in [31] developed a differential-mode isolated ac–ac converter based on Cuk ac–ac modules. However, the differential configuration increases the number of switching devices and passive elements. Alternatively, a nondifferential ac chopper-based isolated bipolar ac–ac converter is suggested, though it exhibits a buck-type structure with discontinuous current draw from ac mains [32]. Despite these innovations, none of the developed isolated ac–ac converters are tailored for FACL applications. Specifically, implementing a three-phase FACL converter from [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32] requires six converter units, substantially increasing the required HFTs to six and raising the number of semiconductor switches and passive components, ultimately increasing the system's cost and size.

This article proposes a HFT isolated symmetric bipolar ac–ac converter for application as FACL converter. The proposed topology possesses several salient features.

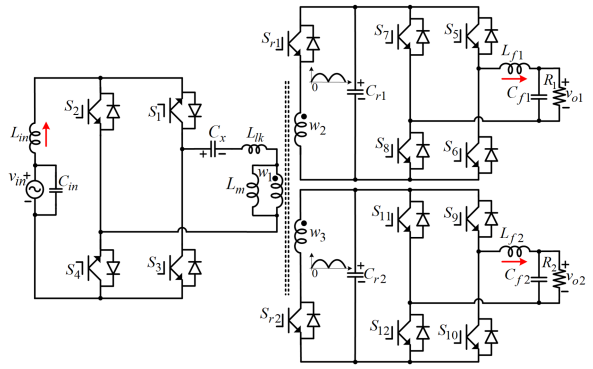


Fig. 3. Proposed HFT isolated bipolar AC–AC converter.

1) It provides two bipolar outputs per converter, with both outputs completely decoupled in terms of their magnitude and voltage polarity.
2) The proposed converter provides symmetric bipolar buck–boost operations, increasing gain coverage and reducing design complexity.
3) When applied in three-phase FACL converter, only three proposed converter units are required, along with three tapped-winding HFTs and a reduced number of overall components.
4) The proposed converter draws a continuous sinusoidal current from ac mains and provides continuous output currents. Moreover, the proposed topology is bidirectional, allowing reverse power flow.
5) Switch modulation strategies are developed for various operations suited for application in FACL converter. Additionally, the proposed modulation and operation enable the sharing of current among parallel device paths on the (high-current) primary side, relieving current stresses and conduction losses of switches.
6) The proposed converter is also free of commutation issue of traditional ac–ac converters with bidirectional (antiseries) connected switches.

II. Proposed High-Frequency Transformer Isolated Bipolar AC–AC Converter

Fig. 3 illustrates the proposed single-phase HFT isolated dual-output bipolar ac–ac converter. It comprises of a primary side module with an input *LC* filter ($L_{\text{in}}C_{\text{in}}$), four switches ($S_1 - S_4$), and a (line-frequency blocking) series capacitor C_x along with the primary winding W_1 of HFT. The magnetizing inductance L_m and leakage inductance L_{lk} of HFT transformer are shown reflected on primary side. The secondary of HFT comprises of two identical windings (W_2 and W_3) supplying power to two output ac modules (1 and 2). Module-1 includes a rectifier switch S_{r1}, a high-frequency ripple filter capacitor (C_{r1}), an H-bridge consisting of switches $S_5 - S_8$, and an output *LC* filter ($L_{f1}C_{f1}$). It generates the first output voltage v_{o1}. Module-2 uses the same configuration and components as module-1 and it generates second output v_{o2}.

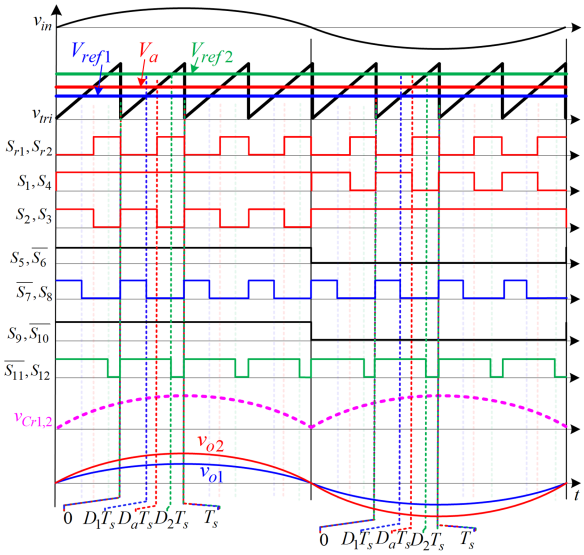


Fig. 4. Switch modulation signals for two in-phase outputs with different magnitudes.

III. Switch Modulation Strategies and Operations of the Proposed Converter

In the application of the proposed topology as a three-phase FACL converter, both of its outputs (v_{o1}, v_{o2}) should be decoupled from each other and from the input line v_{in} in terms of their magnitudes and polarity. Therefore, both outputs can be same-phase or antiphase with the input voltage, or one output can be in-phase and the other can be antiphase with the input voltage. The operation of the proposed converter is explained for two distinct scenarios: 1) when both outputs are in phase with the input voltage but have different magnitudes and 2) when one output is in-phase and the other is in antiphase of input voltage with different magnitudes.

A. Two In-Phase Outputs With Independent Magnitudes

The proposed switch modulation strategy and major waveforms are depicted in Fig. 4. For positive input voltage half-cycle, primary side switches S_1 and S_4 are fully turned-ON, while switches S_2 and S_3 are modulated together at high-frequency by comparing reference signals V_a with high-frequency carrier signalsv_{tri}. For negative half cycle, switches S_2 and S_3 are fully ON and S_1 and S_4 are switched at high-frequency. Switches S_{r1} and S_{r2} are controlled complementary to switches S_2 andS_3. Switches S_5, S_6 of secondary side module-1, and S_9, S_{10} of module-2, are power frequency modulated. Switches S_7, S_8 of module-1, and S_{11}, S_{12} of module-2, are modulated by comparing reference signals V_{ref1} and V_{ref2} with v_{tri}, respectively.

For the positive input voltage half-cycle $v_{\text{in}} > 0$, switches S_1 and S_4 at the primary side are fully on to provide a positive voltage across capacitor C_x and primary winding W_1. The ON-time of switches S_2 and S_3 makes up the time interval D_aT_s, and that of their complementary switches S_{r1} and S_{r2} makes up the interval $(1 - D_a)T_s$. Switches S_5, S_9 are fully turned-ON, and S_5, S_9 are turned-OFF. The ON-time of switches S_8 and S_{12} makes up time intervals D_1T_s and D_2T_s, respectively.

Switches S_7 and S_{11} are complementary switches to S_8 andS_{12}, respectively. Four distinct modes of operation exist for $v_{\text{in}} > 0$, the equivalent circuits of which are shown in Fig. 4. The leakage inductance is ignored for simplifying the analysis.

1) Mode-I [0∼ D_1T_s]: All four switches $S_1 - S_4$ on the primary side are intentionally turned ON [see Fig. 5(a)]. This creates two parallel switch paths (S_1, S_3 and S_2, S_4) for the storage of energy in input inductor L_{in} through the input source v_{in}. Additionally, capacitor C_x discharges and transfers its energy to the magnetizing inductor of HFT. The current through capacitor C_x is clamped to the magnetizing inductor current i_{Lm}, which is also divided into two parallel switch paths of S_1, S_2 and S_3, S_4. This splitting of currents reduce the current stresses of switches S_1 and S_4 to $(i_{Lin} - i_{Lm})/2$ and switches S_2 and S_3 to $(i_{Lin} + i_{Lm})/2$.

On the secondary side, switches S_{r1} and S_{r2} are turned-OFF, thus, no power is transferred on the secondary side. Meanwhile, switches S_5, S_8 of module-1 and switches S_9, S_{12} of module-2 are turned-ON. Capacitors C_{r1} and C_{r2} provide energy to their respective output inductors L_{f1} and L_{f2} and outputs

$$\{v_{Lin} = v_{\text{in}};\ v_{w1} = v_{Cx};\ v_{Lf1} = v_{Cr1} - v_{o1};\ v_{Lf2} = v_{Cr2} - v_{o2}. \tag{1}$$

2) Mode-II [$D_1T_s \sim D_aT_s$]: Switching signals and operation of primary side and module-2 of secondary side remain same. In module-1 of secondary side, switch S_8 is turned-OFF and switch S_7 is turned-ON [see Fig. 5(b)]. Output-1 is disconnected from capacitor C_{r1}, and inductor L_{f1} provides energy to output-1. Inductor L_{f1} current freewheels through switches S_5 and S_7

$$\{v_{Lin} = v_{\text{in}};\ v_{w1} = v_{Cx};\ v_{Lf1} = -v_{o1};\ v_{Lf2} = v_{Cr2} - v_{o2}. \tag{2}$$

3) Mode-III [$D_aT_s \sim D_2T_s$]: The primary side switches S_2, S_3 are turned-OFF and secondary side switches S_{r1}, S_{r2} are turned-ON [see Fig. 5(c)]. The energy stored in input source v_{in} and inductor L_{in} charges the primary side capacitor C_x and it is also transferred on secondary side and charge capacitors C_{r1} and C_{r2}. The energy stored in magnetizing inductor L_m is also reflected to secondary side and participate in the charging of capacitors C_{r1} and C_{r2}. Capacitor C_x current is clamped to input inductor current i_{Lin}. The switching states and operation of secondary side modules-1 and 2 remains the same

$$\begin{cases} v_{Lin} = v_{in} - v_{Cx} - \frac{v_{Cr1}}{N};\ v_{w2} = v_{cr1,2} \\ v_{Lf1} = -v_{o1}; v_{Lf2} = v_{Cr2} - v_{o2}. \end{cases} \tag{3}$$

4) Mode-IV [$D_2T_s \sim T_s$]: The primary side and secondary side operations remain the same except for the module-2 which undergoes transition [see Fig. 5(d)]. Switch S_{12} is turned-OFF and S_{11} is turned-ON. Output-2 is disconnected from main circuit and it is supplied from inductor L_{f2} through switches S_9 and S_{11}

$$\begin{cases} v_{Lin} = v_{\text{in}} - v_{Cx} - \frac{v_{Cr1}}{N};\ v_{w2} = v_{cr1,2} \\ v_{Lf1} = -v_{o1}; v_{Lf2} = -v_{o2}. \end{cases} \tag{4}$$

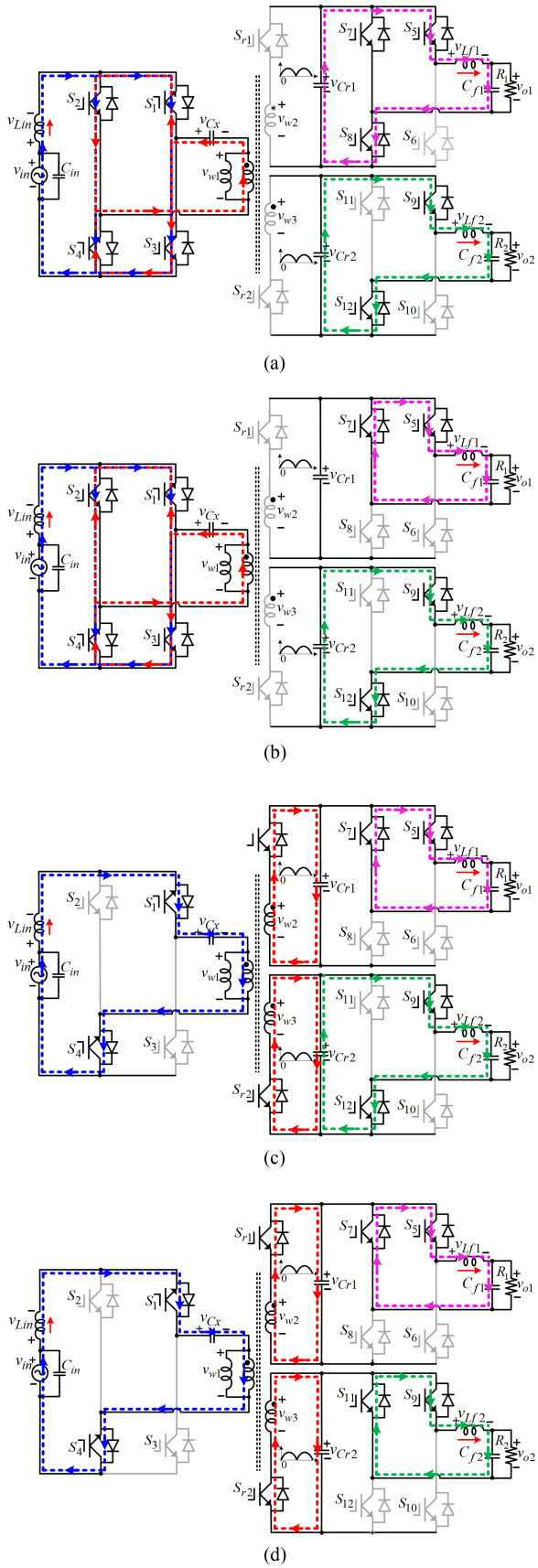


Fig. 5. Equivalent circuits for two in phase outputs with independent magnitudes. (a) Interval-1. (b) Interval-2. (c) Interval-3. (d) Interval-4.

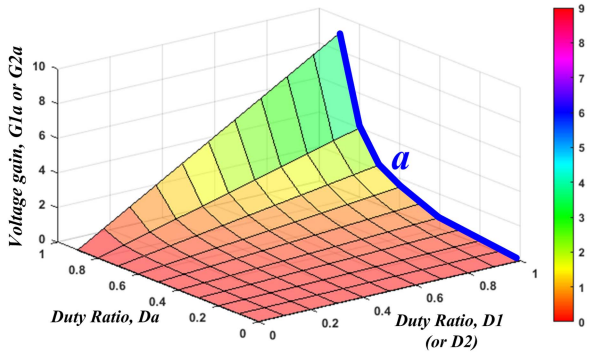


Fig. 6. Three-dimensional voltage gain plots versus two duty ratios.

By applying the voltage-second balance principle on magnetic components, the input-to-capacitors $C_{r1,2}$ voltage transfer ratio G_a ($= v_{Cr1,2}/v_{\text{in}}$) and the voltage transfer ratios G_1, G_2 from capacitors C_{r1} and C_{r2} to their respective outputs-1 and 2 (v_{o1}/v_{Cr1} and v_{o2}/v_{Cr2}) can be found as follows:

$$\begin{cases} G_a = \frac{v_{Cr1,2}}{v_{\text{in}}} = \frac{ND_a}{1-D_a} \\ G_1 = \frac{v_{o1}}{v_{cr1}} = D_{o1}; G_2 = \frac{v_{o2}}{v_{cr2}} = D_{o2}. \end{cases} \tag{5}$$

Then, the (overall) input-to-output voltage transfer ratios $G_{1a} = v_{o1}/v_{\text{in}}$ and $G_{2a} = v_{o2}/v_{\text{in}}$ for both outputs are given by

$$\left\{ G_{1a} = \frac{v_{o1}}{v_{\text{in}}} = \frac{ND_aD_1}{1-D_a};\ G_{2a} = \frac{v_{o2}}{v_{\text{in}}} = \frac{ND_aD_2}{1-D_a}. \right. \tag{6}$$

All three duty ratios D_a, D_1, and D_2 can be adjusted in the full range [0, 1] and are completely independent of each other. Moreover, the primary to secondary turns ratios N adds another degree of freedom for adjusting the voltage gains.

Fig. 6 depicts the three-dimensional (3-D) plot of variations of overall voltage gains G_{1a} (and G_{2a}) against switch duty ratios D_a, D_1 (and D_2). As observed, various combinations of both duty ratios D_a and D_1 (and D_2) can result in the same voltage gain G_{1a} (and G_{2a}). However, for optimal operation, D_1 (and D_2) can be set to 1, and modules-1 and 2 will work at line-frequency and only provide polarity shaping of capacitors C_{r1} and C_{r2} voltages across output-1 and 2. The resultant gain curve is highlighted by the bold blue line "*a*". If the two output voltages v_{o1} and v_{o2} are not equal, duty ratio D_a can be adjusted to raise capacitors C_{r1} and C_{r2} voltages at the required value of higher output voltage v_{o1} or v_{o2}. Then, the output module-1 or 2 corresponding to the higher output voltage can be modulated at line-frequency, and the other module can be modulated at switching-frequency to further step-down its output voltage to desired level.

B. In-Phase Output-1 and Antiphase Output-2 With Independent Magnitudes

The switch modulation strategy for producing in-phase output-1 and antiphase output-2 are illustrated in Fig. 7. The reference signals remain consistent with the previous mode. Moreover, the switch control signals of the primary stage, secondary side switches S_{r1}, S_{r2} and output module-1 remain unchanged. The only difference lies in the alteration of the switch control signals $S_9 - S_{12}$ of output module-2 to invert its output compared to the previous operation. Switches S_9 and S_{10} remain as power-frequency switches, but now switch S_9 is turned-OFF and S_{10} is turned-ON for the positive input voltage half-cycle ($v_{\text{in}} > 0$). Additionally, switches S_{11} and S_{12} are modulated at high-frequency by comparing reference signal $V_{ref2}$with v_{tri}. For $v_{\text{in}} > 0$, the ON-time of switches S_{11} constitutes mode-a (with duration of 0 to D_2T_s), and that of its complementary switch S_{12} constitutes mode-b (with duration D_2T_s to T_s). These two modes-a and b are a combination of the four actual modes (I, II, III, and IV) of operation. Mode-a comprises of modes I, II, and III as in the previous operation, wherein the primary side and module-1 undergo changes while module-2 operation remains unchanged. Mode-b is similar to mode-IV, in which module-2 undergoes a transition. The equivalent circuits of the proposed converter for mode-a and mode-b are depicted in Fig. 7.

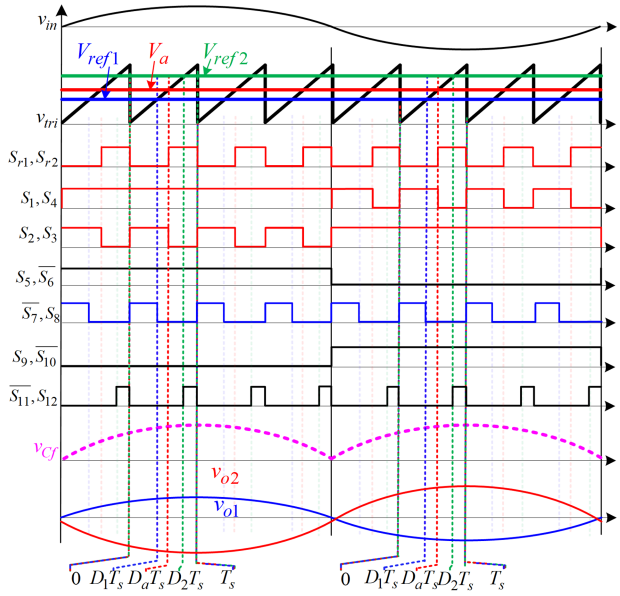


Fig. 7. Switch modulation signals for in-phase output-1 and antiphase output-2 of different magnitudes.

Mode-a [$0 \sim D_2T_s$]: This mode combines the mode-I [$0 \sim D_1T_s$], mode-II [$D_1T_s \sim D_aT_s$], and mode-III [$D_aT_s \sim D_2T_s$] of primary side and secondary side module-1 in previous operation. The operation of primary side and secondary module-I is highlighted using bold blue lines before their mode transition and dotted brown lines after mode transition, as shown in Fig. 8(a). For output module-2, switches S_{10} and $S_{11}$are turned-ON and $S_9, S_{12}$are turned-OFF. Capacitor C_{r2} provides energy to inductor L_{f2} and load-2. The negative voltage polarity of capacitor C_{r2} is applied across output *LC* filter $L_{f2}C_{f2}$, inverting the output voltage polarity

$$\{v_{Lf2} = -v_{Cr1} - v_{o2}. \tag{7}$$

Mode-b [$D_2T_s \sim T_s$]: Switch S_{11} is OFF and S_{12} is ON [see Fig. 8(b)]. Output-2 is disconnected from main circuit and it is

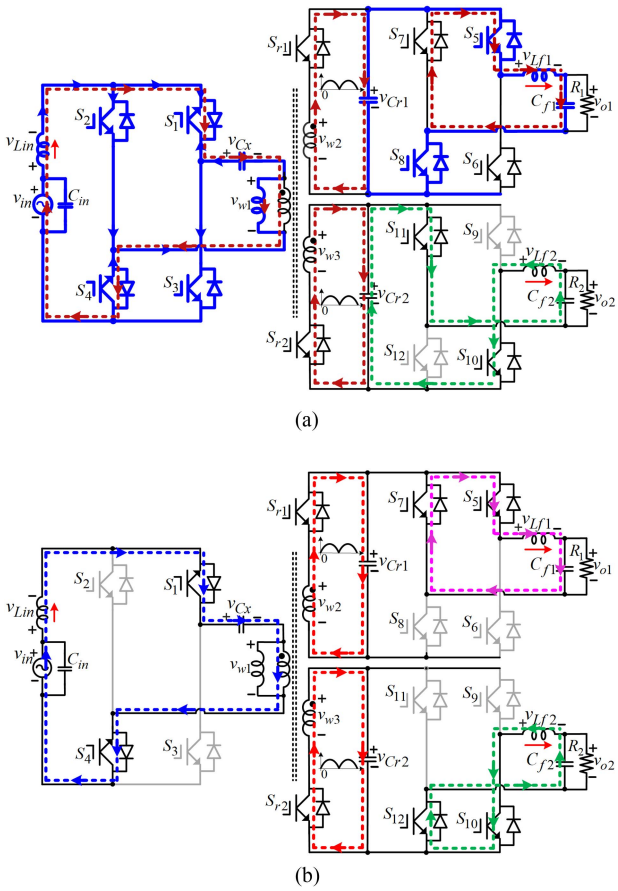


Fig. 8. Equivalent circuits for in-phase output-1 and antiphase output-2. (a) Mode-a. (b) Mode-b.

supplied from inductor L_{f2} through switches S_{10} and S_{12}

$$\{v_{Lf2} = -v_{o2}. \tag{8}$$

The input-to-output voltage transfer ratios for both outputs are given by

$$\left\{G_{1a} = \frac{v_{o1}}{v_{in}} = \frac{ND_aD_1}{1-D_a};\ G_{2a} = \frac{v_{o2}}{v_{in}} = -\frac{ND_aD_2}{1-D_a}. \right. \tag{9}$$

Negative sign "-" in expression of G_{2a} represents the inversion voltage polarity across output-2.

IV. Component Stress/Ripple Analysis and Design Guidelines

A. Semiconductor Device Voltage and Current Stresses

The switch voltage stresses v_s are given by

$$\left\{v_{s1-s4} = \frac{v_{o1,2}}{ND_aD_{1,2}};\ v_{sr1,2} = \frac{v_{o1,2}}{D_aD_{1,2}};\ v_{s5-s12} = \frac{v_o}{D_{1,2}}. \right. \tag{10}$$

By assuming $N = 1$, Fig. 9(a) shows the 3-D plot where z-axis represents the normalized switch voltage stress (v_s/v_o) with respect to duty ratios D_a and D_1 (or D_2). In general, switch voltage stresses increase with a decrease in D_a and D_1 (or D_2) or an increase in input voltage. Curve "a" depicts the variations in switches $S_1 - S_4$ and S_{r1}, S_{r2} voltage stresses when $D_1 = 1$ (or

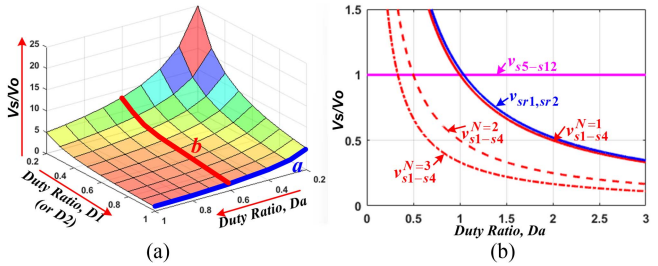


Fig. 9. Plots of normalized switch voltage stresses. (a) With variations in D_a and D_1 (or D_2). (b) With variations in N and D_a.

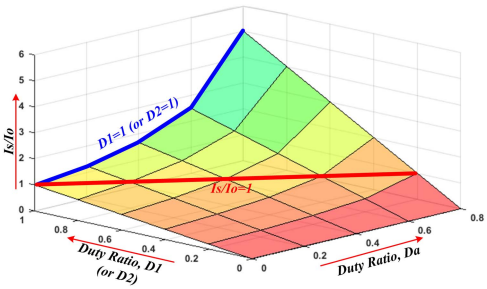


Fig. 10. Plots of normalized switch current stresses (z-axis) with variations in duty ratios.

$D_2 = 1$), indicating that both modules-1 and 2 operate at line-frequency to provide only voltage polarity shaping. In this case, voltage stresses would be minimum for a given input voltage. Curve "b" illustrates the variations in switch $S_5 - S_{12}$ voltage stresses for a fixed value of D_a (=0.6) and variations in D_1 (or D_2). Fig. 9(b) shows the 2-D plot of switch voltage stresses for variable N and D_a while keeping $D_1 = 1$ (or $D_2 = 1$). As observed, switch voltage stresses increase with a decrease in duty ratio D_a. Switch voltage stresses can be reduced by increasing N. However, this would result in higher current stresses of primary side switches. So, $N = 1$ would provide more balanced operation.

The switch current stresses i_s are given by

$$\left\{i_{s1-s4} = \frac{i_oD_{1,2}N}{(1-D_a)};\ i_{sr1,sr2} = \frac{i_oD_{1,2}}{(1-D_a)} \right. \\ \left. i_{s5-s12} = i_o. \right. \tag{11}$$

From (11), Fig. 10 show the plot of normalized switch current stresses (i_s/i_o) on z-axis (for $N = 1$), against variations in duty ratios D_a and D_1 (or D_2). As observed, the switch current stresses increase with the duty ratios. This occurs due to a decrease in input voltage v_{in} and a corresponding increase in input current $i_{\text{in}}$for a constant output voltage v_o and load power. Importantly, despite the primary module providing two secondary modules and, hence, primary current being $2G_{1,2a}i_o$, the current stresses of primary-side switches are the same as those of secondary-side switches S_{r1} and S_{r1} due to the innovative proposed switch modulation, which distributes current in two parallel switching paths. Switches $S_5 - S_{12}$ currents are unaffected by duty ratios as they only depend on load current/power.

B. Inductor Current Ripples and Design

The input inductor L_{in} has a current handling requirement of $i_{\text{in}}(= G_{1a}\ i_{o1} + G_{2a}i_{o2})$. The magnetizing inductor L_m of HFT

TABLE I
COMPARISONS WITH EXISTING CONVERTER TOPOLOGIES FOR FACL APPLICATIONS

Parameters		[18]	[19]	[20]	[30]	[31]	[32]	Proposed converter
Voltage transfer ratio ($\frac{v_o}{v_{in}}$)		$\pm D$	$\pm\frac{0.5-D_{1,2}}{0.5-D_i}$	$\pm\frac{D_{1,2}}{1-D_a}$	$\pm\frac{D}{1-D}$	$\frac{D}{1-D}$	$\frac{D}{2}$	$\pm\frac{D_aD_{1,2}}{1-D_a}$
Operations		Bipolar output with step-down magnitude	Bipolar output with step-down magnitude	Bipolar output with step-up and step-down magnitude	Bipolar output with step-up and step-down magnitude	Unipolar output with step-up and step-down magnitude	Bipolar output with step-down magnitude	Bipolar output with step-down and step-up magnitudes
Switching type		Hard switching	Hard switching	Hard switching	Hard switching	Soft-switching	Soft-switching	Hard switching
Discrete converters needed for FACL application		Six	Three	Three	Six	Six	Six	Three
Number of switching devices		$48(S_1-S_{48})$	$24(S_1-S_{24})$	$36(S_1-S_{36})$	$48(S_1-S_{48})$	$48(S_1-S_{48})$	$84(S_1-S_{84})$	42 (S_1-S_6)
Adjustable range of duty ratios		Flexible, [0, 1]	Limited [0, 0.5]	Flexible, [0, 1]	Flexible, [0, 1]	Flexible, [0, 1]	Flexible, [0, 1]	Flexible, [0, 1]
Input current		Discontinuous	Continuous	Continuous	Continuous	Continuous	Discontinuous	Continuous
Current sharing in input (high-current) side switches		No	No	No	Yes	No	No	Yes
Requirement of isolation transformers	Count	6	6		6	12		3
	Type	Bulky Low-frequency (50/60 Hz) transformers	Bulky Low-frequency (50/60 Hz) transformers	Compact High-frequency 20 kHz transformers	Bulky Low-frequency (50/60 Hz) transformers	Compact High-frequency 20 kHz transformers	Compact High-frequency 20 kHz transformers	Compact High-frequency 20 kHz transformers
Range of voltage magnitude and phase compensation		Limited	Limited	Flexible	Flexible	Limited	Limited	Flexible

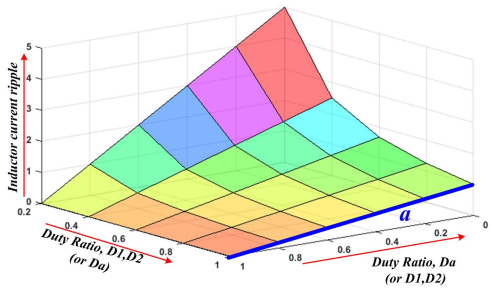


Fig. 11. Normalized inductor current ripples (z-axis) versus two duty ratios.

has a current handling requirement of $i_{o1}+i_{o2}$, and the output filter inductors L_{f1}, L_{f2} have current handling requirements of i_{o1} and i_{o2}, respectively.

The current ripples Δi_L of the input inductor L_{in}, magnetizing inductor L_m, and output filter inductors L_{f1}, L_{f2}, are given by

$$\begin{cases} \Delta\, i_{Lin} = \frac{v_o}{f_s L_{in}} \frac{(1-D_a)}{D_{1,2}} \\ \Delta\, i_{Lm} = \frac{v_o}{f_s L_m} \frac{(1-D_a)}{D_{1,2}} \\ \Delta\, i_{Lf1,2} = \frac{v_{o1,2}(1-D_{1,2})}{f_s L_{f1,2}}. \end{cases} \tag{12}$$

The normalized inductor current ripples ($\Delta i_L f_s L/v_o$) are plotted (on z-axis) in Fig. 11 as a function of D_a and D_1 (or D_2). Line "a" shows the minimum inductor current ripples, Δi_{Lin} and Δi_{Lm}, when $D_1=1$ (or $D_2=1$). The maximum current ripples will occur for minimum D_a (maximum input voltage v_{in}). The same curve also depicts the variation in $\Delta i_{Lf1,2}$ with $D_{1,2}$, which is maximum for minimum $D_{1,2}$. The maximum values of inductors L_{in}, L_m, and $L_{f1,2}$ can be determined from (12) by limiting their current ripples to a fraction "x" of their peak current stresses $I_{L,\text{peak}}$.

C. Capacitor Voltage Ripples and Design

The voltage stresses of capacitors C_x and $C_{1,2}$ are v_{in} and $v_{o1,2}/D_{1,2}$, respectively. The voltage ripples Δv_C of capacitors are given by

$$\begin{cases} \Delta\, v_{Cx} = \frac{i_{o1}+i_{o2}}{f_s L_{in}}\, D_a \\ \Delta\, v_{C1,2} = \frac{i_{o1,2}}{f_s L_{in}}\, D_{1,2}. \end{cases} \tag{13}$$

The maximum values of capacitors C_x and $C_{1,2}$ can be determined from (13) by limiting their voltage ripples to a fraction "y" of their peak voltage stresses $V_{C,\text{peak}}$.

V. COMPARISON WITH EXISTING FACL CONVERTERS

A detailed comparison of the salient features of the proposed and existing bipolar ac–ac converters provided in Table I for application in three-phase FACL configuration. The original nondifferential ac–ac converter [18] used in FACLs offers a limited voltage transfer ratio due to its buck-type operation, leading to restricted phase-shifting and discontinuous input current, which degrades power quality and requires input filters. It also needs six converters for three-phase implementation, increasing cost and complexity. Converter [19] reduces the converter count to three and ensures continuous input current but suffers from a narrow duty ratio (0–0.5), limited overall gain, and high voltage stress and ripple, resulting in increased cost and compromised power quality. A recently proposed high-efficiency bipolar dual-output ac–ac converter [20] addresses the limitations of [19] by providing a wider voltage gain range, lower voltage/current stresses and ripples, and reduced power losses. Nonetheless, it

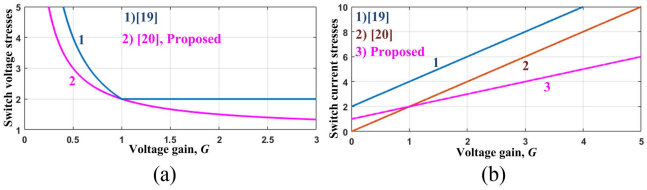


Fig. 12. Comparison of switching device stresses. (a) Switch voltage stress. (b) Switch current stress.

involves a higher number of semiconductor switches than [19]. These converters are nonisolated and require two line-frequency transformers per phase for electrical isolation, totaling six LFTs, which increase system size and losses.

Although several isolated bipolar ac–ac converters [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32] have been developed with integrated high-frequency transformers, none is specifically optimized for FACL applications. All these topologies are single-output, and therefore, realizing a three-phase FACL using these designs demands six converter modules, which significantly increases the number of HFTs, semiconductor switches, and passive components, leading to higher cost and larger system size.

In comparison, the proposed bipolar converter is the only reported high-frequency transformer isolated topology that can implement an FACL module with three discrete units due to its dual-output voltages. It also maintains continuous input and output currents, with duty ratios D_a, D_1, and D_2 controllable within a full range of [0, 1] independently of each other, providing a flexible range of buck and boost outputs. Importantly, the proposed converter integrates high-frequency transformer isolation using a three-winding transformer per phase, requiring only three HFTs to implement a three-phase FACL. Thus, the proposed converter significantly reduces magnetic volume and cost of the FACL converter.

The converters in [19] and [20], and the proposed topology are the only reported dual-output bipolar designs suitable for three-phase FACLs, offering the key advantage of requiring just three single-phase converters. However, unlike [19] and [20], the proposed converter integrates high-frequency transformer isolation, eliminating the need for bulky line-frequency transformers and offering a more compact and efficient solution. A comparison of normalized switch voltage stresses for the proposed converter and the converters in [19] and [20] is shown in Fig. 12(a). As observed, both the proposed topology and the converter in [20] exhibit significantly lower switch voltage stresses than the converter in [19] across the entire operating range In dual-output converters, including the proposed topology, the input-side phase module handles the combined power of both outputs, leading to higher current stress compared to single-output designs. However, the proposed converter, unlike [19] and [20], uses a switching strategy that enables current sharing among input-side switches during high-current intervals, effectively reducing stress and conduction losses. As shown in Fig. 12(b), the proposed design significantly lowers current stress (especially in boost mode) allowing for lower-rated, cost-effective switches with reduced losses.

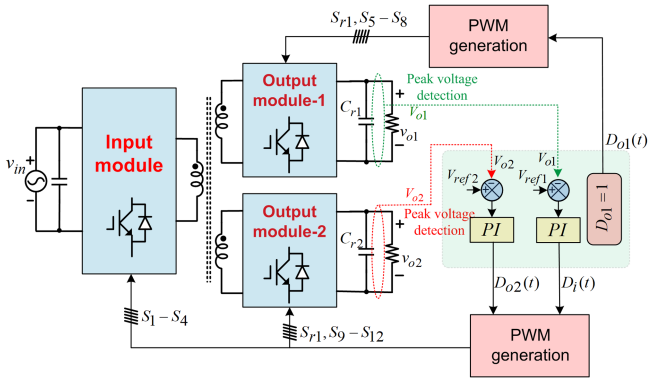


Fig. 13. Control block diagram of the proposed AC–AC converter.

TABLE II
COMPONENT SPECIFICATIONS AND EXPERIMENTAL CONDITIONS

Input line voltage (v_{in})	Buck	200 V_{peak}
	Boost	80 V_{peak}
Output voltages (v_{o1}, v_{o2})		100 V_{peak} or 150 V_{peak}
Switching devices ($S_1 - S_{12}$)		47N60CFD
Inductors (L_{in}, L_{f1}, L_{f2})		600 μH, 500 μH, 500 μH
Capacitors ($C_{in}, C_x, C_{r1,2}, C_{o1,2}$)		(2.2 μF , 4.4 μF, 4.4 μF, 4.4 μF)

VI. CLOSE-LOOP CONTROL OF THE PROPOSED CONVERTER

The control block diagram is presented in Fig. 13 for the condition when output module-1 voltage is larger than output module-2 voltage ($v_{o1} > v_{o2}$). The output voltages v_{o1} and v_{o2} are sensed, and their peak values (V_{o1} and V_{o2}) are detected using the method described in [33]. Since $V_{o1} > V_{o2}$, the duty ratio $D_1(t)$ is set to 1, and output module-1 operates at the line-frequency. The peak voltage V_{o1} is compared with the reference value V_{ref1}, and the error signal is processed by a PI controller to dynamically adjust the duty ratio $D_a(t)$ of primary side modules, thereby controlling the peak voltages (V_{Cr1} and V_{Cr2}) of capacitor C_{r1} and C_{r2} to reach V_{ref1}. Thus, with $D_1\ (t) = 1$, resulting in $V_{o1} = V_{Cr1} = V_{ref1}$. Simultaneously, V_{o2} is compared with V_{ref2}, and the corresponding PI controller adjusts duty ratio $D_1(t)$ to step-down V_{Cr2} through output module-2 and regulate V_{o2} to V_{ref2}.

Conversely, when $V_{o2} > V_{o1}$, $D_2\ (t) = 1$, and the PI controller based on the error between V_{o2} and V_{ref2} generates the dynamic duty ratio $D_a(t)$. Another PI controller processes the error between V_{o1} and V_{ref1} to dynamically control the duty ratio $D_1(t)$.

VII. SIMULATION AND EXPERIMENTAL VALIDATIONS

To verify the operation of the proposed converter, a simulation model was developed using PSIM software, and a hardware prototype was fabricated. The operating conditions and component values are listed in Table II. Both simulation and experimental results are conducted to confirm that the proposed converter can operate in various buck and boost modes, generating two output voltages with independently controlled polarity and magnitude, as required for three-phase FACL applications. To validate identical performance, both outputs were tested under the same voltage and power ranges but at different times, with

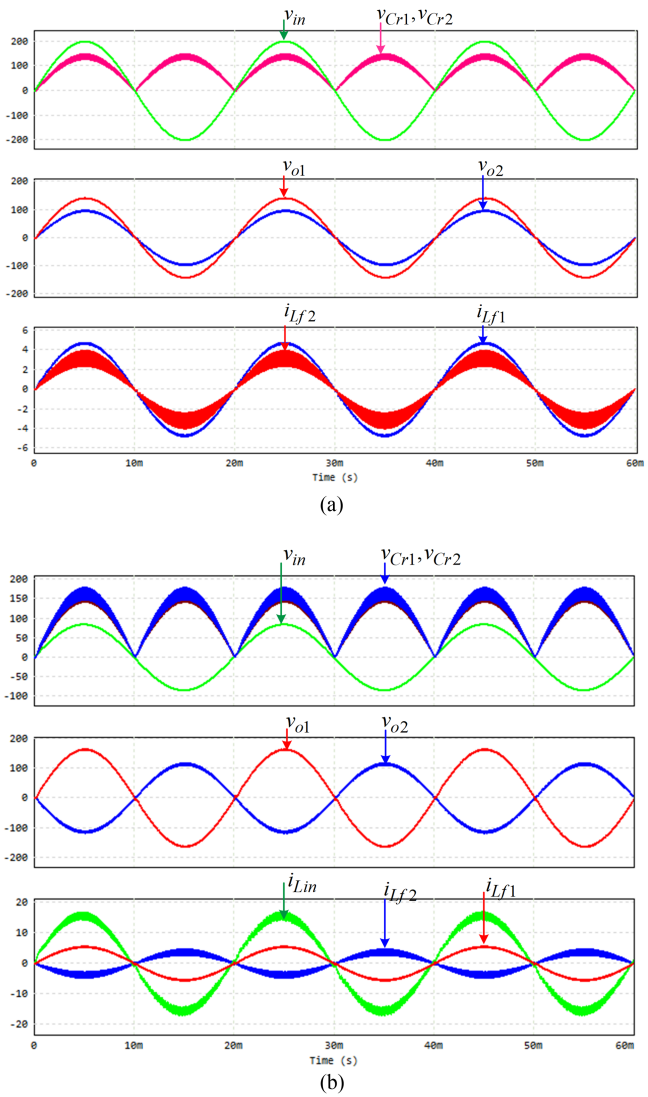


Fig. 14. Simulation waveforms of the proposed converter. (a) Both outputs are noninverting step-down with different magnitudes. (b) Output-1 is noninverting and output-2 is inverting with different step-up magnitudes.

alternating roles of two output modules between high-frequency and line-frequency operation. Due to the aforementioned requirements and limited component availability in the laboratory, same switching devices were used to implement all switches. It is worth mentioning that the voltage and current stresses, as well as power losses, remain identical for all switches within the same full-bridge module, such as $S_1 - S_4$ in the input side module, $S_5 - S_8$ in output module-1, and $S_9 - S_{12}$ in output module-2, due to symmetrical switching and conduction patterns. Each bridge can therefore be reliably implemented using industry-standard IGBT or MOSFET modules, ensuring a compact design with uniform electrical and thermal performance within the modules.

A. Simulation Verifications

Fig. 14(a) shows the simulated waveforms of the input voltage v_{in}, capacitor C_{r1}, C_{r2} voltages, output voltages v_{o1}, v_{o2}, and

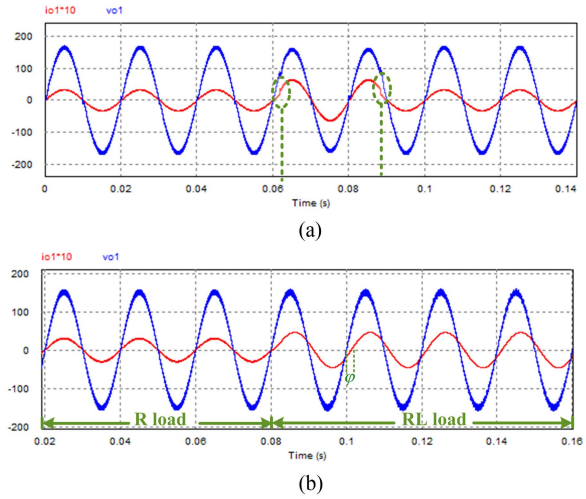


Fig. 15. Simulation results for dynamic response with step-change in load. (a) Resistive loads of different values. (b) Resistive to partial inductive load.

output inductor currents i_{Lf1}, i_{Lf2} for the noninverting buck operation of both outputs with different voltage magnitudes. The input voltage of 200 V_{peak} is stepped down to 150 V_{peak} across load-1 (of 30 Ω) and 100 V_{peak} across load-2 (of 30 Ω). In this case, a primary-side switch duty ratio D_a of 0.43 is selected to generate rectified voltages across capacitors C_{r1}, C_{r2} with a peak value of 150 V_{peak}. The output module-1 (comprising of switches $S_5 - S_8$) is modulated at line-frequency with $D_1 = 1$ to provide the inversion of capacitor C_{r1} voltage across load-1 with a peak value of 150 V_{peak}. Output module-2 (comprising of switches $S_9 - S_{12}$) is modulated with a duty ratio D_2 of 0.67 to step-down and invert the capacitor C_{r2} voltage, producing a voltage v_{o2} of 100 V_{peak} across load-2. As observed, inductor L_{f1} exhibits negligible current ripple since $D_1 = 1$, and it does not undergo high-frequency switching. In contrast, inductor L_{f2} experiences significant current ripple due to high-frequency switching at $D_2 = 0.67$.

Fig. 14(b) shows the simulated waveforms of the input voltage v_{in}, capacitor C_{r1}, C_{r2} voltages, output voltages v_{o1}, v_{o2}, and input/output inductor L_{in}, L_{f1}, and L_{f2} currents for the case of noninverting output-1 and inverting output-2 with different boost magnitudes. The input voltage of 80 V_{peak} is boosted to 150 V_{peak} across resistive load-1 (of 30 Ω) and 100 V_{peak} across resistive load-2 (of 30 Ω). In this case, the input voltage v_{in} is boosted using a duty ratio $D_a = 0.6$, providing a rectified voltage of 150 V_{peak} across capacitors C_{r1} and C_{r2}. Then, duty ratios $D_1 = 1$and $D_2 = 0.67$ are applied to generate ac voltages of 150 V_{peak} and 100 V_{peak} across loads-1 and -2, respectively. Again, the ripple in inductor L_{f1} current is much lower than in L_{f2} due to the absence of high-frequency switching. As observed, a continuous and low-ripple input current is achieved with a THD of 3.8%.

Fig. 15 shows the simulation results of the dynamic response of the proposed converter with load variations. Fig. 15(a) shows the output-1 voltage v_{o1} and output-1 current i_{o1} for a step-change in resistive load from 50 Ω to 25 Ω. As observed, the load current increases with heavy load, but the load voltage remains

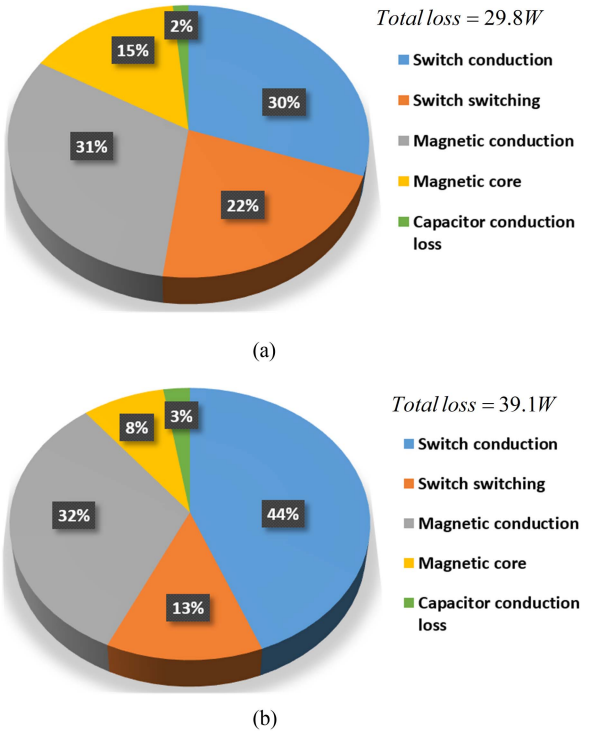


Fig. 16. Loss distribution of the proposed converter. (a) Buck operation. (b) Boost operation.

unchanged. Fig. 15(b) shows the load change from resistive (R) load of 50 Ω to partially inductive (RL) load of 30 Ω+40 mH. As observed, a phase shift φ, is observed between voltage and current with a lagging current. The power factor decreases from unity to 0.86. However, the operation remains normal, proving that the proposed converter is compatible with nonunity power factor loads and can support bidirectional power flow.

Fig. 16 illustrates the loss distribution of various components, including the conduction and switching losses of MOSFETS, conduction and core losses of magnetic elements, and ESR losses of the capacitor. The output voltage v_o is 150 V_{peak} and output load power is 600 W. Fig. 16(a) presents the loss distribution during buck operation with an input voltage v_{in} of 200 V_{peak}, while Fig. 16(b) depicts the same for boost operation with an input voltage of 80 V_{peak}.

B. Experimental Verifications

A hardware prototype was built to validate the theoretical analysis with the specifications listed in Table II. Figs. 17 and 18 show the experimental results for the buck operation. The input supply voltage v_{in} of 200 V_{peak} is used to produce output-1 voltage of $v_{o1} = 150$ V_{peak} and output-2 voltage of $v_{o2} = 100$ V_{peak}. The duty ratio D_a is set to 0.41 and duty ratios D_1 and D_2 are set at 1 and 0.67, respectively. Fig. 17(a) represents the waveforms of input voltage v_{in}, output voltages v_{o1}, v_{o2} and capacitor C_{r1} voltage when both outputs are noninverting. Fig. 17(b) shows the waveforms of input voltage v_{in}, output voltages v_{o1}, v_{o2} and output inductor current i_{Lf1} when output-1 is noninverting and output-2 is inverting. Fig. 18 shows the voltage stresses of

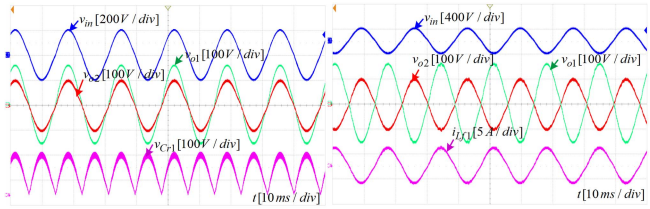


Fig. 17. Experimental results for buck operation with two different output voltage magnitudes. (a) Both outputs are noninverting. (b) Output-1 is noninverting and output-2 is inverting.

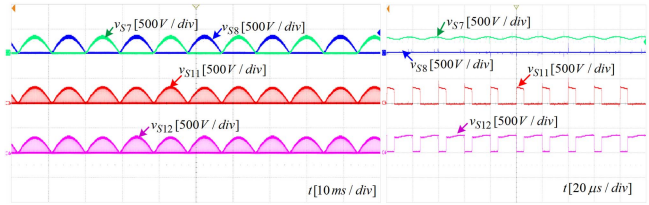


Fig. 18. (a) Experimental results of switch voltage stresses. (b) Zoom-in waveforms of Fig. 14(a).

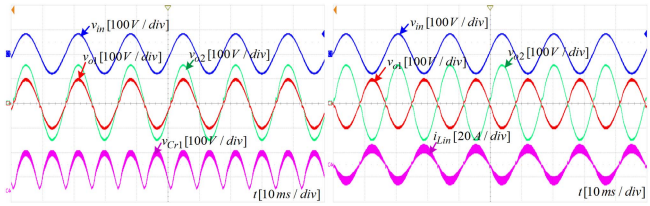


Fig. 19. Experimental results for boost operation with two different output voltage magnitudes. (a) Both outputs are noninverting. (b) Output-1 is noninverting and output-2 is inverting.

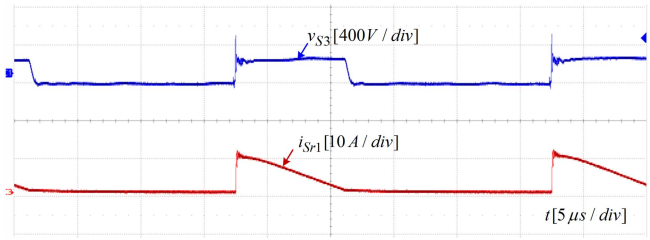


Fig. 20. High-frequency waveforms of switch voltage and current stresses.

switches S_7, S_8, S_{11}, and S_{12} on secondary side. As observed, the switches S_7, S_8 of secondary module-1 have low-frequency voltage stresses, which is in consistent with their function as line-frequency unfolding switches.

Figs. 19 and 20 present the experimental results for boost operation. The low input voltage v_{in} of 80 v_{peak} is stepped-up to $v_{o1} = 100$ V_{peak} across load-1 and $v_{o2} = 150$ V_{peak} across load-2. The duty ratio D_a is set to 0.65, and duty ratios D_1 and D_2 are set at 0.67 and 1, respectively. In Fig. 19(a), the measured waveforms include the input voltage v_{in}, the voltages of output-1 v_{o1}, output-2 v_{o2}, and capacitor $C_{r1}$when both outputs are noninverting. Fig. 19(b) shows the waveforms of $v_{\text{in}}, v_{o1}, v_{o2}$ and

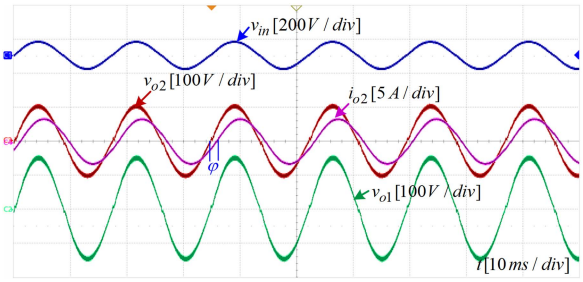


Fig. 21. Experimental results of input and output voltages and currents for boost operation with RL load.

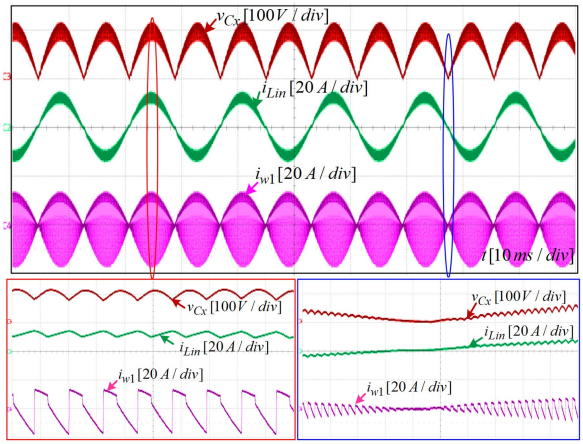


Fig. 22. Experimental results of primary capacitor voltage, input inductor current, and primary winding current for boost operation.

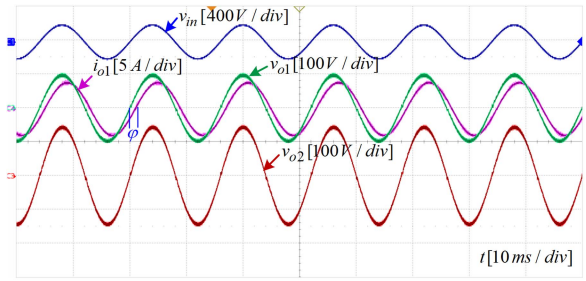


Fig. 23. Experimental results of input and output voltages and currents for buck operation with RL load.

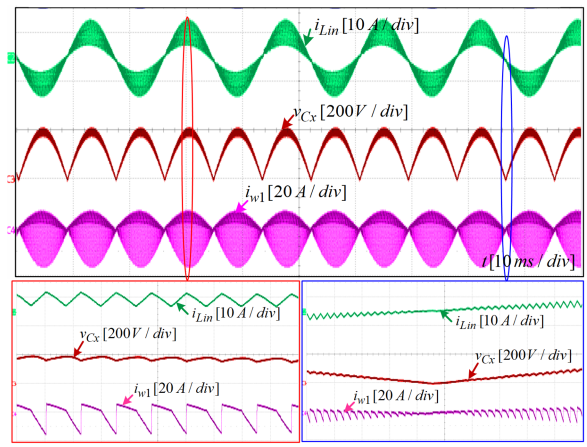


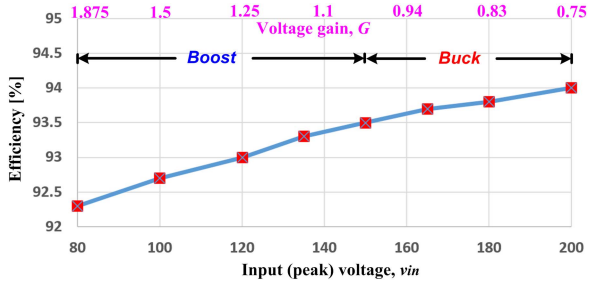
Fig. 24. Experimental results of primary capacitor voltage, input inductor current, and primary winding current for buck operation.

input inductor current i_{Lin} when output-1 is noninverting, and output-2 is inverting. Fig. 21 shows the voltage across switch S_3 and the current through switch S_{r1} (same as the secondary winding current). As observed, voltage spikes occur due to the leakage inductance of the HFT, since the energy stored in the transformer has no path to circulate. Interleaved winding with copper foil can help reduce leakage inductance and suppress these spikes. Alternatively, *RC* snubbers can be connected across the switches by first calculating the leakage inductance and stored energy ($E = 0.5L_K \times I^2$), then determining the snubber capacitance using $E = 0.5C_S \times V_S{}^2$, and the resistance using $(E/(D \times T_S)) = (V_S{}^2/R_S)$. The HFT in the proposed converter operates similarly to that in an isolated SEPIC converter, enabling the use of regenerative snubbers developed for SEPIC topologies [34], [35] in future applications.

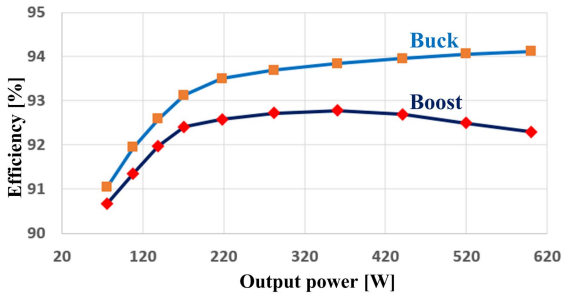
Figs. 21 and 22 present the experimental results for boost operation with a partially inductive load. The input voltage is $v_{\text{in}} = 80\ v_{\text{peak}}$, while the output voltages are $v_{o1} = 150\ v_{\text{peak}}$ and $v_{o2} = 100\ v_{\text{peak}}$. In Fig. 19, the waveforms of v_{in}, v_{o1}, v_{o2}, and i_{o2} are shown when an RL load with $R = 30\ \Omega$ and $L = 20$ mH is connected across load-2. A clear phase shift is observed between v_{o2} and i_{o2}, where the current lags the voltage by an angle φ. Fig. 22 shows the voltage across capacitor C_x, input inductor current i_{Lin}, and current flowing through the transformer primary winding i_{w1}. Enlarged waveforms near peak and zero-crossing points confirm the smooth transitions and normal operation.

Figs. 23 and 24 illustrate the experimental results for buck operation under similar partially inductive loading. Here, the input voltage is $v_{\text{in}} = 200\ v_{\text{peak}}$, and the output voltages are $v_{o1} = 100\ v_{\text{peak}}$ and $v_{o2} = 150\ v_{\text{peak}}$. Fig. 23 shows the waveforms of v_{in}, v_{o1}, v_{o2}, and i_{o1} with an RL load now connected to load-1, where $R = 28\ \Omega$ and $L = 20$ mH. Fig. 24 displays the voltage across capacitor C_x, input inductor current i_{Lin}, and transformer primary winding current i_{w1}. All measured waveforms remain within expected ranges, validating the circuit's reliable performance.

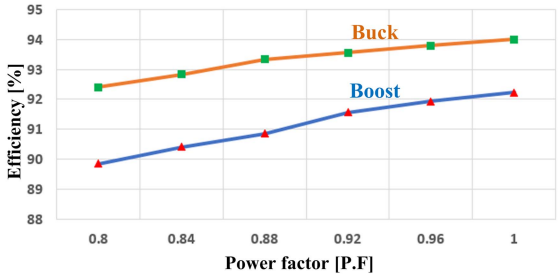
Fig. 25(a) illustrates the measured power conversion efficiency of the proposed converter for both buck and boost operations over a wide input voltage v_{in} range of $80\ V_{\text{peak}} \sim 200\ V_{\text{peak}}$. Both output voltages are constant at $80\ V_{\text{peak}}$ with resistive loads of 300 W each. The resultant gain G variation is 0.7 to 1.875. The efficiency degradation in boost mode at low input voltages is primarily due to increased conduction losses. Since the output power and voltage remain constant, lower input voltages result in higher input currents, which elevate conduction losses in switches and passive components. This trend aligns with the loss breakdown shown in Fig. 16, where boost mode exhibits higher total losses compared to buck mode at rated power due to the dominance of conduction losses. Fig. 25(b) presents the measured efficiency versus output power for both buck and boost operations. In this case, $v_{\text{in}} = 200\ V_{\text{peak}}$ for buck operation and $v_{\text{in}} = 80\ V_{\text{peak}}$ (boost mode), while both output voltages are



(a)



(b)

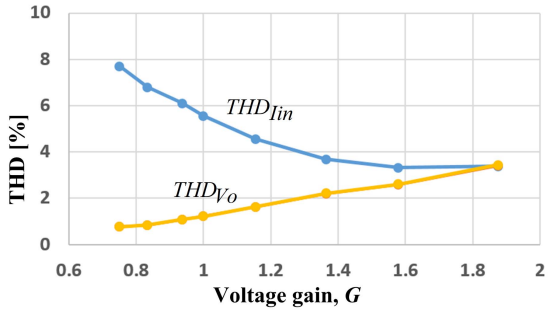


(c)

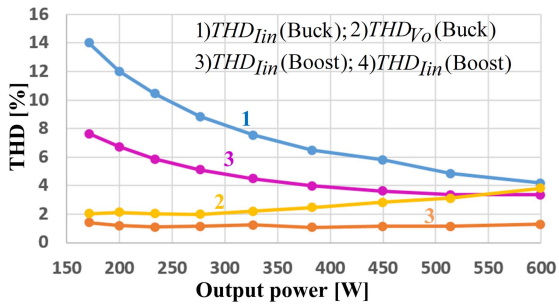
Fig. 25. Measured efficiency of the proposed converter. (a) With variations in input voltage or voltage gain. (b) With variation in output power. (c) With variations in load power factor.

$v_o = 150\ V_{\text{peak}}$. The output power is varied by changing the resistive load across both outputs. As observed, the buck-mode efficiency decreases with lower output power due to relatively more dominant switching and core losses. In contrast, the boost-mode efficiency tends to improve slightly with reduced output power due to the alleviation of conduction losses. Fig. 25(c) presents the measured efficiency versus power factor for both buck and boost operations. For buck mode, the input voltage was set to $v_{\text{in}} = 200\ v_{\text{peak}}$, and for boost mode $v_{\text{in}} = 80\ v_{\text{peak}}$. In both cases, the output voltage v_o was regulated at 150 v_{peak}, and the active load power was maintained at P_o= 560 W. The power factor was reduced by increasing the load inductance, while the resistance was adjusted to maintain constant active power. As shown, efficiency declines with lower power factor due to increased apparent power, which raises conduction currents and associated losses.

Fig. 26(a) shows the measured THD of the input current THD_{Iin} and output voltages THD_{Vo} (for noninverting output-1 and inverting output-2) for both buck and boost operations under varying voltage gain. The output voltage v_o is maintained at 150 V_{peak}, and the output power is fixed at 600 W. The voltage gain is varied by changing the input voltage v_{in} from 80 V_{peak} to 200 V_{peak}. Fig. 26(b) presents the variations in THD



(a)



(b)

Fig. 26. Measured THD of the proposed converter. (a) With variations in voltage gain. (b) With variations in output power.

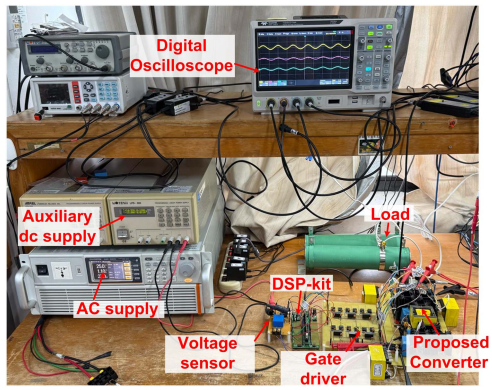


Fig. 27. Picture of the laboratory setup with proposed converter hardware.

of the input current THD_{Iin} and output voltage THD_{Vo} for different output power levels in both buck ($v_{\text{in}} = 200\ V_{\text{peak}}$) and boost ($v_{\text{in}} = 80\ V_{\text{peak}}$) modes, with a fixed output voltage v_o of 150 V_{peak}. The input current exhibits higher THD during buck operation, particularly at lower output power levels. This is attributed to the decrease in the fundamental input current while the inductor current ripple remains relatively constant. Fig. 27 shows the proposed converter hardware and laboratory setup. The experimental results validate the operation and benefits of the proposed converter.

VIII. Conclusion

This article proposes an isolated bipolar buck–boost ac–ac converter that uses an integrated three-winding high-frequency transformer with two independently controlled bipolar outputs. The proposed converter offers various significant features,

including continuous low ripple input and output powers, reversible operation compatible with nonunity power factor loads, and elimination of commutation issues in existing bidirectional ac switch-based converters. Compared to existing flexible ac-link converters, the proposed converter provides two bipolar outputs with independently adjustable step-down and step-up voltage magnitudes and polarities. Moreover, it uses an integrated high-frequency transformer to electrically decouple the input from two outputs, thereby saving two sizeable and costly line-frequency transformers required for counterpart converters, ensuring a compact and cost-effective design. In addition, the proposed converter provides current sharing of input side high-current switches, which relieves their current stresses. Theoretical claims of the proposed converter are verified through extensive simulation and experimental results. Future studies can explore modular multilevel configurations of the proposed topology to enhance both voltage and current handling, and investigate their three-phase implementations with independent control of output voltage magnitudes and phase angles.

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