A General Low-Frequency Zero-Sequence Circulating Current Suppression Approach for Coordinated PWM Schemes in Two-Parallel Three-Phase Two-Level Power Converters

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***Abstract*—This article addresses the challenge of mitigating low-frequency circulating currents caused by imbalanced inductance while preserving the inherent benefits of coordinated pulsewidth modulation (PWM) schemes. The analysis reveals that traditional common-mode injection is incompatible with the coordinated PWM schemes. To resolve this, this article proposes a general approach to suppress the low-frequency circulating current for the coordinated PWM schemes. Unlike the traditional common-mode signal injection, the proposed method features the different-mode signal injection into different phases at specific vector angles. The proposed method preserves the intricate vector sequences of coordinated PWM schemes, maintaining their original benefits. Moreover, a comprehensive control model and structure are developed to support differential-mode signal injection. Finally, two typical coordinated PWM schemes were chosen as case studies, covering both clamping and nonclamping methods. The proposed method was applied to these schemes to suppress low-frequency circulating currents, and the effectiveness was validated through testing on a prototype. Experimental results confirm that the proposed method effectively suppresses low-frequency circulating currents while retaining the performance characteristics of the original PWM schemes. This article is a progressive extension of the existing coordinated PWM schemes to enhance their practical applicability.**

***Index Terms*—Common mode voltage, line current ripple, low-frequency circulating current, paralleled interleaved three-phase inverter.**

I. Introduction

THE growing demand for high-power systems in applications such as high-power motor drives, wind power generation, mining hoists, and electric vehicle charging stations has spurred the implementation of parallel power inverters [1]. In the context of electric and hybrid aircraft, the need for reliable, efficient, and compact power conversion systems is even more critical. The two-parallel converter topology, which features paralleled dc links and ac terminals interconnected via filter inductors, has gained prominence in these applications due to its ability to manage higher power levels and reduce system size (see Fig. 1).

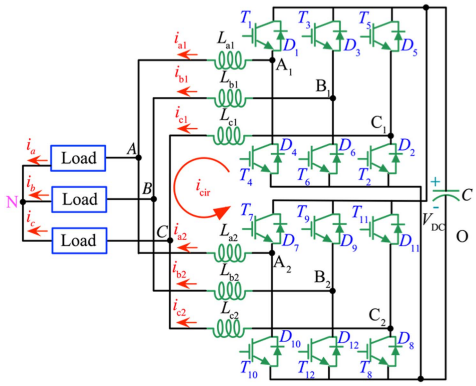

Fig. 1. The two interleaved paralleled three-phase two-level inverter.

In electric aircraft, the performance of power converters is susceptible to switching-related indicators, including line-current ripple, high-frequency zero-sequence circulating current, and common-mode voltage. For instance, a higher zero-sequence circulating current requires a larger filter inductance. This leads to more energy losses and lower efficiency, which are particularly problematic in aircraft with limited space and weight. Additionally, common-mode voltage presents significant challenges in terms of electromagnetic interference, potential damage to insulation, and the generation of common-mode currents, all of which can affect the reliability and performance of critical aircraft systems. Furthermore, excessive ripple in the line current leads to increased noise and vibration—issues that directly impact the comfort and safety of passengers and crew.

The pulsewidth modulation (PWM) schemes play significant roles in managing switching-related performance indicators. Existing PWM schemes for two parallel converters fall into independent [2], [3], [4], [5] and coordinated PWM [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], as shown in Fig. 2. The

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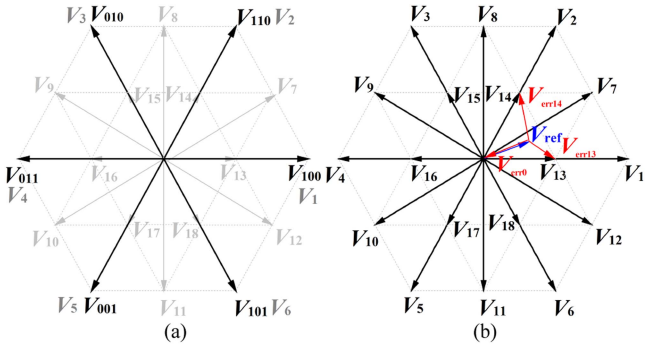

Fig. 2. Space-vector plane of (a) the independent PWM scheme and (b) the coordinated PWM scheme within the centralized architecture.

TABLE I
VECTOR SEQUENCES OF EXISTING METHODS

AZSPWM	V_0	→	V_7	→	V_1	→	V_7	→	V_0
VSC_1	V_{010}		V_{110}		V_{100}		V_{100}		V_{101}
VSC_2	V_{101}		V_{100}		V_{100}		V_{110}		V_{010}
MDPWM	V_7	→	V_1	→	V_0	→	V_1	→	V_7
VSC_1	V_{100}		V_{100}		V_{000}		V_{100}		V_{110}
VSC_2	V_{110}		V_{100}		V_{000}		V_{100}		V_{100}
TLSVM	V_0	→	V_{13}	→	V_7				
VSC_1	V_{101}		V_{101}		V_{100}				
VSC_2	V_{010}		V_{110}		V_{110}				
HPDPWM	V_{13}	→	V_{14}	→	V_0	→	V_{14}	→	V_{13}
VSC_1	V_{101}		V_{111}		V_{111}		V_{110}		V_{110}
VSC_2	V_{110}		V_{110}		V_{111}		V_{111}		V_{101}
LCPWM	V_{13}	→	V_0	→	V_{14}	→	V_{13}	→	V_0
VSC_1	V_{101}		V_{101}		V_{100}		V_{100}		V_{000}
VSC_2	V_{110}		V_{010}		V_{010}		V_{000}		V_{000}
ODPWM	V_{14}	→	V_{13}	→	V_0	→	V_{13}	→	V_{14}
VSC_1	V_{100}		V_{100}		V_{000}		V_{000}		V_{010}
VSC_2	V_{010}		V_{000}		V_{000}		V_{100}		V_{100}
ZCMV	V_0	→	V_7	→	V_{12}	→	V_0		
VSC_1	V_{000}		V_{100}		V_{101}		V_{111}		
VSC_2	V_{111}		V_{110}		V_{100}		V_{000}		

independent PWM modulates each converter separately with the original eight vectors, disregarding coordination between two converters [2], [3], [4], [5]. Notably, the 64 ($= 8\times8$) vector combinations from each converter's eight vector results yield 19 equivalent vectors on the vector plane. This redundancy allows for greater flexibility in optimizing the switching-related performance indicators. The coordinated PWM schemes strategically manage all 64 vector combinations to optimize performance indicators, as shown in Fig. 2(b).

It is important to note that the modulation strategies for two-parallel and multi-parallel (three or more) converters are fundamentally different and belong to distinct research areas. In multi-parallel converters, the large number of vector combinations makes coordinated PWM design impractical, and no coordinated PWM scheme has been reported for such systems [17], [18]. This article focuses explicitly on two parallel converters.

Table I further details the vector sequences of these coordinated PWM schemes. These schemes are characterized by the optimal vector selections (coordination between two converters) and their strategic arrangement within each carrier period (vector sequences). For example, Zeng et al.'s [7] line current ripple minimization PWM (LCPWM) and He et al.'s [8] modified DPWM (MMDPWM) apply near-three-vectors to minimize line current ripples. Besides, Quan and Li [9] three-level space vector modulation (TLSVM), Gohil et al.'s active-zero-state-vector PWM (AZSPWM) and their modified discontinuous PWM (MDPWM) [11] focus on selecting vectors that benefit suppressing high-frequency zero-sequence circulating currents. Moreover, Jiang et al.'s [12] zero common mode voltage (ZCMV)and Zeng and Goetz [13] modified zero common mode voltage (MZCMV) method apply the vector with zero-common mode voltage. Additionally, Zeng et al. proposed optimal discontinuous PWM (ODPWM) and high-performance discontinuous PWM (HPDPWM) [15] to address zero-sequence circulating currents and refine line current ripples. Notably, those coordinated PWM schemes fundamentally rely on the precise selection and arrangement of vectors, which is crucial for optimizing switching-related performance indicators.

On the other hand, the unavoidable manufacturing tolerances result in imbalanced inductances between parallel converters, invariably causing significant low-frequency zero-sequence circulating currents [2], [3], [4], [5]. While existing research has extensively examined the impact of these imbalances on coordinated PWM performance [3], it has not proposed effective solutions to suppress these currents within the coordinated PWM schemes. Notably, these low-frequency circulating currents lead to magnetic core saturation because ferrite materials, which are designed to suppress high-frequency zero-sequence circulating currents, have reduced permeability at low frequencies.

As evidenced by [2], [3], [4], [5], independent PWM schemes commonly inject common-mode signals into one converter to counteract these currents caused by imbalanced inductance. However, our analysis reveals a significant limitation: the common-mode voltage injection approach disrupts the vector sequences of the coordinated PWM schemes. Notably, the coordinated PWM schemes rely on intricate vector sequences to optimize the switching performance-related indicators. The disrupted vector sequences by the common mode injection led to unpredictable outcomes and unclear performance impacts. In other words, the fundamental challenge is to mitigate low-frequency circulating currents while maintaining the inherent benefits of the coordinated PWM scheme. While both unbalanced loads and uneven inductance can cause low-frequency circulating currents, this article focuses on the circulating current caused by inductance imbalance. The case of unbalanced loads is beyond the scope of this article.

This article aims to fill this gap by developing a general approach that seamlessly aligns with coordinated PWM schemes to suppress low-frequency zero-sequence circulating currents. The approach extends existing coordinated PWM schemes to enhance their suitability for real-world implementation. Instead of the common-mode injection, the presented general approach features the different-mode signals injection to different phases at different vector angles. This differential-mode injection strategically modifies the original modulation signals to enable uneven duty ratio redistribution, which preserves the integrity of the original vector sequences while effectively suppressing low-frequency circulating currents. Furthermore, we propose a comprehensive control model that establishes a foundational control structure, and based on this model, we design the general

TABLE II
TWO-PARALLELED INTERLEAVED CONVERTER'S ZERO-SEQUENCE CIRCULATING CURRENT CHANGE RATES AND CMVS OF AVAILABLE VOLTAGE VECTORS

		VSC_2							
		$\mathbf{V_{000}}$	$\mathbf{V_{100}}$	$\mathbf{V_{110}}$	$\mathbf{V_{010}}$	$\mathbf{V_{011}}$	$\mathbf{V_{001}}$	$\mathbf{V_{101}}$	$\mathbf{V_{111}}$
VSC_1	$\mathbf{V_{000}}$	$\mathbf{V_0(-V_{DC}/2, 0)}$	$\mathbf{V_{13}(-V_{DC}/3, -1)}$	$\mathbf{V_{14}(-V_{DC}/6, -2)}$	$\mathbf{V_{15}(-V_{DC}/3, -1)}$	$\mathbf{V_{16}(-V_{DC}/6, -2)}$	$\mathbf{V_{17}(-V_{DC}/3, -1)}$	$\mathbf{V_{18}(-V_{DC}/6, -2)}$	$\mathbf{V_0(0, -3)}$
	$\mathbf{V_{100}}$	$\mathbf{V_{13}(-V_{DC}/3, 1)}$	$\mathbf{V_1(-V_{DC}/6, 0)}$	$\mathbf{V_7(0, -1)}$	$\mathbf{V_{14}(-V_{DC}/6, 0)}$	$\mathbf{V_0(0, -1)}$	$\mathbf{V_{18}(-V_{DC}/6, 0)}$	$\mathbf{V_{12}(0, -1)}$	$\mathbf{V_{13}(V_{DC}/6, -2)}$
	$\mathbf{V_{110}}$	$\mathbf{V_{14}(-V_{DC}/6, 2)}$	$\mathbf{V_7(0, 1)}$	$\mathbf{V_2(V_{DC}/6, 0)}$	$\mathbf{V_8(0, 1)}$	$\mathbf{V_{15}(V_{DC}/6, 0)}$	$\mathbf{V_0(0, 1)}$	$\mathbf{V_{13}(V_{DC}/6, 0)}$	$\mathbf{V_{14}(V_{DC}/3, -1)}$
	$\mathbf{V_{010}}$	$\mathbf{V_{15}(-V_{DC}/3, 1)}$	$\mathbf{V_{14}(-V_{DC}/6, 0)}$	$\mathbf{V_8(0, -1)}$	$\mathbf{V_3(-V_{DC}/6, 0)}$	$\mathbf{V_9(0, -1)}$	$\mathbf{V_{16}(-V_{DC}/6, 0)}$	$\mathbf{V_0(0, -1)}$	$\mathbf{V_{15}(V_{DC}/6, -2)}$
	$\mathbf{V_{011}}$	$\mathbf{V_{16}(-V_{DC}/6, 2)}$	$\mathbf{V_0(0, 1)}$	$\mathbf{V_{15}(V_{DC}/6, 0)}$	$\mathbf{V_9(0, 1)}$	$\mathbf{V_4(V_{DC}/6, 0)}$	$\mathbf{V_{10}(0, 1)}$	$\mathbf{V_{17}(V_{DC}/6, 0)}$	$\mathbf{V_{16}(V_{DC}/3, -1)}$
	$\mathbf{V_{001}}$	$\mathbf{V_{17}(-V_{DC}/3, 1)}$	$\mathbf{V_{18}(-V_{DC}/6, 0)}$	$\mathbf{V_0(0, -1)}$	$\mathbf{V_{16}(-V_{DC}/6, 0)}$	$\mathbf{V_{10}(0, -1)}$	$\mathbf{V_5(-V_{DC}/6, 0)}$	$\mathbf{V_{11}(0, -1)}$	$\mathbf{V_{17}(V_{DC}/6, -2)}$
	$\mathbf{V_{101}}$	$\mathbf{V_{18}(-V_{DC}/6 ,2)}$	$\mathbf{V_{12}(0, 1)}$	$\mathbf{V_{13}(V_{DC}/6, 0)}$	$\mathbf{V_0(0, 1)}$	$\mathbf{V_{17}(V_{DC}/6, 0)}$	$\mathbf{V_{11}(0, 1)}$	$\mathbf{V_6(V_{DC}/6, 0)}$	$\mathbf{V_{18}(V_{DC}/3, -1)}$
	$\mathbf{V_{111}}$	$\mathbf{V_0(0, 3)}$	$\mathbf{V_{13}(V_{DC}/6, 2)}$	$\mathbf{V_{14}(V_{DC}/3, 1)}$	$\mathbf{V_{15}(V_{DC}/6, 2)}$	$\mathbf{V_{16}(V_{DC}/3, 1)}$	$\mathbf{V_{17}(V_{DC}/6, 2)}$	$\mathbf{V_{18}(V_{DC}/3, 1)}$	$\mathbf{V_0(V_{DC}/2, 0)}$

* The first item in parentheses represents the common mode voltage, while the second item in parentheses denotes the normalized rate of change of the high-frequency zero-sequence circulating current as $V_{DC}/(L_1+L_1)$.

approach to facilitate the differential mode injection. Finally, as illustrative examples, we have adapted two coordinated PWM schemes using our proposed general approach. Experimental results show that the method effectively suppresses low-frequency circulating currents to negligible levels under various operating conditions while maintaining the original characteristics of high-frequency components with nearly identical spectra. The proposed method successfully addresses the core challenge of mitigating low-frequency circulating currents while maintaining the inherent benefits of coordinated PWM schemes.

II. BASICS OF THE TWO PARALLEL INTERLEAVED CONVERTERS WITH CENTRALIZED CONTROL ARCHITECTURE

As Fig. 2(a) illustrates, each converter has eight switching states, including six active vectors and two zero-voltage vectors ($\boldsymbol{V_{111}}$/$\boldsymbol{V_{000}}$). The independent PWM scheme modulates each converter independently using those eight vectors. On the other hand, the equivalent output voltages of two parallel converters are the combined output voltage from the two converters:

$$\begin{cases} u_{aN} = [(2S_{a1} + 2S_{a2}) - (S_{b1} + S_{b2}) - (S_{c1} + S_{c2})]\, V_{\mathrm{DC}}/6 \\ u_{bN} = [(2S_{b1} + 2S_{b2}) - (S_{a1} + S_{a2}) - (S_{c1} + S_{c2})]\, V_{\mathrm{DC}}/6 \\ u_{cN} = [(2S_{c1} + 2S_{c2}) - (S_{b1} + S_{b2}) - (S_{a1} + S_{a2})]\, V_{\mathrm{DC}}/6 \end{cases} \tag{1}$$

where x (= 1, 2) enumerates the two paralleled inverters, N denotes the neutral point; S_{a1}, S_{b1}, S_{c1}, S_{a2}, S_{b2}, and S_{c2}, respectively denote the states of S_1, S_3, S_5, S_7, S_9 and S_{11} (see Fig. 1); for example, when $S_{b1} = 0$, S_3 is OFF; if $S_{b1} = 1$, S_3 is ON.

As Fig. 2(b) and Table II illustrate, these 64 combinations produce 19 unique output voltages ($\boldsymbol{V_0}\sim\boldsymbol{V_{18}}$), providing greater redundancy and flexibility for vector sequence design. For example, the common mode voltage is determined by the switching state combinations from the two converters:

$$u_{\mathrm{NO}} = \frac{[(S_{a2} + S_{a1}) + (S_{c2} + S_{c1}) + (S_{b2} + S_{b1})]\, V_{\mathrm{DC}}}{6} - \frac{V_{\mathrm{DC}}}{2}. \tag{2}$$

In addition, switching state combinations from the two converters determine the rates of change of the high-frequency zero-sequence circulating current

$$\frac{\Delta i_{\mathrm{cir}}}{\Delta t} = \frac{3\Delta u_{\mathrm{CMV}}}{L_1 + L_1} = \frac{[(S_{a1} - S_{a2}) + (S_{c1} - S_{c2}) + (S_{b1} - S_{b2})]\, V_{\mathrm{DC}}}{(L_1 + L_1)}. \tag{3}$$

Table II gives the instantaneous common mode voltage and the rate of change of zero-sequence circulating current for each vector. Notably, each vector has multiple common mode voltages and rates of change of the zero-sequence circulating current. This redundancy enables specific objective optimizations by selecting the optimal vectors. For example, it is advantageous to apply vectors with smaller rates of change (±1, 0) rather than larger ones (±2, ±3) to mitigate zero-sequence circulating currents [8], [9], [10], [11]. Similarly, it is also beneficial to select the vector with ZCMV to eliminate the common mode voltage [12], [13].

As detailed in Table I, coordinated PWM schemes select optimal vectors and optimally arrange these vectors per carrier period to enhance specific switching-related performance indicators. For example, by choosing vectors with small rates of change (±1, 0), TLSVM [9], AZSPWM [10], and MDPWM [11] arrange the vectors using a quarter-waveform symmetry approach, effectively minimizing high-frequency circulating currents. Similarly, MZCMV [13] and ZCMV [12] select vectors with ZCMV to eliminate common mode voltage. Additionally, LCPWM [7] and MMDPWM [8] select vectors that satisfy both the near-three vector scheme and small rates of change to cancel out output current ripple and zero-sequence circulating current accumulation.

In summary, the coordinated PWM schemes are characterized by the detailed organization of vector sequences—including the selection of specific vector combinations and their arrangement for each carrier period—enabling precise coordinated operation between the two converters. This precise coordination is crucial for achieving optimal switching-related performance indicators. Therefore, maintaining the integrity of these vector sequences—both in selection and arrangement—is critical for effectively managing the coordinated switching states between the two converters.

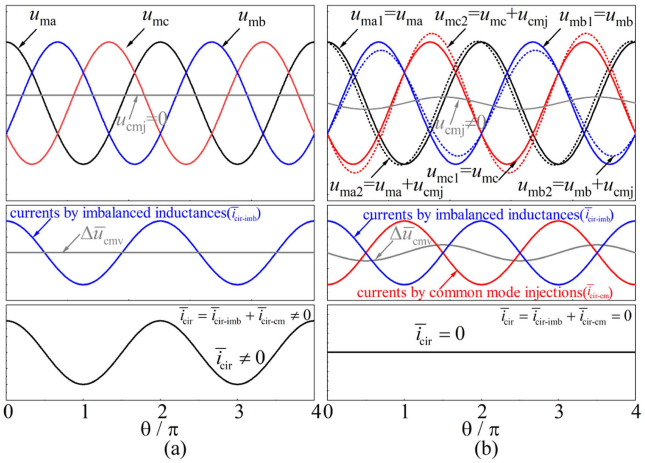

Fig. 3. Resultant low-frequency circulating currents under imbalanced inductance. (a) Without common-mode signal injection ($u_{cmj}=0$). (b) With common-mode signal injection ($u_{cmj}\neq 0$) by existing independent PWM schemes.

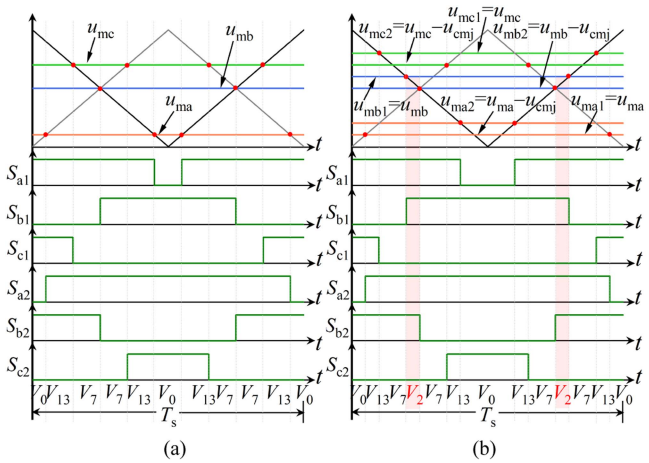

Fig. 4. Vector sequences of the TLSVM of (a) before the common-mode injection and (b) after the common-mode injection.

III. The Limitation of the Existing Methods

As evidenced by [2], [3], [4], [5], the unbalanced inductance generates a low-frequency circulating current between parallel converters:

$$i_{\mathrm{cir-imb}} = -\frac{(L_{a1}-L_{a2})\cos\omega t+(L_{b1}-L_{b2})\cos(\omega t-2\pi/3)}{2(L_{a1}+L_{b1}+L_{c1}+L_{a2}+L_{b2}+L_{c2})}i_d - \frac{(L_{c1}-L_{c2})\cos(\omega t+2\pi/3)}{2(L_{a1}+L_{b1}+L_{c1}+L_{a2}+L_{b2}+L_{c2})}i_d \tag{4}$$

where i_d and i_q are the d-axis and q-axis components, respectively, and obtained by applying the Park transformation to the three-phase currents i_a, i_b, and i_c (see Fig. 1).

Without loss of generality, in this article, we will shift the inductance of Phase B out of balance to study the imbalance inductance's effect, where $L_{a1}=L_{a2}=L_{c1}=L_{c2}=L_1$ and $L_{b2}\neq L_{b1}\neq L_1$ (L_1 is the nominal inductance). Then, the low-frequency circulating currents can be expressed as

$$\bar{i}_{\mathrm{cir-imb}}=\frac{(L_{b2}-L_{b1})\cos(\omega t-2\pi/3)}{2(4L_1+L_{b1}+L_{b2})}\bar{i}_d. \tag{5}$$

As Fig. 3(a) illustrates, the unbalanced inductance causes the low-frequency circulating current, which is aligned with the load's fundamental frequency. On the other hand, each converter's average common mode voltage per carrier period affects the low-frequency common mode voltage difference between the two converters

$$\Delta\bar{u}_{\mathrm{cm}v}=\bar{u}_{\mathrm{cm}v1}-\bar{u}_{\mathrm{cm}v2} = V_{\mathrm{DC}}\left[\underbrace{\left(\frac{d_{a1}+d_{b1}+d_{c1}}{3}\right)}_{d_{\mathrm{cm}v1}}-\underbrace{\left(\frac{d_{a2}+d_{b2}+d_{c2}}{3}\right)}_{d_{\mathrm{cm}v2}}\right] \tag{6}$$

where d_{a1}, d_{b1}, d_{c1}, d_{a2}, d_{b2}, and d_{c2} denote the duty ratios of the switches S_1, S_3, S_5, S_7, S_9, and S_{11}; $d_{\mathrm{cm}v1}$ and $d_{\mathrm{cm}v2}$ denote the common mode duty ratios of the converter #1 and #2.

Notably, this low-frequency common mode voltage difference ($\Delta\bar{u}_{\mathrm{cm}v}$) also leads to low-frequency circulating currents ($\bar{i}_{\mathrm{cir-cm}}$) between two parallel converters. However, each converter's average common mode voltage per carrier period typically equals zero ($d_{\mathrm{cm}v1}-d_{\mathrm{cm}v2}=0$). Under these conditions, the low-frequency circulating currents ($\bar{i}_{\mathrm{cir-imb}}$) resulting from imbalanced inductances remain unresolved, as depicted in Fig. 3(a). In contrast, when both converters' averaged common-mode voltages are correctly regulated to offset the low-frequency circulating currents caused by inductance imbalances, as illustrated in Fig. 3(b), the resultant low-frequency circulating currents can be effectively suppressed.

Indeed, the independent PWM schemes inject the common mode signal to control each converter's averaged common mode voltage per carrier period, counteracting the low-frequency circulating currents caused by the imbalanced inductance. For example, a common mode signal ($u_{\mathrm{cm}j}$) is injected into one converter (e.g., converter #2) while keeping the other converter's signal (e.g., converter #1) unchanged

$$u_{mx1}=\frac{1}{2}+\frac{u_x^*}{2},\ u_{mx2}=\frac{1}{2}+\frac{u_x^*}{2}+u_{\mathrm{cm}j} \tag{7}$$

where $x=(a,\ b,\ c)$ specifies a given phase of the three-phase, and $u_{\mathrm{cm}j}$ is proportional to the low-frequency common mode voltage difference caused by the imbalanced inductance.

Notably, the common-mode signal injection cannot be applied to clamping schemes, such as ODPWM and HPDPWM. In these schemes, one modulation signal is fixed to the dc-link voltage, inherently preventing common-mode injection. Furthermore, even in nonclamping schemes, such as TLSVM and AZSPWM, where common mode injection is theoretically feasible, it disrupts the vector sequence. It undermines the optimization objectives of coordinated PWM schemes. For example, Fig. 4 illustrates how common-mode voltage injections disrupt the resultant vector sequence of the nonclamping coordinated PWM

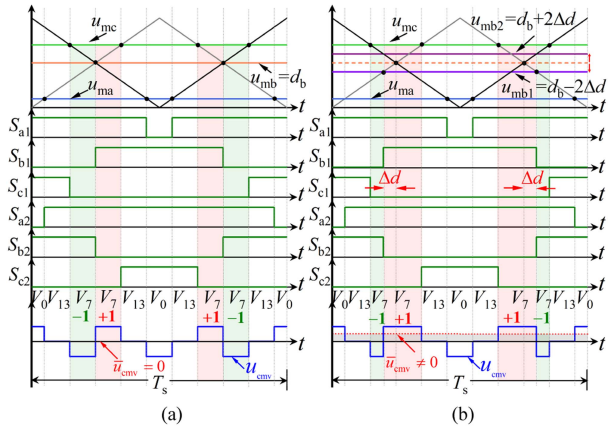

Fig. 5. Vector sequences of the TLSVM of (a) before proposed duty ratio redistribution and (b) after the proposed duty ratio redistribution.

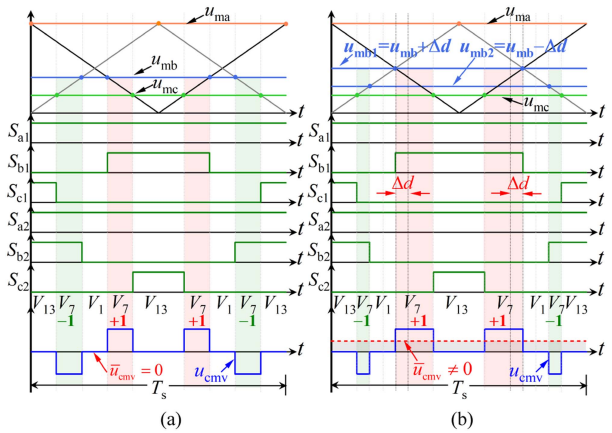

Fig. 6. Vector sequences of the HPDPWM of (a) before proposed duty ratio redistribution and (b) after the proposed duty ratio redistribution.

scheme (TLSVM). These injections introduce an undesired vector ($\boldsymbol{V_2}$) into the originally optimized sequence, disrupting the TLSVM's optimal vector selection. This disruption becomes increasingly pronounced with changes in reference voltages and the injections, leading to a broader range of unpredictable vector sequences. Notably, the coordinated PWM scheme is highly susceptible to these injections, causing significant deviations from its intended optimal performance.

The analysis shows that it is crucial to design a general approach that suppresses low-frequency currents without disrupting the original optimization targets for clamping and nonclamping modulation schemes.

IV. Proposed Duty Ratios Redistribution for Averaged Common Mode Voltage Difference Adjustments

Alternatively, the average common mode voltage difference per carrier period amounts to the sum of the product of the instantaneous common mode voltage difference and the corresponding duty ratio per carrier period, as shown in Fig. 5. For any given vector sequence, the average common mode voltage difference per carrier period can be generalized as

$$\Delta\bar{u}_{\mathrm{CMV}} = \sum_{i=1}^{i=n} u_{\mathrm{CMV}-i} d_i \tag{8}$$

where $\boldsymbol{u_{\mathrm{CMV}\text{-}i}}$ denotes the instantaneous common mode voltage difference caused by a given vector defined by (3), and the variable d_i denotes the corresponding duty ratio.

Fig. 5(a) displays TLSVM's vector sequences in the first 30° sector, where each vector's duty ratio is divided into four intervals across the carrier period. Of these three vectors, $\boldsymbol{V_1}$ and $\boldsymbol{V_{13}}$ do not contribute to the average common mode voltage differences since their instantaneous common mode voltage difference amounts to zero ($\boldsymbol{u_{\mathrm{CMV}}} = \boldsymbol{0}$). In contrast, the vector $\boldsymbol{V_7}$ introduces two complementary instantaneous common mode voltage differences ($\pm V_{\mathrm{DC}}$). According to (8), the average common mode voltage difference per carrier period is calculated

$$\Delta\bar{u}_{\mathrm{CMV}} = (V_{\mathrm{DC}})\, d_7 + (-V_{\mathrm{DC}})\, d_7 = 0. \tag{9}$$

On the other hand, if more duty ratios are assigned to the vector $\boldsymbol{V_7}$ with the positive difference, the resultant averaged voltage shifts to the positive

$$\begin{aligned}\Delta\bar{u}_{\mathrm{CMV}} &= 2\left[(V_{\mathrm{DC}})\,(d_7+\Delta d) + (-V_{\mathrm{DC}})\,(d_7-\Delta d)\right] \\ &= 4\Delta d V_{\mathrm{DC}}\end{aligned} \tag{10}$$

where Δd denotes the adjusted duty ratio.

The complementary common-mode voltage difference of vector $\boldsymbol{V_7}$ arises from the differing switching states in phase B ($\boldsymbol{V_{100}/V_{110}}$ **or** $\boldsymbol{V_{110}/V_{100}}$). To address this, the required duty ratio redistribution is achieved by splitting phase B's original duty ratio (d_b) into two modified duty ratios (d_{b1} and d_{b2}). As illustrated in Fig. 5(b), our approach overcomes a critical challenge: maintaining the original duty ratio distribution of nontarget vectors ($\boldsymbol{V_1}$ and $\boldsymbol{V_{13}}$) while ensuring effective redistribution for the target vector ($\boldsymbol{V_7}$). Specifically, the modified duty ratio d_{b1} is increased by an adjustment $2\Delta d$, while the same amount reduces d_{b2}

$$\begin{cases} d_{b1} = d_b + (\Delta d T_s)/(T_s/2) = d_b + 2\Delta d \\ d_{b2} = d_b - (\Delta d T_s)/(T_s/2) = d_b - 2\Delta d. \end{cases} \tag{11}$$

Unlike existing methods that disrupt the duty ratio distribution of other vectors, our symmetric splitting strategy preserves the equilibrium of vector $\boldsymbol{V_7}$'s duty ratios (d_7) and retains the original distribution of nontarget vectors (d_{13} and d_1). This ensures the original vector sequences are intact and the original optimization of key switching-related performance indicators is correct. The proposed approach can also be applied to the clamping PWM methods. As illustrated in Fig. 6, the vector sequence of HPDPWM remains consistent before and after the duty ratio redistribution. Significantly, generating a nonzero average common-mode voltage difference per carrier period does not disrupt the original vector sequence.

While the presented analysis demonstrates the proposed approach's feasibility in generating an average common-mode voltage difference between two converters, it is essential to develop a general model that captures the relationship between

the adjusted duty ratios and the resulting low-frequency zero-sequence circulating currents. Such a model is critical for formulating a general approach to effectively suppress these low-frequency circulating currents using our duty ratio redistribution.

In the centralized architecture that the coordinated PWM schemes adopt, the voltage differences between the two parallel converters can be generalized as [19]

$$\begin{cases} u_{\mathrm{diff}-a} = u_{\mathrm{A1O}} - u_{\mathrm{A2O}} = 2L_1 \frac{di_{\mathrm{cir}-a}}{dt} \\ +2L_{\mathrm{dev}-a} \frac{di_{\mathrm{cir-a}}}{dt} + L_{\mathrm{diff}-a} \frac{di_a}{dt} \\ u_{\mathrm{diff}-b} = u_{\mathrm{B1O}} - u_{\mathrm{B2O}} = 2L_1 \frac{di_{\mathrm{cir}-b}}{dt} \\ +2L_{\mathrm{dev}-b} \frac{di_{\mathrm{cir-b}}}{dt} + L_{\mathrm{diff}-b} \frac{di_b}{dt} \\ u_{\mathrm{diff}-c} = u_{\mathrm{C1O}} - u_{\mathrm{C2O}} = 2L_1 \frac{\mathrm{d}i_{\mathrm{cir}-c}}{dt} \\ +2L_{\mathrm{dev}-c} \frac{di_{\mathrm{cir-c}}}{dt} + L_{\mathrm{diff}-c} \frac{di_c}{dt} \end{cases} \tag{12}$$

where u_{A1O}, u_{A2O}, u_{B1O}, u_{B2O}, u_{C1O}, and u_{C2O} denote the outputs of two parallel converters (see Fig. 1), respectively; $i_{\mathrm{cir}\text{-}x} = i_{x1} - i_{x2}$ (e.g., $i_{\mathrm{cir}\text{-}a} = i_{a1} - i_{a2}$) denotes the circulating current between two parallel legs of each phase x, with $x = a$, b, and c; and $L_{\mathrm{dev}\text{-}x}$ ($x = a$, b, and c) denotes the inductance's deviation of each phase from the nominal inductance L_1, and $L_{\mathrm{diff}\text{-}x}$ denotes the inductance differences of each phase:

$$L_{\mathrm{dev}-x} = \frac{L_{x1} + L_{x2}}{2} - L_1, L_{\mathrm{diff}-x} = \frac{L_{x1} - L_{x2}}{2}. \tag{13}$$

Applying the Park transformation to (12), we have the zero-sequence projection of the output voltage differences between two parallel converters:

$$\begin{aligned} &\frac{u_{\mathrm{A1O}} - u_{\mathrm{A2O}} + u_{\mathrm{B1O}} - u_{\mathrm{B2O}} + u_{\mathrm{C1O}} - u_{\mathrm{C2O}}}{3} \\ &= \frac{2L_1 + 2L_{\mathrm{dev}-0}}{3} \frac{di_{\mathrm{cir}}}{dt} + u_{\mathrm{forward}} \end{aligned} \tag{14}$$

where u_{forward} amounts to

$$\begin{aligned} u_{\mathrm{forward}} = {} & L_{\mathrm{dev}-d}(-\omega i_{\mathrm{cir}-q}) + L_{\mathrm{dev}-q}(\omega i_{\mathrm{cir}-d}) \\ & - \frac{L_{\mathrm{diff}-d}}{2}(\omega i_q) + \frac{L_{\mathrm{diff}-q}}{2}(\omega i_d) \end{aligned} \tag{15}$$

where $L_{\mathrm{dev}\text{-}d}$, $L_{\mathrm{dev}\text{-}q}$, $L_{\mathrm{diff}\text{-}d}$, and $L_{\mathrm{diff}\text{-}q}$ denote the unbalanced inductances in the dq-frame after the Park transformation, and $i_{\mathrm{cir}\text{-}d}$ and $i_{\mathrm{cir}\text{-}q}$ denote the low-frequency circulating current i_{cir} in the dq-frame. The specific expressions are provided in the Appendix. Submitting (10) into (14) yields

$$\Delta \bar{u}_{\mathrm{CMV}} = \frac{4}{3} \Delta d V_{DC} = \frac{2L_1 + 2L_{\mathrm{dev}-0}}{3} \frac{di_{\mathrm{cir}}}{dt} + u_{\mathrm{forward}} \tag{16}$$

where $L_{\mathrm{dev}\text{-}0}$ denotes the unbalanced inductance in the zero-sequence axis after the Park transformation, and the specific expression is provided in the Appendix.

Notably, the voltage component defined by (15) can be compensated by the forward control. Therefore, the transfer function between the adjusted duty ratio Δd and the low-frequency circulating current can be derived from (16)

$$I_{\mathrm{cir}}(s) = \frac{2\Delta d}{s(L_1 + L_{\mathrm{dev}-0})} V_{\mathrm{DC}}. \tag{17}$$

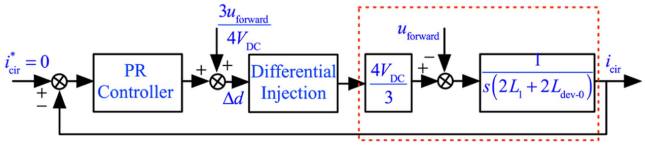

Fig. 7. Generalized control structure for suppressing the low-frequency ZSCCs by the proposed redistributing the duty ratios.

The transfer function presented in (17) offers a general model that describes the relationship between required duty ratio adjustments and the resulting low-frequency zero-sequence circulating current. Although this transfer function was developed specifically for the TLSVM case, where the duty ratios are redistributed among vectors with smaller rates of change (±1), it is universally applicable across all coordinated modulation schemes. This universality originates from the fact that all coordinated modulation methods inherently utilize vectors with small rates of change (±1) to suppress high-frequency circulating currents [8], [9], [10], [11].

With the general transfer function described by (17), Fig. 7 illustrates the general control structure to suppress low-frequency zero-sequence circulating currents through the proposed duty ratio adjustments. In this setup, the feedback from the low-frequency zero-sequence circulating current is compared to a zero-reference value. The resulting error is processed through a proportional-resonant (PR) controller, which applies forward compensation to produce the required adjusted duty ratio. The adjusted duty ratios (Δd) are added to the original ones using the differential injection (explained in the next section) to create the low-frequency common-mode voltage difference, effectively counteracting low-frequency circulating currents caused by the imbalanced inductance. While forward compensation depends on inductor parameters that may vary, it primarily affects transient behavior. Since inductance imbalance is a preexisting condition rather than a dynamic disturbance, transient response is of limited concern, and steady-state performance becomes the primary focus. Closed-loop systems such as PR/PI controllers inherently ensure zero steady-state error even without precise compensation, which supports the robustness of the proposed method under inductance imbalances.

The low-frequency circulating current is typically centered around 50 Hz, and the PR controller is tuned accordingly. As PR controller design is well established and extensively documented in the literature [20], [21], [22], repeating the standard procedure here may not be essential, especially given the space constraints. More detailed discussions can be found in [20], [21], [22].

V. General Duty Ratio Redistribution Approach for Suppressing Low-Frequency Zero-Sequence Circulating Currents

While the case studies in Section IV confirm the feasibility of adjusting the averaged common mode voltage difference by splitting original duty ratios, they only cover two case studies. It is crucial to develop a general duty ratio split rule to facilitate the implementation of the proposed method, ensuring its universal

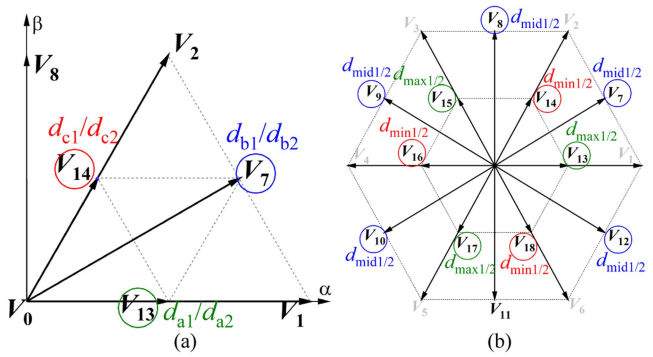

Fig. 8. Duty ratio splitting rules for (a) the three vectors in the first 60° sector and (b) all available vectors across the entire vector plane.

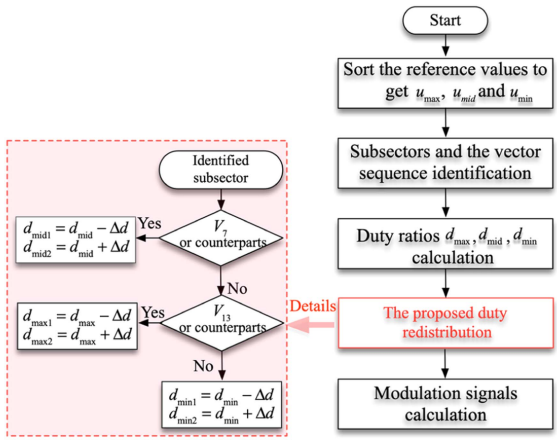

Fig. 9. General chart flow of integrating the proposed duty ratio redistribution approach to the existing PWM schemes.

effectiveness. Notably, in interleaved carriers, all PWM schemes inherently include at least one vector with complementary common mode voltage differences, and this ensures the proposed approach's applicability across existing methods. As shown in Figs. 5 and 6, the duty ratio split depends solely on the specific vector selected for duty ratio adjustment, regardless of the vector sequences. Each vector requires a unique splitting rule to achieve the necessary redistribution. Consequently, the general duty ratio split rule for all available vector sequences reduces to a unified splitting principle for all vectors with the complementary common-mode voltage difference.

As Fig. 8(a) displays, in the first 60° sector, there are three vectors with the complementary common mode voltage difference ($\boldsymbol{V_7}$, $\boldsymbol{V_{13}}$, and $\boldsymbol{V_{14}}$), and each vector corresponds to a distinct duty ratio split. When vector $\boldsymbol{V_7}$ adjusts the duty ratios, phase B's modulation signal is divided into two parts (d_{b1}/d_{b2})

$$\begin{cases} d_{b1} = d_b + 2\Delta d \\ d_{b2} = d_b - 2\Delta d. \end{cases} \tag{18}$$

Similarly, the application of vector $\boldsymbol{V_{14}}$ results in a split of phase C's modulation signals (d_{c1}/d_{c2})

$$\begin{cases} d_{c1} = d_c + 2\Delta d \\ d_{c2} = d_c - 2\Delta d \end{cases} \tag{19}$$

while vector $\boldsymbol{V_{13}}$ causes the modulation signals in phase A to be divided (d_{a1}/d_{a2})

$$\begin{cases} d_{a1} = d_a + 2\Delta d \\ d_{a2} = d_a - 2\Delta d \end{cases}. \tag{20}$$

The duty ratios splitting analysis across the remaining 60°-360° sectors has clarified the general rules for splitting original duty ratios, as Fig. 8(b) illustrates. For example, when the vector $\boldsymbol{V_7}$ or its counterparts ($\boldsymbol{V_8}$, $\boldsymbol{V_9}$, $\boldsymbol{V_{10}}$, $\boldsymbol{V_{11}}$, and $\boldsymbol{V_{12}}$) are utilized, the duty ratios of the phase with the median value among three phases are split

$$\begin{cases} d_{\text{mid1}} = d_{\text{mid}} + 2\Delta d \\ d_{\text{mid2}} = d_{\text{mid}} - 2\Delta d \end{cases} \tag{21}$$

where d_{mid} denotes the original duty ratio of the phase with the median value (u_{mid}) among the three-phase reference voltages; similarly, when vector $\boldsymbol{V_{13}}$ or its counterparts ($\boldsymbol{V_{15}}$ and $\boldsymbol{V_{17}}$) are employed, the modulation signal of the phase with the minimum value is split

$$\begin{cases} d_{\text{max1}} = d_{\text{max}} + 2\Delta d \\ d_{\text{max2}} = d_{\text{max}} - 2\Delta d. \end{cases} \tag{22}$$

Likewise, if vector $\boldsymbol{V_{14}}$ or its counterparts ($\boldsymbol{V_{16}}$ and $\boldsymbol{V_{18}}$) are applied, the modulation signal of the phase with the maximum value is split

$$\begin{cases} d_{\text{min1}} = d_{\text{min}} + 2\Delta d \\ d_{\text{min2}} = d_{\text{min}} - 2\Delta d. \end{cases} \tag{23}$$

Notably, the proposed duty ratio redistribution depends on identifying the vectors with the complementary common-mode voltage difference and splitting the original duty ratios to achieve the required redistribution. Similarly, existing coordinated PWM methods require subsector identification, which is crucial for their implementation. This subsector information is critical to identifying vectors with complementary common-mode voltage differences, which is essential for applying the proposed redistribution approach.

Fig. 9 illustrates a general chart flow for integrating the proposed duty ratio redistribution approach into existing PWM schemes. Our approach utilizes the identified subsector information to redistribute the proposed duty ratio. Significantly, the proposed approach is designed to be added as a subsequent step to the original modulation process, which ensures seamless integration to all PWM schemes. Notably, the differential signal injection relies on simple logical conditions that integrate seamlessly with existing control schemes, requiring negligible computational resources. Additionally, the PR controller employed in this method is widely used in practical applications and has not been associated with significant computational overhead.

Following the workflow outlined in Figs. 9 and 10(a) illustrates the adjusted duty ratios, each phase's injections, and the resultant modified modulation signals in HPDPWM using the proposed duty ratio redistribution. The proposed approach introduces differential-mode signal injections into different

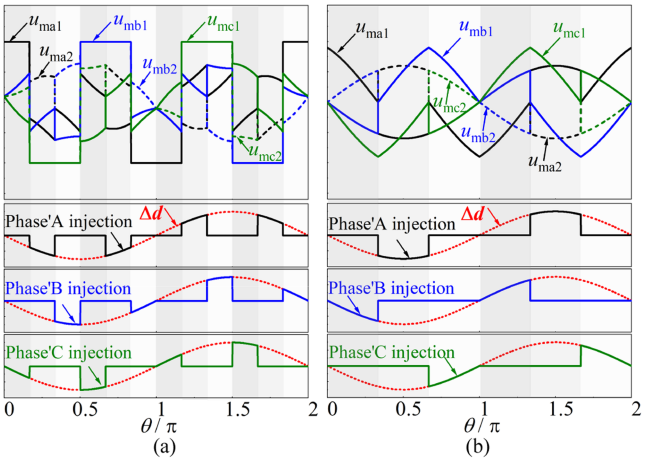

Fig. 10. Modified modulation signals and the adjusted duty ratios for (a) HPDPWM and (b) 3LSVM, both using the proposed differential signal injection.

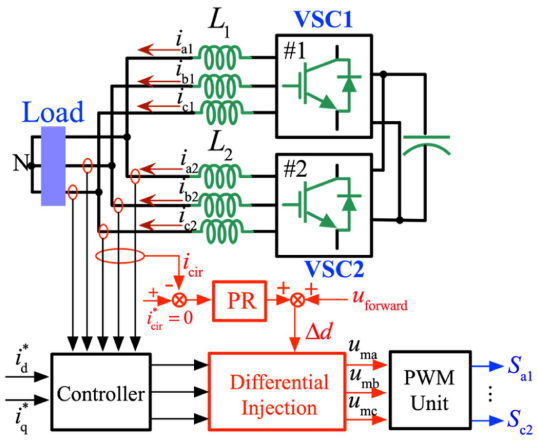

Fig. 11. General centralized control architecture with the proposed differential signal injection for two-parallel converter using the coordinated PWM schemes.

phases based on vector angles. This effectively counteracts low-frequency circulating currents caused by inductance imbalance while preserving the integrity of the original vector sequences.

Similarly, Fig. 10(b) depicts the adjusted duty ratios, each phase's injections, and the resultant modified modulation signals for TLSVM. Differential-mode injections are also applied to different phases at varying vector angles, generating the essential low-frequency common-mode voltage difference. Notably, case studies for both clamping and nonclamping PWM schemes confirm that the proposed duty ratio redistribution integrates seamlessly with existing coordinated modulation schemes, simplifying their implementation.

Fig. 11 illustrates a general centralized control architecture with the proposed differential signal injection method. The specific control strategy (e.g., PI, model predictive control) is not shown, as it varies by application. This simplification highlights the general compatibility of the proposed method and avoids confusion over implementation details. Notably, the proposed method is inserted before the modulation unit, which modifies the modulation signals directly. It is a general approach that can

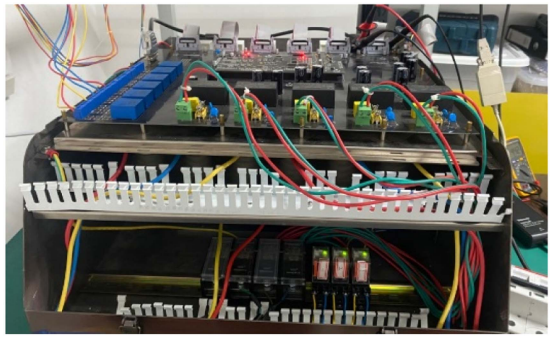

Fig. 12. Photo of the experimental setup.

TABLE III
SYSTEM PARAMETERS

R_L	L_1	V_{DC}	P
10Ω	5mH, 10mH	400V	6kW
	T_s	f	C
	0.0002s	5kHz	1500μF

be integrated into various modulation schemes without structural changes. To further assess its practical feasibility, we measured the execution time of the entire control block—including the PR controller, Park transformation, and differential injection—which was found to be only 6 μs. This minor computational burden confirms that the method is suitable for DSP implementation.

VI. EXPERIMENTS

An experimental setup was developed to validate the presented analysis, as presented in Fig. 12. The assembly includes a TMS320F2808 DSP-based controller interface board, a power supply board utilizing RECOM ac/dc power modules, Concept IGBT gate drivers (2SP0115T2C), Infineon IGBTs (FF300R17ME4), LEM current and voltage sensors, SBE dc-link capacitors (700D158911-590), and filter inductors. Detailed specifications are provided in Table III. The low-frequency circulating current is obtained by sampling the phase currents using current sensors at each half-carrier period, effectively approximating the average current over each switching cycle. Besides, the common-mode voltage is defined as the voltage difference between the load's midpoint and the dc bus's midpoint. A voltage probe is used to measure it by connecting the probe between these two points. We conducted experiments on a hardware prototype operating in inverter mode. A three-phase diode rectifier supplied the dc link, and three resistors were used as the ac load. The main experimental parameters are summarized in Table III.

We selected two typical scenarios: one with an imbalance within the same phase and another with an imbalance distributed across three different phases. Two nominal inductance values—5 mH and 10 mH—were considered. Due to space constraints, we selected three representative imbalance configurations, each with a different nominal inductance and imbalance rate, to demonstrate the method's effectiveness:

1) 10 mH ($L_{a1} = -25\%, L_{a2} = +25\%$).
2) 5 mH ($L_{a1} = -50\%, L_{a2} = +50\%$).
3) 10 mH ($L_{a1} = +10\%, L_{b1} = +20\%, L_{c1} = -10\%$).

For clarity, in the following figures and discussion, we use the notation **5 mH/±50%** to indicate test conditions with 5 mH nominal inductance at ±50% imbalance, and **10 mH/±25%** to indicate test conditions with 10 mH nominal inductance at ±25% imbalance. For the imbalance rates across the three phases, we use the notation **10 mH/{ +10%, +20%, −10%}**.

To further verify the generality of the proposed method, two representative coordinated PWM schemes were tested: TLSVM (a nonclamping scheme) and HPDPWM (a clamping scheme). This selection confirms the applicability of the method across different modulation strategies. The tests and comparisons include the following objectives.

1) *Low-Frequency Current Suppression:* Validate the proposed method's effectiveness in suppressing low-frequency circulating currents caused by imbalanced inductance.
2) *Preservation of Switching-Related Indicators:* Ensure the proposed method preserves the original schemes' primary optimization objectives without disruption.

We used Tektronix current probes (TCP303) for current measurements and displayed real-time waveforms with the Tektronix MSO58B oscilloscope. Experiment data was extracted from the oscilloscope and then processed and visualized using Origin for a more explicit representation. The proposed method was experimentally validated using two representative test cases under the HPDPWM scheme, representing nominal inductance variation and imbalance conditions. The first case uses the **5 mH ±50%**, and the second uses the **10 mH / ± 25 %**.

As shown in Figs. 13 and 14, both cases exhibited significant low-frequency circulating currents before the proposed method was activated. These currents were dominated by a 50 Hz component, which is aligned with the output current frequency and poses risks such as magnetic core saturation. Upon activating the proposed method at $t = 0.06$ s, the circulating current was rapidly and effectively suppressed. Output current waveforms [see Figs. 13(b) and 14(b)] remained consistent before and after activation, confirming that output current quality is preserved. Similarly, the common-mode voltage [see Figs. 13(c) and 14(c)] show no significant change, indicating preservation of the original voltage characteristics.

While Figs. 13 and 14 present results at a typical modulation index of $M = 0.9$, additional tests were conducted across a broader range from 0.1 to 1.0 in 0.1 increments to comprehensively evaluate performance. Due to space constraints, detailed time-domain waveforms are not shown for all cases. Instead, frequency-domain comparisons of the circulating current, output current, and common-mode voltage are provided before and after activation, offering a clearer and quantifiable view of the method's impact on low- and high-frequency components. FFT analysis was applied, and results were visualized in 3D plots to show modulation index, frequency, and amplitude variations.

Notably, the amplitude of the 50 Hz circulating current is significantly larger than that of the high-frequency components (5–10 kHz), which makes it challenging to visualize both in a single figure. To address this, Figs. 15(a) and 16(a) focus exclusively on the 0–500 Hz range under 5 mH/±50% and 10 mH/±25% test cases, respectively. These results confirm that the proposed method effectively suppresses the 50 Hz component to negligible levels. Since the magnitude of the low-frequency current is proportional to the load, different load resistors were used to evaluate performance under varying conditions. The results demonstrate the method's robustness across different amplitudes, inductance values, and imbalance ratios under clamping PWM schemes.

Figs. 15(b) and 16(b) compare the high-frequency components (4–16 kHz) of the zero-sequence circulating current before and after activation. The overlapping spectra confirm that the proposed method preserves high-frequency characteristics across the modulation range. As is well known, a larger nominal inductance results in lower high-frequency ripple amplitudes, which is also evident from the reduced spectral peaks in Fig. 16(b) compared to Fig. 15(b).

Figs. 15(c) and 16(c) present the spectra of the three-phase output currents. Since the load current remains unchanged, the 50 Hz fundamental component is excluded to visualize the high-frequency components better.

Omitting this component does not affect the evaluation of the proposed method. Notably, the overlapping spectra confirm that the current output quality is maintained. Similarly, Figs. 15(d) and 16(d) show the common-mode voltage spectra before and after activation, with a negligible difference, further confirming that switching-related performance indicators are preserved. The results in Figs. 13–16 demonstrate the effectiveness of the proposed method in suppressing low-frequency circulating currents while preserving switching-related performance under various operating conditions.

The method was also validated using the 3LSVM scheme, which represents nonclamping PWM strategies. Again, two test cases were considered: 5 mH/±50% and 10 mH/±25%. As shown in Figs. 17 and 18, significant low-frequency circulating currents were observed before activation and were effectively suppressed once the method was applied at $t = 0.06$ s. Output current and common-mode voltage waveforms remained consistent before and after activation.

Figs. 19(a) and 20(a) show that the 50 Hz component of the circulating current is suppressed to negligible levels. Figs. 19(b) and 20(b) compare the high-frequency components of the circulating current and confirm that high-frequency behavior is preserved. Figs. 19(c) and 20(c) show the output current spectra, which remain consistent after activation. Finally, Figs. 19(d) and 20(d) confirm that the common-mode voltage spectra are also unaffected, further validating that the proposed method preserves switching-related performance under nonclamping PWM schemes.

To further demonstrate the general applicability and robustness of the proposed method in practical scenarios, additional tests were conducted under three-phase imbalance conditions. Specifically, we considered a 10 mH nominal inductance with imbalance rates of +10%, +20%, and −10% across phases A, B, and C, respectively. These tests evaluate the method's performance when different imbalance levels occur simultaneously in all three phases.

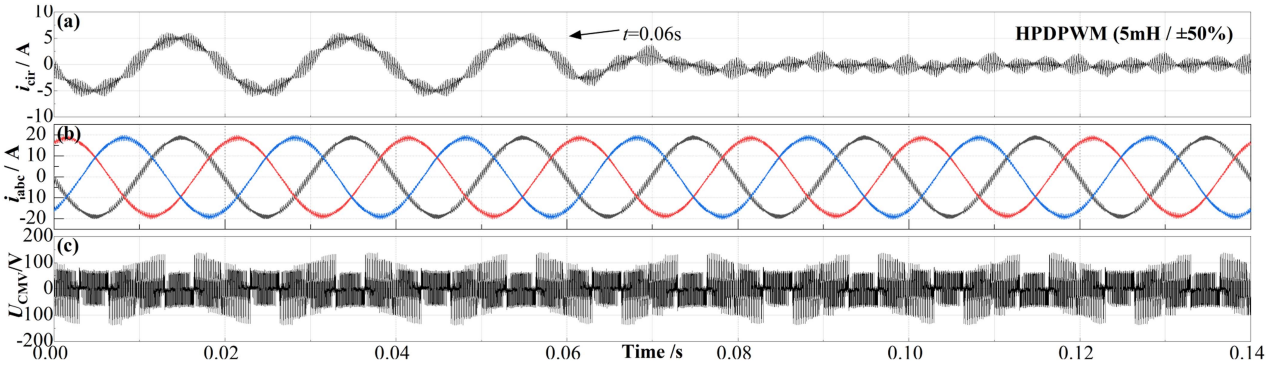

Fig. 13. Experimental results for HPDPWM showing the transition before and after activation of the proposed method under 5 mH nominal inductance with ±50% imbalance at $M = 0.9$. (a) Zero-sequence circulating current (i_{cir}). (b) Three-phase output current (i_{abc}). (c) Common-mode voltage ($u_{\mathrm{cm}v}$).

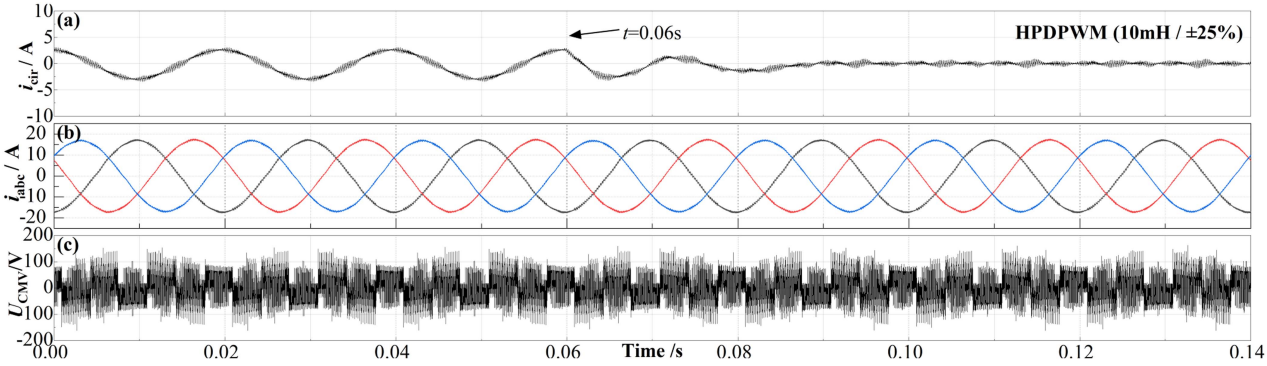

Fig. 14. Experimental results for HPDPWM showing the transition before and after activation of the proposed method under 10 mH nominal inductance with ±25% imbalance at $M = 0.9$. (a) Zero-sequence circulating current (i_{cir}). (b) Three-phase output current (i_{abc}). (c) Common-mode voltage ($u_{\mathrm{cm}v}$).

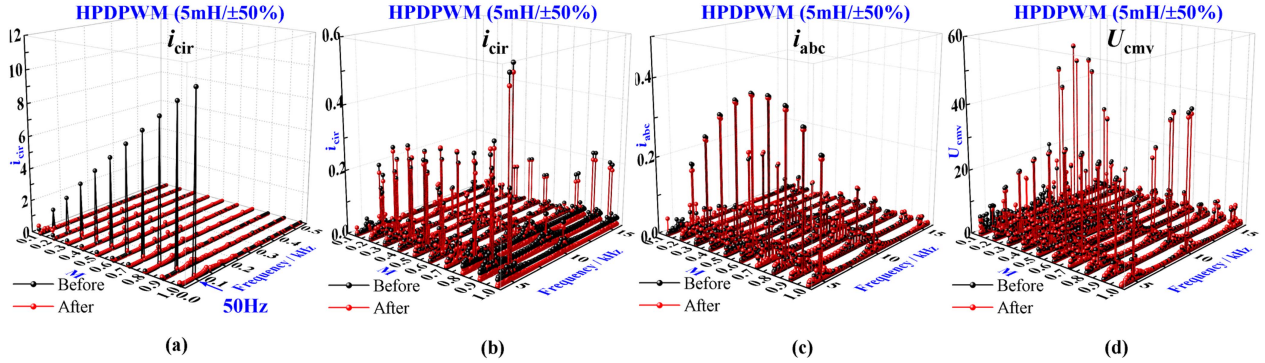

Fig. 15. Spectrum comparison of experimental results for HPDPWM at 5 mH/±50% before and after activation of the proposed method across the full modulation range. (a) Zero-sequence circulating current of low-frequency components from 0 to 500 Hz. (b) Zero-sequence circulating current. (c) Three-phase output current. (d) Common-mode voltage, focusing on high-frequency components from 4 to 16 kHz.

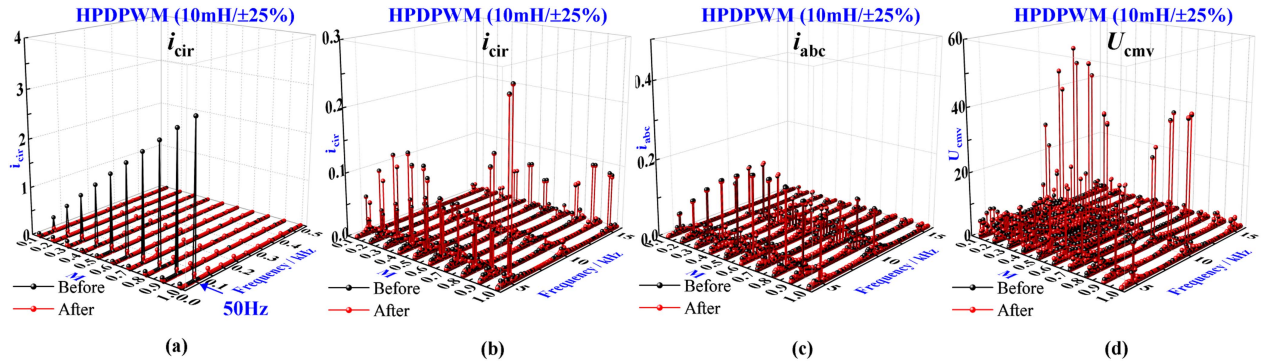

Fig. 16. Spectrum comparison of experimental results for HPDPWM at 10 mH/±25% before and after activation of the proposed method across the full modulation range. (a) Zero-sequence circulating current of low-frequency components from 0 to 500 Hz. (b) Zero-sequence circulating current. (c) Three-phase output current. (d) Common-mode voltage, focusing on high-frequency components from 4 to 16 kHz.

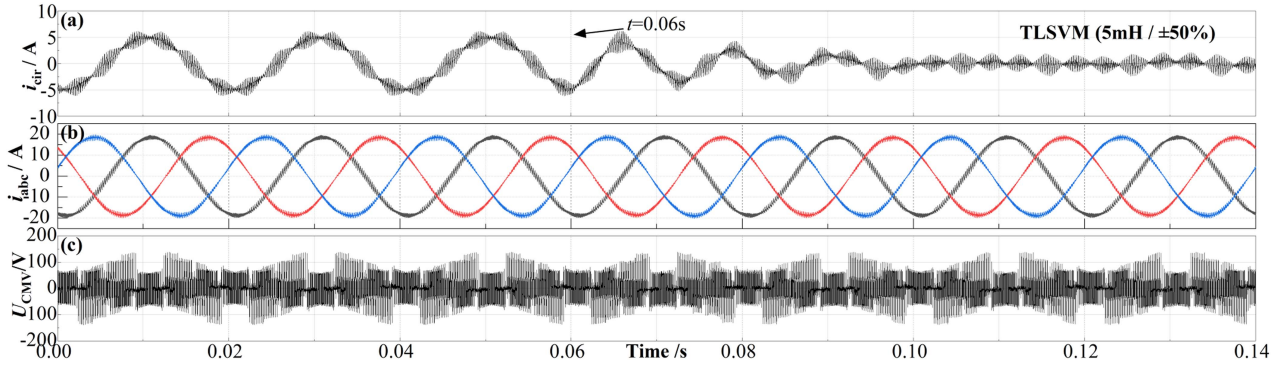

Fig. 17. Experimental results for TLSVM showing the transition before and after activation of the proposed method under 5 mH nominal inductance with ±50% imbalance at $M = 0.9$. (a) Zero-sequence circulating current (i_{cir}). (b) Three-phase output current (i_{abc}). (c) Common-mode voltage ($u_{\mathrm{cm}v}$).

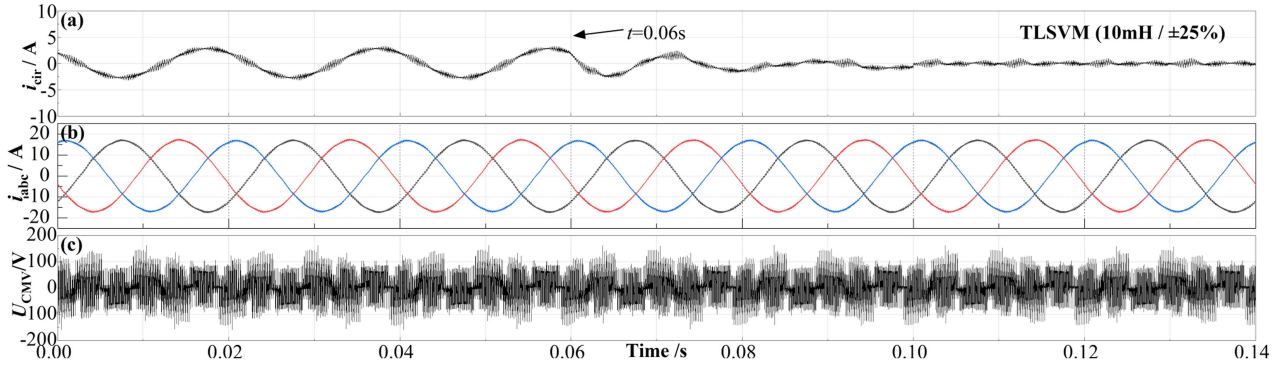

Fig. 18. Experimental results for TLSVM showing the transition before and after activation of the proposed method under 10 mH nominal inductance with ±25% imbalance at $M = 0.9$. (a) Zero-sequence circulating current (i_{cir}). (b) Three-phase output current (i_{abc}). (c) Common-mode voltage ($u_{\mathrm{cm}v}$).

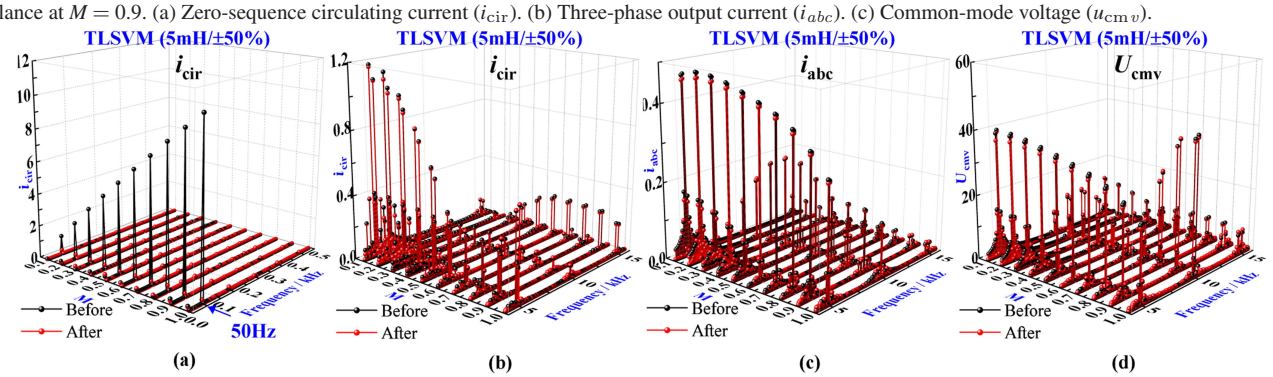

Fig. 19. Spectrum comparison of experimental results for TLSVM at 5 mH/±50% before and after activation of the proposed method across the full modulation range. (a) Zero-sequence circulating current of low-frequency components from 0 to 500 Hz. (b) Zero-sequence circulating current. (c) Three-phase output current. (d) Common-mode voltage, focusing on high-frequency components from 4to 16 kHz.

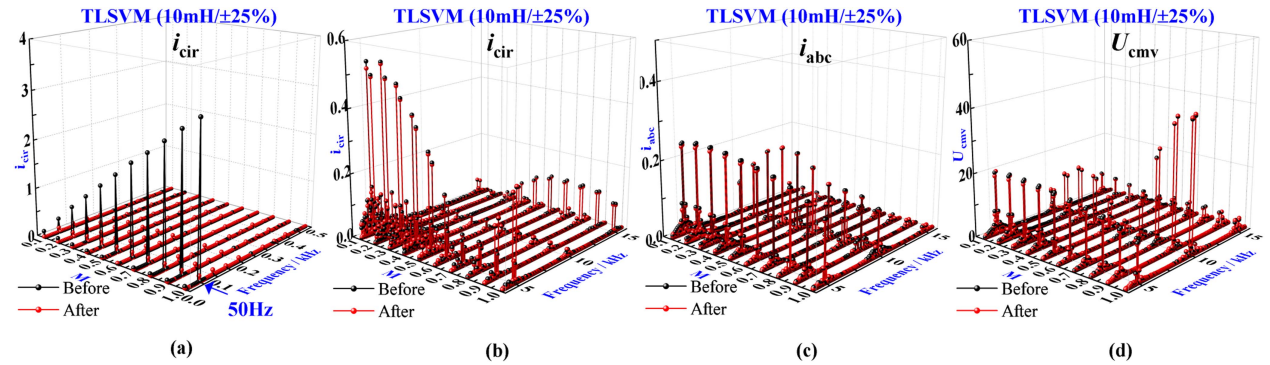

Fig. 20. Spectrum comparison of experimental results for TLSVM at 10mH/±25% before and after activation of the proposed method across the full modulation range. (a) Zero-sequence circulating current of low-frequency components from 0 to 500 Hz. (b) Zero-sequence circulating current. (c) Three-phase output current. (d) Common-mode voltage, focusing on high-frequency components from 4 to 16 kHz.

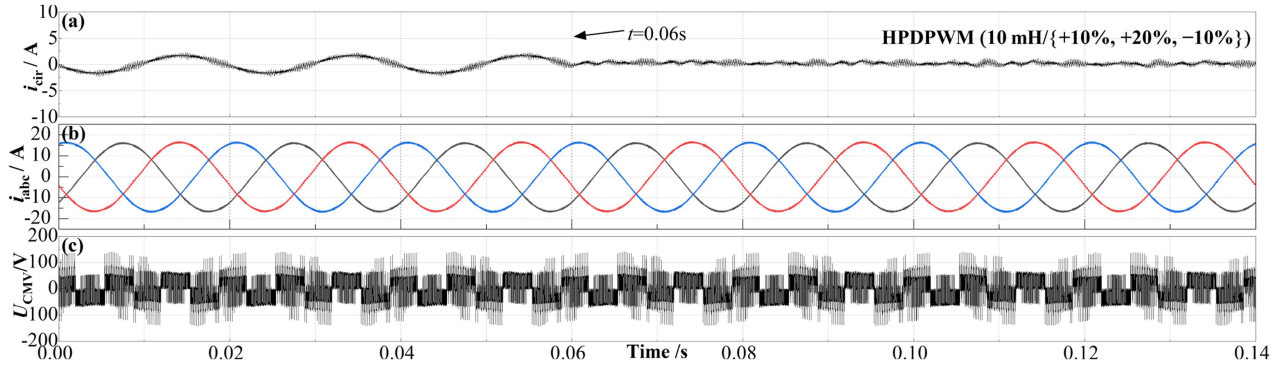

Fig. 21. Experimental results for HPDPWM showing the transition before and after activation of the proposed method under 10 mH/{+10%, +20%, −10%} at $M = 0.9$. (a) Zero-sequence circulating current (i_{cir}). (b) Three-phase output current (i_{abc}). (c) Common-mode voltage ($u_{\mathrm{cm}v}$).

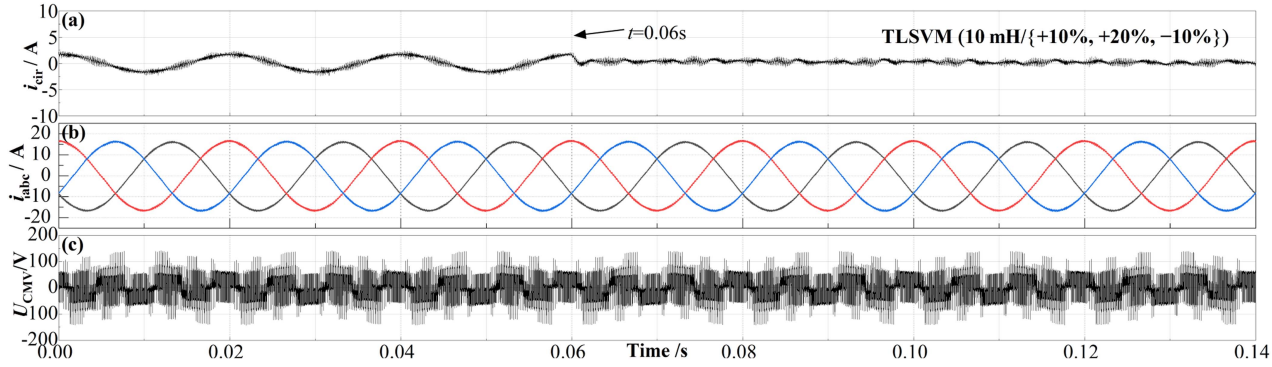

Fig. 22. Experimental results for TLSVM showing the transition before and after activation of the proposed method under 10 mH/{+10%, +20%, −10%} at $M = 0.9$. (a) Zero-sequence circulating current (i_{cir}). (b) Three-phase output current (i_{abc}). (c) Common-mode voltage ($u_{\mathrm{cm}v}$).

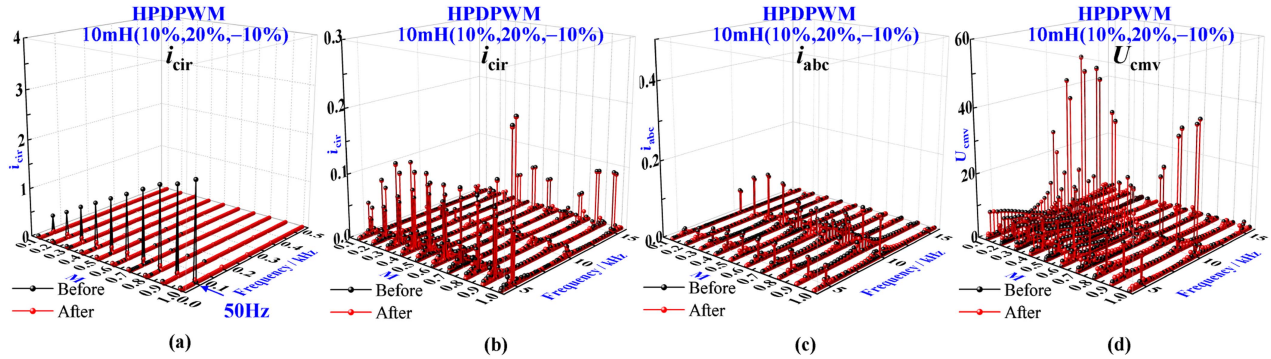

Fig. 23. Spectrum comparison of experimental results for HPDPWM at 10 mH/{+10%, +20%, −10%} before and after activation of the proposed method across the full modulation range. (a) Zero-sequence circulating current of low-frequency components from 0 to 500 Hz. (b) Zero-sequence circulating current. (c) Three-phase output current. (d) Common-mode voltage, focusing on high-frequency components from 4 to 16 kHz.

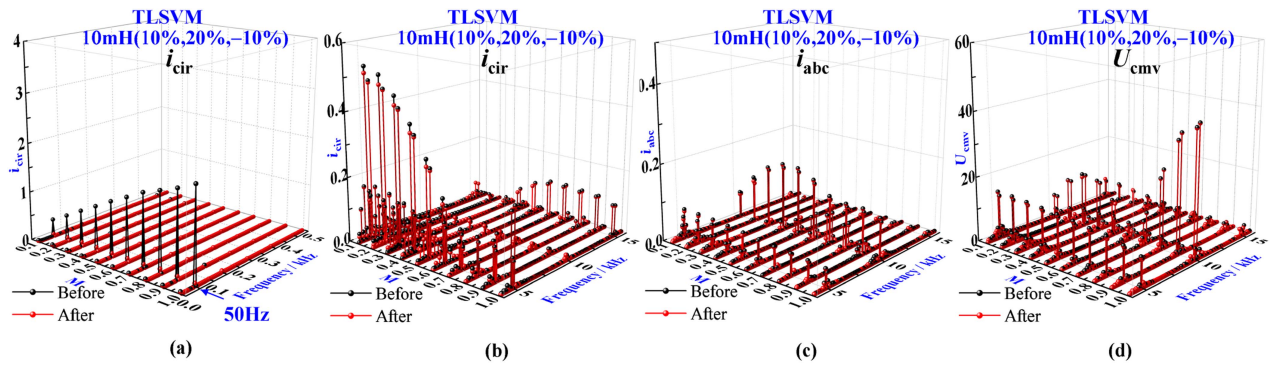

Fig. 24. Spectrum comparison of experimental results for TLSVM at 10 mH/{+10%, +20%, −10%} before and after activation of the proposed method across the full modulation range. (a) Zero-sequence circulating current of low-frequency components from 0 to 500 Hz. (b) Zero-sequence circulating current. (c) Three-phase output current. (d) Common-mode voltage, focusing on high-frequency components from 4 to 16 kHz.

As shown in Figs. 21 and 22, the three-phase inductance imbalance resulted in significant low-frequency circulating currents, which is dominated by a 50 Hz component. When the proposed method was activated at $t = 0.06$ s, the circulating current was rapidly and effectively suppressed for both HPDPWM and TLSVM schemes. Furthermore, the output current waveforms [see Figs. 21(b) and 22(b)] remained consistent before and after activation, confirming that output current quality is preserved. Similarly, the common-mode voltage [see Figs. 21(c) and 22(c)] showed no significant change, indicating that the original common-mode voltage characteristics are maintained.

Figs. 23(b) and 24(b) compare the high-frequency components (4–16 kHz) of the zero-sequence circulating current before and after activation for the three-phase imbalance scenario. The overlapping spectra confirm that the proposed method preserves high-frequency characteristics across the modulation range. Similarly, Figs. 23(c) and 24(c) show the three-phase output current spectra, and Figs. 23(d) and 24(d) show the common-mode voltage spectra, all of which remain unchanged before and after activation. These results demonstrate that the proposed method effectively suppresses low-frequency circulating currents in three-phase imbalance conditions while maintaining switching-related performance.

In summary, the proposed method effectively suppresses low-frequency circulating currents to negligible levels, with robustness demonstrated across various operating conditions—including different modulation indices, nominal inductances, and imbalance levels. At the same time, it preserves the original high-frequency characteristics of output currents, zero-sequence circulating currents, and common-mode voltage. As shown in Figs. 15, 16, 19, 20, 23, and 24, the spectra before and after activation remain nearly identical. Overall, the proposed method successfully addresses the key challenge of mitigating low-frequency circulating currents while maintaining the inherent advantages of coordinated PWM schemes.

VII. Conclusion

This article presents a general approach to suppressing low-frequency zero-sequence circulating currents in coordinated PWM schemes while preserving their inherent benefits. Two typical PWM schemes—clamping and nonclamping—were chosen as case studies. The proposed method was applied to these schemes and validated through prototype testing. Experimental results demonstrate that the method effectively reduces low-frequency circulating currents to negligible levels across various operating conditions. Additionally, it maintains the original characteristics of high-frequency components, with spectra before and after the proposed method's activation remaining nearly identical. In conclusion, the proposed method mitigates low-frequency circulating currents while maintaining the inherent advantages of coordinated PWM schemes. Finally, this article focuses on modifying existing coordinated PWM schemes of two parallel converters to suppress low-frequency circulating currents caused by inductance imbalance. While the core concept of differential signal injection proposed in this article can be extended to a multi-parallel converter through appropriate modeling and vector sequence analysis, such an extension is beyond

Appendix

$$
\begin{aligned}
i_{\mathrm{cir}-d} &= \frac{2}{3}\cos\theta i_{\mathrm{cir}-a} + \frac{2}{3}\cos\left(\theta - \frac{2}{3}\pi\right) i_{\mathrm{cir}-b} \\
&\quad + \frac{2}{3}\cos\left(\theta + \frac{2}{3}\pi\right) i_{\mathrm{cir}-c} \\
i_{\mathrm{cir}-q} &= -\frac{2}{3}\sin\theta i_{\mathrm{cir}-a} - \frac{2}{3}\sin\left(\theta - \frac{2}{3}\pi\right) i_{\mathrm{cir}-b} \\
&\quad - \frac{2}{3}\sin\left(\theta + \frac{2}{3}\pi\right) i_{\mathrm{cir}-c} \\
L_{\mathrm{dev}-d} &= \frac{2}{3}\cos\theta L_{\mathrm{dev}-a} + \frac{2}{3}\cos\left(\theta - \frac{2}{3}\pi\right) L_{\mathrm{dev}-b} \\
&\quad + \frac{2}{3}\cos\left(\theta + \frac{2}{3}\pi\right) L_{\mathrm{dev}-c} \\
L_{\mathrm{dev}-q} &= -\frac{2}{3}\sin\theta L_{\mathrm{dev}-a} - \frac{2}{3}\sin\left(\theta - \frac{2}{3}\pi\right) L_{\mathrm{dev}-b} \\
&\quad - \frac{2}{3}\sin\left(\theta + \frac{2}{3}\pi\right) L_{\mathrm{dev}-c} \\
L_{\mathrm{dev}-0} &= \frac{1}{3}(L_{\mathrm{dev}-a} + L_{\mathrm{dev}-b} + L_{\mathrm{dev}-c}) \\
L_{\mathrm{diff}-d} &= \frac{2}{3}\cos\theta L_{\mathrm{diff}-a} + \frac{2}{3}\cos\left(\theta - \frac{2}{3}\pi\right) L_{\mathrm{diff}-b} \\
&\quad + \frac{2}{3}\cos\left(\theta + \frac{2}{3}\pi\right) L_{\mathrm{diff}-c} \\
L_{\mathrm{diff}-q} &= -\frac{2}{3}\sin\theta L_{\mathrm{diff}-a} - \frac{2}{3}\sin\left(\theta - \frac{2}{3}\pi\right) L_{\mathrm{diff}-b} \\
&\quad - \frac{2}{3}\sin\left(\theta + \frac{2}{3}\pi\right) L_{\mathrm{diff}-c}.
\end{aligned}
$$

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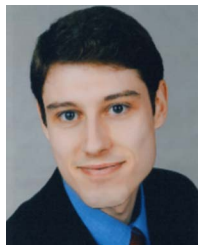

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