A Design of Cost-Efficient Solid-State Circuit Breaker for LVDC Grid Applications

Simon Shek-Mong Wong, Xin Li, Terence Chung-Yin Lau, and River Tin-Ho Li, *Senior Member, IEEE*

***Abstract*—A naturally cooled direct current (dc) solid-state circuit breaker (SSCB) is proposed for residential and commercial dc buildings applications, where cost, acoustic noise, and energy efficiency are critical concerns. By using the matrix connected low voltage MOSFETs to handle the main current, the proposed SSCB achieved 99.90%+ efficiency from 25% load and retained the ultrafast circuit breaking performance. Design is optimized between BoM cost, efficiency, thermal performance, and current interruption capability. Performance of the proposed SSCB has been evaluated analytically. Experimental verification was performed on a 400 V dc / 40A prototype.**

***Index Terms*—Circuit breaker (CB), direct current, solid-state.**

I. Introduction

MORE than 30% of global energy consumption is attributed to buildings [1], [2], [3], [4], and this figure is expected to increase substantially in the near term due to the rising popularity of vehicle electrification and AI computing services. DC grids offer a sustainable and efficient alternative to alternating current (ac) grids, particularly when considering the massive integration of photovoltaic systems, battery storage systems, computing, and electrical vehicle (EV) charging infrastructure, all of which operate fundamentally on dc voltage. By eliminating the system costs and power losses associated with unnecessary ac/dc and dc/ac conversions, dc grids have garnered significant attention in recent years in both academic research and commercial market. Industry are being active in both products and business development in recent years.

Studies have shown that buildings powered by dc grids can reduce energy consumption by 5% to 20% compared to those using ac grids [5], [6], [7], [8]. This presents a significant opportunity for the sustainable development of green buildings, integrating photovoltaic systems and EV charging facilities. However, a key challenge in the widespread adoption of dc grids is the difficulty in effective fault clearance, particularly for short-circuit faults. Due to the constant voltage level of dc, short-circuit currents rise much faster than in ac systems [9]. Therefore, a much faster disconnection mechanism than traditional mechanical circuit breakers (CBs) is required to prevent serious arc flash incidents, which could cause irreparable damage. Additionally, unlike ac voltage, which periodically crosses zero voltage level, the constant dc voltage makes disconnection more challenging. Mechanical disconnection at substantial voltage and current levels simultaneously can lead to serious electric arcs [10].

An electric arc is a breakdown of air initiated by thermionic emission when the current-carrying metal contacts are just separated. The arc is maintained by the ionization of air caused by the electric field between the separation due to the dc voltage [11]. The ionized air forms a plasma channel with mixed positive ions and free electrons, which move in a direction according to the electric field induced by the applied dc voltage across the contact separation. Higher voltage induces a stronger electric field, resulting in lower impedance of the plasma channel and a stronger arc. Therefore, if the applied voltage is high enough or the contact separation is too narrow during disconnection, the arc could be sustained even with a physical gap between the contacts.

Unlike ac voltage, which periodically crosses zero, causing the electric field to become zero and the arc to extinguish naturally even with a narrow separation, dc voltage requires active disconnection and clearance. The arc temperature ranges from 2800 °C to 19000 °C, imposing exceptional thermal stress on mechanical CBs, particularly in dc applications, thereby limiting their operating cycles [12], [13].

Fig. 1 illustrates the exterior and electrical characteristics of an arc induced by a 375 V/7.5 A dc disconnection across metal contacts. The contacts were separated horizontally at approximately 20 mms^{-1}. The top photos show the arc formation across the contacts during disconnection, while the bottom waveform presents the corresponding electrical measurements.

Before 0.291 s, the metal contacts were fully engaged, allowing a 7.5A dc current to flow through. At 0.292 s, the contacts were physically disconnected, initiating an arc between them. The voltage and current waveforms across the metal contacts were measured and are shown in the bottom part of the figure. A step reduction in current and a step increase in voltage (elaborated in the zoom-in figure) were observed. A sharp increase of approximately 100 W in power across the contacts was calculated at around 0.292 s. This power heated the

Received 22 February 2025; revised 28 May 2025 and 7 July 2025; accepted 1 August 2025. Date of publication 7 August 2025; date of current version 22 October 2025. This work was supported in part by the Innovation and Technology Commission of the Hong Kong Special Administrative Region, China, under Project ART/299CP, and in part by the Hetao Shenzhen-Hong Kong Science and Technology Innovation Cooperation Zone Shenzhen Park Project under Project HTHZQSWS-KCCYB-2023042. Recommended for publication by Associate Editor Z. Qin. *(Corresponding author: River Tin-Ho Li.)*

The authors are with Hong Kong Applied Science and Technology Research Institute Company Ltd., Hong Kong, China (e-mail: simonwong@astri.org; xinli@astri.org; terencelau@astri.org; riverli@astri.org).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3596810.

Digital Object Identifier 10.1109/TPEL.2025.3596810

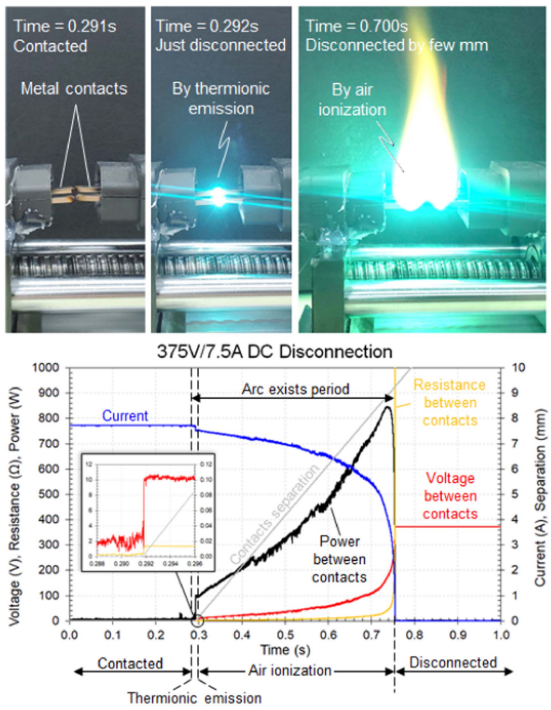


Fig. 1. Exterior and electrical presentations of electric arc.

metal contacts, causing thermionic emission of free electrons, which initiated the arc during the disconnection process.

Between 0.3 and 0.75 s, the separation of the metal contacts and the voltage across them increased. It was found that the arc resistance and arc power, by calculation, increased as the separation widened. The arc power increased, as evidenced by the arc becoming larger, very bright, and extremely hot. The waveform showed the arc power reaching a maximum of around 850 W. During this period, the electric field ionized the air between the contacts, releasing positive ions and free electrons, forming a plasma channel. Current flowed through the plasma channel according to the direction of the electric field across the contacts. Therefore, the arc would not extinguish if the electric field or voltage was present, making dc disconnection difficult and hazardous.

At 0.75 s, the separation became too large for the maximum electric field to continue ionizing the air, extinguishing the arc at a separation of around 9 mm. Due to the very high temperature and prolonged duration of the electric arc, dc disconnection is highly unfavorable for mechanical CBs [14]. To ensure safe electrical disconnection without an arc at dc voltage, current interruption by physical disconnection is not feasible. Conversely, current interruption by semiconductors does not rely on physical separation. For this reason, solid-state circuit breakers (SSCBs) are preferred and critical devices for fault current protection as well as active switches, such as contactors in dc grids. Moreover, the disconnection time of SSCBs is several orders of magnitude shorter than that of mechanical CBs [15]. It helps to ensure an in-time fault clearance.

A 1 kV/1 kA rated SSCB with 99.9% efficiency for shipboard power system applications was presented in [16], [17], and [18]. This SSCB utilizes reverse blocking IGCT technology, designed with a very low forward voltage drop of 0.9 V at 1000 A, resulting in very low conduction loss. However, due to its physical size, cooling method, and cost, this solution is only suitable for medium to high power applications. A 1.5 kV/0.35–5 kA dc breaker using IGBT or IGCT technologies for the marine industry was presented in [19] and [20]. This system requires forced-air or liquid cooling, which consumes substantial power and could be noisy, making it unsuitable for residential and commercial building applications. A 700 V/15A current router with protection against short-circuit, RCD, and overvoltage was presented in [21]. It is applicable for dc building applications, such as offices. However, the total power loss is 15 W, preventing it from achieving 99.90% efficiency. In addition to SSCB products from industry, the academic field has shown great interest in SSCB research. An intelligent SSCB (iBreaker) using 25 mΩ GaN FETs was presented in [22]. It achieved very low on-state loss, but only the loss of the main switches was considered in the design, and the efficiency of the complete CB was not clearly evaluated. The PWM current limit control reduces the CB's output voltage substantially during inrush current, which may cause load equipment to trip due to undervoltage. A SiC SIT-based SSCB was presented for 400 V dc data center applications [23]. However, the power density of the SSCB and the market availability of the SiC SIT device limited the commercialization of this solution. A self-powered SSCB using normally-on SiC JFETs for the main current conducting path was presented in [24], [25]. It provided very fast short-circuit clearance but power efficiency is not the key focus. The relative high power loss makes it difficult for practical applications particular for life long operation. A GaN based 750 V/100A SSCB with superior efficiency of larger than 99.99%. However, the operating temperature of −180 °C that makes it difficult for practical applications.

According to the literature review, the research focus of SSCB for low voltage dc (LVDC) grid is mainly on the application of new or advanced semiconductors to achieve highly efficient ON-state operation. However, the design of SSCBs with comprehensive consideration of actual application criteria is often emphasized. This gap makes it difficult to translate novel technologies into actual commercial applications. In this article, an optimized design of dc SSCB from derivation of circuit topology to full-scale prototype experimental evaluation for residential and commercial buildings applications is presented. The proposed solution comprehensively considers power loss, cost, power density, thermal management, and breaking capacity in accordance with key international standards without sacrificing on innovation.

Fig. 2 shows the circuit schematic of the proposed SSCB. The proposed SSCB has the following merits:

1) 99.90%+ efficiency from ∼25% load.
2) Natural cooling design, basically no acoustic noise.
3) Physical disconnection in the OFF-state.

A 400 V/40 A dc SSCB prototype was built for experimental evaluation. The electrical and thermal performance, as well as the current interruption capability of the proposed solution, were studied analytically and experimentally. Test results showed that

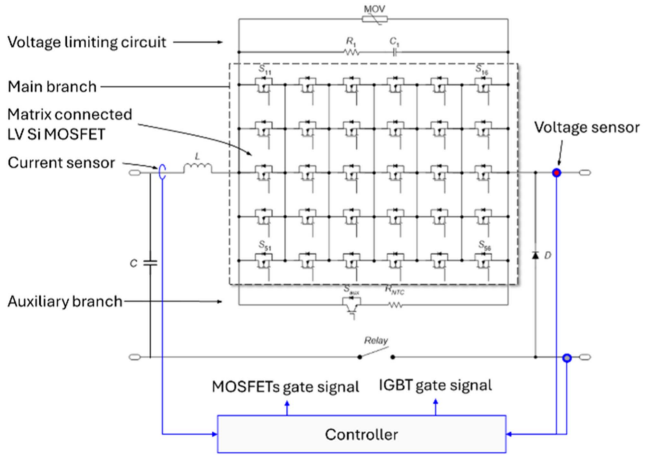


Fig. 2. Power stage topology of the proposed SSCB.

the naturally cooled SSCB achieved 99.90%+ efficiency and was able to response to short-circuit faults in approximately 5 μs. It can provide effective protection against short-circuit, overload, and overvoltage faults. The theoretical predictions and experimental results are in good agreement.

This rest of this article is organized as follows: Section II explains the detailed SSCB design, including circuit topology and digital control. Section III covers the thermal and mechanical design. Experimental verification of the prototype is provided in Section IV. Finally, Section V concludes this article.

II. Electrical Design of the SSCB

A. Proposed SSCB Topology

In circuit breaking applications, CBs operate in conduction mode for most of the time and respond to faults occasionally but immediately to ensure timely protection. Both conduction loss and current interruption capacity are critical electrical factors to be examined. Mechanical CBs are highly efficient, with maximum power loss limited by IEC 60898-3. Power loss should be below 15W for a 2-pole 40A CB. Therefore, efficiency of a 2-pole 400 V/40A dc CB is higher than 99.90%. For an SSCB to achieve equivalent performance, the design of the main current handling branch is highly critical, as semiconductors are generally more lossy than metal contacts. In mechanical CBs, an electric arc is induced across the air during disconnection, necessitating an arc chute to clear the arc and prevent damage to the CB from high temperature. Similarly, in SSCBs, overvoltage during switch-OFF due to the existence of cable inductance and circuit stray inductance could break down the semiconductors. Therefore, the switch-OFF capacity of the semiconductors and the corresponding protection circuit must be carefully designed and examined to ensure the SSCB can meet the ultimate/service short-circuit breaking capacity as per standards (IEC 60898-3 for uninstructed people, IEC 60947-2 for instructed people, IEC 60497-3 with disconnector).

Fig. 2 shows the power stage circuit topology of the proposed SSCB. It is a two-pole device, with the positive pole built using semiconductors to provide ultrafast and arc-less current interruption, while the negative pole is built using a mechanical relay to provide physical disconnection in the OFF-state. For the positive pole, the circuit consists of an inductor, L, to suppress current noise induced by the load and limit the maximum *di/dt* for the SSCB to response in a short-circuit; a main branch with matrix-connected 100 V Si MOSFETs responsible for current conduction in the ON-state and current interruption during faults or normal switch-OFF of the SSCB; an auxiliary branch with an IGBT and negative temperature coefficient (NTC) thermistor responsible for soft start and current commutation to assist the main branch's switching ON and OFF; a voltage limiting RC snubber circuit to suppress voltage overshoot across the main and auxiliary branches during switch-OFF; and an output diode, D, to freewheel the current on the output side immediately after the SSCB is switched OFF. A mechanical relay is designed in the negative pole to provide physical disconnection in the OFF state. The design of the main and auxiliary branches with respect to power loss, switch-OFF capacity, thermal performance, and cost will be detailed in the following section.

B. Design of the Main and Auxiliary Branches

The design of the power stage topology and the use of semiconductors have been carefully considered to achieve 99.90%+ efficiency for the SSCB. The designs of both the main and auxiliary branches are detailed in this section.

The main branch is responsible for conducting the main current during normal operation and ensuring fast and safe current interruption when a fault occurs. Consequently, the main branch topology should be optimized for on-state loss, voltage blocking and current interruption capacities, and cost. To achieve 99.90%+ efficiency at the rated operating condition, i.e., 400 V/40A dc, the maximum semiconductor conduction loss, P_{Cond}, at a junction temperature, T_J, of 100 °C, was set to 8 W, assuming another 8 W loss across the rest of the components. Therefore, the maximum semiconductor equivalent on-state resistance, $R_{\mathrm{on\_max}}$, of the main branch can be calculated by (1) and equals 5 mΩ at 100 °C T_J

$$R_{\mathrm{on\_max}} \leq \frac{P_{\mathrm{cond}}}{I^2_{\mathrm{rated}}}. \tag{1}$$

To achieve the $R_{\mathrm{on\_max}}$ requirement, the topologies of the main branch could involve either parallel-connected high voltage devices, such as 650 V, or matrix-connected (i.e., series-parallel) low voltage devices, such as 100 V. MOSFETs with Si, SiC technologies, and GaN devices were considered. Current can be evenly shared in parallel-connected devices due to the positive temperature coefficient characteristic. IGBTs are not suitable, as a 1 V forward voltage drop on a 400 V dc results in a 0.25% loss, which cannot achieve the 99.90%+ target efficiency. A benchmarking of topologies was conducted based on power loss, market price, and required cooling effort for the semiconductors. Fig. 3 shows the benchmarking results of approximately 100 candidates using the device's market price and on-state resistance at 100 °C T_J. Each bubble on the graph represents the conduction loss and price of one main branch design, either parallel or matrix, with a specified device. The design enables

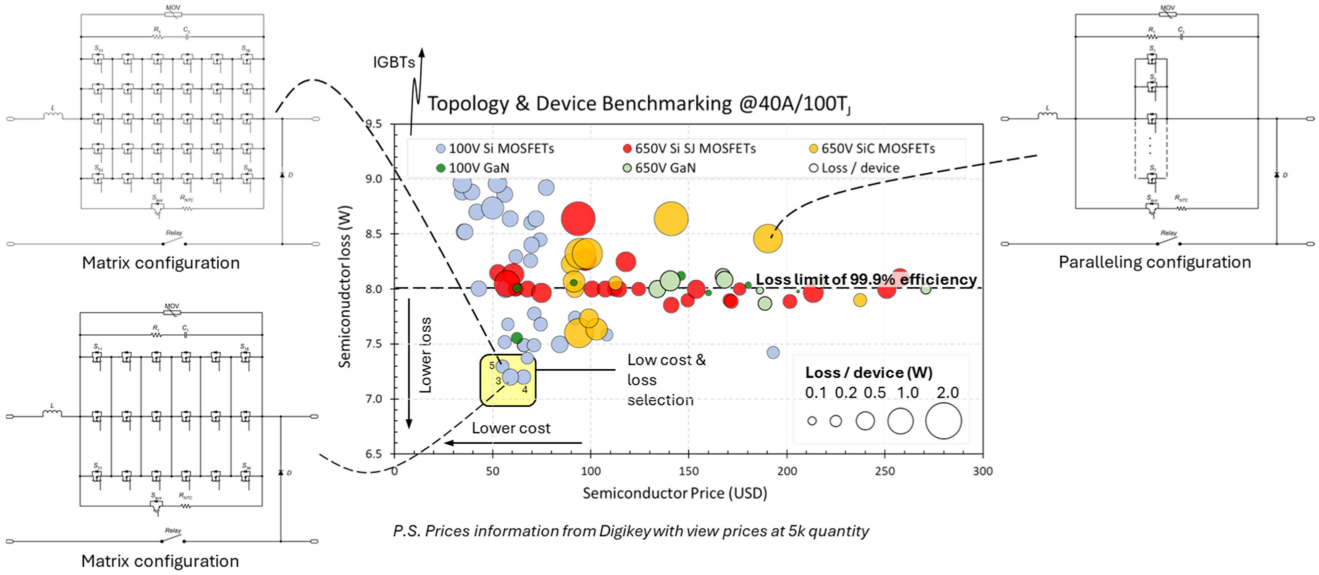


Fig. 3. Topology and semiconductor devices benchmarking.

99.90% efficiency of the SSCB at the rated condition. Bubbles closer to the bottom left-hand corner represent designs with lower conduction loss and price. The size of the bubbles indicates the power loss per device, which significantly affects the cooling requirement and design. Cost of extra gate drive ICs for 100 V device's solutions compared to 600 V/650 V device's solutions is considered. Furthermore, the MOSFETs are mostly at ON-state and switch-OFF occasionally when there is a fault, therefore, difference in gate drive circuit power consumption between the candidates is negligible. Bootstrap method is used to supply the gate drive ICs to eliminate the cost of additional auxiliary power supply.

Natural cooling is preferred to maintain high efficiency and low acoustic noise. From a packaging perspective, higher power density of the SSCB is achievable if the heat sink can be confined to a simple metal plate. Therefore, it is important to limit the device loss such that it can be cooled by a simple metal plate heat sink. A 19 mm × 19 mm × 1.5 mm aluminum plate can provide approximately 70K/W junction-to-air thermal resistance to a ThinPAK MOSFET under natural cooling [26]. The T_J of the MOSFET will reach 100 °C at a 50 °C ambient temperature with a maximum power loss of 0.7W. Therefore, a loss of less than 0.5W per device is preferred to ensure natural cooling with a simple metal plate heat sink, with ∼30% margin.

From the benchmarking results, the candidates below the dotted line ensure 99.90% efficiency of the SSCB. It can be observed that 100 V Si MOSFETs share most of the suitable options. Three candidates in the yellow box are the most preferred, being closer to the bottom left-hand corner. The number next to the bubbles indicates the number of devices in parallel required to reach the $R_{\text{on\_max}}$. The 100 V/100A Si MOSFET, BSC027N10NS5, was finally selected due to its lower price and availability. Therefore, the main branch design is a five-parallel-six-series matrix configuration.

The auxiliary branch is designed to enable a soft start of the SSCB and to maintain a low voltage across the main branch MOSFETs during the turn-OFF transient. The main branch consists of a series connection of six MOSFETs, where inconsistencies in switching speed or delay may occur among the MOSFETs. During the turn-OFF transient, the first turn-OFF MOSFET may need to block the entire voltage across the main branch in the worst-case. To prevent any MOSFET failure due to inconsistency, the auxiliary branch is engineered to commutate the current from the main branch and keep the voltage across the MOSFETs well below their breakdown level. Since the auxiliary branch is not intended for carrying the main current during normal operation, ON-state loss is not a critical consideration in device selection. The auxiliary branch comprises a series connection of a 600 V IGBT and an NTC, chosen for their cost-effectiveness and capability to perform the required functions.

C. Operating Principle

The startup and shutdown sequences are designed to ensure zero-current switching for the mechanical relay, thereby preventing arcing and fatigue, and to create a low-voltage switching environment for the MOSFETs to avoid overvoltage failure. The controller is implemented by using a STM32G474 32-bit MCU. Input inductor current and output voltage are sensed continuously and checked if manual OFF command, short-circuit fault, overload fault, or over voltage fault is triggered. If any of the cases is/are found, the SSCB will go through a disconnection process that firstly turn-OFF the MOSFETs; and turn-OFF the IGBT in a delay of approximately 1 μs that ensure all MOSFETs are completely OFF; finally turn-OFF the relay in a delay of 1s that ensure the load current reached zero. The turn-OFF process ensures a safe turn-OFF of the semiconductors. A control flow chart of the SSCB is shown in Fig. 4.

At startup, the mechanical relay closes under zero-current conditions while both the main and auxiliary branches remain OFF. After an approximate 1 second delay to allow the relay to settle, the IGBT in the auxiliary branch is activated. This action

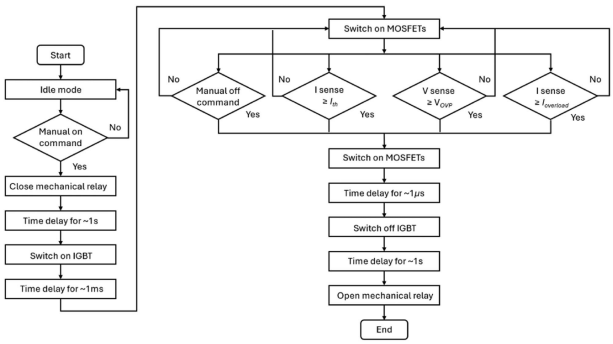


Fig. 4. Control flow chart of the SSCB.

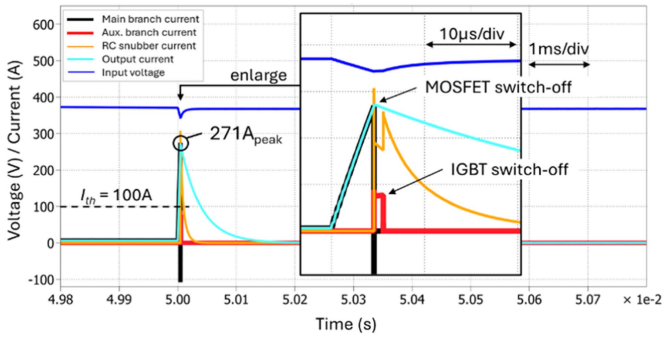


Fig. 5. Simulation result for short-circuit protection.

gradually increases the SSCB's output voltage, with the inrush current limited by the series-connected NTC. Subsequently, the MOSFETs in the main branch are turned ON after approximately 1ms, bypassing the auxiliary branch. The current naturally commutates to the main branch due to the lower ON-state resistance of the MOSFETs. ON-resistance of the matrix connected MOSFETs ∼3.24 mΩ compared to the auxiliary brand 5.011 Ω (11 mΩ from IGBT plus 5 Ω from NTC thermistor). Furthermore, voltage drop across the MOSFETs is ∼0.130 V at rated current 40 A and ∼1.30 V at maximum overload current, lower than the 1.50 V collect-emitter threshold voltage of the IGBT in the auxiliary branch. The turn-ON process is thus completed, with the current conducted through the main branch, resulting in very low ON-state conduction loss.

When disconnection is triggered, either by a short-circuit fault or a manual command, the MOSFETs are switched off immediately. The current then commutates from the main branch to the auxiliary branch, where the NTC limits the current. To prevent the MOSFETs from experiencing overvoltage during turn-OFF due to asymmetrical switching speeds, the IGBT remains on for approximately 1 μs, allowing all MOSFETs to complete the turn-OFF action. The IGBT is then turned OFF, and the current commutates to the voltage-limiting branch. The energy stored in the input inductor and input cable inductance is absorbed by the snubber circuit in the voltage-limiting circuit, protecting the MOSFETs and IGBT from overvoltage. The mechanical relay is turned OFF approximately 1 s after the IGBT, ensuring a zero-current switching condition for the relay.

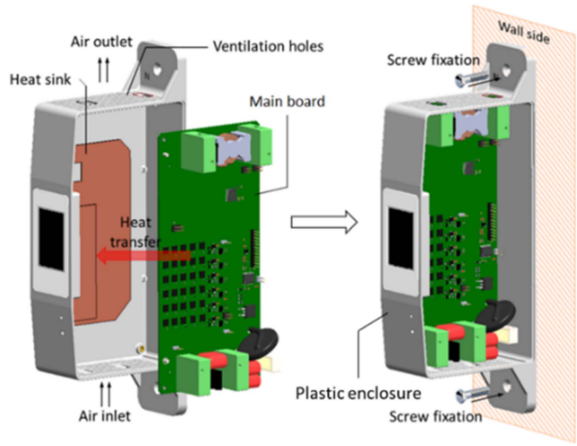


Fig. 6. Structure design of the proposed SSCB.

Fig. 5 presents the simulation results of the SSCB switch-OFF process with a 100 A short-circuit current threshold by PLECS. During a short-circuit, the main branch current (shown in black) increases with the *di/dt* limitation imposed by the input inductor, *L*, and cable inductance. When the current exceeds the threshold, $I_{\rm th}$, of 100 A, the MOSFETs switch-OFF in an around 2 μs response time delay, and the current in the main branch commutates to the auxiliary branch (shown in red) and the voltage-limiting *RC* snubber circuit (shown in orange), according to the instantaneous resistance ratio $R_{\rm NTC}$: R_1. After an approximate 1 μs delay, the IGBT switches OFF, and the current in the auxiliary branch commutates to the voltage-limiting circuit, naturally reducing to zero within 1ms.

III. Thermal Design of the SSCB

The proposed SSCB features a natural cooling design to ensure low acoustic noise and high efficiency. Fig. 6 provides an overview of the prototype's structure design. It is a wall-mounted design with a plastic enclosure to maintain lightweight and electrical insulation for the user. A heat sink is installed between the enclosure and the main board PCB to dissipate heat from the semiconductors. Ventilation holes are strategically placed on both the top and bottom sides of the enclosure to facilitate air flow. Detailed design considerations are outlined below.

A. Design of Heat Sink for Weak Natural Ventilation

The heat sink design is aimed to cool the MOSFETs, i.e., the critical component, with minimal space and power consumption. Due to the very limited space, it is preferred to have a heat sink with higher heat capacity thus a lower thermal equilibrium temperature for a given ventilation. Power dissipation per MOSFET is controlled below 0.5 W, a passive heat sink without fins to keep small size is deemed the most appropriate solution. Copper was selected as the heat sink material due to its high specific heat capacity (0.376 J/g·K), density (8.92 g/cm^3), and thermal conductivity (401W/m·K), outperforming common heat sink materials such as aluminum and ceramic. These characteristics allow a copper plate heat sink to absorb heat rapidly and buffer

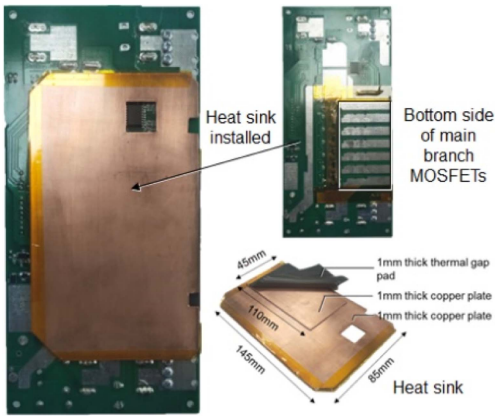


Fig. 7. Heat sink of the SSCB.

the weak natural ventilation of the SSCB and achieving thermal equilibrium at a lower temperature.

All power semiconductors are surface mounted on the top layer of the main board. The copper plate heat sink is attached to the bottom side to extract heat from the MOSFETs through the PCB's vias. Fig. 7 shows the heat sink of the SSCB prototype. The heat sink consists of a small copper plate ($45 \times 110 \times 1$ mm) which covers the bottom side of the MOSFETs and transfers heat from the MOSFETs to a large copper plate ($85 \times 145 \times 1$ mm). The small copper plate acts as a thermal bridge between the main board and the large copper plate and ensures sufficient clearance between them to avoid short-circuit between the solder joints on the bottom layer. The small copper plate is attached to the main board via a thermal gap pad, providing electrical insulation with good thermal conductivity (5W/m·K). The large copper increases the entire heat sink heat capacity. Compared to the aluminum and ceramic such as aluminum nitride, the heat sink made by copper resulted around 1.4 times higher in heat capacity this gives a lower equilibrium temperature under weak ventilation condition.

B. Design of Enclosure for Natural Ventilation

Thermal simulations were conducted using SOLIDWORKS Flow Simulation to facilitate the thermal design and predict the thermal performance of the SSCB prototype. It is aiming to understand the air flow and MOSFETs junction temperature at different enclosure designs and load conditions. The simulations covered load conditions ranging from 50% to 125% at an ambient temperature of 25 °C. Junction temperatures of the MOSFETs at 40 A 100% load were recorded and shown in Fig. 8. From the simulation, the outlet air temperature is ~55 °C maximum which implies the temperature inside the enclosure is 30 °C higher than the ambient temperature. It gives the reference of component selection respect to thermal. Due to the vertical mounting of the SSCB, MOSFETs in the upper rows are generally hotter than those in the lower rows. The highest temperature MOSFETs are located at the top region at fourth to sixth rows. This is attributed to two factors: first, hot air rises due to natural convection; second, MOSFETs are heated by their neighboring MOSFETs, resulting in higher temperatures for the inner MOSFETs compared to the outer.

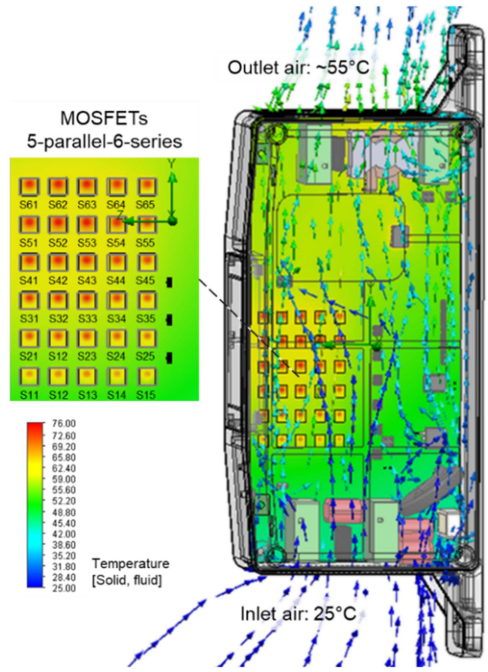


Fig. 8. Thermal simulation result of the SSCB 40A, 25 °C Ta.

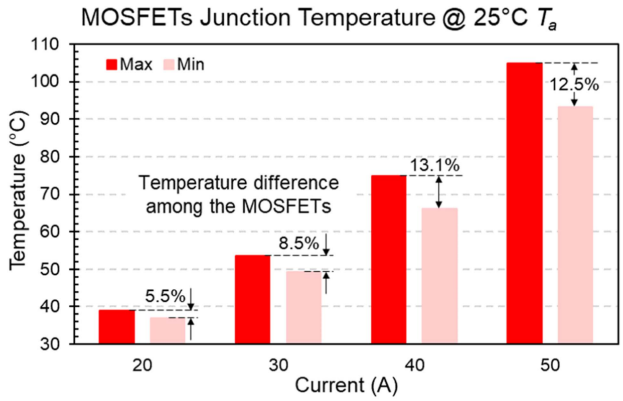


Fig. 9. MOSFETs temperature at different load current.

At equilibrium, MOSFETs in the fourth to sixth rows experience the highest thermal stresses. The average temperature rise is 47.0 °C, and the maximum temperature difference among the MOSFETs is around 13.1% as shown in Fig. 9. Simulations were repeated with 20 A, 30 A, and 50 A.

At 50 A load, it is assumed that the current is evenly shared among the five parallel MOSFET strings, with an on-state resistance of 2.75 mΩ, resulting in a power dissipation of 0.275 W. The results indicate that MOSFETs S53, S52, and S62 are the hottest, with maximum junction temperatures of 104.8 °C, 104.4 °C, and 104.2 °C, respectively, at 25 °C ambient temperature. There is a sufficient margin, around 70 °C, to the selected MOSFETs' maximum T_J of 175 °C [27].

Ventilation holes are strategically designed on both the top and bottom sides of the enclosure to facilitate vertical natural ventilation by providing air inlets and outlets. Larger hole sizes

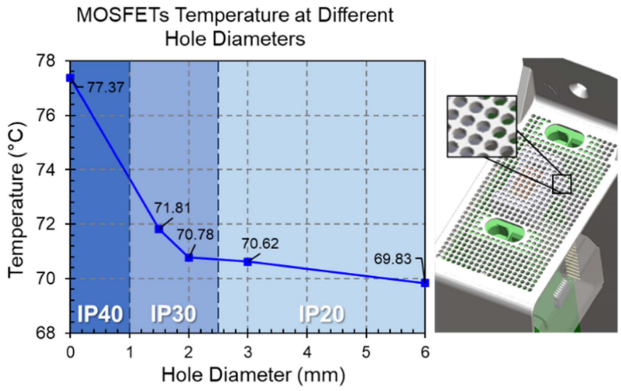


Fig. 10. SSCB ventilation holes design @ 40A, 25 °C.

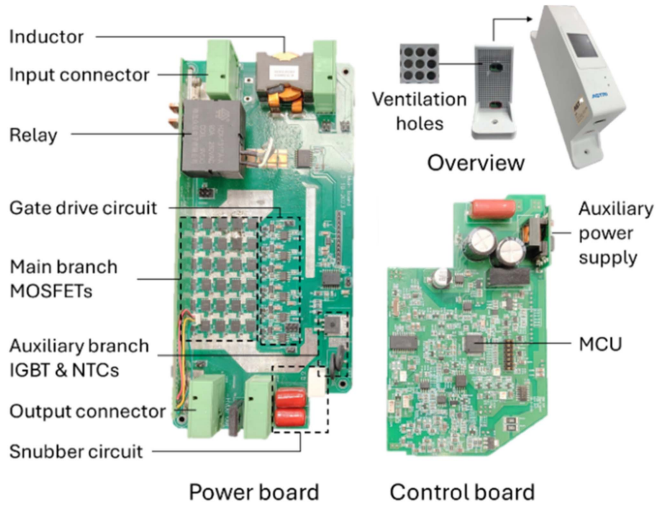


Fig. 11. Photo of the prototype.

enhance airflow through the SSCB, but compromise protection against foreign object intrusion. Thermal simulations were conducted under a 40A load and 25 °C ambient temperature to optimize the hole size, diameter ranging from 0 to 6.0 mm with keeping the total hole area the same, considering both thermal performance and ingress protection (IP) rating. Simulation results are shown in Fig. 10, a reference MOSFET junction temperature reached 77.37 °C in an enclosure without ventilation holes. Increasing the hole diameter to 2.0 mm reduced the temperature by 8.52% to 70.78 °C. However, further increasing the diameter to 6.0 mm resulted in only a 1.34% reduction. A higher IP rating is preferred for safety. From the simulation results, increasing the IP rating from IP30 to IP40 caused a 7.74% increase in MOSFET temperature, while reducing the rating from IP30 to IP20 caused only a 0.23% temperature reduction. Consequently, a 2.0 mm ventilation hole diameter was selected that balanced thermal performance and IP rating.

IV. Experimental Verification

A natural cooled, 400 V/40A, SSCB prototype was built for experimental verification. Fig. 11 shows the prototype with the topology shown in Fig. 2 and key components parameter given in Table I. The main branch is a matrix connected five-parallel-six-series 100 V MOSFETs. The auxiliary branch is a series connected IGBT and NTC.

TABLE I
SSCB Prototype Parameters

Item	Value / PN	Item	Value / PN
$S_{11}-S_{65}$	BSC027N10NS5	S_{aux}	IGB50N60T
Rated voltage	400 V	C_1	3 μF
Rated current	40 A	L	3.3 μH
R_1	1.5 Ω	R_{NTC}	5 Ω
Controller	STM32G474		

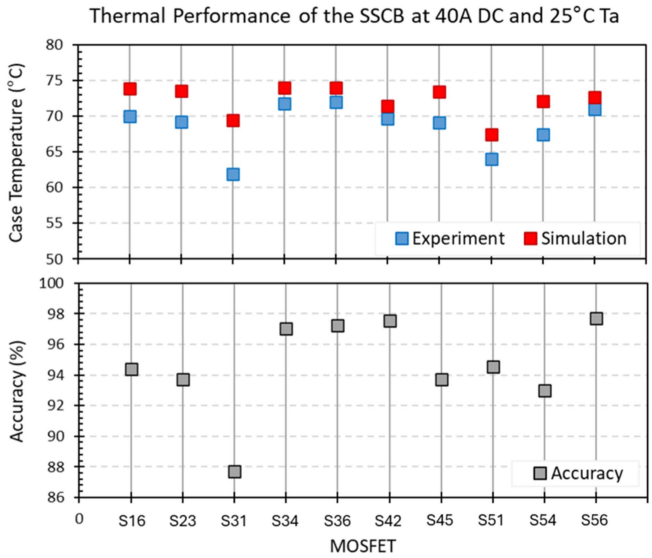


Fig. 12. Thermal measurement result of the prototype.

Thermal measurement was carried out at 40A rated current condition and 25 °C T_a. Top side case temperature of ten MOSFETs have been recorded by using thermal couples until thermal equilibrium. Measurement results are shown in Fig. 12 together with the simulation results. The red and blue markers are the simulation and experimental results respectively. The maximum temperature of the MOSFETs is below 75 °C. The measured temperatures are in good agreement with the simulated results with difference mainly below 8%. According to the datasheet, junction-to-case (top side) thermal resistance, $R_{th\_j\text{-}c(\mathrm{top})}$ of the selected MOSFET is 20K/W; it can be estimated by (2) that the junction temperature will be 3.52 °C higher than the case temperature. Therefore, there is significant margin from the maximum operating junction temperature, that is 175 °C.

$$T_J = T_{c(\mathrm{top})} + P_{\mathrm{loss}} \times R_{\mathrm{th\_}J-c(\mathrm{top})} \tag{2}$$

$$T_J - T_{c(\mathrm{top})} = \left(\frac{40A}{5}\right)^2 \times 2.75\ \mathrm{m\Omega} \times 20\ \mathrm{K/W} = 3.52^{\circ}C_{\max}.$$

SSCB prototype's efficiency has been measured at ambient temperatures from 20 °C to 50 °C. The SSCB was powered by a dc power supply at current level from 10 to 40 A. Power stage's power loss and control stage's power consumption were

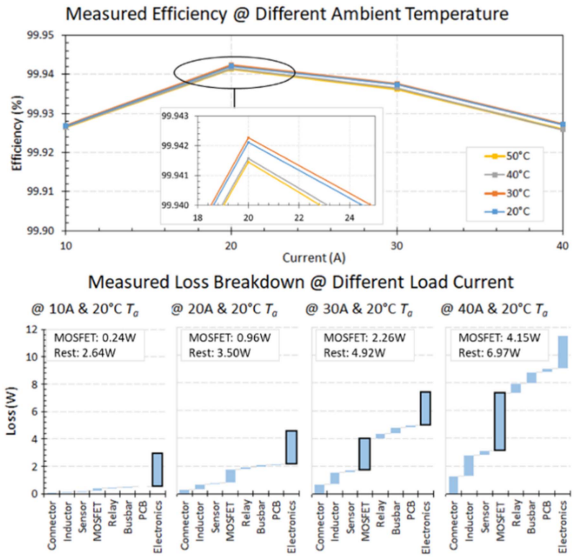


Fig. 13. Measured efficiency and loss breakdown at different ambient temperatures and load current.

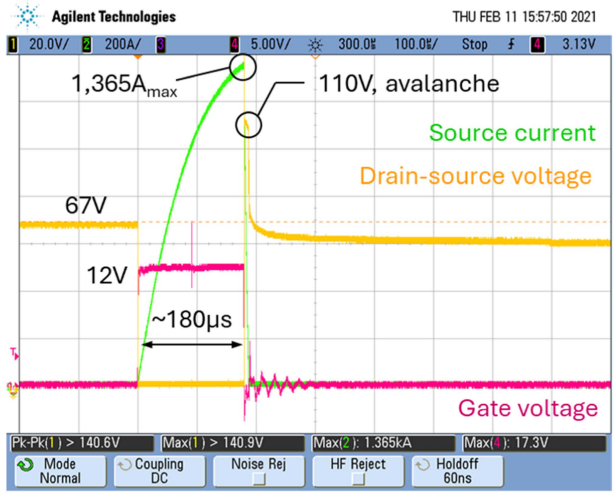


Fig. 14. Maximum switch-OFF capability of five paralleled BSC027N10NS5.

measured separately and carefully to ensure accurate results. Power loss at different load current is calculated

$$\text{Eff.} = \frac{P_{\text{in}} - P_{\text{power stage loss}} - P_{\text{contorl stage consumption}}}{P_{\text{in}}}. \quad (3)$$

Measurement results are shown in the top figure of Fig. 13. The efficiency is constantly higher than 99.92% and the peak efficiency is ∼99.94% @ 20A load condition across the ambient temperature. It shows power loss of the SSCB is basically very consistence from 20 °C to 50 °C T_a. The efficiencies were very close at 20 °C T_a and slightly reduced at higher T_a when load current went higher. The reduced in efficiency is mainly due to the increased in ON-resistance of the MOSFETs at high T_a. Respect to the datasheet of the selected MOSFET, the ON-resistance will be increased by ∼15% for a 30 °C increasement in T_j between 20 °C and 100 °C. Therefore, conduction loss of the MOSFETs in the main branch will be increased by ∼15% which caused the reduce in efficiency.

A. Thermal and Efficiency Measurement

Loss breakdown of key components was measured at load currents from 10 to 40 A and 25 °C T_a, results are shown in Fig. 13 bottom figure. By inspection, loss of electronics, i.e., power consumption of the auxiliary power supply, MCU, ICs, signal level circuitry, were the major loss of the SSCB at 10 and 20A loads; it became similar to the MOSFETs loss at 30A; and MOSFETs loss dominant at 40 A. The total loss at 40 A is below 12 W, it is comparable to state-of-the-art electromechanical CB which allows maximum 15 W for 2 poles [28]. Almost 7 W loss is shared by rest of the components at 40 A condition. It is close to the assumption made in Section II-B.

B. Semiconductors Switch-off Capability Test

Semiconductor switches are the most fragile component in the SSCB; to evaluate the margin of the switch-OFF capability between the selected semiconductors compared to the maximum switch-OFF conditions of the SSCB; a clamped inductive switching test was conducted. The selected 100 V Si MOSFET and 600 V Si IGBT were tested and analyzed. The inductance in the characterization is in a close value to the loop inductance of the SSCB prototype that justifies the results is applicable for the prototype. The pulse width was incrementally increased by 1 μs steps, and the switch-OFF current across the device under test (DUT) was increased accordingly until breakdown occurred. The test conditions, specifically the current level and pulse width immediately before DUT breakdown, define the switch-OFF capability of the DUT [29].

For the MOSFET, five parallel-connected BSC027N10NS5 devices were used with a 67 V supply voltage (equivalent to 400 V across six series-connected MOSFETs) and a 12 V gate voltage at 25 °C ambient temperature. The test results, shown in Fig. 14, indicate a maximum switch-OFF capability of approximately 1365 A at an ambient temperature of 25 °C, with a short-circuit duration of approximately 180 μs. For the IGBT, the short-circuit withstand time is around 9 μs at 12 V gate-emitter voltage. To ensure the IGBT can be safely turned OFF in a short-circuit event; the turn-OFF delay time is set to ∼1 μs after the MOSFET gate turn-OFF signal is applied. Therefore, the short-circuit withstand time to the IGBT is ∼1 μs.

C. Short-Circuit Breaking Capacity Test

A short-circuit breaking capacity test on the SSCB was conducted in accordance with IEC 60947-1 standard. Fig. 15 illustrates the simplified test setup and the measured waveforms. A dc power supply provides 400 V to charge the capacitor bank. The input of the SSCB under test is connected to the capacitor bank, and the output is connected to a short-circuit switch via a 10 m length, 70 mm^2 cross-sectional area cable, as shown in the top part of Fig. 15.

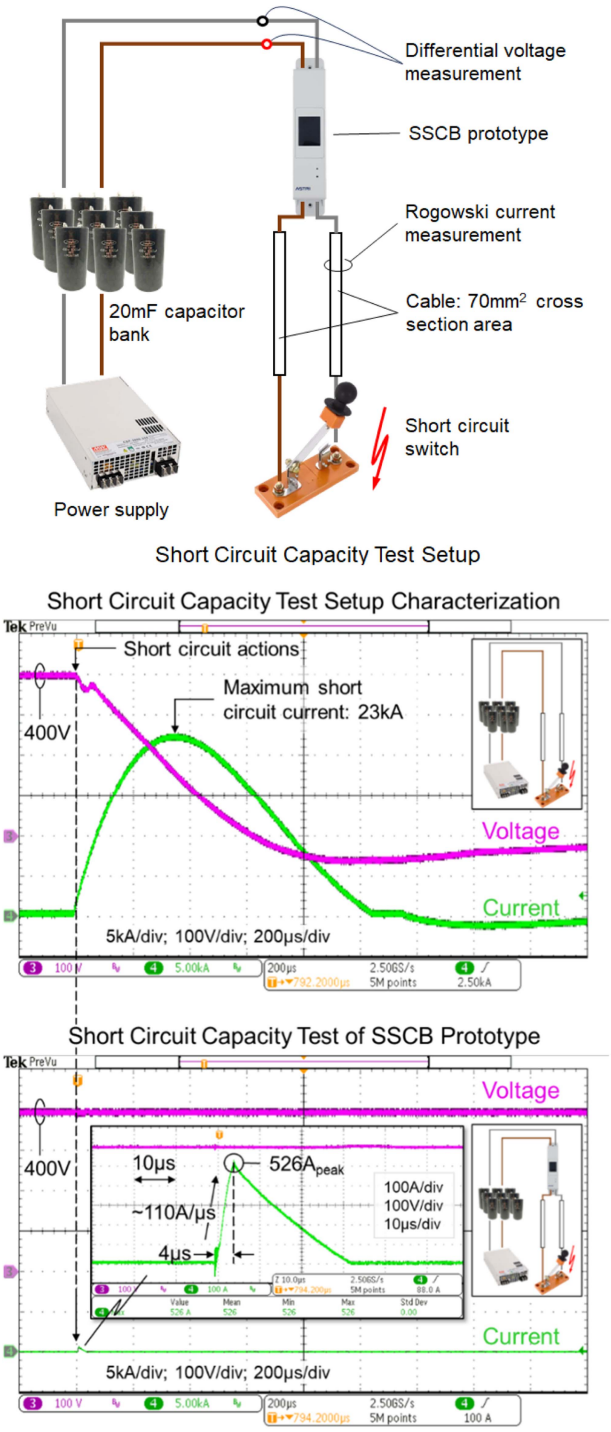


Fig. 15. Breaking capacity test setup and the test results.

The test procedure involved charging the capacitor bank to 400 V, switching ON the SSCB prototype, and then closing the short-circuit switch to record the waveforms. Prior to testing with the SSCB; a test was conducted to evaluate the maximum current of the test setup can provide in a short-circuit with without the SSCB. The results, shown in the first waveform of Fig. 15, include the short-circuit current and voltage waveforms of the test setup without the SSCB, indicating a maximum short-circuit current of approximately 23 kA at 400 V dc. The SSCB prototype was then installed in the test setup, and the test was repeated. The SSCB successfully disconnected, with the switch-OFF action occurring shortly after the short-circuit take place as shown in the bottom waveform of Fig. 15. The switching moment is enlarged that clearly shows the *di/dt* is around 110 A/μs and peak current is 526 A. The response to the short-circuit is ~4 μs. Test verified the SSCB has 23 kA short-circuit breaking capacity at 400 V dc. It is able for residential and commercial applications which typically require 6 kA and 10 kA breaking capacity. The short-circuit current is returned to zero in ~28 μs from the peak. The I^2t is calculated and equal to ~4.43 A^2s at 23 kA prospective short-circuit current. The I^2t is very small that helps to minimize the thermal stress on the cable in a short-circuit fault.

Short-circuit tests were conducted on the SSCB prototype at settings D10, D20, and D40. The "D" indicate that the short-circuit tripping current is ten to twenty times of the nominal current level, specifically 100–200 A for D10, and similarly for the other settings. The SSCB prototype successfully tripped in all three tests. The response time to the short-circuit fault was below 5 μs after the current reached the minimum tripping levels, as shown in Fig. 16. At the D40 setting, the current peak was approximately 612A, indicating that the MOSFETs in the main branch switched OFF at 612 A, which is about 45% of their maximum switch-OFF capability. Due to the 5:2 resistance ratio between the auxiliary branch and the voltage limiting circuit; the IGBT in the auxiliary branch switched OFF at approximately 175 A, representing about 57% of its maximum switch-OFF capability. Switch-OFF capability for the semiconductors in both the main and auxiliary branches are larger than 40%.

D. Thermal Sensitivity Test

The SSCB has been rigorously tested at ambient temperatures ranging from 20 °C to 50 °C to assess its thermal sensitivity. The SSCB was configured to D20, and the measured short-circuit tripping waveforms are illustrated in Fig. 17. The waveforms indicate a current increase rate of 20 A/μs, with the SSCB's response time remaining highly consistent across the ambient temperatures (20 °C, 40 °C, and 50 °C). It confirmed the sensing and driving circuits are insensitive to ambient temperature variation; these guarantee a consistence short-circuit protection performance. Furthermore, it has been verified both the power stage and the control methodology across the temperature range.

E. Voltage Balancing and Current Sharing Between Main Branch MOSFETs

Each MOSFET is driving with its own gate drive resistor and a relatively large resistance, 27 Ω, is selected. It helps to minimize gate-source and drain-source voltages oscillation at turn-OFF transient and diminish the voltage unbalance effect cause by different in turn-OFF processing time between the series connected MOSFET. Fig. 18 shows the drain-source voltage waveforms at turn-OFF of the first, third, and sixth rows MOSFET. From the results, voltage level of all three rows MOSFETs are well balanced. The time difference is ~26 ns maximum.

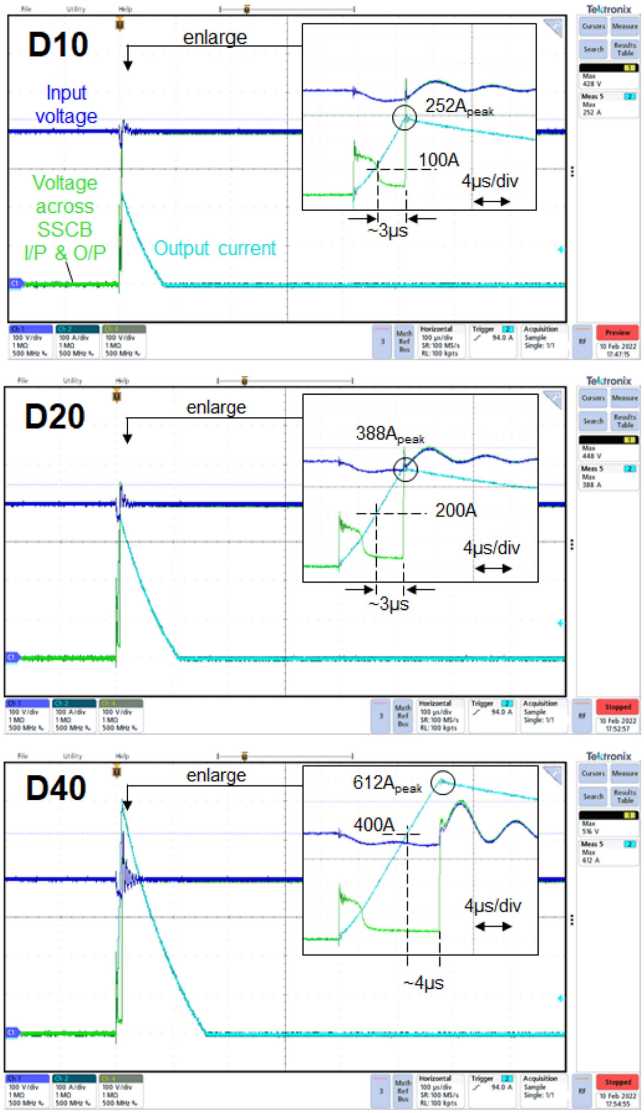


Fig. 16. Short-circuit protection test at different current ratings.

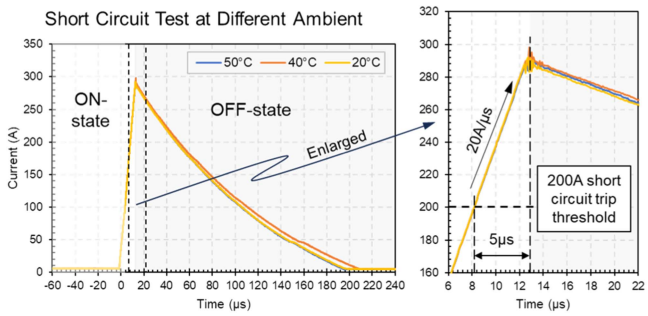


Fig. 17. Short-circuit protection of SSCB at different ambient temperatures.

An evaluation of current sharing between parallel MOSFETs was conducted. The SSCB was operated at 40A and 20 °C ambient temperature until thermal equilibrium was reached. Fig. 19 left-hand side shows the thermal image of the MOSFETs, while the case temperatures are tableted in the table on the right-hand side. When comparing the MOSFETs temperature within each

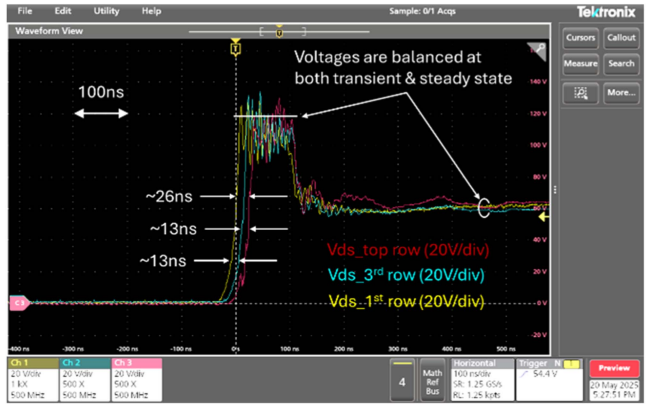
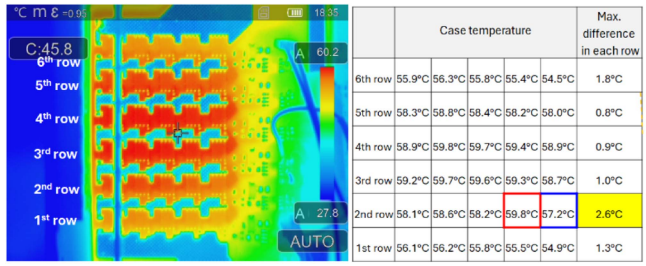


Fig. 18. Voltage balancing between MOSFETs at turn-OFF transient.



	Case temperature					Max. difference in each row
6th row	55.9°C	56.3°C	55.8°C	55.4°C	54.5°C	1.8°C
5th row	58.3°C	58.8°C	58.4°C	58.2°C	58.0°C	0.8°C
4th row	58.9°C	59.8°C	59.7°C	59.4°C	58.9°C	0.9°C
3rd row	59.2°C	59.7°C	59.6°C	59.3°C	58.7°C	1.0°C
2nd row	58.1°C	58.6°C	58.2°C	59.8°C	57.2°C	2.6°C
1st row	56.1°C	56.2°C	55.8°C	55.5°C	54.9°C	1.3°C

Fig. 19. Current sharing between MOSFETs at steady state.

row, the maximum temperature difference ranged from 0.8 °C to 2.6 °C. Since the on-state resistance of the MOSFETs varies with junction temperature, MOSFETs in the second row exhibited the maximum case temperature difference, ranging from 59.8 °C to 57.2 °C. The corresponding on-state resistance were approximately ∼2.506 mΩ and ∼2.447 mΩ respect to the datasheet. The difference in on-state resistance is only about 2.4%, indicating that current sharing between the five parallel-connected MOSFETs had a maximum difference of approximately ∼2.4%.

F. Overload Protection Test

Overload protection of the SSCB is designed respect to the MCB thermal trip curves. It is to tolerance the inrush current caused by the load. The overload duration varies with the multiple of the rated current as shown in Fig. 20 right-hand side [31]. The green area is the allowable region to switch-OFF the breaker under overload condition. Figures on the left-hand side show the test results from two times of rated current to eight times. The prototype is successfully trip within the green region. Absolute limitation of the overload duration has been investigated to ensure the proposed SSCB not only able to trip according to the standard requirement but also the with sufficient margin.

Semiconductor is the most fragile component in the SSCB. Experiment has been performed to investigate the thermal margin of the main branch MOSFETs at overload conditions. The maximum junction temperature of the selected MOSFET is 175 °C. Since junction temperature cannot be directly measured; case temperature of the MOSFET is measured at different load

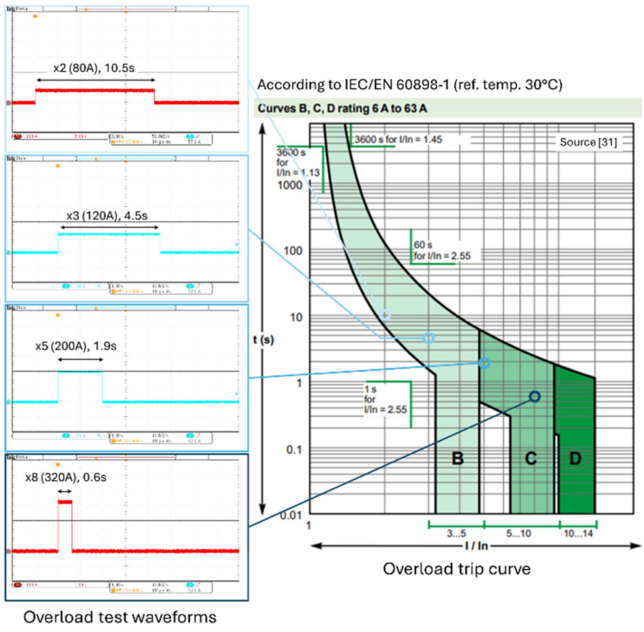


Fig. 20. Overload protection test of SSCB.

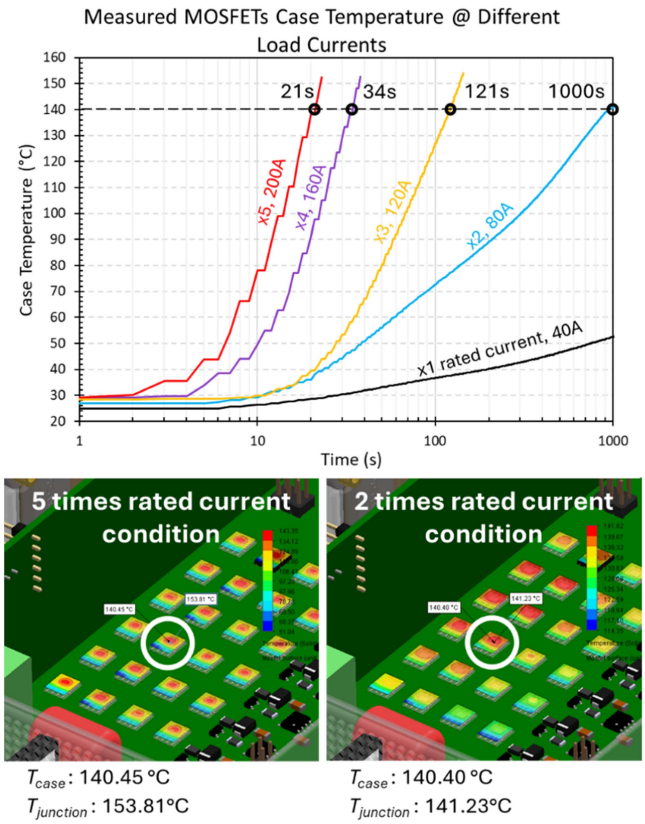


Fig. 21. Maximum thermal limit of the main branch MOSFETs.

current levels. Time to reach 140 °C case temperature is set as the maximum limit with considering 35 °C difference between case and junction. This ensured the junction temperature will not exceed 175 °C. Fig. 21 top figure shows the measurement results. Time to reach 140 °C case temperature of 2 to 5 times of the rated current is around 1000 s, 121 s, 34 s, and 21 s, respectively. It is much longer than the required overload duration of the CB. Therefore, the proposed SSCB is able to handle the overload with sufficient thermal margin.

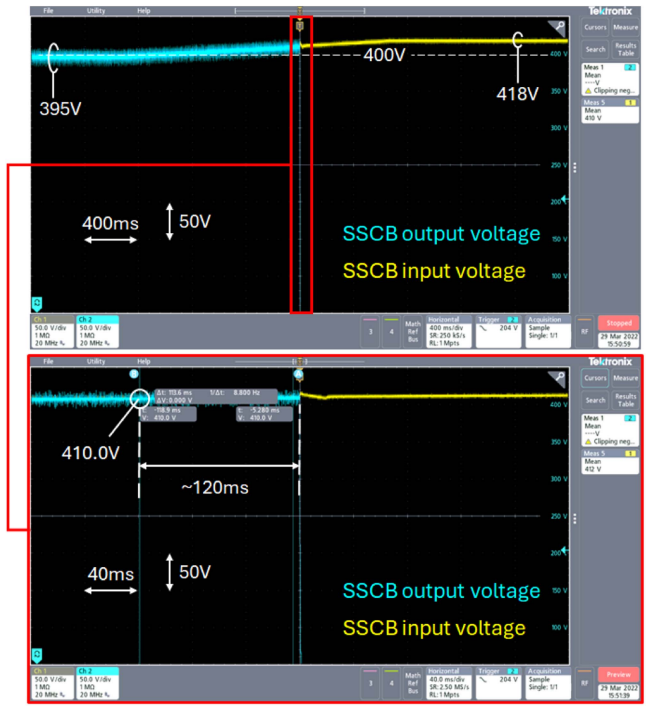


Fig. 22. Overvoltage protection test of SSCB.

A SolidWorks Flow simulation was conducted to understand the difference between junction and case temperatures of MOSFETs. The simulation condition is two and five times of the rated current. Results are shown in the lower part of the Fig. 21. Left-hand side figure is the simulation of two times rated current and right-hand side is five times. The junction temperature is higher than the case temperature by about 0.83 °C and 13.36 °C, respectively. Therefore, considering 35 °C margin between case and junction temperature is secured.

G. Overvoltage Protection Test

The overvoltage protection function has been designed and implemented. Input voltage of the SSCB is sensed and compared to a preset threshold, such as, 410 V. Once the sensed input voltage reaches this threshold, the SSCB will trip. Fig. 22 shows the test results. The top waveform provides an overview, showing the SSCB input voltage increasing from 395 to 418 V. When the input voltage reached 410 V, it takes approximately 120 ms to trip the SSCB as shown in the bottom enlarged waveform. This demonstrates the proposed SSCB can protect against overvoltage effectively.

V. Conclusion

This article presents the design and verification of a cost-efficient 400 V/40A SSCB tailored for LVDC applications in

residential and commercial buildings. The proposed SSCB solution ensures 99.90%+ efficiency, utilizing a simple copper plate heat sink under natural cooling conditions. This design guarantees low acoustic noise, extended lifespan, and compact size. Benchmarking of the SSCB topology and semiconductor selection for the main branch has confirmed that a matrix connection of 100 V Silicon MOSFETs is the optimal solution in terms of both efficiency and today cost information. Experimental results demonstrate that the proposed SSCB achieves a consistent response time of 3–5 μs to a 400 V dc short-circuit from 20 °C to 50 °C ambient temperature. Additionally, the SSCB has been tested with 23 kA short-circuit breaking capacity which adequately covers the requirements for general residential and commercial applications which are up to 10 kA.

REFERENCES

[1] H. R. Chethan, P. S. Puttaswamy, S. Dakshayini, M. Likhitha, V. Sneha, and B. U. Yashaswini, "Green charge: Managing solar energy in smart buildings," in *Proc. Int. Conf. Elect., Electron., Commun., Comput. Technol. Optim. Techn.*, Dec. 2021, pp. 53–57.

[2] M. W. Akram, M. F. M. Zublie, M. Hasanuzzaman, and N. A. Rahim, "Global prospects, advance technologies and policies of energy-saving and sustainable building systems: A review," *Sustainability*, vol. 14, 2022, Art. no. 1316, doi: 10.3390/su14031316.

[3] S. A. Nabavi, N. H. Motlagh, M. A. Zaidan, A. Aslani, and B. Zakeri, "Deep learning in energy modeling: Application in smart buildings with distributed energy generation," *IEEE Access*, vol. 9, pp. 125439–125461, 2021.

[4] UNEP and GlobalABC, "Global status report for buildings and construction," 2024.

[5] W. Huynh, T. T. Hoang, A. Ukil, and N.-K. C. Nair, "Comparison of low-voltage AC and DC distribution networks for EV charging," in *Proc. IEEE Workshop Electron. Grid*, Nov. 2022, pp. 1–5.

[6] R. Chacko, S. T. Raju, Z. V. Lakaparampil, and J. Thomas, "Computation based comparison of LVDC with AC for off-grid energy efficient residential building," in *Proc. IEEE Int. Power Renew. Energy Conf.*, Oct. 2020, pp. 1–6.

[7] R. Weiss, L. Ott, and U. Boeke, "Energy efficient low-voltage DC-grids for commercial buildings," in *Proc. Int. Conf. DC Microgrids*, Jun. 2015, pp. 154–158.

[8] G. AlLee and W. Tschudi, "Edison redux: 380 VDC brings reliability and efficiency to sustainable data centers," *IEEE Power Energy Mag.*, vol. 10, no. 6, pp. 50–59, Nov./Dec. 2012.

[9] X. Feng, Q. Xiong, D. Wardell, A. L. Gattozzi, S. M. Strank, and R. E. Hebner, "Extra-fast DC distribution system protection for future energy systems," *IEEE Trans. Ind. Appl.*, vol. 55, no. 4, pp. 3421–3430, Jul./Aug. 2019.

[10] C. N. M. Ajmal, I. V. Raghavendra, S. Naik, A. Ray, and H. S. Krishnamoorthy, "A modified hybrid DC circuit breaker with reduced arc for low voltage DC grids," *IEEE Access*, vol. 9, pp. 132267–132277, 2021.

[11] K. T. Compton, "The electric arc," *Trans. Amer. Inst. Elect. Engineers*, vol. 46, pp. 868–883, 1927.

[12] What Causes Arc Flash? Electrical Arc Blast Explained | Fluke.

[13] X. Zhou, and B. Ding, and J. V. R. Heberlein, "Temperature measurement and metallurgical study of cathodes in DC arcs," *IEEE Trans. Compon., Packag., Manuf. Technol., Part A*, vol. 19, no. 3, pp. 320–328, Sep. 1996.

[14] C. N. M. Ajmal, R. I. Venkata, and B. S. Naik, "Enhancement of DC MCB performance using power semiconductor devices," in *Proc. Annu. Conf. IEEE Ind. Electron. Soc.*, Oct. 2021, pp. 1–5.

[15] R. Rodrigues, Y. Du, A. Antoniazzi, and P. Cairoli, "A review of solid-state circuit breakers," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 364–377, Jan. 2021.

[16] F. Agostini et al., "1MW bi-directional DC solid state circuit breaker based on air cooled reverse blocking-IGCT," in *Proc. IEEE Elect. Ship Technol. Symp.*, Jun. 2015, pp. 287–292.

[17] P. Cairoli, L. Qi, C. Tschida, V. R. V. Ramanan, L. Raciti, and A. Antoniazzi, "High current solid state circuit breaker for DC shipboard power systems," in *Proc. IEEE Elect. Ship Technol. Symp.*, Aug. 2019, pp. 468–476.

[18] L. Qi et al., "Solid-state circuit breaker protection for DC shipboard power systems: Breaker design, protection scheme, validation testing," *IEEE Trans. J. Emerg. Sel. Topics Power Electron.*, vol. 56, no. 2, pp. 952–960, Mar./Apr. 2020.

[19] Astrolkwx, Solid-state DC breakers, [Online]. Available: https://astrolkwx.com/solid-state-dc-breakers/

[20] ABB, SACE Infinitus, [Online]. Available: https://search.abb.com/library/Download.aspx?DocumentID=1SDC230001D0201&LanguageCode=en&DocumentPartId=&Action=Launch

[21] DC Systems, Current Router, 2022. [Online]. Available: https://www.dc.systems/assets/public/Datasheet-Current-Router.pdf

[22] Y. Zhou, R. Na, Y. Feng, and Z. J. Shen, "GaN-based tri-mode intelligent solid-state circuit breakers for low-voltage DC power networks," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6596–6607, Jun. 2021.

[23] Y. Sato, Y. Tanaka, A. Fukui, M. Yamasaki, and H. Ohashi, "SiC-SIT circuit breakers with controllable interruption voltage for 400-V DC distribution systems," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2597–2605, May 2014.

[24] D. Marroquí, J. M. Blanes, A. Garrigós, and R. Gutierrez, "Self-powered 380 V DC SiC solid-state circuit breaker and fault current limiter," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9600–9608, Oct. 2019.

[25] Z. Miao, G. Sabui, A. M. Roshandeh, and Z. J. Shen, "Design and analysis of DC solid-state circuit breakers using SiC JFETs," *IEEE Trans. J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 863–873, Sep. 2016.

[26] P. Wolfgang, "AN 2012-04 – Cooling of thinPAK 8x8," Apr. 2012.

[27] Infineon, BSC027N10NS5 datasheet, 2020. [Online]. Available: https://www.infineon.com/dgdl/Infineon-BSC027N10NS5-DataSheet-v02_01-EN.pdf?fileId=5546d462689a790c0168c7cb36906441

[28] *Electrical Accessories - Circuit-Breakers for Overcurrent Protection for Household and Similar Installations - Part 3: Circuit-Breakers for DC Operation*, IEC 60898-3:2019, 2019.

[29] X. Perpina et al., "Analysis of clamped inductive turnoff failure in railway traction IGBT power modules under overload conditions," *IEEE Trans. Ind. Electonics*, vol. 58, no. 7, pp. 2706–2714, Jul. 2011.

[30] C.-H. Yang et al., "A high efficiency 750 V/100 A cryogenically cooled solid state circuit breaker module for aviation applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, Oct./Nov. 2023, pp. 1745–1751.

[31] CA908024E_Trip_curve_2021, 2021. [Online]. Available: https://www.tekdok.dk/files/CA908024E_Trip_curve_2021.pdf