A Cost-Effective Simultaneous Wireless Power and Data Transfer System With High-Rate Half-Duplex Communication

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***Abstract*—In simultaneous wireless power and data transfer (SWPDT) systems, which adopt coupling coils with taps, the selection of the tap position to obtain good performance of communication is a major problem. To solve the problem, this article proposes a novel SWPDT system based on tapped coils with ferrite cores. The proposed system is cost-effective while achieving high-rate half-duplex communication and improving power transfer efficiency (PTE). In the proposed system, additional wave trappers and coupling coils are not needed, reducing the costs and size of the system. A double-sided *LLCC* compensation topology is employed to filter most of the high-order harmonics generated by the H-bridge inverter and rectifier, while suppressing common-mode (CM) current. Zero-voltage (ZVS) switching is considered in the compensation design to suppress electromagnetic interference. Amplitude-shift keying (ASK) technology, which is low-cost and easy to implement, is used for modulation. In addition, this article presents a comprehensive parameter design method by analyzing the data transmission gain and power interference. Finally, an experimental prototype was constructed to validate the proposed system. The prototype successfully achieved an output power of 545 W with a maximum PTE of 95.55% and a maximum data rate of 1.25 Mb/s.**

***Index Terms*—Amplitude-shift keying (ASK), half-duplex communication, interference suppression, simultaneous wireless power and data transfer (SWPDT), wireless power transfer (WPT), zero-voltage switching (ZVS).**

NOMENCLATURE

U_{in}	DC voltage source.
R_L and R_{eq}	Resistive load and equivalent ac input impedance of rectifier.
C_{fi} and C_{fo}	Filter capacitors at the input and output terminals.
Q_1-Q_4	MOSFET transistors in the full-bridge inverter.
D_1-D_4	Diodes in the full-bridge rectifier.
L_p and L_s	Primary and secondary inductors.
M	Mutual inductance between primary and secondary inductors.
L_{f11}, L_{f12} L_{f21}, and L_{f22}	Compensation inductors.
L_{f1} and L_{f2}	Equivalent compensation inductors.
C_{f1} and C_{f2}	Parallel compensation capacitors.
C_p and C_s	Series compensation capacitors.
U_{TXp} and U_{TXs}	Data signals transmitted from the primary and secondary sides.
U_{RXp} and U_{RXs}	Data signals received at the primary and secondary sides.
R_{dp} and R_{ds}	Sampling resistors at the primary and secondary sides.
C_{dp} and C_{ds}	Coupling capacitor of the data channel on the primary and secondary sides.
f_p and ω_p	Frequency and angular frequency of power carrier.
A_m, f_d, and ω_d	Amplitude, frequency, and angular frequency of high-frequency carrier.
$R_{p\text{-}in}$ and $R_{p\text{-}out}$	Inner and outer diameters of the primary coil.
$R_{s\text{-}in}$ and $R_{s\text{-}out}$	Inner and outer diameters of the secondary coil.
D_{ps}	Nominal gap between coaxial coils.
N_{w1} and N_{w3}	Number of turns in the outer windings of primary and secondary coils.
N_{w2} and N_{w4}	Number of turns in the inner windings of primary and secondary coils.
T_p and T_s	Primary and secondary coil taps.
L_{w1} and L_{w2}	Self-inductances of the outer and inner windings at the transmitter side.
L_{w3} and L_{w4}	Self-inductances of the outer and inner windings at the receiver side.
M_{pq}	Mutual inductances between various winding combinations.
T_{dp} *and* T_{ds}	Isolation transformers.

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L_{dp}, L_{ds}	Coil inductance of isolation transformers.
u_{AB}, U_{AB}, and U_{ab}	Output voltage of inverter, root mean square value of the fundamental harmonic of u_{AB}, and input voltage of rectifier.
I_{AB}, I_{ab}, I_{Lp}, and I_{Ls}	Output current of inverter, input current of rectifier, current flowing through L_p, and current flowing through L_s.
$U_{AB,\max}$, I_{OFF}, C_{oss}, and t_{dead}	Maximum input voltage of the inverter, turn-OFF current, junction capacitance, and dead-time.
R_{Lpi} and R_{Lsi}	ESR of each turn of coil in primary and secondary sides.
L_{pi} and L_{si}	Inductance of each turn of coil in primary and secondary sides.
$M_{pi,j}$ and $M_{si,j}$	Mutual inductance between any two turns of coil in primary and secondary sides.
$C_{pi,j}$ and $C_{si,j}$	Parasitic capacitance between turns of coil in primary and secondary sides.
$R_{pi,j}$ and $R_{si,j}$	ESR between turns of coil in primary and secondary sides.
U_{pi} and U_{si}	Node voltage of each turn of coil in primary and secondary sides.
I_{pi} and I_{si}	Current flowing through each turn of the coil in primary and secondary sides.
M_{pgsh}	Mutual inductance between any turn of the primary coil and any turn of the secondary coil.
$I_{\mathrm{pin}x}$ and $I_{\mathrm{sin}x}$	Current flowing through C_{dp} and C_{ds} at the *x*th node.
M_{turn}	Mutual inductance between any two turns.
C_{tt}	Turn-to-turn capacitance.
$\boldsymbol{T}_{N1}$, $\boldsymbol{T}_{N2}$, and $\boldsymbol{T}_{N3}$	Transmission parameter matrix of network N_1, N_2, and N_3.
$\boldsymbol{A}$, $\boldsymbol{B}$, $\boldsymbol{Y}_{\mathrm{C}1}$, $\boldsymbol{Y}_{\mathrm{C}2}$, $\boldsymbol{Z}_p$, $\boldsymbol{Z}_s$, $\boldsymbol{M}_{ps}$, $\boldsymbol{M}_p$, $\boldsymbol{M}_s$	*n*x*n* matrix.
$\boldsymbol{U}_p$, $\boldsymbol{U}_s$, $\boldsymbol{I}_p$, $\boldsymbol{I}_s$, $\boldsymbol{I}_{in,p}$, $\boldsymbol{I}_{in,s}$	*n*x1 matrix.
I_{TXp} and I_{RXs}	Current generated by data signal source and current flowing through sampling resistor at the receiving end.
L_w and M_{ww}	Inductance of wingding and mutual inductance between any two wingdings.

I. INTRODUCTION

WIRELESS power transfer (WPT) technology has attracted significant attention due to its flexibility, security, and high efficiency [1], [2], [3], [4]. Its applications span various fields, including mobile phones, robotics, electric vehicles, and medical equipment [5], [6], [7], [8]. Practical WPT systems require real-time communication between the primary and secondary sides to maintain stability and reliability. While traditional technologies, such as bluetooth, radio frequency (RF), ZigBee, and Wi-Fi, can facilitate the communication, they often introduce significant transmission delays [9], increase system size and cost [10], and even are susceptible to interference from wireless power transmission [11], [12]. To address these challenges, researchers have proposed integrating the simultaneous wireless power and data transfer (SWPDT) technique into WPT systems.

To achieve SWPDT, an additional pair of coils for simultaneous data transmission is introduced while retaining the original coupling coils [13], [14], [15]. This approach is conducive to achieving a larger data rate and higher power transfer efficiency (PTE). Nevertheless, the size of the system will be increased because of the auxiliary coupler, constraining the deployment of this sort of system in space-constrained applications. To address this limitation, SWPDT systems that achieve synchronous transmission of power and data with the same pair of coupling coils have been proposed. These SWPDT systems can be divided into two types based on their data transmission mechanisms. The first type transmits data by directly modulating the power carrier [16], [17], [18], whereas the second type transmits data by modulating the high-frequency data carrier that is injected at one side [19], [20], [21], [22]. In detail, direct modulation of the power carrier refers to altering the phase, amplitude or frequency of the power carrier. However, this easy-to-implement method will limit data rates due to the low-frequency power carrier and cause output power fluctuations [23], [24]. Therefore, it is not suitable for high-power and high-data-rate SWPDT systems. The second type can help avoid the above limitations [9], [10], [11], [12], [19], [20], [21], [22]. With data carrier frequency in the megahertz range and power carrier frequency typically in tens of kilohertz range, interference between carriers can be minimized, resulting in high data rates without power fluctuations. Among various modulation techniques, amplitude-shift keying (ASK) and frequency-shift keying (FSK) are both common modulation techniques. Compared with FSK modulation, ASK modulation has lower design complexity and is easier for implementation. Furthermore, ASK modulation maintains a constant data carrier frequency, ensuring the data transfer system remains at its resonant frequency. These advantages led to the adoption of ASK modulation in SWPDT systems with high-frequency data carriers [12], [20], [25], [26].

SWPDT systems utilizing a shared inductive link with high-frequency data carriers have gained significant attention due to its advantages of low cost, compact size, high data rates and stable power transmission. In [12], parallel transmission of power and data are proposed. Wave trappers are added into the system, ensuring that data transmission does not interfere with power transmission. However, this design affects the system's PTE. In addition, the tightly coupled coils limit practical application scenarios. In [19], double-sided *LCCL* compensation and loosely coupled transformers (LCT) of receivers are utilized to prevent power interference with data transmission. However, this design makes the system bulky. In [21], a SWPDT system that achieves high output power and bidirectional communication with four resonance dual-rejection structure is proposed. However, it employs numerous wave trappers in the transfer channels that potentially compromise PTE. In [12], [19], and [21], the circuits for data carrier injection and extraction are directly parallel to the shared coupling coils. Wave trappers or additional trap inductors need to be added to the power channels to mitigate the interference between power and data transmission. These additional passive components not only increase the system's complexity, size and cost but also easily cause significant power loss in power transmission. To overcome this problem, [20], [25], [27], [28] use partial coupled coils as a medium for data transmission. In [20], an effective data injection solution is proposed. It injects the data carrier through taps on the coupling coils. In detail, the coil is divided into two parts with taps, one for data transmission and the other functioning as an equivalent trap inductor. Therefore, tapping coils not only conserve space but also avoids PTE degradation. However, the accuracy of the analysis needs to be improved because the skin effect and proximity effect of the tightly wound coils are ignored. Furthermore, the applicability is poor since there are no magnetic cores. Wei et al. [25] injected the data carrier into one of the D coils. Additional wave trappers are not required; thus, high PTE can be achieved. However, it has limited applicability due to the specialized coil structure. Furthermore, it only implements forward data transmission and only reaches an output power of 150 W. In [27], a SWPDT system with a hybrid injection communication method utilizing part of the receiving end (Rx) coil, transmitting end (Tx) coil, and an additional transformer for data transmission is proposed. The PTE can reach 92.25% under a coupling coefficient of 0.11. However, only backward data transmission is implemented. In all the above research on SWPDT, the power interference generated by the inverter is unavoidable, which may lead to spike voltage on the data channel. Fan et al. [26] effectively filtered the high-order harmonics of the power using *LCLC* compensation topology. However, the tightly coupled coils limit practical application scenarios, and the performance of the system with an output power above 300 W needs further research. Wang et al. [28] effectively suppressed the common-mode (CM) interference generated by the inverter utilizing double-sided *LLCC* compensation. In addition, it considers parasitic parameters when analyzing the gain of the data transmission channel. However, similar to [25] and [27], the impact of tap positions on signal-to-noise ratio (SNR) was not studied. Based on the above literature, there is currently a lack of research on the selection of tap positions in a SWPDT system based on tapped coils with ferrite cores, considering high frequency effects.

To address the aforementioned challenges, this article proposes a novel SWPDT system that utilizes tapped coils without the need for additional wave trappers. Double-sided *LLCC* compensation is applied, thus the high-order harmonics as well as the CM interference from the inverter can be effectively suppressed. A simplified high-frequency distributed parameter model is used to analyze the transfer characteristics for the data channel. A comprehensive parameter design method is given after analyzing the data transmission gain and power interference. A prototype that operates at 545 W transmission power with 95.55% efficiency and a maximum data rate of 1.25 Mb/s verifies the effectiveness of the proposed parameter design method. Furthermore, the robustness of the proposed system under varying load or coupling conditions is validated.

Hence, the main contributions of this work are as follows.

1) Development of an SWPDT system based on tapped coils
2) Establishment and simplification of a high-frequency distributed-parameter model for data channel characteristics with derivation of comprehensive SNR expressions;
3) Proposal of a novel tap-positioning method for SWPDT system with ferrite cores accounting for parasitic parameters.
4) Experimental validation of an SWPDT system based on tapped coils with ferrite cores under varying load/coupling conditions.

The rest of this article is organized as follows. Section II presents an overview of the system. Section III introduces the equivalent circuit of the power channel. Section IV analyzes the data channel based on high-frequency distributed parameter model. Section V discusses the interference between power and data transmission. Section VI gives the design method of the power and data transfer channel. Section VII provides experimental validation of the theoretical analysis and compares it with other studies. Finally, Section VIII concludes this article.

II. OVERVIEW OF THE PROPOSED SWPDT SYSTEM

The system proposed in this article consists of the power channel and data channel, as illustrated in Fig. 1. The power channel employs a double-sided *LLCC* compensation topology, which can offer constant current output. Moreover, the compensation inductors L_{f11}, $L_{f12,}$ L_{f21}, and L_{f22} can effectively filter out higher order harmonics generated by the H-bridge inverter and rectifier and mitigate CM electromagnetic interference (EMI) generated by the switching [28]. Consequently, it effectively suppresses interference between power and data channels.

The power channel comprises several key components. U_{in} serves as the dc voltage source, while R_L represents the resistive load. Filter capacitors C_{fi} and C_{fo} are positioned at the input and output terminals, respectively. The full-bridge inverter is composed of four MOSFET transistors, Q_1–Q_4, while the diodes D_1–D_4 form the full-bridge rectifier on the secondary side. The loosely coupled transformer includes primary and secondary inductors (L_p and L_s), with M representing their mutual inductance. Other components include parallel compensation capacitors (C$_{f1}$ and C_{f2}), and series compensation capacitors (C$_p$ and C$_s$) on both primary and secondary sides, respectively.

The communication channel of the system shares a pair of coupling coils with the power channel. The coupling coils are divided into two sections, with high-frequency carrier signals injected through taps on the coils. This design eliminates the need for separate communication coils, reducing system complexity and size. U_{TXp} and U_{TXs} represent the data signal transmitted from the primary and secondary sides, respectively. U_{RXp} and U_{RXs} are the data signal received at the primary and secondary sides, respectively. R_{dp} and R_{ds} are the sampling resistors at the primary and secondary sides, while C_{dp} and C_{ds} are the coupling capacitors of the data channel on the primary and secondary sides. T_{dp} and T_{ds} are isolation transformers for data carrier injections. The data channel is connected to the system via taps of the coils. The power carrier frequency f_p is set to 85 kHz, and the data carrier frequency f_d is set to 27.7 MHz.

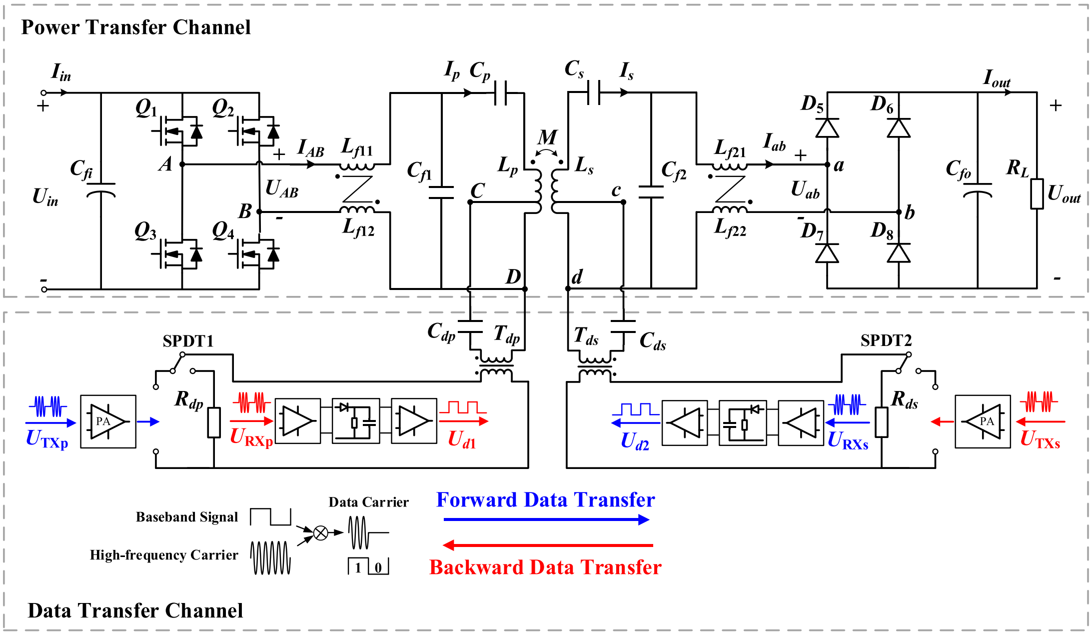
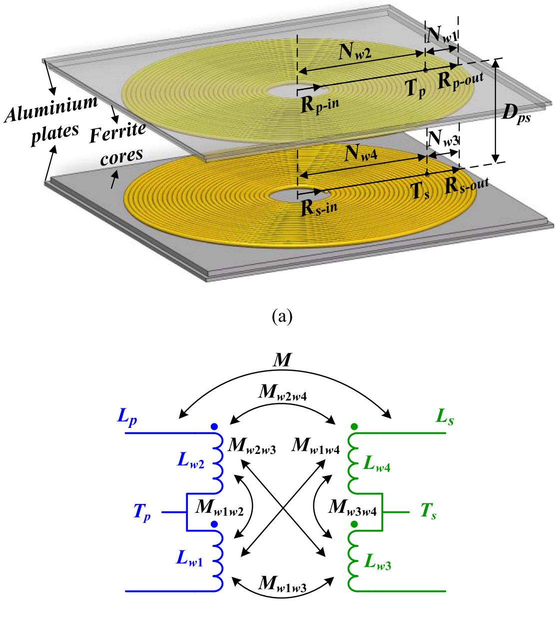


Fig. 1. Topology of the proposed SWPDT system with high-rate half-duplex communication.



(a)

(b)

Fig. 2. Planar circular coils with taps and ferrite core. (a) Geometry view of the coils. (b) Equivalent model of the coils.

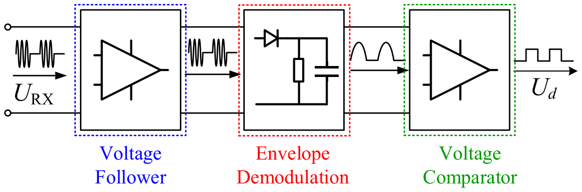


Fig. 3. Signal demodulation circuit.

sides, as illustrated in Fig. 2(a). The coupling coils are wound by Litz wire with a diameter of 4 mm. $R_{p\text{-in}}$ and $R_{p\text{-out}}$ represent the inner and outer diameters of the primary coil. $R_{s\text{-in}}$ and $R_{s\text{-out}}$ represent the inner and outer diameters of the secondary coil. D_{ps} is the nominal gap between coaxial coils. N_{w1} and N_{w3} denote the number of turns in the outer windings of primary and secondary coils, respectively. N_{w2} and N_{w4} represent the number of turns in the inner windings of primary and secondary coils, respectively. T_p and T_s are the primary and secondary coil tap, respectively. Fig. 2(b) illustrates an equivalent model of coupling coils with taps. L_{w1} and L_{w2} correspond to the self-inductances of the outer and inner windings at the transmitter side, respectively, while L_{w3} and L_{w4} correspond to the self-inductances of the outer and inner windings at the receiver side.

M_{pq} $(p = w1, w2, w3, w4, q = w1, w2, w3, w4, p \neq q)$ denotes the mutual inductances between various winding combinations. For data transmission, the proposed system employs ASK modulation, which can be expressed as [21]

$$f(t) = \begin{cases} 0 & \text{bit} = 0 \\ A_m \sin(\omega_d t) & \text{bit} = 1 \end{cases} \tag{1}$$

where A_m and ω_d represent the amplitude and angular frequency of the high-frequency carrier, respectively. In this configuration, the absence of a carrier signal represents a "0," while a sinusoidal wave indicates a "1." Then, the signal demodulation process is facilitated by the circuit shown in Fig. 3, which consists of a voltage-following module, an envelope extraction module, and a voltage comparator. In detail, the demodulation process begins with voltage following, proceeds through envelope extraction, and recovers the baseband signal via comparison. Table I gives the values of the main parameters utilized in the following theoretical analysis.

TABLE I
MAIN PARAMETERS UTILIZED IN ANALYSIS

Symbol	Value	Symbol	Value
L_p, L_s	286 μH	$R_{p\text{-}in}$, $R_{s\text{-}in}$	0.02 m
C_p, C_s	17.71 nF, 20.15 nF	$R_{p\text{-}out}$, $R_{s\text{-}out}$	0.14 m
C_{f1}, C_{f2}	39.84 nF	N_{w1}, N_{w3}	7 turns
L_{f1}, L_{f2}	88 μH	N_{w2}, N_{w4}	23 turns
C_{fi}, C_{fo}	1000 μF	L_{w1}, L_{w3}	40.9 μH
C_{dp}, C_{ds}	560 pF	L_{w2}, L_{w4}	161.7 μH
f_p	85 kHz	M_{w1w2}, M_{w3w4}	41.2 μH
f_d	27.7 MHz	M_{w1w3}	7.2 μH
k	0.26	M_{w2w4}	41 μH
R_L	60.5 Ω	M_{w1w4}, M_{w2w3}	17.5 μH
D_{ps}	10 cm	R_{dp}, R_{ds}	50 Ω
U_{in}	181 V	L_{dp}, L_{ds}	4 μH

III. ANALYSIS OF POWER CHANNEL OF THE PROPOSED SWPDT SYSTEM

A. Characteristics of Power Channel

In the subsequent analysis, a frequency-domain equivalent circuit is adopted and only the fundamental component is considered here for simplicity based on fundamental harmonic analysis. The fundamental component approximation is sufficiently accurate for a high-quality factor resonant circuit that works near resonance, where the tank–inductor–current and tank–capacitor–voltage waveforms are mostly sinusoidal [29].

The dc power supply U_{in} is converted into a square wave u_{AB} through the full-bridge inverter. U_{AB} represents the root mean square value of the fundamental harmonic of u_{AB} and can be expressed as

$$U_{AB} = \frac{2\sqrt{2}U_{\text{in}}}{\pi}. \tag{2}$$

The equivalent ac input impedance of the rectifier R_{eq} can be expressed as

$$R_{\text{eq}} = \frac{8R_L}{\pi^2}. \tag{3}$$

Here, $Z_{\text{CD-TX}}$ represents the impedance of the primary data transmitter at the CD port and $Z_{\text{cd-RX}}$ represents the impedance of the secondary data receiver at the CD port, which are derived as follows:

$$Z_{\text{CD}-\text{TX}} = \frac{1}{j\omega C_{dp}} + \frac{j\omega L_{dp}R_{dp}}{R_{dp} + j\omega L_{dp}} \tag{4}$$

$$Z_{\text{cd}-\text{RX}} = \frac{1}{j\omega C_{ds}} + \frac{j\omega L_{ds}R_{ds}}{R_{ds} + j\omega L_{ds}} \tag{5}$$

where ω refers to signal angular frequency, and L_{dp} (L_{ds}) refers to the coil inductance when T_{dp} (T_{ds}) is regarded as an ideal transformer. Given that $\omega = \omega_p = 2\pi f_p$, the impedances $Z_{\text{CD-TX}}$ and $Z_{\text{cd-RX}}$ are high enough to ignore their impact on the power transfer channel due to the substantial difference between the power carrier frequency and the data carrier frequency [19]. Hence, for the analytical simplicity, we can omit the data channel entirely and focus on a simplified model of the power transfer channel, as depicted in Fig. 4. In this simplified model, Z_s represents the equivalent impedance of the circuit at the right side of L_s, which can be formed as

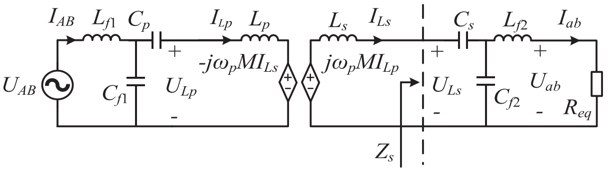


Fig. 4. Simplified equivalent model of power transfer channel with mutual inductances between two inductors L_p and L_s.

$$Z_s = \frac{1}{j\omega_p C_s} + \frac{(R_{\text{eq}} + j\omega_p L_{f2})}{1 + j\omega_p C_{f2}(R_{\text{eq}} + j\omega_p L_{f2})}. \tag{6}$$

Compensation inductors L_{f11} (L_{f21}) and L_{f12} (L_{f22}) form the equivalent compensation inductor L_{f1} (L_{f2}). L_{f1} can be expressed as

$$L_{f1} = L_{f11} + L_{f12} + k_{f1}\sqrt{L_{f11}L_{f12}} \tag{7}$$

where k_{f1} is the coupling coefficient of L_{f11} and L_{f12}

L_{f2} can be expressed as

$$L_{f2} = L_{f21} + L_{f22} + k_{f2}\sqrt{L_{f21}L_{f22}} \tag{8}$$

where k_{f2} is the coupling coefficient of L_{f21} and L_{f22}. To simplify the analysis, the value of L_{f11} (L_{f21}) is consistent with the value of L_{f12} (L_{f22}). Since L_{f11} (L_{f21}) and L_{f12} (L_{f22}) are wound on the same core, k_{f1} (k_{f2}) is greater than 0.9 [28].

Here, L_p, L_s, and M are expressed by the following equations:

$$\begin{cases} L_p = L_{w1} + L_{w2} + 2M_{w1w2} \\ L_s = L_{w3} + L_{w4} + 2M_{w3w4} \\ M = M_{w1w3} + M_{w1w4} + M_{w2w3} + M_{w2w4}. \end{cases} \tag{9}$$

The compensation parameters of the double-side *LCC* topology are tuned by the following equations:

$$\begin{cases} \omega_p L_p - \frac{1}{\omega_p C_p} = \omega_p L_{f1} = \frac{1}{\omega_p C_{f1}} \\ \omega_p L_s - \frac{1}{\omega_p C_s} = \omega_p L_{f2} = \frac{1}{\omega_p C_{f2}}. \end{cases} \tag{10}$$

The currents generated by U_{AB} and U_{ab} and the input power of the inverter can be expressed as follows [33]:

$$\begin{cases} \dot{I}_{AB} = \frac{M\dot{U}_{ab}}{\omega_p L_{f1} L_{f2}} \\ \dot{I}_{ab} = \frac{M\dot{U}_{AB}}{j\omega_p L_{f1} L_{f2}} \\ \dot{I}_{Lp} = \frac{\dot{U}_{AB}}{j\omega_p L_{f1}} \\ \dot{I}_{Ls} = \frac{j\dot{U}_{ab}}{\omega_p L_{f2}} \\ \dot{U}_{ab} = \dot{I}_{ab} R_{\text{eq}}. \end{cases} \tag{11}$$

B. Consideration of Zero-Voltage Switching (ZVS)

To eliminate switching losses and severe EMI, it is significant to implement ZVS during the MOSFET turn-ON [30]. To achieve

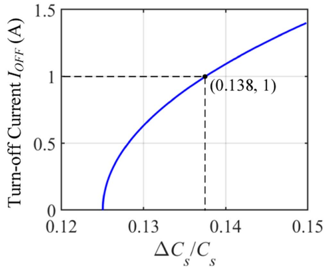


Fig. 5. Relationship between turn-OFF current I_{OFF} and $\Delta C_s/C_s$.

TABLE II
PARAMETERS OF THE COMPENSATION NETWORK

Symbol	Design Value
L_{f1}	88 μH
L_{f2}	88 μH
C_{f1}	39.84 nF
C_{f2}	39.84 nF
C_p	17.71 nF
C_s	20.15 nF

ZVS, a negative current must flow through the MOSFET's body diode prior to turn-ON. It means ensuring a positive turn-OFF current for one MOSFET to facilitate zero-voltage turn-ON of its complementary MOSFET in the same bridge arm. This condition necessitates an inductive input impedance for the resonant network. Furthermore, ZVS operation requires the turn-OFF current to be large to discharge the junction capacitors within the dead-time, which can be represented as [31]

$$I_{\mathrm{OFF}} > \frac{2C_{\mathrm{oss}}U_{AB,\max}}{t_{\mathrm{dead}}} \tag{12}$$

where C_{oss} represents the MOSFET junction capacitance, $U_{AB,\max}$ represents the maximum output voltage of the inverter, and t_{dead} represents the dead-time. For this study, the SCT3120AL N-channel SiC MOSFET was selected as the inverter switch. Given the specific parameters of this MOSFET, calculations indicate that the turn-off current must be at least 1 A to successfully achieve ZVS. In this article, ZVS is achieved by slightly increasing the series capacitor C_s on the secondary side [32]. Initially, the system parameters were designed based on (8). The inductors L_{f1} and L_{f2} that serve as reactive power compensators are typically designed to be significantly smaller than the main coils [33]. After determining the preliminary compensation parameters, simulation results yielded a curve illustrating the relationship between the relative change in ΔC_s /C_s and turn-OFF current, as depicted in Fig. 5. This analysis reveals that the turn-OFF current increases proportionally with ΔC_{s}. Notably, the turn-OFF current exceeds the required 1 A threshold when $\Delta C_{\mathrm{s}}/C_{\mathrm{s}}$ surpasses 0.13. Based on these findings, the values designed for the compensation network were determined and are presented in Table II.

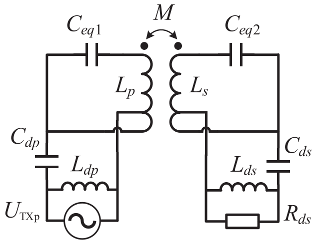


Fig. 6. Simplified equivalent circuit of data transfer channel.

IV. PARAMETER DESIGN AND COMMUNICATION-FREE CONTROL STRATEGY

A. Characteristics of Data Channel

The impedance of L_{f1}, L_{f2}, C_{f1}, and C_{f2}, as well as the ratio Q_1 and Q_2, can be expressed as

$$\begin{cases} Z_{Lf1} = j\omega_d L_{f1}, & Z_{Lf2} = j\omega_d L_{f2} \\ Z_{Cf1} = \frac{1}{j\omega_d C_{f1}}, & Z_{Cf2} = \frac{1}{j\omega_d C_{f2}} \\ Q_1 = \frac{Z_{Lf1}}{Z_{Cf1}}, & Q_2 = \frac{Z_{Lf2}}{Z_{Cf2}} \end{cases} \tag{13}$$

where $\omega_d = 2\pi f_d$.

By substituting the parameters from Table I into (13), the following results can be obtained:

$$\begin{cases} |Q_1| > 4100 \\ |Q_2| > 4100. \end{cases} \tag{14}$$

Therefore, the compensation inductance branch on both the primary and secondary sides can be considered as an open circuit. C_p and C_{f1}, as well as C_s and C_{f2} are in series. C_{eq1} and C_{eq2} are introduced as the equivalent capacitances, expressed as

$$\begin{cases} C_{eq1} = \frac{C_{f1}C_p}{C_{f1}+C_p} \\ C_{eq2} = \frac{C_{f2}C_s}{C_{f2}+C_s}. \end{cases} \tag{15}$$

Then, the symmetry of the data transfer channel allows for simplification of the analysis by using forward data transmission as a representative example. The simplified equivalent circuit of data transfer channel is given in Fig. 6. It is significant to note that inductors and transformers behave differently at high frequencies compared to low frequencies. In high-frequency operation, tightly wound coils introduce parasitic parameters due to skin effect and proximity effect. The parasitic capacitances of the winding cannot be neglected [34]. Hence, the conventional lumped-parameter circuit model loses accurate [28], and the distributed parameters of the coils need to be considered.

To address these high-frequency effects and provide a more accurate analysis of the data channel's transfer characteristics, this study employs a high-frequency distributed-parameter coupling coil model, as depicted in Fig. 7. The circuit model consists of coil self-inductances, coil mutual inductances, turn-to-turn capacitances and equivalent series resistances (ESRs). R_{Lpi} and L_{pi} are ESR and inductance of each turn of the primary coil. R_{Lsi} and L_{si} are ESR and inductance of each turn of the secondary coil. $M_{pi,j}$ is the mutual inductance between any two turns of the primary coil. $M_{si,j}$ is the mutual inductance between any two turns of the secondary coil. $C_{pi,j}$ and $R_{pi,j}$ are the parasitic capacitance and its ESR between turns of the primary coil. $C_{si,j}$

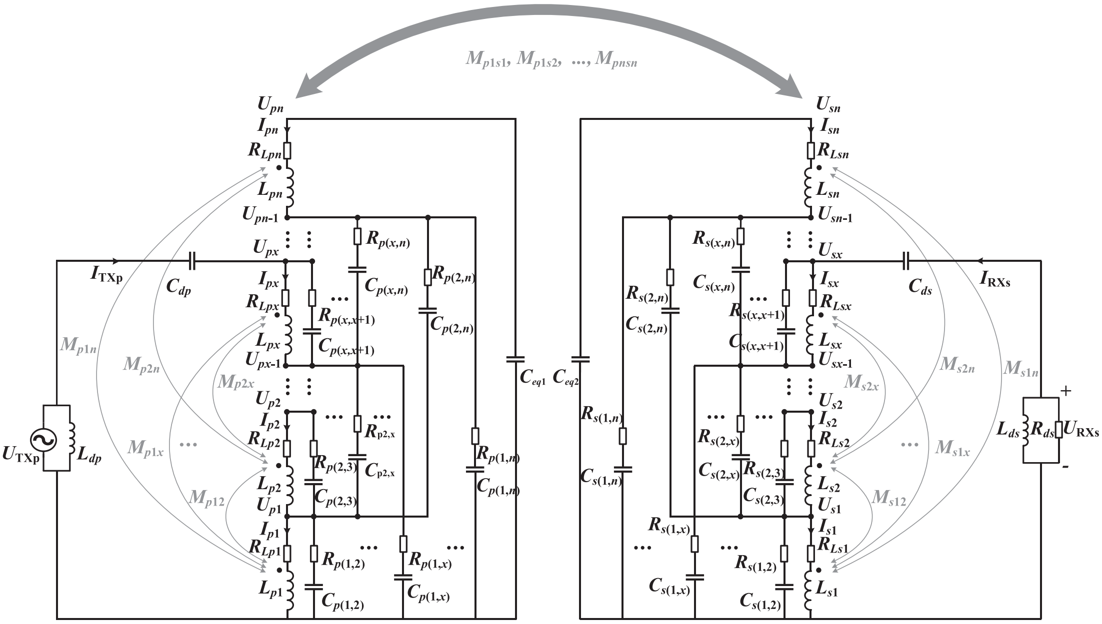


Fig. 7. High-frequency distributed-parameter coupling coil model of data transfer channel.

and $R_{si,j}$ are the parasitic capacitance and its ESR between turns of the secondary coil. U_{pi} and U_{si} represent the node voltage of each turn of the primary and secondary coils, while I_{pi} and I_{si} represent the current flowing through each turn of the primary and secondary coils. Here, $i = 1, 2, \ldots, n$, $j = 1, 2, \ldots, n$, $i \neq j$. n refers the number of turns. M_{pgsh} ($g = 1, 2, \ldots, n$, $h = 1, 2, \ldots, n$) represents the mutual inductance between any turn of the primary coil and any turn of the secondary coil. I_{pinx} and I_{sinx} represent the current flowing through C_{dp} and C_{ds} at the xth node, respectively.

The ESR of per turn of the primary and secondary coil in air can be represented by the following formula [35]:

$$R_{Lpi} = R_{Lsi} = \frac{\pi \mu \omega^4 {r_l}^4}{6c^3} \tag{16}$$

where μ is the permeability of medium and r_l is the radius of the loop in meters. The self-inductance of per turn of circular coil with ferrite core can be calculated as

$$\begin{cases} {L_{pi}}' = {L_{si}}' = \mu a \left(\ln \frac{8r_l}{r_c} - 2\right) \\ L_{pi} = {L_{pi}}' + M_{Lpi'Lpi'1} + M_{Lpi'Lpi'2} + M_{Lpi'Lpi'3} \\ L_{si} = {L_{si}}' + M_{Lsi'Lsi'1} + M_{Lsi'Lsi'2} + M_{Lsi'Lsi'3} \end{cases} \tag{17}$$

where r_c is the cross-sectional radius of the loop. ${L_{pi}}^{'}({L_{si}}^{'})$ is the self-inductance of per turn of circular coil without ferrite [36]. L_{pi} (L_{si}) is the self-inductance of per turn of circular coil with ferrite core. $L_{pi\,'1}$, $L_{pi\,'2}$, and $L_{pi\,'3}$ are self-inductances after mirroring [37]. The mutual inductance between any two turns can be calculated as

$$\begin{cases} {M_{turn}}' = \frac{\mu_0}{(R_2 - R_1)(R_4 - R_3)} \int_0^{\pi} \int_{R_1}^{R_2} \int_{R_3}^{R_4} \\ \qquad \frac{\cos\theta d\theta r_1 dr_1 r_2 dr_2}{\sqrt{{z_Q}^2 + {r_1}^2 + {r_2}^2 - 2r_1 r_2 \cos\theta}} \\ M_{turn} = M_{Lsi'Lpj'1} + M_{Lsi'Lpj'2} \end{cases} \tag{18}$$

where μ_0 is the magnetic permeability of the vacuum. R_2 and R_4 represent the outer radii of the two turns, respectively. R_1 and R_3 represent the inner radii of the two turns, respectively.

z_Q is the axial distance between the two turns, ${M_{\text{turn}}}^{'}$ is the mutual inductance between any two turns without ferrite [38], and M_{turn} is the mutual inductance between any two turns with ferrite cores. $L_{pj\,'1}$ and $L_{pi\,'2}$ are self-inductances after mirroring [37].

The turn-to-turn capacitance can be calculated as [34]

$$C_{tt} = \varepsilon_0 l_t \frac{2\varepsilon_r \arctan\left[\frac{(-1+\sqrt{3})(2\varepsilon_r + \ln\frac{D_0}{D_c})}{(1+\sqrt{3})\sqrt{\ln\frac{D0}{Dc}(2\varepsilon r + \ln\frac{D0}{Dc})}}\right]}{\sqrt{2\varepsilon_r \ln\frac{D_0}{D_c} + (\ln\frac{D_0}{D_c})^2}} \tag{19}$$

where ε_0 and ε_r refer to the absolute permittivity in vacuum and the relative permittivity of the medium, respectively. l_t is the turn length. D_0 is the outer diameter of the wire, including the thickness of the insulation layer. D_c is the inner diameter of the wire. Ferrite core is non-conductive, so, we don't need to consider the parasitic capacitance between coil and core [39]. Only turn-to-turn parasitic capacitance is considered in this article.

B. Voltage Gain of Data Channel

This article uses the theory of two-port networks and transmission parameters to calculate the voltage gain of the data channel. The circuit shown in Fig. 7 is equivalent to a cascade of three two-port networks (N_1, N_2, and N_3), as illustrated in Fig. 8. $\boldsymbol{T}_{N1}$ and $\boldsymbol{T}_{N3}$ represent the transmission parameter (ABCD parameter) matrix of network N_1 and network N_3, respectively, which can be directly obtained from the circuit structure as

$$\boldsymbol{T}_{N1} = \begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix} = \begin{bmatrix} 1 & \frac{1}{sC_{dp}} \\ \frac{1}{sL_{dp}} & \frac{1+sC_{dp}}{s^2 C_{dp} L_{dp}} \end{bmatrix} \tag{20}$$

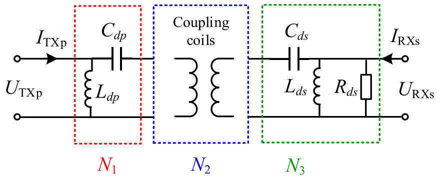


Fig. 8. Cascade of two-port networks N_1, N_2, and N_3.

$$\boldsymbol{T}_{N3} = \begin{bmatrix} A''' & B''' \\ C''' & D''' \end{bmatrix} = \begin{bmatrix} \frac{s^2 L_{ds} C_{ds} R_{ds} + s L_{ds} + R_{ds}}{s^2 L_{ds} C_{ds} R_{ds}} & \frac{1}{s C_{ds}} \\ \frac{s L_{ds} + R_{ds}}{s L_{ds} R_{ds}} & 1 \end{bmatrix} \tag{21}$$

where $s = j\omega_d$.

By applying the nodal analysis to the circuit shown in Fig. 7, the following equations can be obtained:

$$\begin{cases} \boldsymbol{Y}_{C1}\boldsymbol{U}_p + \boldsymbol{B}\boldsymbol{I}_p = \boldsymbol{I}_{in,p} \\ \boldsymbol{A}\boldsymbol{U}_p = \boldsymbol{Z}_p\boldsymbol{I}_p + s\boldsymbol{M}_p\boldsymbol{I}_p + s\boldsymbol{M}_{ps}\boldsymbol{I}_s \\ \boldsymbol{Y}_{C2}\boldsymbol{U}_s + \boldsymbol{B}\boldsymbol{I}_s = \boldsymbol{I}_{in,s} \\ \boldsymbol{A}\boldsymbol{U}_s = \boldsymbol{Z}_s\boldsymbol{I}_s + s\boldsymbol{M}_s\boldsymbol{I}_s + s\boldsymbol{M}_{ps}\boldsymbol{I}_p. \end{cases} \tag{22}$$

Matrices for the above equations are shown in the appendix. From (22) and (42)–(52), the impedance parameter (Z parameter) matrix of network N_2 can be written as

$$\boldsymbol{Z}_{N2} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \tag{23}$$

where Z_{11}, Z_{12}, Z_{21}, and Z_{22} can be calculated as (53), as shown in the appendix.

The ABCD parameters of N_2 can be converted from Z petameters, and then $\boldsymbol{T}_{N2}$ can be expressed as

$$\boldsymbol{T}_{N2} = \begin{bmatrix} A'' & B'' \\ C'' & D'' \end{bmatrix} = \begin{bmatrix} \frac{Z_{11}}{Z_{21}} & \frac{Z_{11}Z_{22} - Z_{12}Z_{21}}{Z_{21}} \\ \frac{1}{Z_{21}} & \frac{Z_{22}}{Z_{21}} \end{bmatrix}. \tag{24}$$

The ABCD parameter matrix of the two-port network shown in Fig. 8 can be calculated as

$$\boldsymbol{T}_N = \boldsymbol{T}_{N1}\boldsymbol{T}_{N2}\boldsymbol{T}_{N3}. \tag{25}$$

Here, U_{TXp}, I_{TXp}, U_{RXs}, and I_{RXs} can be obtained by (23) as

$$\begin{bmatrix} U_{TXp} \\ I_{TXp} \end{bmatrix} = \boldsymbol{T}_N \begin{bmatrix} U_{RXs} \\ -I_{RXs} \end{bmatrix} = \boldsymbol{T}_{N1}\boldsymbol{T}_{N2}\boldsymbol{T}_{N3} \begin{bmatrix} U_{RXs} \\ -I_{RXs} \end{bmatrix}. \tag{26}$$

From (23), the forward voltage gain of the data channel can be expressed as

$$G_{df} = \frac{U_{RXs}}{U_{TXp}} = \frac{1}{[\boldsymbol{T}_N]_{11}} = \frac{1}{[\boldsymbol{T}_{N1}\boldsymbol{T}_{N2}\boldsymbol{T}_{N3}]_{11}}. \tag{27}$$

According to the symmetry of the system, the backward gain G_{db} of the data channel is equal to the forward gain G_{df}, G_d is used to represent the data channel gain, which can be expressed as

$$G_{db} = G_{df} = G_d. \tag{28}$$

Research presented in [40] gives the distribution of parasitic capacitance between coil turns when operating planar disk coils at MHz frequencies. The results indicate that the parasitic capacitance between neighboring coils is significantly larger than other parasitic capacitances. In fact, the parasitic capacitance between nonadjacent turns is so small that it can be considered negligible for practical purposes. Based on these observations, our analysis focuses primarily on the parasitic capacitance between neighboring turns since this is the dominant factor affecting high-frequency behavior. Furthermore, to further enhance the simplicity of the analysis, we have chosen to disregard the ESR of the parasitic capacitances. Then, the high-frequency distributed-parameter coupling coil model of data transfer channel of the proposed SWPDT system is simplified as shown in Fig. 9.

V. ANALYSIS OF INTERFERENCE

According to the analysis in Section IV, the compensation inductance branch on both the primary and secondary sides can be neglected. Furthermore, given that the power level of the data carrier is much lower than that of the power carrier, we can reasonably ignore the effect of data transfer on the power channel in this system. However, the power signal will generate interference in the data channel. Therefore, it is necessary to evaluate the impact of the power signal on the data channel.

Based on kirchhoff's voltage law (KVL), the voltage of primary and secondary coils U_{Lp} and U_{Ls} in the simplified circuit shown in Fig. 4 can be derived as

$$\begin{cases} \dot{U}_{Lp} = j\omega_p L_p \dot{I}_{Lp} - j\omega_p M \dot{I}_{Ls} \\ \dot{U}_{Ls} = j\omega_p M \dot{I}_{Lp} - j\omega_p L_s \dot{I}_{Ls}. \end{cases} \tag{29}$$

By substituting (11) into (29), the following equations can be obtained:

$$\begin{cases} \dot{U}_{Lp} = \frac{\dot{U}_{AB}}{L_{f1}} \left(L_p - \frac{jM^2 R_{eq}}{\omega_p {L_{f2}}^2} \right) \\ \dot{U}_{Ls} = \frac{M\dot{U}_{AB}}{L_{f1}} \left(1 - \frac{jL_s R_{eq}}{\omega_p {L_{f2}}^2} \right). \end{cases} \tag{30}$$

From (30), the power interference transfer gain from the inverter output to the primary coil $G_{Lp\text{-}AB}$ and the power interference transfer gain from the inverter output to the secondary coil $G_{Ls\text{-}AB}$ can be obtained as

$$\begin{cases} G_{Lp-AB} = \frac{\dot{U}_{Lp}}{\dot{U}_{AB}} = \frac{1}{L_{f1}} \left(L_p - \frac{jM^2 R_{eq}}{\omega_p {L_{f2}}^2} \right) \\ G_{Ls-AB} = \frac{\dot{U}_{Ls}}{\dot{U}_{AB}} = \frac{M}{L_{f1}} \left(1 - \frac{jL_s R_{eq}}{\omega_p {L_{f2}}^2} \right). \end{cases} \tag{31}$$

As the taps divide a pair of coils into four inductors, the mutual inductance M between the primary and secondary coils can be considered as the sum of the mutual inductances among these four inductors. The simplified equivalent model of power transfer channel showing mutual inductance details is presented in Fig. 10. By applying KVL and (9), the following equations can be derived:

$$\begin{cases} \dot{U}_{Lp} = j\omega_p L_p \dot{I}_{Lp} - j\omega_p M \dot{I}_{Ls} \\ 0 = j\omega_p M \dot{I}_{Lp} - j\omega_p L_s \dot{I}_{Ls} - Z_s \dot{I}_s. \end{cases} \tag{32}$$

Then, I_{Lp} and I_{Ls} can be obtained as

$$\begin{cases} \dot{I}_{Lp} = \frac{j\omega_p L_s + Z_s}{-{\omega_p}^2 L_p L_s + j\omega_p L_p Z_s + {\omega_p}^2 M^2} \dot{U}_{Lp} \\ \dot{I}_{Ls} = \frac{j\omega_p M}{-{\omega_p}^2 L_p L_s + j\omega_p L_p Z_s + {\omega_p}^2 M^2} \dot{U}_{Lp}. \end{cases} \tag{33}$$

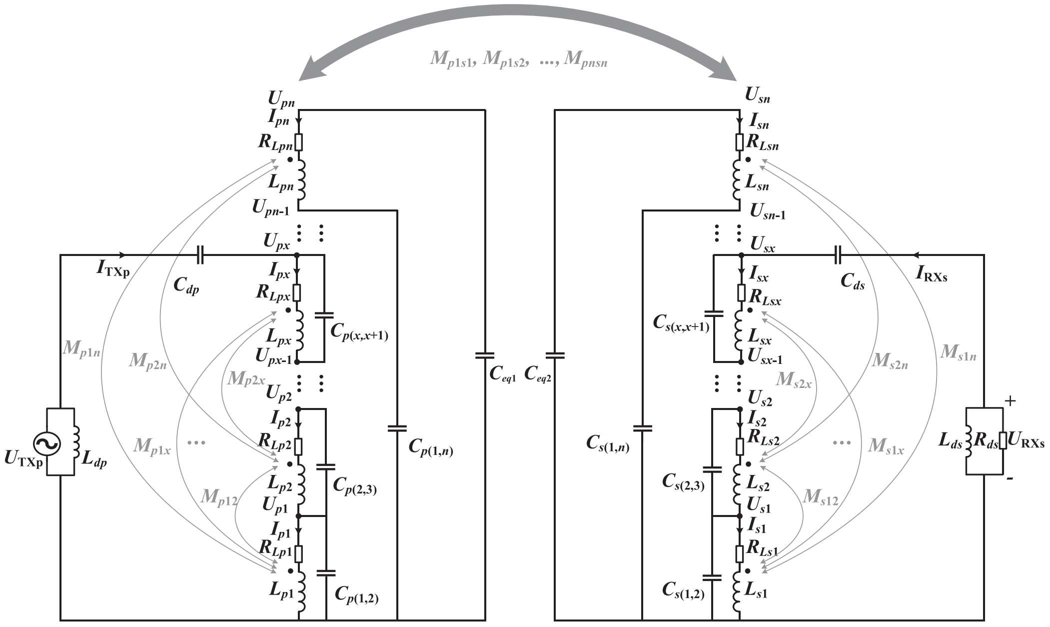


Fig. 9. Simplified high-frequency distributed-parameter coupling coil model of data transfer channel.

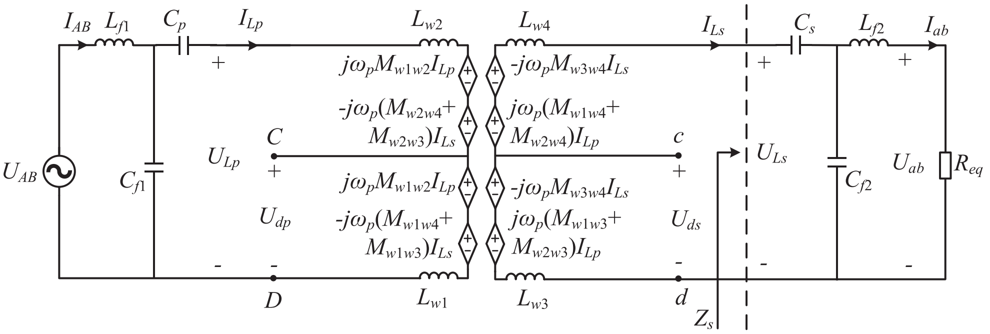


Fig. 10. Simplified equivalent model of power transfer channel with mutual inductances between four inductors L_{w1}, L_{w2}, L_{w3}, and L_{w4}.

The voltages U_{dp}, U_{ds}, and U_{Ls} can be expressed as

$$\begin{cases} \dot{U}_{dp} = (j\omega_p L_{w1} + j\omega_p M_{w1w2})\dot{I}_{Lp} \\ \qquad -(j\omega_p M_{w1w4} + j\omega_p M_{w1w3})\dot{I}_{Ls} \\ \dot{U}_{ds} = (j\omega_p M_{w1w3} + j\omega_p M_{w2w3})\dot{I}_{Lp} \\ \qquad -(j\omega_p M_{w3w4} + j\omega_p L_{w3})\dot{I}_{Ls} \\ \dot{U}_{Ls} = Z_s \dot{I}_{Ls}. \end{cases} \tag{34}$$

The inductance of winding can be calculated as

$$\begin{cases} L_w{}' = \frac{\mu_0 n_w{}^2}{2(R_2-R_1)^2} \int_0^{\pi} \int_{R_1}^{R_2} \int_{R_1}^{R_2} \frac{\cos\theta d\theta r_1 dr_1 r_2 dr_2}{\sqrt{r_1{}^2+r_2{}^2-2r_1 r_2 \cos\theta}} \\ L_w = L_w{}' + M_{Lw'Lw'1} + M_{Lw'Lw'2} + M_{Lw'Lw'3} \end{cases} \tag{35}$$

where n_w is the number of turns [41]. $L_w{}^{'}$ is the self-inductance of winding without ferrite [36]. L_w is the self-inductance of winding with ferrite core. $L_{w'1}$, $L_{w'2}$, and $L_{w'3}$ are the self-inductances after mirroring [37]. The mutual inductance between any two windings can be calculated as

$$\begin{cases} M_{ww}{}' = \frac{\mu_0 n_1 n_2}{(R_2-R_1)(R_4-R_3)} \int_0^{\pi} \int_{R_1}^{R_2} \int_{R_3}^{R_4} \\ \qquad \frac{\cos\theta d\theta r_1 dr_1 r_2 dr_2}{\sqrt{z_Q{}^2+r_1{}^2+r_2{}^2-2r_1 r_2 \cos\theta}} \\ M_{ww} = M_{Lw'Lw'1} + M_{Lw'Lw'2} \end{cases} \tag{36}$$

where n_1 and n_2 are number of turns [41]. $M_{ww}{}^{'}$ is the mutual inductance between any two windings without ferrite [38], M_{ww} is the mutual inductance between any two windings with ferrite cores. The voltage gains from U_{Lp} to U_{dp} and U_{Ls} to U_{ds} are expressed as (54), as shown in the appendix. The voltage gains from U_{Rdp} to U_{dp} and U_{Rds} to U_{ds} are obtained as

$$\begin{cases} G_{Rdp-dp} = \frac{\dot{U}_{Rdp}}{\dot{U}_{dp}} = \frac{j\omega_p L_{dp} R_{dp}}{(R_{dp}+j\omega_p L_{dp}) Z_{CD-TX}(\omega_p)} \\ G_{Rds-ds} = \frac{\dot{U}_{Rds}}{\dot{U}_{ds}} = \frac{j\omega_p L_{ds} R_{ds}}{(R_{ds}+j\omega_p L_{ds}) Z_{cd-RX}(\omega_p)}. \end{cases} \tag{37}$$

Then, the interference gains $G_{Rdp\text{-}AB}$ from U_{AB} to U_{Rdp} and $G_{Rds\text{-}AB}$ from U_{AB} to U_{Rds} can be expressed as follows:

$$\begin{cases} G_{Rdp-AB} = \frac{\dot{U}_{Rdp}}{\dot{U}_{AB}} = G_{Rdp-dp} G_{dp-Lp} G_{Lp-AB} \\ G_{Rds-AB} = \frac{\dot{U}_{Rds}}{\dot{U}_{AB}} = G_{Rds-ds} G_{ds-Ls} G_{Ls-AB}. \end{cases} \tag{38}$$

The forward SNR related to power signal is defined as

$$SNR_f = \frac{\dot{U}_{RXs}}{\dot{U}_{AB} G_{Rds-AB}} = \frac{\dot{U}_{TX\text{p}} G_{df}}{\dot{U}_{AB} G_{Rds-AB}} = \frac{\dot{U}_{TX\text{p}} G_d}{\dot{U}_{AB} G_{Rds-AB}} \tag{39}$$

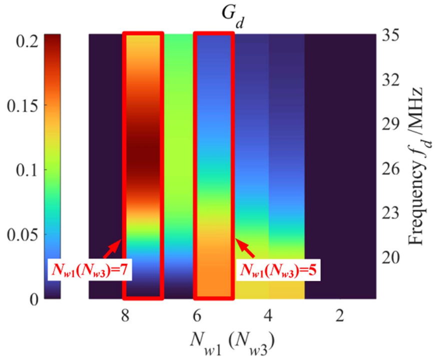


Fig. 11. Data transmission gain G_d versus N_{w1} (N_{w3}) and f_d.

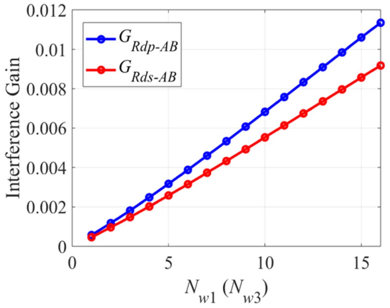


Fig. 12. Interference gains $G_{Rdp\text{-}AB}$ and $G_{Rds\text{-}AB}$ versus N_{w1} (N_{w3}) when C_{dp} (C_{ds}) = 560 pF.

Due to the symmetry of the system, the backward SNR related to power signal can be expressed as follows:

$$SNR_b = \frac{\dot{U}_{RX\text{p}}}{\dot{U}_{AB}G_{Rdp-AB}} = \frac{\dot{U}_{TX\text{s}}G_{db}}{\dot{U}_{AB}G_{Rdp-AB}} = \frac{\dot{U}_{TX\text{s}}G_d}{\dot{U}_{AB}G_{Rdp-AB}}. \tag{40}$$

In SWPDT systems, SNRs are crucial indicators of the power transfer's interference with data transmission. To optimize SNRs in the system, it requires increasing data transfer gain while minimizing power interference transfer gains. From the above analysis, it can be concluded that G_d, $G_{Rdp\text{-}AB}$, and $G_{Rds\text{-}AB}$ are related to the turn number of the outer windings N_{w1} and N_{w3} and the capacitances C_{dp} and C_{ds} at both sides. Therefore, it is essential to select appropriate values for N_{w1} (N_{w3}) and C_{dp} (C_{ds}) for improving SNRs. Generally, for data carriers operating above megahertz frequencies, the series capacitance in the data channel is usually below 1 nF [19]. In this system, the capacitor C_{dp} and C_{ds} are initially set to 560 pF, forming high-pass filter with L_{dp} and L_{ds}, respectively. Fig. 11 shows the data channel gain G_d versus N_{w1} (N_{w3}) and f_d, where only integer values of N_{w1} and N_{w3} are considered. The results indicate that higher G_d can be achieved at N_{w1} (N_{w3}) = 5 and 7. Specifically, when N_{w1} (N_{w3}) = 7, the peak G_d is approximately 0.201 at 27.7 MHz, while N_{w1} (N_{w3}) = 5 yields a peak G_d of approximately 0.15 at 17.5 MHz. To ensure adequate communication quality this system, G_d should not be below 0.2. Therefore, N_{w1} (N_{w3}) is selected as 7, with the data carrier frequency f_d set to 27.7 MHz. Fig. 12 shows the power interference gain $G_{Rds\text{-}AB}$ and $G_{Rdp\text{-}AB}$ versus N_{w1} (N_{w3}) when C_{dp} (C_{ds}) is equal to 560 pF. When N_{w1} (N_{w3}) = 7, the gain $G_{Rds\text{-}AB}$ is 0.004, and the gain $G_{Rdp\text{-}AB}$ is 0.005. Fig. 13 shows voltage gains $G_{Rdp\text{-}AB}$, $G_{Rds\text{-}AB}$ and G_d versus C_{dp} (C_{ds}) when N_{w1} (N_{w3}) = 7. The results confirm that with N_{w1} and N_{w3} set to 7, a capacitance value of 560 pF for C_{dp} (C_{ds}) maintains interference gains below 0.005 while ensuring a data channel gain above 0.2, thereby optimizing the SNRs. Consequently, both C_{dp} and C_{ds} can be finally designed as 560 pF in the final system configuration.

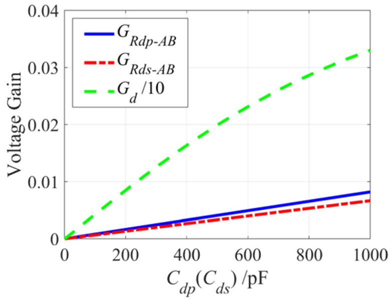


Fig. 13. Voltage gains $G_{Rdp\text{-}AB}$, $G_{Rds\text{-}AB}$, and G_d versus C_{dp} (C_{ds}) when N_{w1} (N_{w3}) =7.

In conclusion, this section derives SNR expressions and outlines the process for selecting appropriate N_{w1} (N_{w3}) and C_{dp} (C_{ds}) values to enhance SNR. The selection criteria for these parameters are as follows.

1) Data transfer gain G_d greater than 0.2.
2) Forward power interference $G_{Rds\text{-}AB}$ below 0.005.
3) Backward power interference $G_{Rdp\text{-}AB}$ below 0.005.

VI. DESIGN METHOD FOR POWER AND DATA TRANSFER CHANNEL

To achieve stable transmission of power and data, the proposed SWPDT system needs to meet the requirements as shown in the following:

$$\begin{cases} I_{\text{OFF}} > \frac{2C_{\text{oss}}U_{AB,\max}}{t_{\text{dead}}} \\ G_d > 0.2 \\ G_{Rds-AB}, G_{Rdp-AB} < 0.005 \\ SNR_f, SNR_b > 20dB. \end{cases} \tag{41}$$

Fig. 14 illustrates the parameter design flowchart. The design process begins with establishing fundamental parameters including input voltage, load value, power carrier frequency, and coupling coils parameters based on the specific requirements. Subsequently, setting the values of double-winding inductors (L_{f11}, L_{f12}, L_{f21}, and L_{f22}). Then, calculating the values of equivalent compensation inductances (L_{f1} and L_{f2}) according to (7) and (8) and confirming the values of compensation capacitors (C_{f1}, C_{f2}, C_p, and C_s) by (10). The value of the capacitor C_s should be adjusted to fulfill the requirement of turn-off current. After finalizing the parameters of the power transfer channel, start designing the data transfer channel. The values of N_{w1} (N_{w3}) and f_d are confirmed according to the peak G_d. C_{dp} (C_{ds}) should be designed to meet the requirements of the data transfer gain G_d, the interference gains $G_{Rds\text{-}AB}$ and $G_{Rdp\text{-}AB}$. Then, calculating the *SNR*$_f$ and *SNR*$_b$ using (39) and (40). If either

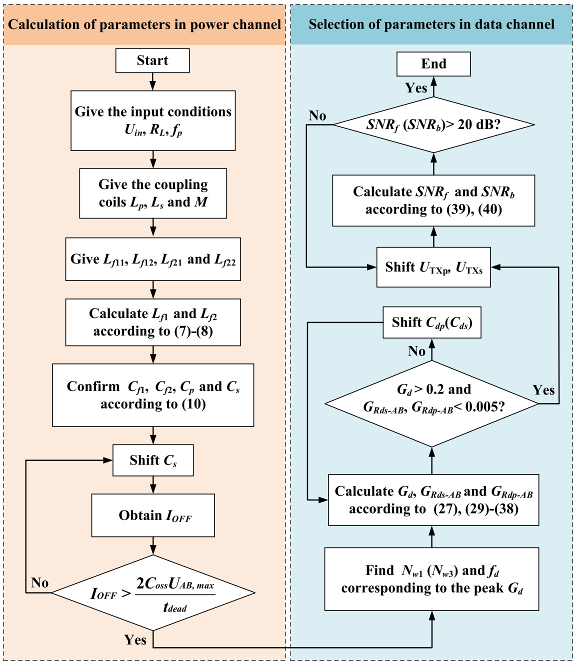


Fig. 14. Design flowchart of power and data channel parameters.

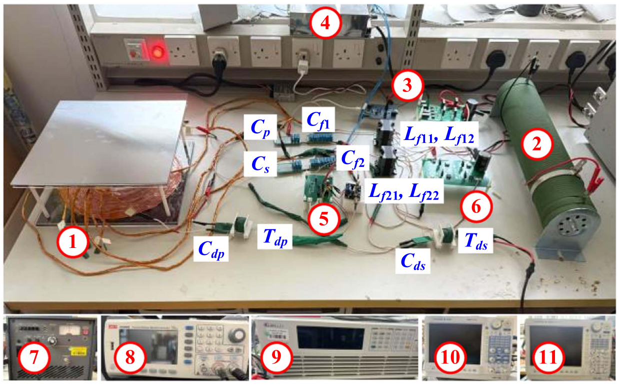


Fig. 15. Experimental platform of the whole SWPDT system.

SNR_f or SNR_b fall below 20 dB, U_{TXp} and U_{TXs} are required to be adjusted again.

VII. EXPERIMENTAL VERIFICATION

To validate the proposed SWPDT system, a 545-W prototype was constructed as shown in Fig. 15. The setup comprises ten key components including the coupler, resistor load, inverter, auxiliary power supply, signal demodulation circuit, rectifier, power amplifier, signal generator, dc power supply, oscilloscope, and power analyzer. These are indicated by circled numbers 1 through 11 in Fig. 15. Table III provides a comprehensive list of system parameters.

For data transmission, we employed ASK modulation. In the data demodulation circuit, the voltage follower is THS4001, and the voltage comparator is TLV3501. In this scheme, the presence of a data carrier wave represents a binary “1”, while its absence indicates a “0”. The data reception and demodulation process involve several stages, as shown in Fig. 3. First, a voltage follower tracks and isolates the received data signal at the sampling resistor. Next, an envelope demodulation module extracts the signal’s envelope. Finally, a voltage comparator recovers the transmitted data by comparing the extracted envelope with a reference voltage.

TABLE III
EXPERIMENTAL PARAMETERS IN THE PROPOSED SYSTEM

Symbol	Value	Symbol	Value
L_p, L_s	286.8 μH, 286.5 μH	$R_{p\text{-}in}$, $R_{s\text{-}in}$	0.02 m
C_p, C_s	17.78 nF, 20.1 nF	$R_{p\text{-}out}$, $R_{s\text{-}out}$	0.14 m
C_{f1}, C_{f2}	40.08 nF, 40.1 nF	N_{w1}, N_{w3}	7 turns
L_{f1}, L_{f2}	87.82 μH, 87.93 μH	N_{w2}, N_{w4}	23 turns
C_{fi}, C_{fo}	1000 μF	L_{w1}, L_{w3}	41.58 μH, 39 μH
C_{dp}, C_{ds}	560 pF	L_{w2}, L_{w4}	164 μH, 164.8 μH
f_p	85 kHz	M_{w1w2}, M_{w3w4}	40.86 μH, 41.4 μH
f_d	27.72 MHz	M_{w1w3}	7.83 μH
k	0.266	M_{w2w4}	40.98 μH
R_L	60.5 Ω	M_{w1w4}, M_{w2w3}	18.71 μH, 16 μH
D_{ps}	10 cm	R_{dp}, R_{ds}	50 Ω
U_{in}	181 V	L_{dp}, L_{ds}	3.85 μH

A. *Experimental Results*

The proposed SWPDT system operates with a power carrier frequency of 85 kHz, a 60.5 Ω load, and a data carrier frequency of 27.7 MHz. Figs. 16 and 17 show power and data transmission waveforms. The output voltage and current of the inverter, input voltage and current of the rectifier, dc input voltage and current, and dc output voltage and current are shown in Figs. 16(a) and 17(a), while Figs. 16(b) and 17(b) display the output voltage and current of the inverter, output voltage of the transmitter, input voltage of the receiver, and demodulated data.

Power transmission waveforms in Figs. 16 and 17 show negligible high-frequency carriers, indicating minimal influence of data transmission on power transmission. The turn-OFF current exceeds 1 A, and the voltage leads to the current in the inverter, thus ZVS is achieved, aligning with our theoretical analysis in Section III. The bit rate of data transmission is 1.25 Mb/s. Fig. 18 shows that with an input power of 570.4 W and an output of 545 W, the system achieves a PTE of approximately 95.55%.

Fig. 19(a) shows the waveforms of U_{Lp} and U_{Ls}. Fig. 19(b) shows the waveforms of U_{dp} and U_{ds}. The amplitudes of U_{Lp}, U_{Ls}, U_{dp}, and U_{ds} are 843, 825, 240, and 229 V, respectively. Thus, the calculated values for $G_{dp\text{-}Lp}$ and $G_{ds\text{-}Ls}$ in the experiment are 0.285 and 0.272, respectively. The theoretical values calculated by (56) are 0.275 and 0.268, respectively. It was found that the experimental values closely matched theoretical values. The correctness of the inferences in Section V is verified. Fig. 20 shows the spectrums of the data channel. From the spectrums, the amplitude around 85 kHz is very small, not exceeding −30.06 dB. In addition, the amplitudes of U_{RXs} and

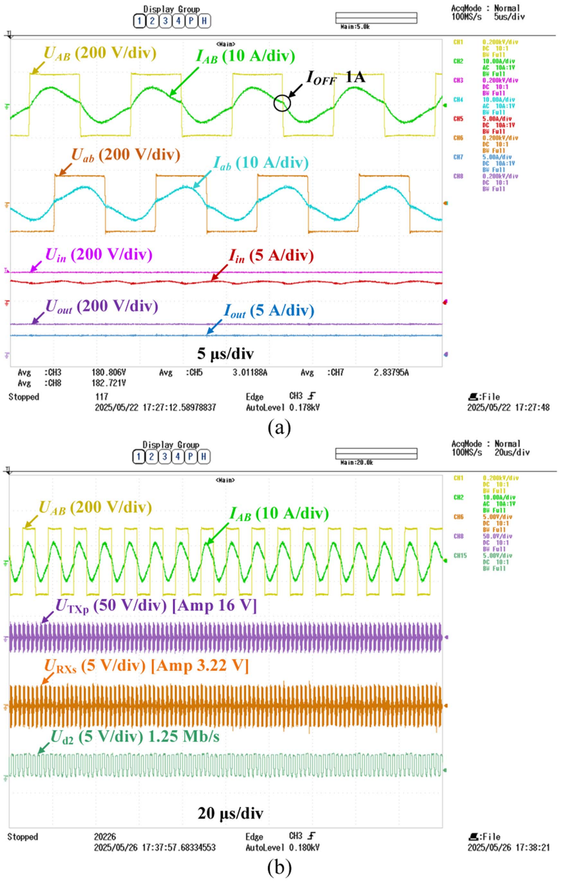


Fig. 16. Waveforms of power and forward data transmission. (a) Output voltage and current of the inverter, input voltage and current of the rectifier, dc input voltage and current and dc output voltage and current. (b) Output voltage and current of the inverter, output voltage of the primary transmitter, input voltage of the secondary receiver and demodulated data.

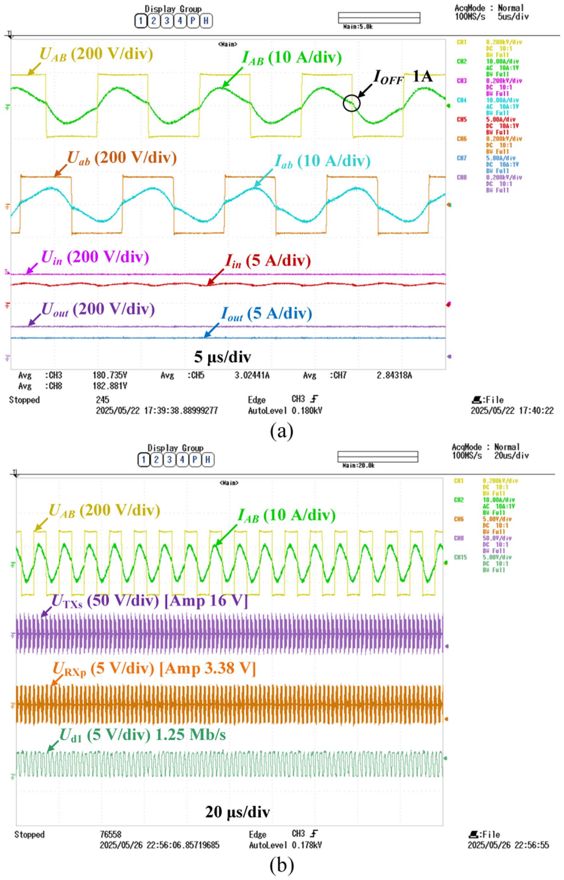
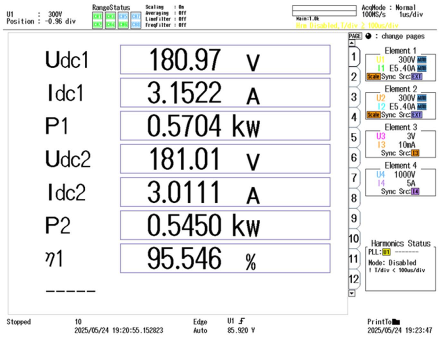


Fig. 17. Waveforms of power and backward data transmission. (a) Output voltage and current of the inverter, input voltage and current of the rectifier, dc input voltage and current and dc output voltage and current. (b) Output voltage and current of the inverter, output voltage of the secondary transmitter, input voltage of the primary receiver and demodulated data.

U_{RXp} can be estimated as 3.22 and 3.38 V, as shown in Fig. 22, indicating that SNR_f and SNR_b are both larger than 20 dB. The amplitude of U_{TXp} (U_{TXs}) is 16 V, thus, practical G_{ds} and G_{dp} can be estimated at approximately 0.201 and 0.211, respectively. These findings are aligned with the analysis in Fig. 11. The above experimental results confirm the simultaneous transmission of data and power in our SWPDT system.

In addition, the system's performance is also evaluated under different load/coupling conditions. Fig. 21 illustrates the PTE versus load resistance R_L under different coupling coefficient k. It can be inferred from Fig. 21 that the proposed system can maintain the PTE above 90% across both load resistance (20 Ω $\leq R_L \leq$ 60 Ω) and coupling coefficient ($0.187 \leq k \leq 0.266$) variation ranges. Fig. 22 shows the waveforms of power and data transmission under $R_L = 20$ Ω and $k = 0.187$. The bit rate still remains at 1.25 Mb/s. These experimental results demonstrate that the proposed SWPDT system has great robustness under load variation or coupling misalignment. Fig. 23 illustrates the PTE both with and without the data transfer channel. The output power with the data channel is almost identical to that without the data channel, indicating that the added data channel has little impact on power transfer.



Udc1	180.97 V
Idc1	3.1522 A
P1	0.5704 kW
Udc2	181.01 V
Idc2	3.0111 A
P2	0.5450 kW
η1	95.546 %

Fig. 18. Power and PTE of the proposed system.

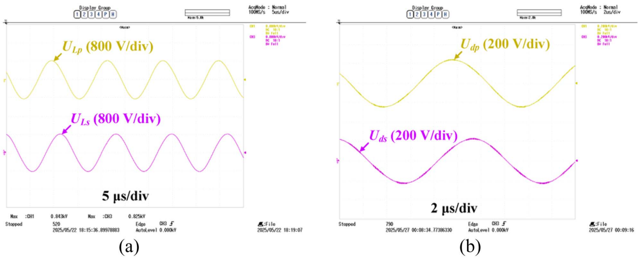
B. Comparison With Previous Works

Table IV summarizes a comprehensive comparison between the proposed system and previous research. In detail, the authors in [25] and [27] only implemented one-direction communication. The authors in [12], [19], and [21] added multiple wave trappers or trap inductors into the system, increasing the overall size and cost. Fan et al. [26] successfully realized bidirectional

TABLE IV
COMPARISON BETWEEN THE PROPOSED SWPDT SYSTEM AND THE PREVIOUS WORKS

Reference	[12]	[19]	[20]	[21]	[25]	[26]	[27]	[28]	This Work
Number of Shared Inductive Link	1	1	1	1	1	1	1	1	1
Communication Mode	Half-Duplex	Full-Duplex	Full-Duplex	Full-Duplex	Simplex	Half-Duplex	Simplex	Full-Duplex	Half-Duplex
Modulation	ASK	ASK	FSK	ASK	ASK	ASK	ASK	FSK	ASK
Coupling Coefficient	0.94	0.21	0.222	0.3	-	0.8	0.11	0.29	0.266
Transferred Power / W	250	500	300	600	150	300	200	518	545
Maximum Data Rate / kb/s	19.2	600	500	80	166.7	40	30	700	1250
Bidirectional or Unidirectional	B	B	B	B	U	B	U	B	B
Number of Additional Passive Components	8	12	4	20	6	9	6	6	4
PTE	86.08%	84%	90.1%	86%	90%	90.5%	92.25%	92%	95.55%
Analyze Distributed Parameter with Considering Ferrite Cores	No	No	No	No	No	No	No	No	Yes
Optimal Tap Position $N_{w1}(N_{w3})$	Not analyze	Not analyze	8	Not analyze	Not analyze	Not analyze	Not analyze	Not analyze	7
Verification under Coupling Variation	No	Yes	Yes	No	Yes	No	Yes	No	Yes
Verification under Load Variation	Yes	Yes	No	Yes	No	No	No	No	Yes

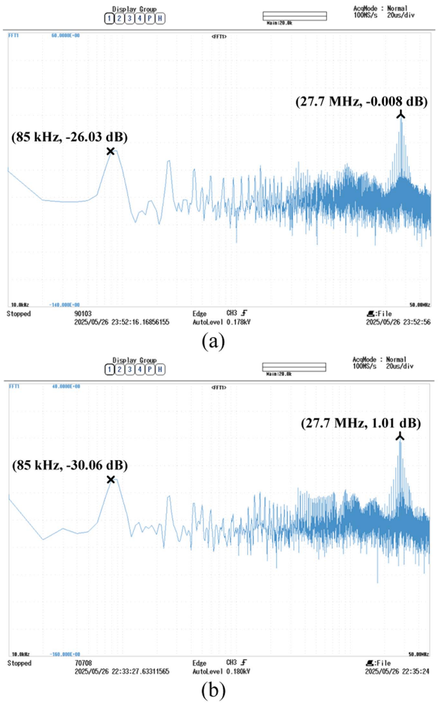
Note: The shaded areas mean the desirable performance.



(a) (b)

Fig. 19. Voltage waveforms of power and forward data transmission. (a) Voltages across the coils. (b) Voltages across the outer windings.

communication and achieved high transmission efficiency. However, the performance of the system in [26] still requires further study when the output power exceeds 300 W. Yao et al. [20] considered the optimal tap position. However, it does not consider distributed parameter with ferrite cores. Wang et al. [28] simultaneously considered the parasitic parameters of the coil, and the system has excellent performance. However, it does not consider the optimal tap position and lacks performance analysis under varying coupling or load conditions. Compared with these works, the proposed SWPDT system has several advantages. It achieves high power output, efficient power transfer, and high-rate communication while requiring minimal additional passive components, resulting in a cost-effective and scalable solution.



(a)

(b)

Fig. 20. Waveforms of the data channel with data transmission. (a) Spectrum of U_{RXs}. (b) Spectrum of U_{RXp}.

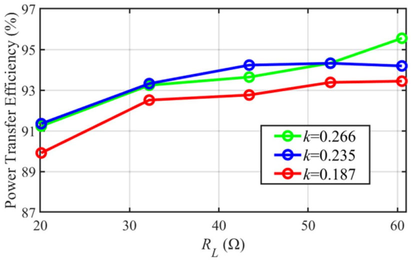
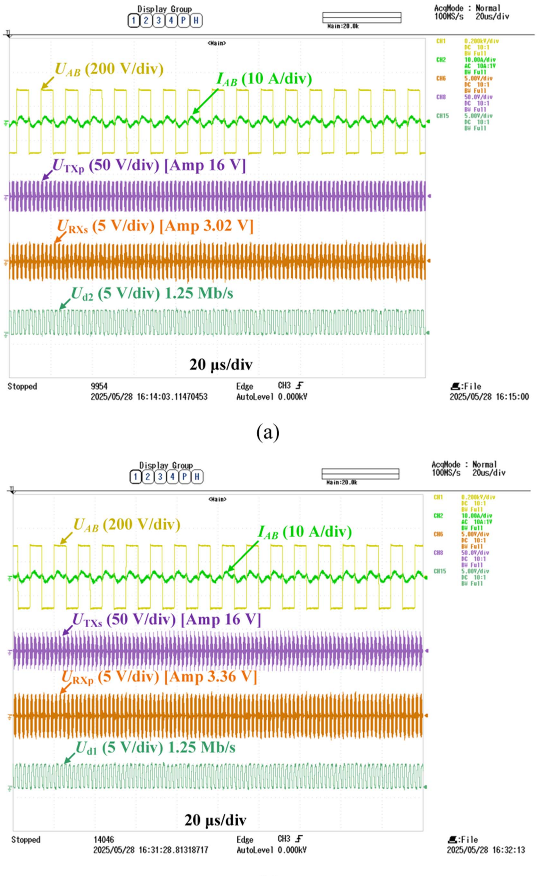


Fig. 21. PTE versus R_L under different k.



(a)

(b)

Fig. 22. Waveforms of the power and data transmission under $R_L = 20\ \Omega$ and $k = 0.187$. (a) Forward data transmission. (a) Backward data transmission.

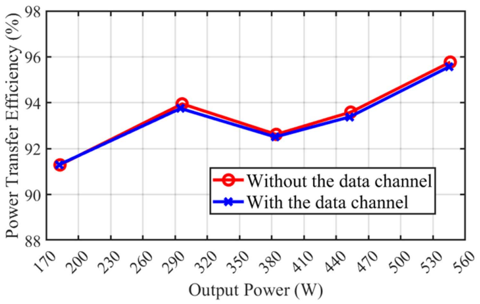


Fig. 23. PTE with and without the data transfer channel.

Furthermore, it comprehensively considers both distributed parameters of coil with ferrite cores and tap position selection, with the performance verification provided under varying coupling and load conditions.

VIII. CONCLUSION

This article proposes a novel SWPDT system based on tapped coils with ferrite cores. The proposed SWPDT system enables the synchronous transmission of power and data through a shared inductive link. The equivalent model of power channel was established to analyze power transfer. A distributed parameter model for data transfer is established and simplified. It allows for thorough analysis of communication performance and crosstalk. Then, a systematic parameter design method for both power and data channels is proposed. The experimental prototype demonstrates the system's viability, which can achieve an output power of 545 W, 95.55% PTE, and 1.25 Mb/s bidirectional half-duplex communication.

APPENDIX

Matrices for the (22), Z_{11}, Z_{12}, Z_{21}, Z_{22}, $G_{dp\text{-}Lp}$ and $G_{ds\text{-}Ls}$, are shown as (44), (47) (53), (54) shown at the bottom of this page, follows:

$$\boldsymbol{A} = \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 \\ -1 & 1 & 0 & \dots & 0 \\ 0 & -1 & 1 & \dots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & -1 & 1 \end{bmatrix} \tag{42}$$

$$\boldsymbol{B} = \boldsymbol{A}^T = \begin{bmatrix} 1 & -1 & 0 & \cdots & 0 \\ 0 & 1 & -1 & \dots & 0 \\ 0 & 0 & 1 & \dots & \vdots \\ \vdots & \vdots & \vdots & \ddots & -1 \\ 0 & 0 & \dots & 0 & 1 \end{bmatrix} \tag{43}$$

$$\boldsymbol{Z}_p = \begin{bmatrix} sL_{p1} + R_{Lp1} & 0 & \dots & 0 \\ 0 & sL_{p2} + R_{Lp2} & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & sL_{pn} + R_{Lpn} \end{bmatrix} \tag{45}$$

$$\boldsymbol{Z}_s = \begin{bmatrix} sL_{s1} + R_{Ls1} & 0 & \dots & 0 \\ 0 & sL_{s2} + R_{Ls2} & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & sL_{sn} + R_{Lsn} \end{bmatrix} \tag{46}$$

$$\boldsymbol{U}_p = \begin{bmatrix} U_{p1} \\ U_{p2} \\ \vdots \\ U_{pn} \end{bmatrix}, \boldsymbol{U}_s = \begin{bmatrix} U_{s1} \\ U_{s2} \\ \vdots \\ U_{sn} \end{bmatrix}, \tag{48}$$

$$\boldsymbol{Y}_{C1}=\begin{bmatrix}\sum\limits_{K=1,K\neq 2}^{n} Y_{C_{p(2,K)}} & \frac{-sC_{p(2,3)}}{1+sC_{p(2,3)}R_{p(2,3)}} & \cdots & \frac{-sC_{p(2,n)}}{1+sC_{p(2,n)}R_{p(2,n)}} & 0\\ \frac{-sC_{p(3,2)}}{1+sC_{p(3,2)}R_{p(3,2)}} & \sum\limits_{K=1,K\neq 3}^{n} Y_{C_{p(3,K)}} & \cdots & \frac{-sC_{p(3,n)}}{1+sC_{p(3,n)}R_{p(3,n)}} & 0\\ \vdots & \vdots & \ddots & \vdots & \vdots\\ \frac{-sC_{p(n,2)}}{1+sC_{p(n,2)}R_{p(n,2)}} & \frac{-sC_{p(n,3)}}{1+sC_{p(n,3)}R_{p(n,3)}} & \cdots & \sum\limits_{K=1}^{n-1} Y_{C_{p(n,K)}} & 0\\ 0 & 0 & \cdots & 0 & sC_{eq1}\end{bmatrix} \tag{44}$$

$$\boldsymbol{Y}_{C2}=\begin{bmatrix}\sum\limits_{K=1,K\neq 2}^{n} Y_{C_{s(2,K)}} & \frac{-sC_{s(2,3)}}{1+sC_{s(2,3)}R_{s(2,3)}} & \cdots & \frac{-sC_{s(2,n)}}{1+sC_{s(2,n)}R_{s(2,n)}} & 0\\ \frac{-sC_{s(3,2)}}{1+sC_{s(3,2)}R_{s(3,2)}} & \sum\limits_{K=1,K\neq 3}^{n} Y_{C_{s(3,K)}} & \cdots & \frac{-sC_{s(3,n)}}{1+sC_{s(3,n)}R_{s(3,n)}} & 0\\ \vdots & \vdots & \ddots & \vdots & \vdots\\ \frac{-sC_{s(n,2)}}{1+sC_{s(n,2)}R_{s(n,2)}} & \frac{-sC_{s(n,3)}}{1+sC_{s(n,3)}R_{s(n,3)}} & \cdots & \sum\limits_{K=1}^{n-1} Y_{C_{s(n,K)}} & 0\\ 0 & 0 & \cdots & 0 & sC_{eq2}\end{bmatrix} \tag{47}$$

$$\begin{cases} Z_{11}=\frac{U_{px}}{I_{TXp}}\Big|_{I_{RXs}=0}=\frac{1}{\{\boldsymbol{Y}_{C1}+\boldsymbol{B}[\boldsymbol{Z}_p+s\boldsymbol{M}_p-s^2\boldsymbol{M}_{ps}^2(\boldsymbol{A}\boldsymbol{Y}_{C2}^{-1}\boldsymbol{B}+\boldsymbol{Z}_s+s\boldsymbol{M}_s)^{-1}]^{-1}\boldsymbol{A}\}_{xx}}\\ Z_{22}=\frac{U_{sx}}{I_{RXs}}\Big|_{I_{TXp}=0}=\frac{1}{\{\boldsymbol{Y}_{C2}+\boldsymbol{B}[\boldsymbol{Z}_s+s\boldsymbol{M}_s-s^2\boldsymbol{M}_{ps}^2(\boldsymbol{A}\boldsymbol{Y}_{C1}^{-1}\boldsymbol{B}+\boldsymbol{Z}_p+s\boldsymbol{M}_p)^{-1}]^{-1}\boldsymbol{A}\}_{xx}}\\ Z_{12}=\frac{U_{px}}{I_{RXs}}\Big|_{I_{TXp}=0}=\frac{1}{\begin{array}{l}\{\boldsymbol{Y}_{C2}\boldsymbol{A}^{-1}[(\boldsymbol{Z}_s+s\boldsymbol{M}_s)s^{-1}\boldsymbol{M}_{ps}^{-1}(\boldsymbol{A}+\boldsymbol{Z}_p\boldsymbol{B}^{-1}\boldsymbol{Y}_{C1}+s\boldsymbol{M}_p\boldsymbol{B}^{-1}\boldsymbol{Y}_{C1})-s\boldsymbol{M}_{ps}\boldsymbol{B}^{-1}\boldsymbol{Y}_{C1}]\\ +\boldsymbol{B}s^{-1}\boldsymbol{M}_{ps}^{-1}(\boldsymbol{A}+\boldsymbol{Z}_p\boldsymbol{B}^{-1}\boldsymbol{Y}_{C1}+s\boldsymbol{M}_p\boldsymbol{B}^{-1}\boldsymbol{Y}_{C1})\}_{xx}\end{array}}\\ Z_{21}=\frac{U_{sx}}{I_{TXp}}\Big|_{I_{RXs}=0}=\frac{1}{\begin{array}{l}\{\boldsymbol{Y}_{C1}\boldsymbol{A}^{-1}[(\boldsymbol{Z}_p+s\boldsymbol{M}_p)s^{-1}\boldsymbol{M}_{ps}^{-1}(\boldsymbol{A}+\boldsymbol{Z}_s\boldsymbol{B}^{-1}\boldsymbol{Y}_{C2}+s\boldsymbol{M}_s\boldsymbol{B}^{-1}\boldsymbol{Y}_{C1})-s\boldsymbol{M}_{ps}\boldsymbol{B}^{-1}\boldsymbol{Y}_{C2}]\\ +\boldsymbol{B}s^{-1}\boldsymbol{M}_{ps}^{-1}(\boldsymbol{A}+\boldsymbol{Z}_s\boldsymbol{B}^{-1}\boldsymbol{Y}_{C2}+s\boldsymbol{M}_s\boldsymbol{B}^{-1}\boldsymbol{Y}_{C2})\}_{xx}\end{array}} \end{cases} \tag{53}$$

$$\begin{cases} G_{dp-Lp}=\frac{U_{dp}}{U_{Lp}}=\frac{-\omega_p L_s L_{w1}-\omega_p L_s M_{w1w2}+jZ_s L_{w1}+jZ_s M_{w1w2}+\omega_p M(M_{w1w4}+M_{w1w3})}{-\omega_p L_p L_s+jL_p Z_s+\omega_p M^2}\\ G_{ds-Ls}=\frac{U_{ds}}{U_{Ls}}=\frac{(M_{w1w3}+M_{w2w3})(j\omega_p L_s+Z_s)-j\omega_p M M_{w3w4}-j\omega_p M L_{w3}}{Z_s M}. \end{cases} \tag{54}$$

$$\boldsymbol{I}_p=\begin{bmatrix}I_{p1}\\ I_{p2}\\ \vdots\\ I_{pn}\end{bmatrix},\boldsymbol{I}_s=\begin{bmatrix}I_{s1}\\ I_{s2}\\ \vdots\\ I_{sn}\end{bmatrix},\boldsymbol{I}_{in,p}=\begin{bmatrix}0\\ \vdots\\ I_{\mathrm{TXp}}\\ \vdots\\ 0\end{bmatrix},I_{in,s}=\begin{bmatrix}0\\ \vdots\\ I_{\mathrm{RXs}}\\ \vdots\\ 0\end{bmatrix} \tag{49}$$

$$\boldsymbol{M}_{ps}=\begin{bmatrix}M_{p1s1} & M_{p1s2} & \cdots & M_{p1sn}\\ M_{p2s1} & M_{p2s2} & \cdots & M_{p2sn}\\ \vdots & \vdots & \ddots & \vdots\\ M_{pns1} & M_{pns2} & \cdots & M_{pnsn}\end{bmatrix} \tag{50}$$

$$\boldsymbol{M}_p=\begin{bmatrix}0 & M_{p12} & \cdots & M_{p1n}\\ M_{p21} & 0 & \cdots & M_{p2n}\\ \vdots & \vdots & \ddots & \vdots\\ M_{pn1} & M_{pn2} & \cdots & 0\end{bmatrix} \tag{51}$$

$$\boldsymbol{M}_s=\begin{bmatrix}0 & M_{s12} & \cdots & M_{s1n}\\ M_{s21} & 0 & \cdots & M_{s2n}\\ \vdots & \vdots & \ddots & \vdots\\ M_{sn1} & M_{sn2} & \cdots & 0\end{bmatrix} \tag{52}$$

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