Quadratic High Step-Up Interleaved Z-Source DC-DC Converters Based on Asymmetric Gamma Cell

Sareh Daneshgar, Ebrahim Babaei, *Senior Member, IEEE*, and Mohammad Bagher Bannae Sharifian

***Abstract*—This article proposes a group of interleaved dc–dc converters based on quasi-impedance source cells with quadratic voltage gain. Using the developed asymmetric gamma impedance source cell with an interleaved technique, the proposed structure minimizes the current stress on the MOSFETs, the fluctuation of the input current, and losses. Apart from the benefits mentioned above, the proposed structure includes a shared ground, fewer components, low voltage stress across the components, and high efficiency. Necessary theoretical studies are carried out on the proposed structures, including voltage gain calculations, element voltage stress, element design, and element loss calculations. Additionally, a thorough analysis compares the proposed structures with other interleaved converters. Finally, a 400-watt laboratory sample of the first proposed design, operating with a 30 V input voltage, is implemented to validate the stated advantages. The prototype implemented at 400 watts has an efficiency of 96.7%.**

***Index Terms*—Coupled inductors, dc–dc converter, impedance source cell, interleaved converter.**

I. Introduction

TODAY, the use of renewable energy holds great significance in environmental policies. Therefore, substantial investments are being made to harness renewable energy sources such as solar and wind [1], [2]. The implementation of renewable energies necessitates intermediate devices like dc–dc converters for energy processing [3], [4]. By utilizing dc–dc converters with high-power energy processing capabilities and high efficiency, the overall revenue of the system can be enhanced.

Recently, many dc–dc converters have been introduced with different structures [5]. Among these structures are interleaved converters, which have attracted significant attention due to their advantages, such as continuous input current with low ripple and high power processing capability [6], [7]. The interleaved structure presented in [8] is one of these designs that can increase the output voltage. The interleaved converters described in [9] and [10] utilize four inductors with four separate cores in their design. These converters produce low output voltage, and certain components are bulky, leading to an increase in their size and losses. coupled inductors. However, as discussed in [11] and [12], the voltage gain can be enhanced through interleaved structures, which reduce the need for magnetic components and incorporate. Nonetheless, the abundance of elements in these structures results in a higher volume and losses for the converters. The interleaved converters presented in [13] and [14] are additional step-up converters that utilize fewer elements than other existing converters.

Interleaved converters based on impedance source cells represent a type of interleaved converter that, while maintaining the characteristics of interleaved converters, also overcomes the limitations of impedance source converters [15]. The interleaved converter, which utilizes the quasi-impedance source cell described in [16], employs the interleaved technique to connect the cells within the quasi-impedance source structure. Despite the reduction in input current ripple, this structure still experiences high voltage and current stress, and although a large number of elements are used, there has been no change in its voltage gain.

The boost interleave converter described in [17] improves the voltage gain by employing two input inductors and a three-winding coupled inductor. Despite including the coupled inductor, switched capacitors, and other additional components, this design has succeeded in increasing the voltage gain to a satisfactory level. However, excessive voltage stress still exists on its components. The structure mentioned also shares a similarity between the input and output. In [18], the interleaved converter utilizes three-winding coupled inductors to achieve the desired output voltage. Including three-winding coupled inductors in this converter design results in higher leakage inductances, leading to increased losses and output voltage. This converter includes a shared ground and experiences a slight increase in voltage gain. Additionally, there is a high voltage stress on the components of this converter. In contrast to the interleaved converter discussed in [17], this converter achieves the same voltage gain as the interleaved converter by eliminating one ferrite core in the design and utilizing similar components. Moreover, the voltage stress across the components of both converters remains consistent.

Received 25 February 2025; revised 18 May 2025; accepted 14 June 2025. Date of publication 8 July 2025; date of current version 8 September 2025. Recommended for publication by Associate Editor W. Huang. *(Corresponding author: Ebrahim Babaei.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3586855.

Digital Object Identifier 10.1109/TPEL.2025.3586855

The converter described in [19] is a boost interleaved converter based on Dickson cells. This converter utilizes a common ground and provides a high-voltage boost. Despite its benefits, there are drawbacks, such as the requirement for high-voltage capacitors, leading to increased size and volume of both the capacitors and the converter itself. The converter presented in [20] is an improved Dickson-based boost interleave converter that overcomes the disadvantages of the Dickson cell-based boost interleave converter presented in [19] and reduces the voltage stress across its capacitors. However, this converter suffers from a lack of a common ground. In [21], an interleaved converter utilizing three-winding coupled inductors is introduced. This converter, having a shared ground, enhances voltage gain through the use of three-winding coupled inductors, despite having high leakage inductance. [22] discusses another interleaved converter that also employs three-winding coupled inductors. This converter utilizes a shared ground and enhances voltage amplification through the use of three-winding coupled inductors and switched capacitors. Despite this, it still experiences significant leakage inductance, and employing more switched cells to further boost voltage amplification leads to increased losses. The interleaved converter discussed in [23] incorporates voltage multiplier cells (consisting of a capacitor/diode/inductor) to raise the output voltage, consequently increasing the number of components in the converter. Nonetheless, this specific converter falls short of delivering high-voltage amplification. The voltage stress on the switches in this converter is lower compared to the traditional boost SEPIC converter. One notable drawback of this converter is the absence of a shared ground.

The interleaved converter described in [24] utilizes switched capacitors to enhance the voltage gain. To achieve a high voltage gain, this converter requires a significant number of cells. In contrast, the interleaved converter detailed in [25] employs a combination of a three-winding coupled inductor and two double-winding coupled inductors at the input to amplify the voltage gain. Nevertheless, this converter suffers from high losses due to its leakage inductance. The interleaved converter outlined in [26] features two three-winding inductors and utilizes capacitors and modified inductors to boost the voltage gain. Similarly, the converter discussed in [27] utilizes a coupled inductor to enhance the voltage gain, although the voltage gain achieved is not particularly high.

This article introduces a new family of dc–dc interleaved converters that utilize impedance source cells. These converters have several advantages, including high voltage gain, continuous input current with minimal ripple, common ground, low stress on both voltage and current across elements, and high efficiency. The interleaved converters based on impedance source cells were studied in various operating modes, and their performance in steady-state mode was analyzed. The design of the converter elements was optimized for efficiency by operating in boundary current mode. The proposed converters were compared to existing interleaved converters to highlight their benefits. To validate the theoretical findings, a 400-watt prototype of the first proposed converter was implemented and tested in a laboratory setting.

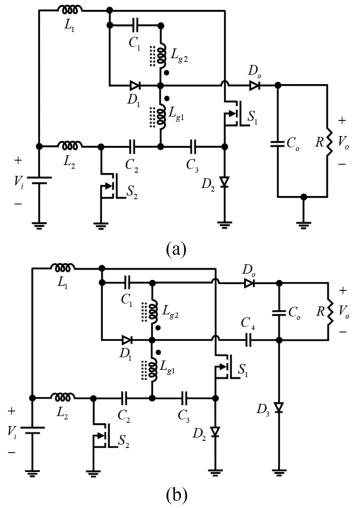


Fig. 1. Proposed structures. (a) First proposed structure based on asymmetric gamma impedance cell. (b) Second proposed structure based on extended asymmetric gamma impedance cell.

II. Operation Principles of the Proposed DC–DC Impedance Source Interleaved Converter

In this article, two structures of impedance source converters based on the interleaved technique are proposed. The first proposed structure has a common ground, but the second proposed structure does not have a common ground. In the structure of these converters, an asymmetric gamma impedance source cell and an improved asymmetric gamma are used along with other auxiliary elements, such as a capacitor and a diode. The power circuits of the first and second proposed converters are illustrated in Fig. 1(a) and (b), respectively. Using an asymmetric gamma impedance cell enhances the voltage gain, though it lacks a shared ground. The operating modes of the first proposed converter will be examined, and the final relations of the second proposed converter will also be calculated. The analysis of the proposed structures is based on the following assumptions.

1) To simplify the analysis, it is assumed that all components used in the proposed structures are ideal.
2) The converter's input voltage is considered to be an ideal dc voltage source without any fluctuations.
3) The examination of the converter's operating modes focuses on the continuous operation mode and the steady state.
4) In the proposed converter, the coupled inductor is seen as an ideal transformer with leakage inductance (L_k) connected in series with the primary winding and magnetizing inductance (L_m) in parallel with the primary winding. Additionally, for simplicity, the ratios $N_2/N_1 = n_{21} = n$ are assumed.

A. Proposed Interleaved Z-Source Converter Based on Asymmetric Γ-Source Cells

The first proposed structure includes four different operating modes, which can be observed in Fig. 2.

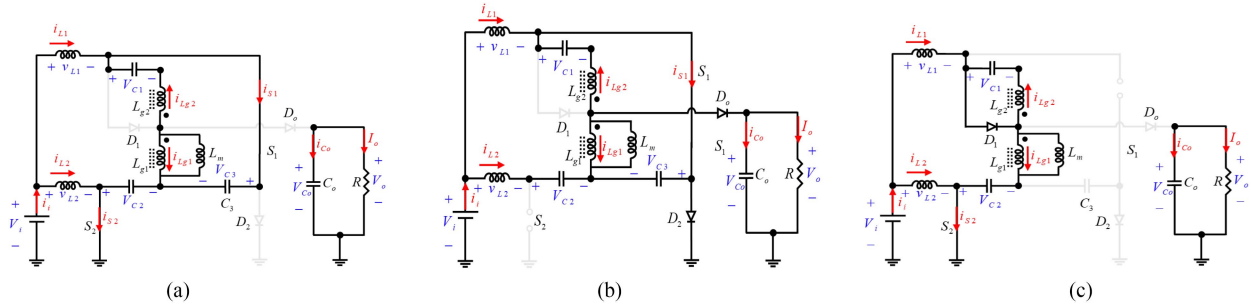


Fig. 2. First proposed converter's operation modes: (a) Mode I and Mode III. (b) Mode II. (c) Mode IV.

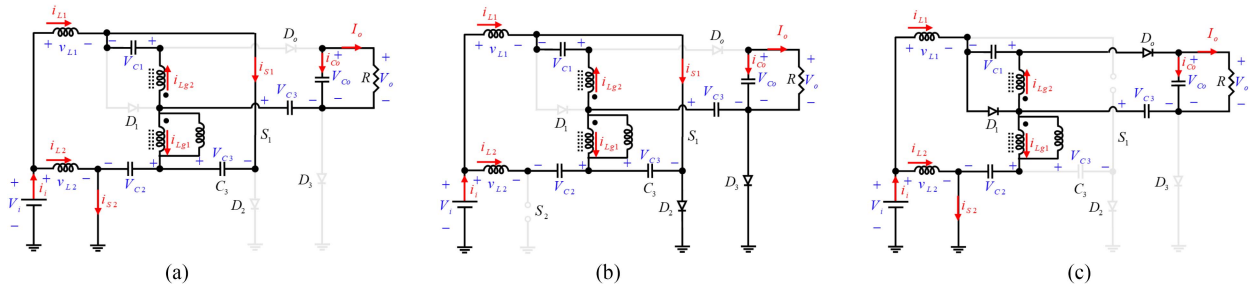


Fig. 3. Second proposed converter's operation modes, (a) Mode I and Mode III. (b) Mode II. (c) Mode IV.

Mode I: When both switches are turned on in this mode, diodes D_1, D_2, and D_o become reverse-biased and do not conduct. In this mode, inductors L_1 and L_2 are charged, and the load is powered through the output capacitor as shown in the equivalent circuit in Fig. 2(a).

Mode II: In the second operating mode, switch S_1 remains on while switch S_2 is turned OFF. With switch S2 OFF, inductor L_2 discharges and charges capacitor C_2. Diode D_1 remains reverse-biased, while diodes D_2 and D_o are forward-biased and conduct. The equivalent circuit for this mode is illustrated in Fig. 2(b).

Mode III: In the third operating mode, switch S_1 remains ON, and switch $S2$ starts conducting again. This mode is similar to the first operating mode, depicted in Fig. 2(a).

Mode IV: In the fourth mode of operation, switch $S1$ is conducting while switch S_2 is turned OFF, making diode D_1 forward-biased and conducting, and diodes D_2 and D_o reverse-biased and OFF. The equivalent circuit for this mode is illustrated in Fig. 2(c). As per the equivalent circuit for the first mode, inductor L_1 discharges and charges capacitor C_1, while inductor L_2 is charged during this mode.

B. Proposed Interleaved Z-Source Converter Based on Improved Asymmetric Γ-Source Cells

The second proposed structure has four operating modes, as illustrated in Fig. 3.

The first and second proposed converters have a similar switching mechanism. Therefore, a brief overview of the operational modes of the second proposed converter is provided.

Mode I: The switches are conducting, while diodes D_1, D_2, D_3, and D_o are reverse-bias and therefore nonconducting. In this particular mode, the inductors $L1$ and $L2$ receive energy and charge up while the load is supplied with power through the output capacitor. The schematic representation of the initial operating mode can be viewed in Fig. 3(a).

Mode II: During the second operating mode, switch S_1 stays in its previous state while switch S_2 is deactivated. The deactivation of switch S_2 results in the discharging of inductor L_2 and the continued charging of inductor L_1. Diodes D_1 and D_o are OFF in this mode, while diodes D_2 and D_3 are in forward bias. The operation mode circuit can be seen in Fig. 3(b).

Mode III: The third mode of operation is comparable to the first mode, and its corresponding circuit is illustrated in Fig. 3(a).

Mode IV: During the fourth mode of operation, switch $S1$ is conducting while switch S_2 is turned OFF. Furthermore, diodes D_1 and D_o are in forward bias and conducting, while diodes D_2 and D_3 are in reverse bias and therefore inactive. The equivalent circuit for the fourth mode is depicted in Fig. 3(c).

The theoretical voltage and current waveforms for the converters are shown in Fig. 4.

C. Steady-State Analysis of Proposed Converters

The first proposed converter can be described by the following relations, utilizing the operation modes displayed in Fig. 2(a) and (c)

$$\begin{cases} v_{L1,I} = V_i + V_{C3} - V_{C2} \\ v_{Lg1,I} = \frac{V_{C3} - V_{C1}}{n_{21} - 1} \\ v_{L2,I} = V_i \end{cases}. \tag{1}$$

Using the second operating mode demonstrated in Fig. 2(b), the relations listed below can be acquired for the first proposed

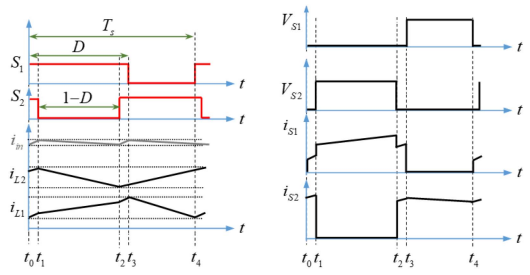


Fig. 4. Theoretical waveforms.

converter

$$\begin{cases} v_{L1,II} = V_i \\ v_{Lg1,II} = \frac{V_{C3}-V_{C1}}{n_{21}-1} \\ v_{L2,II} = V_i + V_{C2} - V_{C3} \end{cases}. \tag{2}$$

Using the fourth operating mode demonstrated in Fig. 2(c), the relationships listed below can be acquired for the first proposed converter

$$\begin{cases} v_{Lg1,IV} = \frac{-V_{C1}}{n_{21}} \\ v_{L1,IV} = V_i + \frac{V_{C1}}{n_{21}} - V_{C2} \\ v_{L2,IV} = V_i \end{cases}. \tag{3}$$

By applying the volt-second balance to (1) through (3), the following equations can be calculated:

$$< v_{Lg1} >= 0 : V_{C3} = \frac{-V_{C1}.(n_{21}-1+D)}{D.n_{21}} \tag{4}$$

$$< v_{L1} >= 0 : V_i - D.V_{C2} + (2.D-1).V_{C3} + \frac{1-D}{n_{21}}.V_{C1} = 0 \tag{5}$$

$$< v_{L2} >= 0 : V_{C3} = \frac{(1-D).V_{C2} - V_i}{1-D}. \tag{6}$$

Using (4) to (6), the voltage across capacitors C_1, C_2, and C_3 is calculated as follows:

$$V_{C1} = \frac{n.D.V_i}{(n-1).(1-D)^2} \tag{7}$$

$$V_{C2} = \frac{2.(n-1)-(n-2).D}{(n-1).(1-D)^2} V_i \tag{8}$$

$$V_{C3} = \frac{n-1+D}{(n-1).(1-D)^2} V_i. \tag{9}$$

To the equivalent circuit of the second operational state, as shown in Fig. 2(b), the output voltage of the initial converter design is calculated using the following equation:

$$V_o = V_i - v_{L2,II} + V_{C2} + v_{Lm,II}. \tag{10}$$

By substituting the relations $v_{L2,\mathrm{II}}$ and $v_{Lm,\mathrm{II}}$ from (2) into (10), the resulting relationships can be expressed as follows:

$$V_o = \frac{n_{21}.V_{C3} - V_{C1}}{n_{21}-1}. \tag{11}$$

By substituting the voltages of capacitors C_1 and C_3 from (7) and (8), respectively, into (11), the following equation is calculated for the output voltage of the first proposed converter:

$$V_o = \frac{n.V_i}{(n-1).(1-D)^2}. \tag{12}$$

Based on (12), the voltage amplification of the proposed converter and the range of its duty cycle are determined as follows:

$$G = \frac{V_o}{V_i} = \frac{n}{(n-1).(1-D)^2} \quad 0 \le D \le 1. \tag{13}$$

The voltage across the switches of the proposed converter is calculated using the equivalent circuit of the second and fourth operating modes, with the following equations provided:

$$V_{S2} = V_i - v_{L2,II}. \tag{14}$$

By substituting $v_{L2,\mathrm{II}}$ from (2), the voltage stress across switch S_2 is calculated as follows:

$$V_{S2} = V_{C3} - V_{C2}. \tag{15}$$

The voltage stress on switch S_2 can be determined by replacing the voltages of capacitors C_2 and C_3 from (8) and (9) into (15) about the input voltage

$$V_{S2} = \frac{V_i}{1-D}. \tag{16}$$

Using KVL on the equivalent circuit in the fourth operational mode allows for the calculation of the voltage stress on switch S_1, as shown in

$$V_{S2} = -V_{C1} + (1-n).v_{Lm,IV} + V_{C3}. \tag{17}$$

By substituting V_{C1}, V_{C3}, and $v_{Lm,\mathrm{IV}}$ from (7), (9), and (3), respectively, into (17), the voltage stress across switch S_1 can be calculated as follows:

$$V_{S1} = \frac{V_i}{(1-D)^2}. \tag{18}$$

The maximum voltage stress experienced by diode D_1 can be determined by analyzing the equivalent circuit in the first operating mode, as shown in Fig. 2(a)

$$V_{D1} = V_{C1} + n.\ v_{Lm,I}. \tag{19}$$

By substituting V_{C1} and $v_{Lm,I}$ from (7) and (1) respectively, into (20), the maximum voltage stress across diode D_1 is calculated according to the following equation:

$$V_{D1} = \frac{n.V_i}{(n-1).(1-D)^2}. \tag{20}$$

The highest voltage that diode D_2 can withstand can also be determined by analyzing the equivalent circuit of the first operating mode, as shown in Fig. 2(a)

$$V_{D2} = V_{C3} - V_{C2}. \tag{21}$$

By substituting V_{C2} and V_{C3} from (8) and (9), respectively, into (21), the maximum voltage stress across diode D_2 is calculated according to the following equation:

$$V_{D2} = \frac{(1-D).V_i}{(1-D)^2}. \tag{22}$$

The highest voltage experienced by diode D_o can be determined by analyzing the equivalent circuit of the fourth operating mode [see Fig. 2(c)].

$$V_{Do} = \frac{(2-D).(n-1)-n}{(n-1).(1-D)^2} V_i. \tag{23}$$

By analyzing the equivalent circuit of the different operation modes of the second proposed converter and utilizing KVL on them, the equations for the second proposed converter can be derived as the equations for the first proposed converter. Consequently, the voltage applied to the capacitors of the second proposed converter can be determined in the following manner:

$$V_{C1} = \frac{n.D.V_i}{(n-1).(1-D)^2} \tag{24}$$

$$V_{C2} = \frac{2.(n-1)-(n-2).D}{(n-1).(1-D)^2} V_i \tag{25}$$

$$V_{C3} = \frac{n-1+D}{(n-1).(1-D)^2} V_i \tag{26}$$

$$V_{C4} = \frac{n}{(n-1).(1-D)^2} V_i. \tag{27}$$

The output voltage of the second proposed converter can be determined by analyzing the equivalent circuit of the fourth operating mode shown in Fig. 3(c), using the following equation:

$$V_o = V_{C1} + V_{C4}. \tag{28}$$

By substituting the relations V_{C1} and V_{C2} from (24) and (27) into (28), the following relation is obtained as

$$V_o = \frac{(n+D).V_i}{(n-1).(1-D)^2}. \tag{29}$$

The voltage gain and duty cycle range of the second proposed converter are calculated using (29)

$$G = \frac{V_o}{V_i} = \frac{n+D}{(n-1).(1-D)^2} \quad 0 \le D \le 1. \tag{30}$$

The voltage stress across the switches of the second proposed converter is determined by utilizing the equivalent circuit of the second and fourth operating modes. This calculation is based on the following equations:

$$V_{S2} = V_i - v_{L2,II}. \tag{31}$$

By substituting $v_{L2,\mathrm{II}}$ from (2), the voltage stress across switch S_2 is calculated as follows:

$$V_{S2} = V_{C3} - V_{C2}. \tag{32}$$

By substituting the voltage of capacitors C_2 and C_3 from (25) and (26) into (32), the voltage stress of switch S_2 is calculated in terms of the input voltage as follows:

$$V_{S2} = \frac{V_i}{1-D}. \tag{33}$$

By applying KVL to the equivalent circuit of the fourth operating mode [see Fig. 3(c)], the voltage stress across the switch S1 is calculated according to the following equation:

$$V_{S2} = -V_{C1} + (1-n)\, v_{Lm,IV} + V_{C3}. \tag{34}$$

By substituting V_{C1}, $V_{C3,}$ and $v_{Lm,IV}$ from (24), (26), and (3), respectively, into (34), the voltage stress across switch S_1 can be calculated according to the following equation:

$$V_{S2} = \frac{V_i}{(1-D)^2}. \tag{35}$$

The maximum voltage stress across the diodes of the second proposed converter can be calculated according to the following equations:

$$V_{D1} = \frac{n.V_i}{(n-1).(1-D)^2} \tag{36}$$

$$V_{D2} = \frac{(1-D).V_i}{(1-D)^2} \tag{37}$$

$$V_{D3} = \frac{n.V_i}{(n-1).(1-D)} \tag{38}$$

$$V_{Do} = \frac{(2-D).(n-1)-n}{(n-1).(1-D)^2}.V_i. \tag{39}$$

D. Calculating the Current Stress Passing Through the Elements

The current passing through the inductors, capacitors, diodes, and switches is determined by analyzing the equivalent circuit of the first converter mode. In situations where the diodes and switches are conducting current, their respective currents can be calculated in the following manner:

$$i_{D1,IV} = \frac{I_o}{1-D} \tag{40}$$

$$i_{D2,II} = \frac{n.I_o}{(n-1).(1-D)^2} \tag{41}$$

$$i_{Do,II} = \frac{I_o}{1-D}. \tag{42}$$

The following equations can be utilized to determine the value of the current passing through the switches:

$$I_{S1} = \frac{(n+1).I_o}{(n-1).(1-D)} \tag{43}$$

$$I_{S2} = \frac{n.I_o}{(n-1).(1-D)^2}. \tag{44}$$

The average current moving through the inductors can also be computed in the following manner:

$$I_{L1} = \frac{n.I_o}{(n-1).(1-D)} \tag{45}$$

$$I_{L2} = \frac{n.D.I_o}{(n-1).(1-D)^2}. \tag{46}$$

The first converter's magnetizing current has an average value of zero

$$I_{Lm} = 0. \tag{47}$$

E. Loss Analysis

Specifically, the losses of power switches (P_{sw}), diodes (P_D), capacitors (P_C), and inductors (P_L) are determined in this section. The switch losses, which include conduction losses and switching losses, can be calculated according to the following equations:

$$P_{\text{SW}} = P_{\text{con}} + P_{\text{switching}}. \tag{48}$$

Using the RMS value of the switch current, the switch conduction losses can be calculated according to the following equation:

$$\begin{aligned} P_{\text{con}} &= R_{\text{DS(on)}}.\left(I_{S1(\text{rms})}{}^2 + I_{S2(\text{rms})}{}^2\right) \\ &= R_{\text{DS(on)}}\left[\frac{D(n+1)^2}{(n-1)^2.(1-D)^2} + \frac{Dn^2}{(n-1)^2.(1-D)^4}\right] I_o{}^2. \end{aligned} \tag{49}$$

The switching losses (P_{on} & P_{off}) of the switches are calculated as follows:

$$P_{\text{switching}} = P_{\text{on}} + p_{\text{off}} = \frac{V_{ds} I_{\text{on}} t_{\text{on}}}{2T_s} + \frac{V_{ds} I_{\text{off}} t_{\text{off}}}{2T_s}. \tag{50}$$

The loss of the diodes is calculated as follows:

$$P_D = V_{fD}.\, I_{D(\text{avg})}. \tag{51}$$

Using the average value of the diodes' current, the losses can be calculated according to the following equation:

$$P_D = V_{fD}.\left(\frac{n + (n-1).D}{(n-1).(1-D)} + 1\right).I_o. \tag{52}$$

The loss of the capacitors is calculated as follows:

$$P_C = \text{ESR}.\, I_{C(\text{rms})}{}^2. \tag{53}$$

Using the RMS value of the capacitors' current, the conduction losses can be calculated as follows:

$$P_C = \text{ESR}.\left(\frac{2.(1-D) + D.n^2}{(n-1)^2.(1-D)^2}\right).I_o{}^2. \tag{54}$$

The loss of the inductors is calculated as follows:

$$P_L = r_L.\, I_{L(\text{rms})}{}^2. \tag{55}$$

Using the RMS value of the inductors' current, the conduction losses of is calculated as follows:

$$P_L = \left(\frac{n.r_{L1}}{(n-1).(1-D)} + \frac{n.D.r_{L2}}{(n-1).(1-D)^2}\right).I_o{}^2 \tag{56}$$

where $R_{\text{DS(on)}}$ refers to the conductive resistance of the switch, V_{fD} is the voltage drop across the diodes in the forward direction, ESR represents the resistance of the capacitor, and r_{L1} and r_{L2} indicate the resistance of the inductors.

III. Design Considerations

DC–DC converters are usually designed for continuous current mode. Therefore, to design these converters for continuous operation, the least value of their elements is calculated for the boundary conduction mode. By calculating the size of the inductors and capacitors for boundary operation, the converter can be designed for continuous operation by applying an engineering factor to the size of the elements.

A. Inductors Design

To determine the minimum size of the inductors, we use the average current flowing through them. Using (2), we can write:

$$v_{L1,II} = L.\frac{di_{L1}}{dt} = V_i. \tag{57}$$

Using (57), we can write

$$i_{L1}(t) = \frac{1}{L}.\int_0^t v_{L1}.dt + i_L(0). \tag{58}$$

Using (58) and considering the initial value of zero for the critical operating state, we can write

$$I_{L1,\text{peak}} = \frac{V_i.(1-D).T_S}{L_1}. \tag{59}$$

By utilizing (59), one can compute the average value of the current flowing through inductor L_1 in the boundary current mode in the following manner:

$$I_{L1B} = \frac{V_i.(1-D).T_S}{2.L_1}. \tag{60}$$

Using (60), the smallest value of inductor L_1 can be computed as below:

$$L_{1,B} = \frac{V_i.(1-D).T_S}{2.I_{LB}}. \tag{61}$$

By replacing the value of the current flowing through inductor L_1 from (46) into (61), we can determine the magnitude of inductor L_1 in the following manner:

$$L_{1B} = \frac{(n-1).(1-D)^2}{2.n.f_s.I_o}V_i. \tag{62}$$

Similarly, the size of the inductor L_2 can be calculated as follows:

$$v_{L2,II} = L.\frac{di_{L2}}{dt} = V_i + V_{C2} - V_{C3}. \tag{63}$$

Using (57), the following equation can be written:

$$L_{2B} = \frac{(V_i + V_{C2} - V_{C3}).(1-D).T_S}{2.I_{L2,B}}. \tag{64}$$

By substituting the current of inductor L_2 from (46) into (64), the size of inductor L_2 can be calculated as follows:

$$L_{2B} = \frac{(n-1).(2-D).(1-D)^2.V_i}{2.n.D.I_o.f_s}. \tag{65}$$

Similarly, from (3) for the magnetizing inductor, the following equation can be written:

$$I_{Lm,\text{peak}} = \frac{V_{C1}.(1-D).T_S}{L_m}. \tag{66}$$

Also, the peak of the magnetizing current in the fourth operating mode can be calculated according to the following equation:

$$i_{Lm,IV} = \frac{1}{1-D}I_o. \tag{67}$$

TABLE I
MINIMUM SIZE OF THE CAPACITORS

$C_1 \geq \frac{(1-D)^2.I_o}{x\,\%.n.D.V_i.f_s}$	$C_2 \geq \frac{n.D.(1-D).I_o}{x\,\%.[2.(n-1)-(n+2).D].V_i.f_s}$
$C_3 \geq \frac{n.(1-D).(2D-1).I_o}{x\,\%.(n-1+D).V_i.f_s}$	$C_3 \geq \frac{n.(1-D).(2D-1).I_o}{x\,\%.(n-1+D).V_i.f_s}$

Using (66) and (67), the minimum size of the magnetizing inductance is calculated as follows:

$$L_{m,\min} = \frac{n.D.V_i}{2.(n-1).I_o.f_s}. \tag{68}$$

B. Capacitors Design

The equation below is utilized to create the capacitors in the proposed converter

$$C \geq \frac{I_{DT}.dt}{\Delta V_C}. \tag{69}$$

Using the capacitor current, the minimum number of capacitors used in the first proposed converter can be calculated according to the following relations are given in Table I.

C. Coupled Inductors Core Design

The first step in selecting the appropriate core is to calculate the geometrical constant of the high-frequency coupled inductor core (Kg), which is calculated as follows:

$$K_g = \frac{A_C^2 W_A}{MLT} \geq \frac{\rho L^2 I_{\max}^2}{r_L K_u B_{\max}^2} \tag{70}$$

where ρ Is the resistivity of the copper, A_C is the effective cross section of the ferrite core, W_A is the core window area, MLT is the mean length turn, K_u is the window utilization factor, and $B_{\max}$ is the maximum flux density.

Using (70), the numerical value of K_g is calculated as follows:

$$K_g \geq 8.71 \times 10^{-13} m^5. \tag{71}$$

According to the value obtained and according to the ferrite core datasheets, the closest core to the coupled inductor is the E-E42×42×15 ferrite core. According to the selected core, the air gap is calculated as follows:

$$l_g = \frac{\mu_0 L I_{\max}^2}{2 B_{\max}^2 A_C} = 1.34mm \tag{72}$$

where μ_0 is the permeability of air.

In the third step, the number of turns is calculated according to the selected core as follows:

$$n = \frac{L I_{\max}}{B_{\max} A_C} = 25. \tag{73}$$

According to the number of turns calculated, the cross-sectional area of the wire is calculated as follows:

$$K_u W_A \geq n A_W \tag{74}$$

where A_W is the wire bare area.

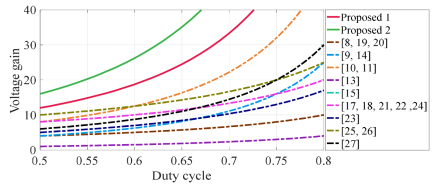


Fig. 5. Voltage gain of the converters.

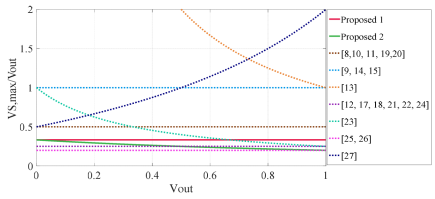


Fig. 6. Maximum switches' normalized voltage stress of the converters.

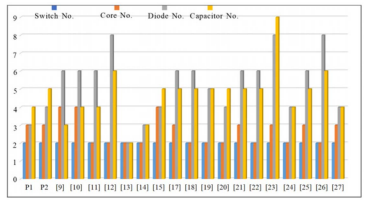


Fig. 7. Number of elements comparison.

IV. COMPARISON BETWEEN DIFFERENT TOPOLOGIES

This section examines the proposed converters in comparison to recently introduced interleaved converters. The comparison evaluates variables like voltage gain, number of components, maximum voltage stress, and common ground. The analysis is conducted using consistent conditions for all converters, showcasing the strengths and weaknesses of each. Table II gives the essential parameters and specifications for this comparison.

Using the voltage gain relations presented in Table I, the voltage gain curves of the converters are plotted in Fig. 5. According to this figure, it is observed that the proposed converters, which are plotted in green and red, produce higher voltage gain under the same conditions compared to other converters presented in [8], [19], [12], [9], [14], [10], [11], [13], [15], [17], [18], [21], [22], [24], [23], [25], [26], and [27].

The voltage stress across the switches of the converters being compared is illustrated in Fig. 6. From the data presented in the figure, it is evident that the voltage stress on the switches of the new converters is lower than that of the converters discussed in previous studies [8], [19], [9], [14], [10], [11], [13], [15], [23], and [27].

The comparison between the proposed converters and other interleaved converters can be seen in Fig. 7 in terms of the number of elements. It is noted that the proposed converters have fewer elements than converters [9], [10], [11], [12], [15], [17], [18], [19], [20], [21], [22], [23], and [25], [26], [27], as shown in the figure. Nonetheless, the proposed converters exhibit a higher

TABLE II
EXAMINING THE DIFFERENCES BETWEEN THE PROPOSED AND OTHER SIMILAR CONVERTERS

Topology	Component					Gain	Winding coefficient	Duty cycle range	V_{Smax}/V_i	V_{Dmax}/V_i	V_{Cmax}/V_i	V_{out} (D=0.6, V_i=30V)	
	S	Core	D	C	Total								
Proposed 1	2	3	3	4	12	$\frac{n}{(n-1)(1-D)^2}$	N_2/N_1	$0 \le D \le 1$	$\frac{1}{(1-D)^2}$	$\frac{n}{(n-1)(1-D)^2}$	$\frac{2-\frac{n-2}{n-1}D}{(1-D)^2}$	562.5 V	Yes
Proposed 2	2	3	4	5	14	$\frac{n+D}{(n-1)(1-D)^2}$	N_2/N_1	$0 \le D \le 1$	$\frac{1}{(1-D)^2}$	$\frac{n}{(n-1)(1-D)^2}$	$\frac{\frac{n}{n-1}}{(1-D)^2}$	787.5 V	No
Zhou et al. [8]	2	2	3	3	10	$\frac{2}{1-D}$	-	$0 \le D \le 1$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	150 V	Yes
Balci et al. [9]	2	4	6	3	15	$\frac{1}{(1-D)^2}$		$0 \le D \le 1$	$\frac{1}{(1-D)^2}$	$\frac{1}{(1-D)^2}$	$\frac{1}{(1-D)^2}$	187.5 V	Yes
Samuel et al. [10]	2	4	6	4	16	$\frac{2}{(1-D)^2}$	-	$0 \le D \le 1$	$\frac{1}{(1-D)^2}$	$\frac{1}{(1-D)^2}$	$\frac{1}{(1-D)^2}$	375 V	Yes
Samuel et al. [11]	2	2	6	4	14	$\frac{2}{(1-D)^2}$	N_2/N_1	$0 \le D \le 1$	$\frac{1}{(1-D)^2}$	$\frac{2}{(1-D)^2}$	$\frac{1}{(1-D)^2}$	375 V	Yes
Samuel et al. [12]	2	2	8	6	18	$\frac{2+2n}{(1-D)^2}$	N_2/N_1	$0 \le D \le 1$	$\frac{1}{(1-D)^2}$	$\frac{2}{(1-D)^2}$	$\frac{2D}{(1-D)^2}$	750 V	Yes
Bussa et al. [13]	2	2	2	2	8	$\frac{1}{D(1-D)}$	-	$0 \le D \le 1$	$\frac{1}{1-D}$	$\frac{1}{D(1-D)}$	$\frac{1}{D(1-D)}$	125 V	Yes
Daneshgar et al. [14]	2	2	3	3	10	$\frac{1}{(1-D)^2}$	-	$0 \le D \le 1$	$\frac{1}{(1-D)^2}$	$\frac{1}{(1-D)^2}$	$\frac{1}{(1-D)^2}$	187.5 V	Yes
Rashid et al. [15]	2	4	4	5	15	$\frac{1}{1-2D}$	-	$0 \le D \le 0.5$	$\frac{1}{1-2D}$	$\frac{1}{1-2D}$	$\frac{1}{1-2D}$	75 V	Yes
Li et al. [17]	2	3	6	5	16	$\frac{2(N+1)}{1-D}$	N_2/N_1	$0 \le D \le 1$	$\frac{1}{1-D}$	$\frac{2N+1}{1-D}$	$\frac{2(N+1)}{1-D}$	300 V	Yes
Li et al. [18]	2	2	6	5	15	$\frac{2(N+1)}{1-D}$	N_2/N_1	$0 \le D \le 1$	$\frac{1}{1-D}$	$\frac{2N+1}{1-D}$	$\frac{2N+1}{1-D}$	300 V	Yes
Prabhala et al. [19]	2	2	5	5	14	$\frac{m+1}{1-D}$	$m \ge 1$	$0 \le D \le 1$	$\frac{1}{1-D}$	$\frac{2}{1-D}$	$\frac{m+1}{1-D}$	225 V	Yes
Baddipadiga and Ferdowsi [20]	2	2	4	5	13	$\frac{2m}{1-D}$	$m \ge 1$	$0 \le D \le 1$	$\frac{1}{1-D}$	$\frac{2m}{1-D}$	$\frac{2m}{1-D}$	225 V	No
He and Liao [21]	2	3	6	5	16	$\frac{2(N+1)}{1-D}$	N_2/N_1	$0 \le D \le 1$	$\frac{1}{1-D}$	$\frac{2(N+1)}{1-D}$	$\frac{2(N+1)}{1-D}$	300 V	Yes
Tseng and Huang [22]	2	2	6	5	15	$\frac{2(N+1)}{1-D}$	N_2/N_1	$0 \le D \le 1$	$\frac{1}{1-D}$	$\frac{2N}{1-D}$	$\frac{2(N+1)}{1-D}$	300 V	Yes
Haixiong et al. [23]	2	3	8	9	22	$\frac{1+3D}{1-D}$	-	$0 \le D \le 1$	$\frac{1}{1-D}$	$\frac{1+3D}{1-D}$	$\frac{1+3D}{1-D}$	210 V	No
Zhou et al. [24]	2	2	4	4	12	$\frac{4}{1-D}$	-	$0 \le D \le 1$	$\frac{1}{1-D}$	$\frac{2}{1-D}$	$\frac{2}{1-D}$	300 V	Yes
Nouri et al. [25]	2	3	6	5	16	$\frac{2(N+1)+n}{1-D}$	N_2/N_1	$0 \le D \le 1$	$\frac{1}{1-D}$	$\frac{2(N+1)+n}{1-D}$	$\frac{2(N+1)+n}{1-D}$	375 V	Yes
Li et al. [26]	2	2	8	6	18	$\frac{3N+2}{1-D}$	N_1/N_2	$0 \le D \le 1$	$\frac{1}{1-D}$	$\frac{2N+1}{1-D}$	$\frac{2N+1}{1-D}$	375 V	Yes
Alizad eh et al. [27]	2	3	4	4	13	$\frac{1+n(1-D)}{(1-D)^2}$	N_2/N_1	$0 \le D \le 1$	$\frac{(1+D)}{(1-D)^2}$	$\frac{1}{(1-D)^2}$	$\frac{2D-D^2+1}{(1-D)^2}$	262.5 V	Yes

voltage gain compared to these other converters. Achieving a higher voltage gain with fewer elements is a crucial aspect for power electronic converters, as it helps reduce costs, volume, and size of the converter.

Among the limitations of the proposed converters, one can mention the limitation of the turn ratio of the coupled inductors, which makes the design and implementation of the coupled inductors more sensitive, and more precision must be used in the design of the coupled inductors.

The efficiency comparison of the proposed converters with the converters presented in [7], [9], [11], [14], [19], [20], [23], and [27] is shown in Fig. 8. According to this figure, it can be seen that the efficiency of the first proposed converter is higher compared to the second proposed converter and other compared

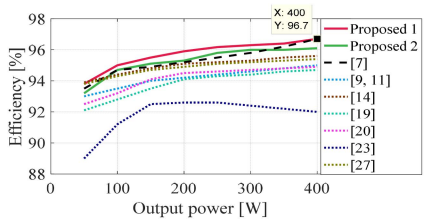


Fig. 8. Efficiency comparison.

TABLE III
PARAMETERS AND ELEMENTS USED IN THE LABORATORY SAMPLE OF THE FIRST PROPOSED CONVERTER

$V_i = 30$ V	$V_o = 562$ V	$f_s = 50$ kHz	$D = 0.6$	$R = 800\ \Omega$
$L_1 = L_2 = 220\ \mu$H	S_1 = IRFP260N	Diodes: MUR860	N_1:N_2 = 1:1.5	

converters, and the power of 400 watts is equal to 96.7%. It can also be seen that the efficiency of the second proposed converter is also higher compared to converters [9], [11], [14], [19], [20], [23], and [27].

V. EXPERIMENTAL RESULTS

An experimental model of the proposed converter was created to validate the theoretical results. The specifications and components used in the lab prototype are given in Table III. A switching frequency of 50 kHz was selected, along with a load resistance of 800 Ω. The converter operates with an input voltage of 30 V and an output voltage of 562 V, delivering a total output power of 400 W. MOSFETs IRFP260n are utilized for the active switches due to their low $R_{\mathrm{ds(on)}}$ and minimal switching loss. The MUR860 diodes, known for their excellent performance and quick recovery, were chosen. Using the design section relations, the minimum values of the inductor and the capacitor used in the experimental sample of the proposed converter are calculated as $L_1 = 22.8\ \mu$H, $L_2 = 53.3\ \mu$H, $L_m = 77.1\ \mu$H, $C_1 = 81.2\ \mu$F, $C_2 = 152.7\ \mu$F, $C_3 = 50.9\ \mu$F, and $C_o = 14.93\ \mu$F.

Fig. 9(a) shows the output voltage of the proposed converter alongside the input voltage. According to the illustration, the measured output voltage is 548 V, indicating a 14 V drop from the theoretical value due to nonideal components. Fig. 9(b) illustrates the voltage across the switches of the proposed converter. The diagram indicates that the voltage across switches S_1 and S_2 is 185 V and 73 V, respectively, differing by 2.5 V and 2 V from their expected values. The voltage across capacitors C_1 and C_2 can be seen in Fig. 9(c), with recorded voltages of 328 V and 479 V, respectively. Additionally, the current flowing through switches S_1 and S_2, as displayed in Fig. 9(d), is 8 and 12 A, respectively.

The graph in Fig. 9(e) illustrates the current flowing through the input inductors. The total input current of the proposed converter is the combination of these two currents, resulting in minimal ripple. The voltage stress across diodes D_1 and D_2 is depicted in Fig. 9(f) as well. According to the graph, the voltage stresses on D_1 and D_2 are 550 V and 74 V, respectively. Upon comparing the expected values with both theoretical and practical results, it is clear that the proposed converter design

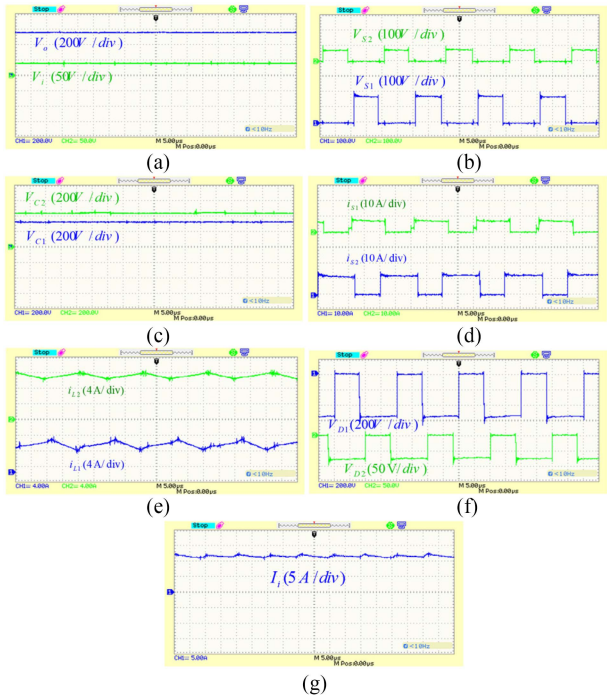


Fig. 9. Experimental results of the first proposed converter. (a) Input and output voltages. (b) V_{S1} and V_{S2}. (c) V_{C1} and V_{C2}. (d) i_{S1} and i_{S2}. (e) i_{L1} and i_{L2}. (f) V_{D1} and V_{D2}. (g) Input current.

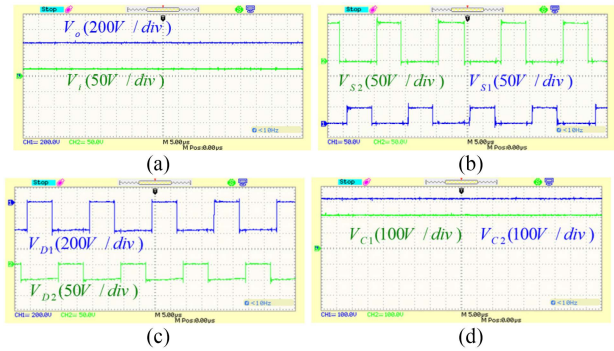


Fig. 10. Experimental results of the second proposed converter. (a) Input and output voltages. (b) V_{S1} and V_{S2}. (c) V_{D1} and V_{D2}. (d) V_{C1} and V_{C2}.

operates efficiently. The input current of the proposed converter is shown in Fig. 9(g). According to this figure, it can be seen that the input current has low ripple and is approximately equal to 1 A, which is one of the important features of this converter.

To verify the correct operation of the second proposed structure, a laboratory sample of this converter has been implemented for a power of 400 W. The goal of implementing the second proposed converter is to produce 525 V at the output from 20 V at the input. To achieve this goal, the second proposed converter must operate at a duty cycle of 0.6. Also, the switching frequency of the second proposed converter is 50 kHz, similar to the first proposed converter.

The output voltage of the proposed converter, alongside its input voltage, is illustrated in Fig. 10(a). As shown in this

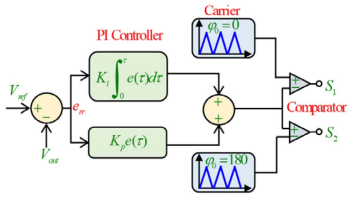
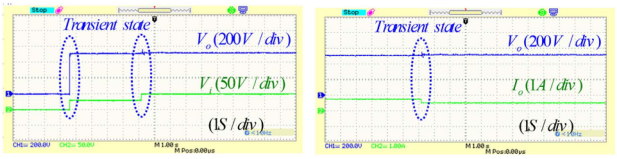


Fig. 11. Control block diagram of the proposed converter.



(a) (b)

Fig. 12. Dynamic response of the proposed converter. (a) Input voltage sudden change. (b) Output load sudden change.

figure, the output voltage of the second proposed converter is 509 V, which is 17 V lower than the ideal value, attributed to the nonideality of the consumed elements. Considering this, it can be concluded that the second proposed structure demonstrates good performance. The voltage stress of the proposed converter switches is also shown in Fig. 10(b). According to this figure, it can be seen that the practical voltage stress of switches S_1 and S_2 is equal to 48 and 123 V, respectively. The voltage stress of diodes $D1$ and $D2$ is shown in Fig. 10(c). The practical voltage stress values of diodes D_1 and D_2 are 358 V and 48 V, respectively. The voltage stress of the capacitors C_1 and C_2 is also shown in Fig. 10(d), which is 120 V and 220 V, respectively.

The pulsewidth modulation technique is utilized in regulating the switches of the converter being proposed. A PI controller is implemented to maintain a constant output voltage from the converter under consideration. The control approach is illustrated in Fig. 11. This diagram displays a control circuit comprising four elements: an adder, a PI controller, a carrier wave, and a comparator. The primary objective of controlling the proposed converter is to ensure a consistent output voltage despite fluctuations in the input voltage. To achieve closed-loop control of the proposed converter, the STM32F407ZGT6-168MHz, equipped with a Cortex-M4 core, is employed for managing the converter.

Using error and iteration, the transfer function is obtained as follows for the proposed converter:

$$K_p + K_i/S = 0.00025 + 0.00003/S. \tag{75}$$

The dynamic response of the proposed converter to sudden changes in input voltage from 30 V to 50 V is shown in Fig. 12(a). The purpose of the closed-loop control of the proposed converter is to stabilize the output voltage at 500 V at a load of 800 Ω. According to this figure, it is observed that with a sudden increase in the input voltage, the output voltage stabilizes at 500 V by passing through the transition state.

The dynamic response of the proposed converter to sudden changes in the output load is shown in Fig. 12(b). The sudden increase in the load causes a sudden decrease in the output current from 0.8 A to 0.5 A. With the sudden decrease in the output current, it is observed that the closed-loop control has worked properly and has stabilized the output voltage of the proposed converter at 500 V.

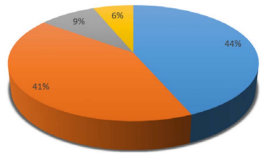


Fig. 13. Distribution of losses among the components of the proposed converter.

Using the datasheet for the switch and the diodes in the proposed converter prototype, the voltage drops for the switch in the on state and the diodes are 1.1 and 1.2 V, respectively. Additionally, the datasheet for the G20N50C indicates that the static drain-to-source on-resistance of the switch is 0.04 Ω. The parasitic resistances of the capacitors and inductors are considered to be 0.05 and 0.1 Ω, respectively. Using the datasheet values and (48)–(61), the loss distribution of the proposed converter can be calculated. Fig. 13 shows the proposed converter's loss distribution. According to the figure, the losses are divided into the following categories: switches account for 44%, diodes 41%, inductors 6%, and capacitors 9%. It should be emphasized that the laboratory prototype of this converter achieves an efficiency of 96.7%.

VI. Conclusion

A family of quasi-impedance source dc–dc converters with an interleaved structure designed for high-voltage applications is presented in this article. The proposed structures were analyzed in terms of theoretical relations. These structures have minimal input current ripple and are suitable for high-power operation, even when utilizing impedance source cells. The decreased input current leads to smaller input inductors, making them ideal for renewable energy applications. Additionally, the proposed structures exhibit low voltage and current stresses on switches. This reduction in voltage stresses improves efficiency and enables more compact component sizing. Components in the proposed structure were designed, and their minimum values were calculated to validate this claim. The proposed converters were also compared theoretically with similar converters, showing that they achieve higher voltage gain with fewer elements and reduced voltage and current stress on their switches. Furthermore, the first proposed converter demonstrated high efficiency and a common ground. A laboratory prototype of the first proposed converter was implemented with an output power of 400 watts and an efficiency of 96.7%, confirming the theoretical findings.

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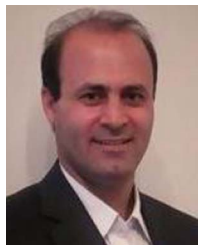

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