Modeling and Stability Analysis of Sustained Oscillations During the Miller Region for Medium-Voltage SiC MOSFET Power Modules

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***Abstract*—Sustained oscillations during the Miller region have been observed in a 10 kV SiC MOSFET power module, which can reduce the robustness or even prevent the proper operation of the module. These oscillations become worse with increased parasitic gate-to-baseplate capacitance. However, the underlying oscillation mechanism involving the parasitic capacitance is still unclear in previous studies. To fill this gap, this article develops the small-signal model considering parasitic capacitances in a half-bridge circuit. Then, the stability analysis of the sustained oscillation in a 10 kV SiC MOSFET power module is conducted. The developed theoretical model agrees well with the experimental results. Finally, possible solutions for mitigating sustained oscillations are provided.**

***Index Terms*—10 kV silicon carbide (SiC) metal oxide semiconductor field effect transistor(MOSFET), grounding, power module, stability analysis, sustained oscillations.**

I. Introduction

RENEWABLE energy sources are central to the shift toward less carbon-intensive and more sustainable energy systems [1]. In recent years, generation capacity has grown rapidly, driven by green transition policies and significant cost reductions, especially for solar photovoltaic and wind power [2]. In addition, with increased electric power output, adopting higher system voltage level has become one of common solutions [3]. This is because higher system voltages help reduce energy losses during transmission and enhance grid compatibility [4], [5], [6].

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As the system voltage increases, silicon carbide (SiC) devices are attracting widespread attention due to their ability to overcome the blocking voltage limitations of silicon devices [7]. In past ten years, Wolfspeed demonstrated medium-voltage (MV) SiC metal oxide semiconductor field effect transistors (MOSFETS) in 10 and 15 kV voltage classes, with reduced switching losses due to dv/dt values up to 250 V/ns [8], [9], [10]. These MV SiC MOSFETs can be directly used for MV system without the complex series connection resulting in a simpler and more reliable converter structure [11], [12], [13], [14].

More electrical field energy is stored in parasitic capacitances at MV systems due to $E = \frac{1}{2}CV^2$ [15]. Consequently, the impact of parasitic capacitances in MV converters becomes more significant, leading to considerable power loss in the power modules [16]. Moreover, during the switching transitions with high dv/dt, capacitive couplings in the converter system can generate high-frequency displacement currents that may circulate within the system [17]. Therefore, more emphasis is placed on parasitic capacitances in layout considerations of MV power modules [15], as opposed to parasitic inductances in low-voltage (LV) module layouts [18].

Our conference paper [19] identifies that the parasitic gate-baseplate (BP) capacitance introduces sustained oscillations during the Miller region in a half-bridge 10 kV SiC MOSFET power module. These oscillations become even worse with increased gate-BP capacitance [20]; however, the underlying oscillation mechanism is still unclear. Similar oscillation waveforms are observed in LV wide bandgap devices, where these oscillations are categorized into parasitic *LC* oscillations and false triggering oscillations [21]. The coupled parasitic *LC* oscillations in the power loop and driver loop are a well-understood phenomena, where passive components cause unintended resonance [22]. False triggering oscillations occur when the reverse recovery current of the body diode in the inactive switch, combined with the common source inductance, causes false turn-ON of inactive switch during the Miller region of active switch [23].

However, the above oscillation mechanisms do not consider the grounded BP and the grounding loop, which are inconsistent with the sustained oscillations observed in [19]. To address the sustained oscillations, A ceramic BP-less 10 kV power module concept is proposed to eliminate the gate-BP capacitance,

demonstrating that the oscillations are no longer sustained [19]. This BP-less power module shows promising potential, however it is still an immature technology, with many constraints, e.g., mechanical strength of the ceramic, in comparison to conventional BP assembled power modules [24]. Furthermore, for conventional MV modules, grounding the BP is still essential to provide a safe path of least resistance in the MV system [25]. Therefore, it is necessary to further investigate the oscillation mechanism and propose possible mitigation solutions.

To address this research gap, the major contributions of this work are as follows.

1) The small-signal model, considering parasitic capacitances and inductances in a half-bridge power module, is developed to investigate the oscillation mechanism. The system stability analysis for the sustained oscillations during the Miller region is conducted.

2) The influence of circuit parameters on stability is discussed, and potential solutions for mitigating sustained oscillations are provided.

The rest of the article is organized as follows. Section II formulates the research problem, reviewing the phenomenon of sustained oscillations during the Miller region reported in [19]. Section III theoretically derives the small-signal model of a half-bridge power module, incorporating both parasitic capacitance and inductance from transistors and power module layout. Section IV reveals the influence of circuit parameters on the sustained oscillation, verified by experiments using 10 kV SiC MOSFET power module. Finally, Section V concludes this article and summarizes the possible solutions for mitigating the observed sustained oscillations.

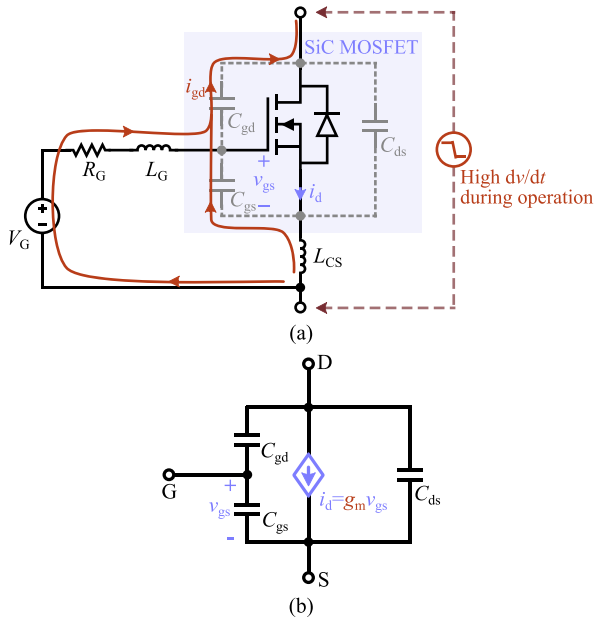


Fig. 1. Causes of oscillation. (a) Miller current i_{gd} introduced by high dv/dt during the Miller region. (b) Small-signal model of SiC MOSFET.

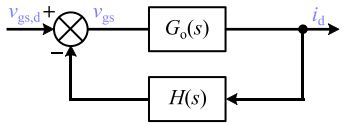


Fig. 2. Closed-loop feedback diagram of an SiC MOSFET during the Miller region.

II. Sustained Oscillations during the Miller Region

A. Causes of Sustained Oscillations

A simplified circuit model of SiC MOSFET and the corresponding small signal model are presented in Fig. 1. As illustrated in Fig. 1(a), during the Miller region, the SiC MOSFET is acting as a voltage-controlled current source [26]. The drain-source current i_d depends on the gate-source voltage v_{gs}. The transfer characteristic is

$$i_d = g_m v_{gs} \tag{1}$$

where g_m is the transconductance.

During the Miller region, high dv/dt induces high-frequency displacement current i_{gd} through the gate-drain capacitances C_{gd}. This displacement current flows through the gate driver, gate-source capacitor C_{gs}, and common source inductances L_{CS}, causing fluctuations in the gate-source voltage v_{gs}. Consequently, v_{gs} fluctuates, the drain-source output current i_d also fluctuates, passing through L_{CS} and feeding back to the voltage slew rate.

This process forms a closed-loop feedback system, as shown in Fig. 2. The disturbance signal of the gate-source voltage, $v_{gs,d}$, is induced by gate driver. $G_o(s)$ represents the transconductance, while $H(s)$ is the feedback transfer function. In this closed-loop feedback system, sustained oscillations occurs when the closed-loop feedback system satisfies the Barkhausen stability criterion [27].

B. Impacts of Parasitic Gate-BP Capacitance

Regarding state-of-the-art research, Fig. 1 presents a general circuit model used to evaluate system stability. However, this model does not account for the grounded BP of the power module. Meanwhile, Kjgaard et al. [19] pointed out that the parasitic gate-BP capacitance introduce sustained oscillations during the Miller region in a half-bridge 10 kV SiC MOSFET power module, as shown in Fig. 3. Moreover, these sustained oscillations become more severe with increased gate-BP capacitance [20]. Therefore, modeling the sustained oscillation during the Miller region while considering the impacts of the parasitic gate-BP capacitance is a clear research gap and an important area for further investigation.

Similar to C_{gd}, the gate-BP capacitance $C_{\sigma GH}$ also introduce a feedback path in the high-side (HS) MOSFET, as depicted in Fig. 4. During the Miller region, the high-frequency displacement current induced by dv/dt flows through C_{gs}, $C_{\sigma GH}$, and the output capacitance of the low-side (LS) MOSFET. These current paths introduce another closed-loop feedback loop between dv/dt and v_{gs}, potentially leading to the sustained oscillations observed in [19].

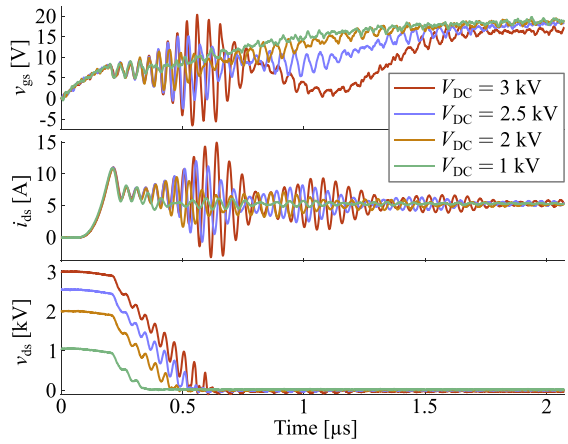


Fig. 3. Turn-ON switching waveforms at customized module with 33.5 pF gate-BP capacitance.

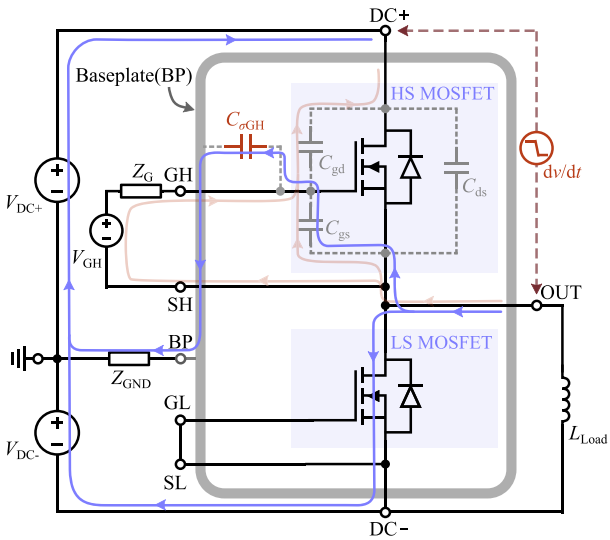


Fig. 4. HS DPT circuit schematic illustrating the high-frequency current paths at grounded BP.

III. Small-Signal Model in a Half-Bridge Power Module

To further explain the oscillation mechanism, this section will present the small-signal model in a half-bridge power module, accounting for parasitic capacitances.

A. Circuit Schematic

The HS double-pulse test (DPT) circuit, as shown in Fig. 5, is selected to study the impacts of the parasitic gate-BP capacitance $C_{\sigma GH}$. Fig. 5 includes active HS MOSFET, inactive LS MOSFET in a half-bridge module, load inductor (L_{Load}), bipolar dc-bus capacitors (C_{DC+} and C_{DC-}), decoupling capacitor ($C_{decouple}$), HS gate driver (V_{GH} and R_G), and relevant parasitic parameters.

Compared to previous research [21], [22], [28], [29], the major different part here is the inclusion of the BP, the corresponding parasitic capacitances ($C_{\sigma+}$, $C_{\sigma GH}$, $C_{\sigma OUT}$, $C_{\sigma GL}$, and $C_{\sigma-}$), and grounding impedance networks (R_{GND} and L_{GND}).

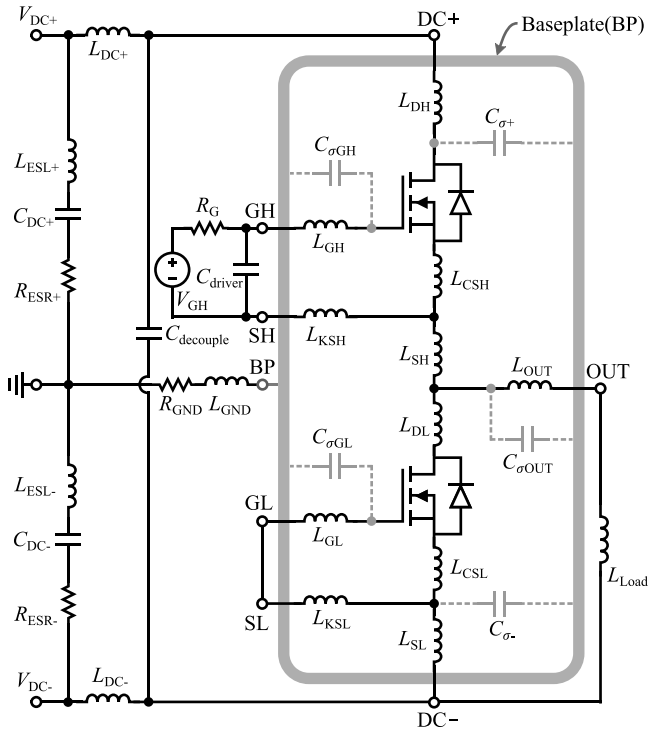


Fig. 5. HS DPT circuit.

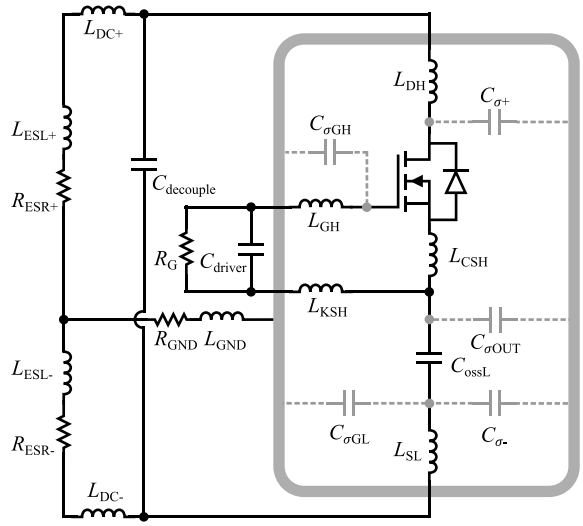


Fig. 6. Small-signal circuit in a half-bridge power module.

B. Circuit Equivalent Transformation

Due to nature nonlinear of the transconductance and capacitance of MOSFETs, directly establishing a large-signal model to analyze circuit system stability is complex. Instead, a linearized small-signal model enables the application of linear system stability theory to evaluate transient operating conditions [26]. Based on the switching transient waveform, an unstable operating point can be selected for modeling and analysis. Fig. 6 shows the small-signal circuit derived from Fig. 5. In the small-signal model, the dc-bus capacitors C_{DC+} and C_{DC-}, and the gate driver V_{GH} are considered short circuits, while the load inductor L_{Load}

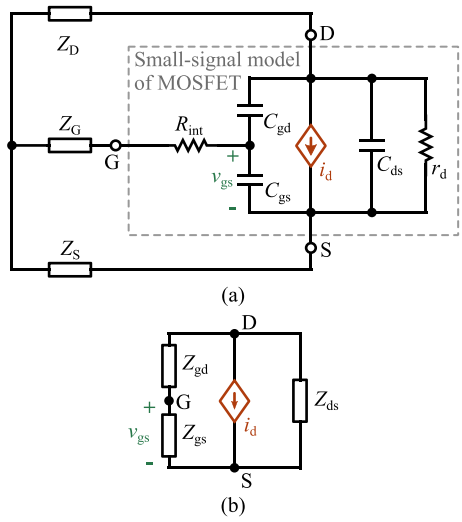


Fig. 7. Circuit equivalent transformation for deriving the feedback transfer function (detailed step-by-step simplification process is given in Appendix).

is treated as open circuit. The LS MOSFET is inactive, and can therefore be simplified to the output capacitance C_{ossL}, thus omitting any gate-loop parasitics and the parasitic inductances L_{DL}, L_{GL}, L_{KSL}, L_{CSL}, and L_{SH}. Terminal inductances L_{DH}, L_{GH}, L_{KSH}, and L_{SL} are typically in the tens of nanohenries and therefore cannot be ignored. The common-source inductance L_{CSH} is a key parameter between the HS gate loop and power loop, and it also cannot be ignored.

The impedance networks in Fig. 6 can be simplified using multiple star-delta transformations, as detailed in Appendix. The MOSFET can be modeled as a voltage-controlled current source with parasitic parameters. Consequently, as shown in Fig. 7(a), the impedance networks outside the MOSFET is transformed into Z_D, Z_G, and Z_S. The small-signal model of the MOSFET includes a voltage-controlled current source i_d, terminal capacitances C_{gs}, C_{gd}, and C_{ds}, an internal gate resistor R_{int}, and an output resistance r_d.

Furthermore, the circuit in Fig. 7(a) can be further simplified to Fig. 7(b) using star-delta transformation. The impedances Z_{gs}, Z_{gd}, and Z_{ds} are derived as

$$\begin{cases} Z_{gs} = \dfrac{1}{\dfrac{1}{Z_{\Delta GS}} + sC_{gs}} \\ Z_{gd} = \dfrac{1}{\dfrac{1}{Z_{\Delta GD}} + sC_{gd}} \\ Z_{ds} = \dfrac{1}{\dfrac{1}{Z_{\Delta DS}} + \frac{1}{r_d} + sC_{ds}} \end{cases} \tag{2}$$

where

$$\begin{cases} Z_{\Delta GS} = Z_G + R_{int} + Z_S + \dfrac{(Z_G + R_{int})Z_S}{Z_D} \\ Z_{\Delta GD} = Z_G + R_{int} + Z_D + \dfrac{(Z_G + R_{int})Z_D}{Z_S} \\ Z_{\Delta DS} = Z_D + Z_S + \dfrac{Z_D Z_S}{Z_G + R_{int}}. \end{cases} \tag{3}$$

Based on Kirchhoff's laws, the feedback transfer function $H(s)$ is derived as follows:

$$H(s) = -\frac{v_{gs}}{i_d} = \frac{Z_{gs}Z_{ds}}{Z_{gs} + Z_{gd} + Z_{ds}}. \tag{4}$$

The feedforward transfer function $G_o(s)$ is determined by the transconductance g_m of the MOSFET

$$G_o(s) = \frac{i_d}{v_{gs}} = g_m. \tag{5}$$

Therefore, the closed-loop transfer function of Fig. 2 is given by

$$T(s) = \frac{G_o(s)}{1 + G_o(s)H(s)}. \tag{6}$$

The system stability is determined by the poles of the closed-loop characteristic polynomial. The system is unstable if any pole has a positive real part. Once the necessary circuit parameters are known, all poles can be calculated and the stability is assessed [30].

IV. Stability Analysis of 10 kV SiC MOSFET Half-Bridge Power Module

In section III, the relevant small-signal model is developed. It is emphasized that the system stability is determined by the closed-loop transfer function. In this section, the circuit parameters are substituted into the model to analyze the influence on stability.

A. Stability Criteria

To access system stability, the circuit parameters are substituted into the small-signal model. Subsequently, the closed-loop transfer function is evaluated and its poles are computed. While all poles contribute to the system response, the analysis of high-order systems is simplified by applying the concept of pole dominance [31]. The dominant pole, identified as the complex conjugate pole pair $p_1, p_2 = -\sigma \pm j\omega_d$ with the lowest damping ratio ζ, determines the oscillatory behavior of the system. The most important damping ratio ζ is defined as follows:

$$\zeta = \frac{\sigma}{|p_1, p_2|} = \frac{\sigma}{\sqrt{\sigma^2 + \omega_d^2}}. \tag{7}$$

If the damping ratio ζ of the dominant pole pair is positive, then any initial disturbance signal will be attenuated over time, thereby preventing undamped oscillations. Conversely, if the damping ratio ζ is negative, then any disturbance signal $v_{gs,d}$ will result in divergent oscillations over time. Note that it is evident that the sign of ζ depends on the sign of σ from (7). The general equation for an exponentially damped sinusoid can be expressed as

$$v_{osc} = \underbrace{v_{gs,d} \cdot e^{-\sigma \cdot t}}_{\text{amplitude}} \cdot \underbrace{sin(\omega_d \cdot t - \varphi)}_{\text{frequency, phase angle}}. \tag{8}$$

Therefore, according to (8), the oscillation amplitude increases exponentially over time when the circuit system is unstable [32]. Meanwhile conversely, the oscillation amplitude

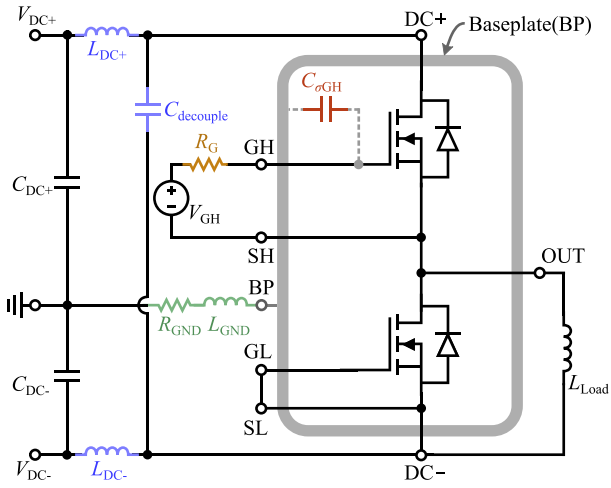


Fig. 8. HS DPT circuit illustrating different loops involved in the sustained oscillation with grounded BP.

decreases exponentially over time when the circuit system is stable.

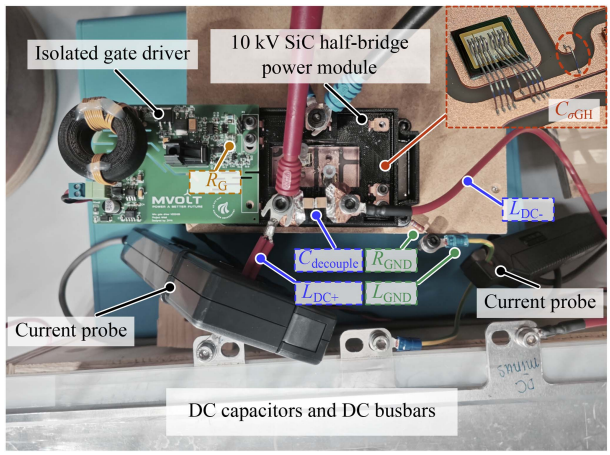
It should be noted that since the Miller region conditions are transient rather than static, even divergent oscillations do not necessarily lead to module failure. This outcome also depends on the damping ratio and oscillation frequency, as well as whether the oscillations diverge quickly enough to cause an issue before the Miller period concludes.

B. Circuit Parameters and Loop Analysis

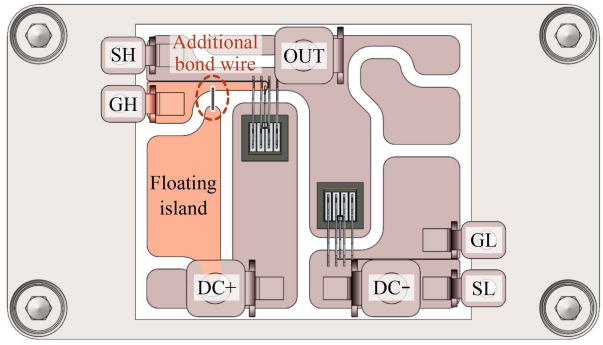
This section takes the 10 kV SiC MOSFET power module, as discussed to examine the influence of circuit parameters in different loops. As illustrated in Fig. 8, four loops are involved in the gate oscillation with a grounded BP.

Fig. 9(a) presents the experimental prototype, highlighting its significant elements. The internal layout of the 10 kV half-bridge SiC MOSFET power module is given in Fig. 9(b), where the additional bone wire and the relevant floating island for revising the gate-BP capacitance $C_{\sigma GH}$ are illustrated.

The corresponding benchmark circuit parameters are detailed in Table I. The dc-bus capacitors, load inductor, parasitic capacitances, and loop elements are measured using the E4990A Impedance Analyzer from Keysight Technologies [33]. The parasitic inductances are extracted using ANSYS Q3D Extractor, while the MOSFET parameters are measured with the B1506A Power Device Analyzer. The gate resistance is selected to obtain suitable switching speed for the device. It plays a critical role in controlling $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$, thereby reducing switching noise and minimizing losses [34]. Typically, $\mathrm{d}v/\mathrm{d}t$ is designed to be between 10 and 50 V/ns [35]. To achieve this, gate resistance is usually a few ohms for LV SiC MOSFETs and tens of ohms for MV SiC MOSFETs [36]. Accordingly, a gate resistance of 50 Ω is chosen for the benchmark circuit, corresponding to a $\mathrm{d}v/\mathrm{d}t$ of



(a)



(b)

Fig. 9. Experimental prototype. (a) Significant elements involved in the sustained oscillation with grounded BP. (b) Internal layout of the 10 kV half-bridge SiC MOSFET power module, illustrating the additional bond wire connection used to adjust the gate-BP capacitance $C_{\sigma GH}$.

TABLE I
BEMCHMARK CIRCUIT PARAMETERS

Category	Symbol	Value	Symbol	Value
DC bus capacitors and load inductor	C_{DC+}, C_{DC-}	50 µF	L_{ESL+}, L_{ESL-}	50 nH
	R_{ESR+}, R_{ESR-}	350 mΩ	L_{Load}	47 mH
Parasitic inductances	L_{DH}	17.9 nH	L_{GH}	17 nH
	L_{CSH}	3.27 nH	L_{KSH}	17.9 nH
	L_{SL}	17.9 nH		
Parasitic capacitances	$C_{\sigma+}$	44.6 pF	$C_{\sigma GH}$	8.7 pF
	$C_{\sigma OUT}$	53.9 pF	$C_{\sigma GL}$	23.2 pF
	$C_{\sigma-}$	21.5 pF	C_{driver}	400 pF
Power loop	L_{DC+}	168 nH	L_{DC-}	168 nH
	$C_{decouple}$	N/A	$R_{C.ESR}$	N/A
Gate loop	R_G	50 Ω	V_{GH}	+20 V/−5 V
Grounding loop	R_{GND}	69 mΩ	L_{GND}	156 nH
10 kV SiC MOSFET @3 kV/70 A	R_{int}	2 Ω	C_{gs}	6.55 nF
	g_m	11 S	C_{gd}	3.86 pF
	r_d	256 Ω	C_{ds}	51.2 pF
LS SiC MOSFET	C_{ossL}	55.06 pF		

approximately 20 V/ns. Due to the nonlinear characteristics of 10 kV SiC MOSFETs, the transconductance g_m varies with drain current, and the capacitances C_{gd} and C_{ds} vary with drain-source voltage. To simplify the model, key parameters are selected at an unstable operating point of 3 kV/70 A, corresponding

TABLE II
MODIFIED CIRCUIT PARAMETERS AT DIFFERENT LOOPS

Loops	Control parameter	Benchmark value	Modified value
Capacitive coupling loop	$C_{\sigma GH}$	8.7 pF	33.5 pF
	g_m	11 S	4.5 S
Power loop (6 different cases listed in Table III)	L_{DC+}, L_{DC-}	168 nH	316 nH, 33 nH
	$C_{decouple}$	N/A	377 pF
	$R_{C.ESR}$	N/A	1.1 Ω
Gate loop	R_G	50 Ω	200 Ω
Grounding loop	R_{GND}	69 mΩ	3.3 Ω, 5.6 Ω
	L_{GND}	156 nH	70 nH, 17 nH

to C_{gd} and C_{ds} at 3 kV and g_m at 70 A, derived from the $g_m - I_d$ and $C - V_{ds}$ curves. Using a small-signal model at this point, rather than a large-signal model, may introduce slight differences with practical waveforms but significantly reduces computational complexity. For higher accuracy, discrete values of transconductance and capacitances can be derived from the $g_m - I_d$ and $C - V_{ds}$ curves, corresponding to specific drain current and drain-source voltage conditions [28], [32].

Based on the benchmark circuit, the stability influence of different loop parameters will be investigated individually. The modified circuit parameters for comparisons across different loop configurations are detailed in Table II.

1) Capacitive Coupling Loop: In a power module, the chip is typically mounted on direct bond copper (DBC) and connected externally via bonding wire, copper trace, and copper bar. The parasitic gate-BP capacitance, $C_{\sigma GH}$, primarily arises between the HS gate copper trace plane and the BP plane. To investigate the influence of $C_{\sigma GH}$, a customized module with an additional bond wire connection from HS gate copper layer to the floating island on the DBC was made, as shown in Fig. 9(b). This modification increases the effective copper area facing the BP from 80 to 385 mm^2. The DBC is built on a 1 mm thick aluminium nitride (AlN) ceramic substrate. The combination of the increased copper area and the dielectric properties of the AlN substrate directly results in an increase in the parasitic capacitance from 8.7 to 33.5 pF.

Fig. 10 illustrates the damping ratio ζ as a function of $C_{\sigma GH}$ and g_m, demonstrating that theoretically, the system becomes more unstable with an increased $C_{\sigma GH}$. In this plot, the transconductance g_m is set to 4.5 S, corresponding to a drain current i_d of 5 A. This g_m value deviates from the benchmark circuit parameter to allow $C_{\sigma GH}$ to be adjusted to a tradeoff value that induces significant oscillations without damaging the module. Consequently, the experimental comparison maintains consistent DPT voltage and current at 3 kV/5 A across different $C_{\sigma GH}$ values, while keeping g_m constant. Fig. 11 presents the 3 kV/5 A DPT waveforms for both the standard 10 kV SiC MOSFET power module and the customized module with increased $C_{\sigma GH}$. With the increased $C_{\sigma GH}$, the negative damping ratio ζ leads to divergent oscillations during the turn-ON process, indicating instability at this operating point. Once the turn-ON process concludes, the oscillations begin to decay, and the system transitions into a stable region due to the changing characteristics of the SiC MOSFET. However, a longer transition time in the unstable region, such as

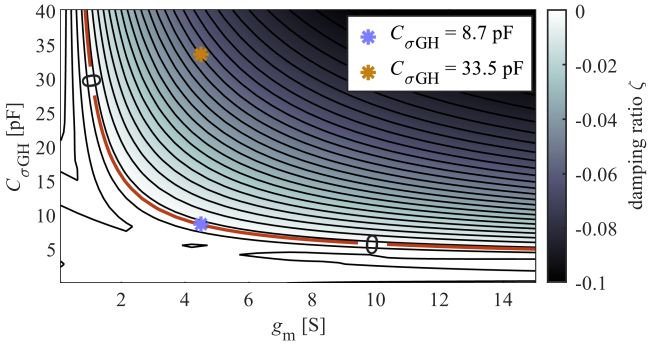


Fig. 10. Calculated damping ratio ζ as a function of $C_{\sigma GH}$ and g_m ($g_m = 4.5$ when $i_d = 5$A).

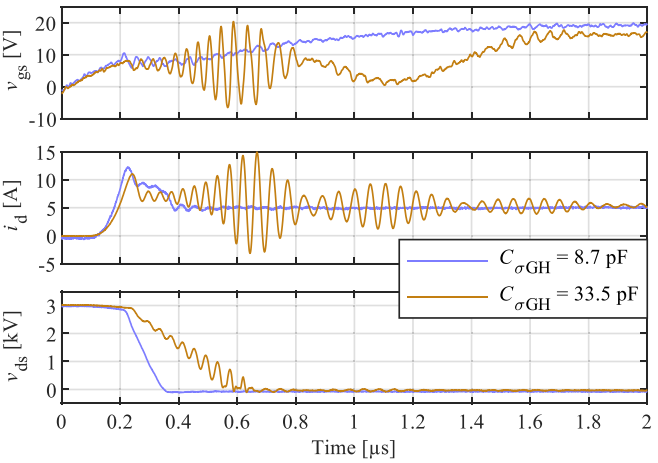


Fig. 11. Experimental turn-ON waveform with different $C_{\sigma GH}$ at 3 kV/5 A, showing alignment with the theoretical model in Fig. 10.

slower switching, results in higher amplitude oscillations over time, potentially damaging the SiC MOSFET device. Therefore, the system should be optimized to prevent entry into the unstable region.

2) Power Loop: In the power loop, three significant parameters are the dc-bus inductances (L_{DC+}, L_{DC-}) and the decoupling capacitor ($C_{decouple}$). Figs. 12 and 13 illustrate the damping ratio ζ as a function of L_{DC+} and L_{DC-}, showing ζ is not linearly related to the inductances of L_{DC+} or L_{DC-}. Fig. 12 shows the damping ratio without the decoupling capacitor $C_{decouple}$, whereas Fig. 13 includes the decoupling capacitor and its associated equivalent series resistance (ESR), with six experimental cases listed in Table III to verify the model. In the latter calculation, to simplify the computational effort, this article assumes that the parasitic inductances L_{DH} and L_{SL} are zero; without this simplification, the numerical values exceed MATLAB's maximum precision.

The 6 kV/70 A DPT waveforms for cases 1–3 are presented in Fig. 14. In case 1, which has symmetrical inductances, the system enters an unstable region, and the oscillation amplitude in the waveform increases slowly over time. Conversely, in cases 2 and 3, the oscillation amplitude decreases over time, indicating that the systems are stable with unsymmetrical inductances. While both cases 2 and 3 display unstable behavior overall, the calculated damping ratio in case 2 is slightly larger than that in case 3. However, experimental results reveal that the oscillations

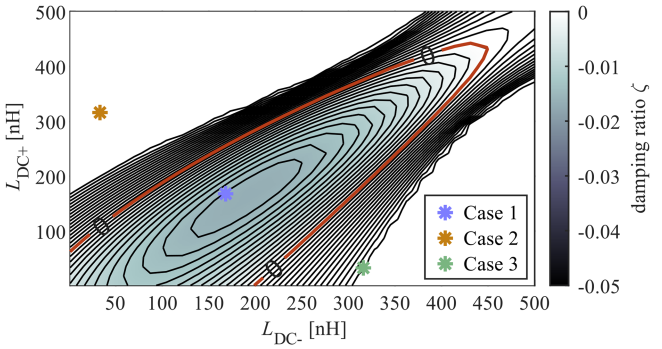


Fig. 12. Calculated damping ratio ζ as a function of L_{DC+} and L_{DC-} without the decoupling capacitor $C_{decouple}$.

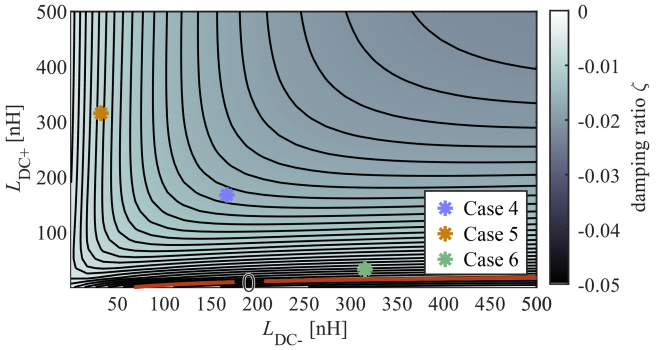


Fig. 13. Calculated damping ratio ζ as a function of L_{DC+} and L_{DC-} with the decoupling capacitor $C_{decouple}$ and corresponding equivalent series resistance $R_{C.ESR}$, assuming that $L_{DH} = L_{SL} = 0$.

TABLE III
EXPERIMENTAL CASES AT POWER LOOP

Cases	L_{DC+}	L_{DC-}	$C_{decouple}$	$R_{C.ESR}$
Case 1 (Benchmark)	168 nH	168 nH	N/A	N/A
Case 2	316 nH	33 nH	N/A	N/A
Case 3	333 nH	316 nH	N/A	N/A
Case 4	168 nH	168 nH	377 pF	1.1 Ω
Case 5	316 nH	33 nH	377 pF	1.1 Ω
Case 6	33 nH	316 nH	377 pF	1.1 Ω

are damped somewhat faster in case 3 than in case 2. This minor inconsistency is likely due to measurement errors in the parasitic parameters as well as the influence of additional parasitic effects not considered in our model.

Two 1 nF/5 kV ceramic capacitors in series are used as the decoupling capacitor. The capacitance $C_{decouple}$ and corresponding equivalent series resistance $R_{C.ESR}$ are measured by impedance analyzer. Theoretically, with the decouple capacitor, the dc-bus inductances will be bypassed during switching transients. Therefore, as shown in Fig. 13, with $C_{decouple}$, the dc-bus inductances in cases 4–6 are closed to zero. The experimental waveforms are given in Fig. 15. The oscillation amplitudes in all three cases are divergent. Consequently, the decoupling capacitor in the power loop leads to symmetrical inductances, thus entering an unstable region.

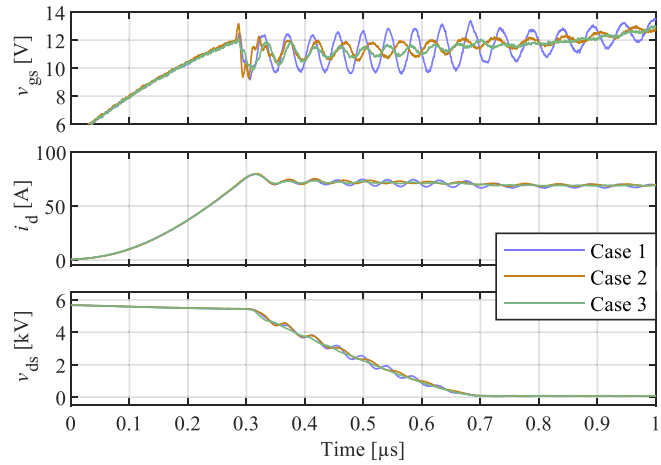


Fig. 14. Experimental turn-ON waveform with different dc-bus inductances at 6 kV/70 A, showing alignment with the theoretical model in Fig. 12 (case 1: $L_{DC+} = L_{DC-} = 168$ nH, case 2: $L_{DC+} = 316$ nH, $L_{DC-} = 33$ nH, and case 3: $L_{DC+} = 33$ nH, $L_{DC-} = 316$ nH).

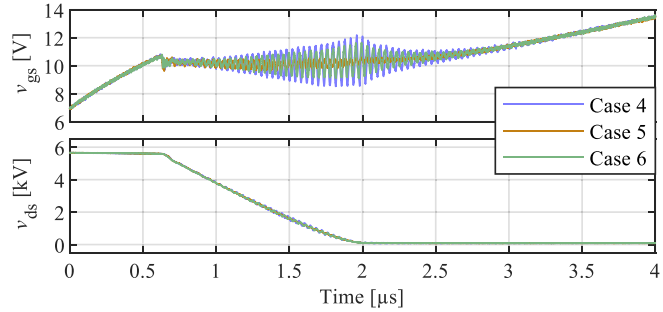


Fig. 15. Experimental turn-ON waveform with decoupling capacitor $C_{decouple}$ and different dc-bus inductances at 6 kV/70 A, showing alignment with the theoretical model in Fig. 13 (case 4: $L_{DC+} = L_{DC-} = 168$ nH, case 5: $L_{DC+} = 316$ nH, $L_{DC-} = 33$ nH, and case 6: $L_{DC+} = 33$ nH, $L_{DC-} = 316$ nH).

3) Gate Loop: Generally, the gate resistor is a crucial component for adjusting switching performance and mitigating ringing in the gate loop. It is necessary to evaluate the influence of the gate resistor on sustained oscillations during the Miller region introduced by a grounded BP. Fig. 16 depicts the damping ratio ζ as a function of the gate resistor R_G and g_m, indicating that, theoretically, system stability is not significantly dependent on R_G.

Fig. 17 shows the DPT waveforms with 50 and 200 Ω gate resistor at 6 kV/70 A, where the switching speeds are 15 and 4 V/ns, respectively. Both waveforms enter unstable regions, resulting in undamped oscillation. Meanwhile, the oscillation amplitude slowly increases because the damping ratio is very close to zero. Therefore, the waveform with 50 Ω exhibits a faster switching speed and shorter Miller region period, allowing it to ride through the unstable region within ten oscillation cycles, thereby limiting the oscillation amplitude. In contrast, the longer transition time of the 200 Ω resistor leads to higher amplitude oscillations over time.

However, it is important to note that the gate loop also forms an *LC* resonant circuit involving the parasitic inductances (L_{GH} and L_{KSH}) and capacitances (C_{gs} and C_{gd}). When R_G is low,

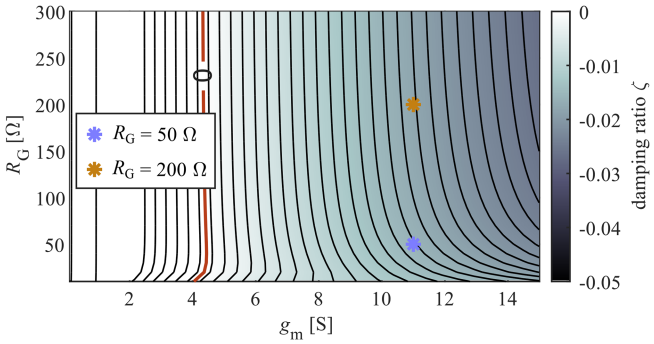


Fig. 16. Calculated damping ratio ζ as a function of R_G and g_m.

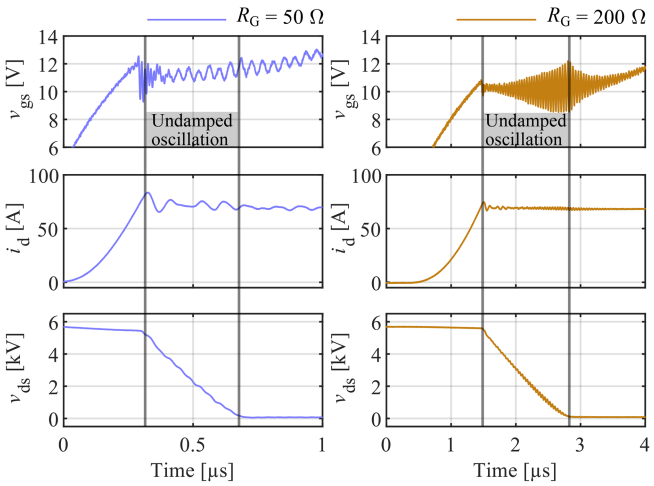


Fig. 17. Experimental turn-ON waveform with decoupling capacitor and different R_G at 6 kV/70 A, showing alignment with the theoretical model in Fig. 16.

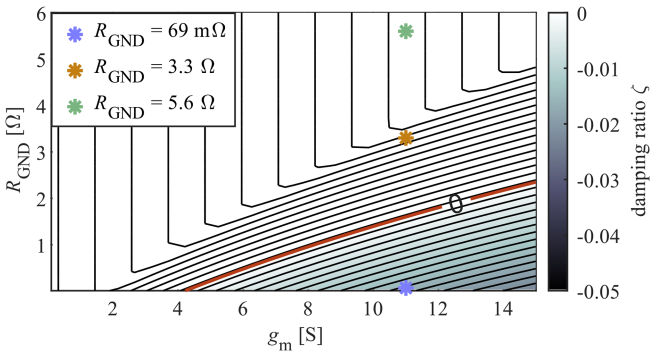


Fig. 18. Calculated damping ratio ζ as a function of R_{GND} and g_m.

these *LC* oscillations become more pronounced, which can lead to high-frequency ringing that may damage the power module. Therefore, while lower gate resistance can help limit sustained oscillations by reducing the time spent in the unstable region, it may also exacerbate *LC* ringing. A careful balance must be achieved to optimize both switching speed and damping of high-frequency oscillations.

4) Grounding Loop: Kjgaard et al. [19] pointed out that the oscillations are no longer sustained during the Miller region switching transience with a floating BP. This is because floating BP leads to high-grounding impedance, which can limit the

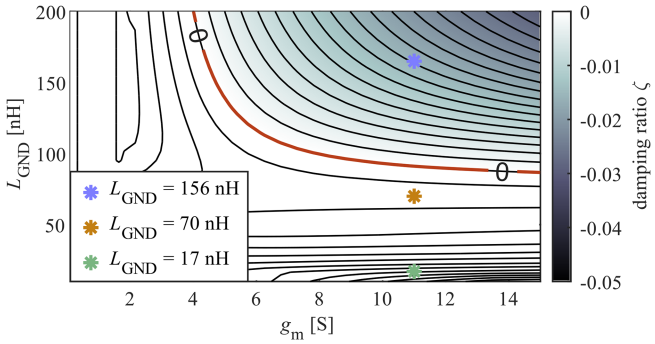


Fig. 19. Calculated damping ratio ζ as a function of L_{GND} and g_m.

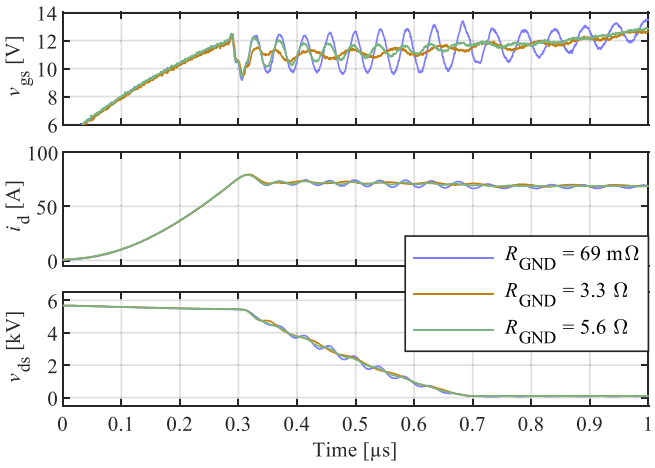


Fig. 20. 6 kV/70 A DPT experimental waveform with different R_{GND} at $L_{GND} = 156nH$, showing alignment with the theoretical model in Fig. 18.

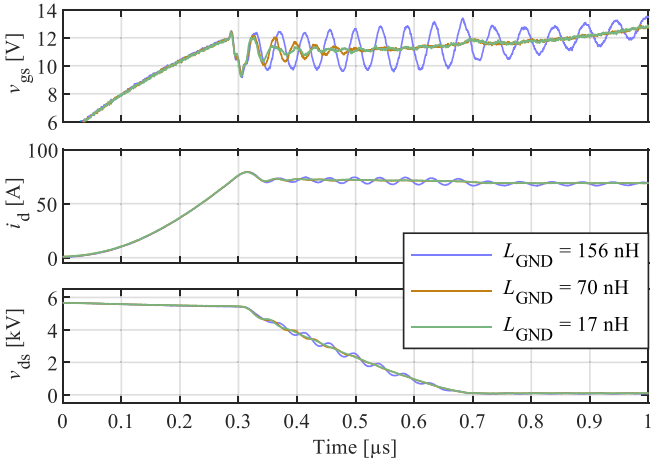


Fig. 21. 6 kV/70 A DPT experimental waveform with different L_{GND} at $R_{GND} = 69$ mΩ, showing alignment with the theoretical model in Fig. 19.

high-frequency displacement current induced by $C_{\sigma GH}$. However, since a floating or high-impedance grounding configuration introduces potential safety risks due to the indirectly grounded heatsink [25], our study focuses exclusively on configurations with direct grounding or low-impedance grounding.

In the grounding loop, the grounding resistor R_{GND} and grounding inductance L_{GND} construct the path that the high-frequency oscillation current flows between the BP and the

TABLE IV
POSSIBLE SOLUTIONS FOR MITIGATING SUSTAINED OSCILLATIONS DURING THE MILLER REGION

Effect on circuit	Practical modifications	Implementation	Costs	Trade-off considerations
Reducing parasitic gate-baseplate capacitance $C_{\sigma GH}$	Narrow gate-track width on DBC	Easy	Low	Thin trace introduces higher leakage inductance, causing crosstalk issues
	Increase substrate layer thickness	Easy	Low	Weakens thermal peformance
	Elevated gate circuit board above DBC	Difficult	High	N/A
	Baseplate-less power module	Difficult	High	Cutting-edge concept, but its reliability remains unproven
Asymmetrical DC bus inductances	Apply asymmetrical DC busbars	Medium	Low	Increased power loop inductance causes voltage overshoot during switching
	Implement unipolar DC bus architecture	Easy	High	Requires additional insulation
Faster turn-on switching speed	Lower gate resistance	Easy	Low	Additional gate loop ringing, more severe EMI issue with higher dv/dt values
	Adopt multi-level gate driver	Medium	Medium	More severe EMI issue with higher dv/dt values
Grounding with damping resistor	Insert resistor between heatsink and ground	Easy	Low	Potential safety risks due to the indirectly grounded heatsink
Low inductance grounding	Reduce grounding inductance from heatsink to DC bus	Difficult	Medium	More compact system architecture is required, limited design flexibility

ground. Therefore, these two key parameters are crucial for system stability. The damping ratio ζ as functions of these parameters and g_m are shown in Figs. 18 and 19, respectively. It is evident that the grounding resistor R_{GND} can significantly dampen the sustained oscillations, while increased grounding inductance L_{GND} makes the sustained oscillations worse.

The DPT waveforms with different values of R_{GND} and L_{GND} are shown in Figs. 20 and 21, respectively. The experimental results align well with the theoretical model. With a larger R_{GND} or a smaller L_{GND}, the damping ratio ζ increases, causing the oscillation amplitude to decay faster.

The above experimental results for the presented loops agree well with the small-signal model.

V. POSSIBLE SOLUTIONS FOR MITIGATING OSCILLATIONS

Section III introduces the small-signal model of sustained oscillations during the Miller region, followed by the stability analysis and corresponding experimental verification in section IV. Based on the experimental results, this section provides some possible solutions for mitigating oscillations in practical applications. Furthermore, the relevant implementation complexity, associated costs, and tradeoff considerations are discussed. A summary of the possible solutions are provided in Table IV.

A. Reducing Parasitic Gate-BP Capacitance

As illustrated in Fig. 10, the circuit system becomes increasingly unstable as the parasitic gate-to-BP capacitance, $C_{\sigma GH}$, increases. Therefore, reducing $C_{\sigma GH}$ is an effective method to prevent the system from entering an unstable region.

In a practical power module, $C_{\sigma GH}$ is formed between the gate copper trace and the BP plane. The simplest methods to mitigate this include narrowing the gate trace width and increasing the substrate layer thickness. However, these approaches lead to increased leakage inductance and thermal resistance, respectively [37], [38]. Another proposed solution is elevating the gate circuit board to reduce parasitic capacitance, as presented in [39], but this requires a complete redesign of the power module layout. A cutting-edge concept, involving a 3D-printed ceramic heatsink with a BP-less design, is introduced in [24], which can potentially eliminate parasitic capacitances altogether. However, its reliability is still unproven.

B. Asymmetrical DC-Bus Inductances

As illustrated in Fig. 12, the circuit system exhibits increased stability as the dc-bus inductances become asymmetrical. Consequently, applying asymmetrical dc busbars between the power module and dc capacitors can effectively reduce sustained oscillations at a lower cost. However, this approach increases power loop inductance, resulting in voltage overshoot during switching, which can reduce the voltage utilization of the power module. An alternative solution is to adopt an unipolar system architecture instead of a bipolar one, where the ground terminal is connected to the V_{DC-} terminal. As shown in Fig. 5, this configuration removes the dc- capacitor C_{DC-} and the corresponding equivalent series inductance and resistance (L_{ESL-} and R_{ESR-}), creating asymmetrical dc-bus inductances. However, this method requires additional insulation in the MV system [40].

C. Faster Turn-On Switching Speed

As illustrated in Fig. 16, system stability is not significantly affected by the gate resistor. However, the gate resistor can

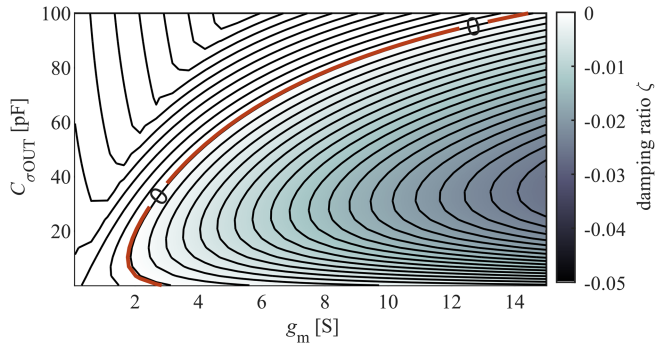


Fig. 22. Calculated damping ratio ζ as a function of $C_{\sigma \mathrm{OUT}}$ and g_{m}.

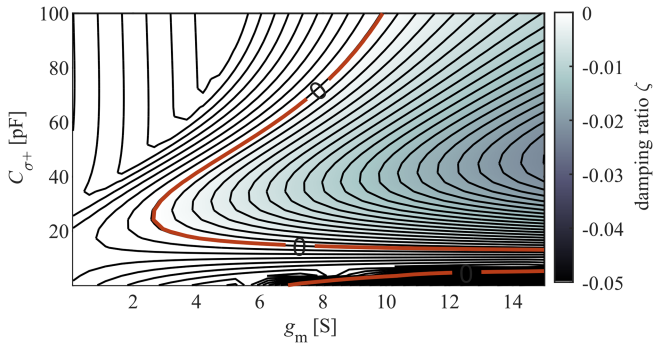


Fig. 23. Calculated damping ratio ζ as a function of $C_{\sigma+}$ and g_{m}.

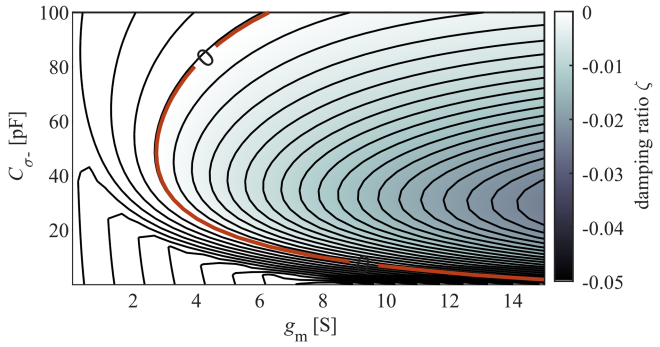


Fig. 24. Calculated damping ratio ζ as a function of $C_{\sigma-}$ and g_{m}.

be used to adjust the switching speed during the transition. A faster switching speed and shorter Miller region period allow the system to quickly ride through the unstable region, which helps limit the increase in oscillation amplitude. Nonetheless, lower gate resistance may introduce additional gate loop ringing. To address this, a multilevel gate driver has been proposed in [41], which temporarily increases the driver output voltage during the switching transition. It is also important to note that electromagnetic interference (EMI) becomes more severe at higher dv/dt or di/dt values when increasing the switching speed. In the case of LV SiC MOSFETs, the tradeoff between suppressing *LC* oscillations within the module power loop and achieving a faster turn-ON switching speed to mitigate sustained oscillations during the Miller region requires more careful consideration.

D. Grounding With Damping Resistor

As illustrated in Fig. 18, the grounding resistor R_{GND} can significantly dampen the sustained oscillations during the Miller region, leading to a more stable circuit system. Since the BP is typically mounted on the heatsink, one solution to mitigate sustained oscillations is to insert a resistor between the heatsink and ground. However, this approach introduces potential safety risks due to the indirectly grounded heatsink. Moreover, ground bounce may also act as noise in the converter system.

E. Low Inductance Grounding

As illustrated in Fig. 19, the circuit system becomes increasingly unstable as the grounding inductance L_{GND} increases. Consequently, reducing grounding inductance from heatsink to dc bus to lower L_{GND} is an effective solution to prevent system instability. However, this solution requires a more compact converter system architecture, thereby limiting design flexibility.

F. Module Power-Loop Layout Optimization

Figs. 22– 24 illustrate the damping ratio ζ as a function of $C_{\sigma \mathrm{OUT}}$, $C_{\sigma+}$, $C_{\sigma-}$, and g_{m}, respectively. The theoretical results demonstrate that increasing the parasitic capacitances improves system stability. However, even when the parasitic capacitances are increased up to 100 pF, the damping ratios remain close to the stability boundary, providing only a limited safety margin. Furthermore, higher parasitic capacitances reduce the available space within the module, and an increased $C_{\sigma \mathrm{OUT}}$ results in additional capacitive losses during operation [16].

Therefore, improving stability by revising the module power-loop layout is not recommended.

G. Discussion

Table IV summarizes ten possible solutions for mitigating sustained oscillations. However, their practical cost-effectiveness depends on specific application constraints. The following discussion outlines the key tradeoffs in different design phases.

1) Power Module Phase: If the design starts from the power module phase, then reducing the parasitic gate-BP capacitance $C_{\sigma \mathrm{OUT}}$ is recommended. Increasing the substrate thickness and narrowing the gate-track width on the DBC are relatively simple solutions, although they may introduce crosstalk and thermal management issues in the power stack. In addition, elevating the gate driver printed circuit board (PCB) has been implemented by Wolfspeed [42] and some customized power modules [10], [39].

2) Power Stack Phase: In industrial designs, power modules are often standardized, limiting access to internal modifications. If the design begins at the power stack phase, then using an asymmetrical dc busbar or increasing switching speed can help mitigate oscillations. However, asymmetrical busbars may increase voltage overshoot and require additional insulation, while higher switching speeds can introduce gate-loop ringing and EMI concerns.

3) Power Converter System Phase: For applications where the power stack is treated as a standardized unit (e.g., half-bridge,

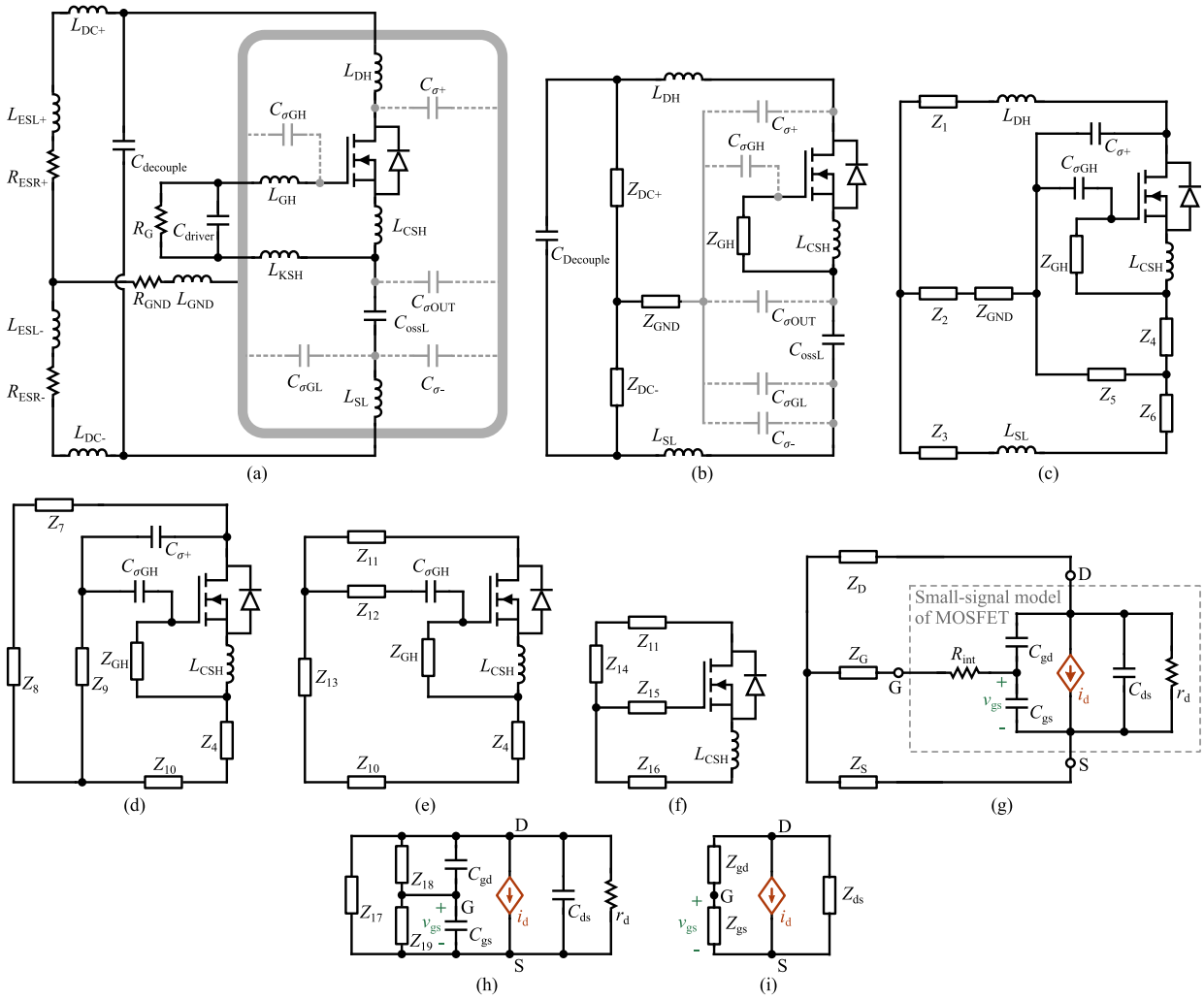


Fig. 25. Step-by-step circuit transformation to obtain equivalent circuit in the form of enabling stability criteria method analysis.

full-bridge, or three-phase circuits), modifying the grounding impedance is an effective solution. Inserting a resistor between the heatsink and ground or reducing the grounding inductance between the heatsink and busbar can help suppress oscillations without revising the power stack itself.

In practical applications, it is also essential to incorporate design margins to ensure robust system stability. Although the stability curves (the damping ratio curves) transition smoothly without abrupt changes, providing additional design margin by keeping the operating point safely away from the zero damping ratio can enhance flexibility in converter layout and account for component tolerances and degradation in power modules.

VI. Conclusion

This article investigates the underlying mechanisms of sustained oscillations during the Miller region in MV SiC MOSFET power modules. A small-signal model is developed in a half-bridge configuration that includes parasitic capacitances to analyze the circuit system stability. The analyses reveal that four key loops contribute to the sustained oscillations related to the grounded BP: the capacitive coupling loop, power loop, gate loop, and grounding loop. Stability analyses for each of these loops have been conducted and experimentally validated. Based on these results, this article provides possible practical solutions for mitigating sustained oscillations to enhance the stability and performance of SiC MOSFET power modules.

Appendix

The detailed impedance network simplification process from Figs. 6 and 7 will be explained in this section. The step-by-step circuit schematics are presented in Fig. 25.

Fig. 25(a) is the small-signal model derived from DPT circuit. Then, in Fig. 25(b), series impedance can be combined by

$$Z_{\mathrm{DC+}} = sL_{\mathrm{DC+}} + sL_{\mathrm{ESL+}} + R_{\mathrm{ESR+}} \tag{9}$$

$$Z_{\mathrm{DC-}} = sL_{\mathrm{DC-}} + sL_{\mathrm{ESL-}} + R_{\mathrm{ESR-}} \tag{10}$$

$$Z_{\mathrm{GND}} = sL_{\mathrm{GND}} + R_{\mathrm{GND}} \tag{11}$$

$$Z_{\mathrm{GH}} = \frac{1}{\frac{1}{R_{\mathrm{G}}} + sC_{\mathrm{driver}}} + sL_{\mathrm{GH}} + sL_{\mathrm{KSH}}. \tag{12}$$

From Fig. 25(b) and (c), there are two delta-star transformations. Impedance Z_1, Z_2, Z_3 can be derived as

$$\begin{cases} Z_1 = \dfrac{Z_{\Delta12}Z_{\Delta13}}{Z_{\Delta12}+Z_{\Delta23}+Z_{\Delta13}} \\ Z_2 = \dfrac{Z_{\Delta12}Z_{\Delta23}}{Z_{\Delta12}+Z_{\Delta23}+Z_{\Delta13}} \\ Z_3 = \dfrac{Z_{\Delta13}Z_{\Delta23}}{Z_{\Delta12}+Z_{\Delta23}+Z_{\Delta13}} \end{cases} \tag{13}$$

where

$$\begin{cases} Z_{\Delta12} = Z_{\mathrm{DC+}} \\ Z_{\Delta23} = Z_{\mathrm{DC-}} \\ Z_{\Delta13} = \dfrac{1}{sC_{\mathrm{Decouple}}} + R_{\mathrm{C.ESR}}. \end{cases} \tag{14}$$

Impedance Z_4, Z_5, Z_6 can be derived as

$$\begin{cases} Z_4 = \dfrac{Z_{\Delta12}Z_{\Delta13}}{Z_{\Delta12}+Z_{\Delta23}+Z_{\Delta13}} \\ Z_5 = \dfrac{Z_{\Delta12}Z_{\Delta23}}{Z_{\Delta12}+Z_{\Delta23}+Z_{\Delta13}} \\ Z_6 = \dfrac{Z_{\Delta13}Z_{\Delta23}}{Z_{\Delta12}+Z_{\Delta23}+Z_{\Delta13}} \end{cases} \tag{15}$$

where

$$\begin{cases} Z_{\Delta12} = \dfrac{1}{sC_{\sigma\mathrm{OUT}}} \\ Z_{\Delta23} = \dfrac{1}{s(C_{\sigma\mathrm{GL}}+C_{\sigma-})} \\ Z_{\Delta13} = \dfrac{1}{sC_{\mathrm{ossL}}}. \end{cases} \tag{16}$$

From Fig. 25(c) and (d), impedance Z_7, Z_8, Z_9, Z_{10} can be derived as

$$Z_7 = Z_1 + sL_{\mathrm{DH}} \tag{17}$$

$$\begin{cases} Z_8 = \dfrac{Z_{\Delta12}Z_{\Delta13}}{Z_{\Delta12}+Z_{\Delta23}+Z_{\Delta13}} \\ Z_9 = \dfrac{Z_{\Delta12}Z_{\Delta23}}{Z_{\Delta12}+Z_{\Delta23}+Z_{\Delta13}} \\ Z_{10} = \dfrac{Z_{\Delta13}Z_{\Delta23}}{Z_{\Delta12}+Z_{\Delta23}+Z_{\Delta13}} \end{cases} \tag{18}$$

where

$$\begin{cases} Z_{\Delta12} = Z_2 + Z_{\mathrm{GND}} \\ Z_{\Delta23} = Z_5 \\ Z_{\Delta13} = Z_3 + Z_6 + sL_{\mathrm{SL}}. \end{cases} \tag{19}$$

From Fig. 25(d) and (e), based on delta-star transformation, impedance Z_{11}, Z_{12}, Z_{13} can be derived as

$$\begin{cases} Z_{11} = \dfrac{Z_{\Delta12}Z_{\Delta13}}{Z_{\Delta12}+Z_{\Delta23}+Z_{\Delta13}} \\ Z_{12} = \dfrac{Z_{\Delta12}Z_{\Delta23}}{Z_{\Delta12}+Z_{\Delta23}+Z_{\Delta13}} \\ Z_{13} = \dfrac{Z_{\Delta13}Z_{\Delta23}}{Z_{\Delta12}+Z_{\Delta23}+Z_{\Delta13}} \end{cases} \tag{20}$$

where

$$\begin{cases} Z_{\Delta12} = \dfrac{1}{sC_{\sigma+}} \\ Z_{\Delta23} = Z_9 \\ Z_{\Delta13} = Z_7 + Z_8. \end{cases} \tag{21}$$

From Fig. 25(e) and (f), impedance Z_{14}, Z_{15}, Z_{16} can be derived as

$$\begin{cases} Z_{14} = \dfrac{Z_{\Delta12}Z_{\Delta13}}{Z_{\Delta12}+Z_{\Delta23}+Z_{\Delta13}} \\ Z_{15} = \dfrac{Z_{\Delta12}Z_{\Delta23}}{Z_{\Delta12}+Z_{\Delta23}+Z_{\Delta13}} \\ Z_{16} = \dfrac{Z_{\Delta13}Z_{\Delta23}}{Z_{\Delta12}+Z_{\Delta23}+Z_{\Delta13}} \end{cases} \tag{22}$$

where

$$\begin{cases} Z_{\Delta12} = Z_{12} + \dfrac{1}{sC_{\sigma\mathrm{GH}}} \\ Z_{\Delta23} = Z_{\mathrm{GH}} \\ Z_{\Delta13} = Z_4 + Z_{10} + Z_{13}. \end{cases} \tag{23}$$

Therefore, the impedance Z_D, Z_G, Z_S can be obtained

$$\begin{cases} Z_{\mathrm{D}} = Z_{11} + Z_{14} \\ Z_{\mathrm{G}} = Z_{15} \\ Z_{\mathrm{S}} = Z_{16} + sL_{\mathrm{CSH}}. \end{cases} \tag{24}$$

From Fig. 25(g) and (h), according to star-delta transformation, impedance Z_{17}, Z_{18}, Z_{19} can be derived as

$$\begin{cases} Z_{17} = Z_{\mathrm{D}} + Z_{\mathrm{S}} + \dfrac{Z_{\mathrm{D}}Z_{\mathrm{S}}}{Z_{\mathrm{G}}+R_{\mathrm{int}}} \\ Z_{18} = Z_{\mathrm{G}} + R_{\mathrm{int}} + Z_{\mathrm{D}} + \dfrac{(Z_{\mathrm{G}}+R_{\mathrm{int}})Z_{\mathrm{D}}}{Z_{\mathrm{S}}} \\ Z_{19} = Z_{\mathrm{G}} + R_{\mathrm{int}} + Z_{\mathrm{S}} + \dfrac{(Z_{\mathrm{G}}+R_{\mathrm{int}})Z_{\mathrm{S}}}{Z_{\mathrm{D}}}. \end{cases} \tag{25}$$

By combining the impedance, $Z_{\mathrm{gs}}, Z_{\mathrm{gd}}, Z_{\mathrm{ds}}$ can be obtained

$$\begin{cases} Z_{\mathrm{gs}} = \dfrac{1}{\dfrac{1}{Z_{19}} + sC_{\mathrm{gs}}} \\ Z_{\mathrm{gd}} = \dfrac{1}{\dfrac{1}{Z_{18}} + sC_{\mathrm{gd}}} \\ Z_{\mathrm{ds}} = \dfrac{1}{\dfrac{1}{Z_{17}} + \dfrac{1}{r_{\mathrm{d}}} + sC_{\mathrm{ds}}}. \end{cases} \tag{26}$$

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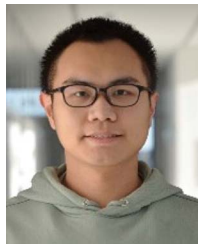

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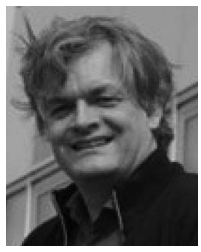

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