Modeling and Design of a Frequency-Regulated Series Resonant Inverter With a Linear Variable Capacitor

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***Abstract*—Resonant power inverters are among the most efficient power conversion topologies. However, their widespread adoption is hindered by inefficient operation and control limitations under light-load conditions. This research focuses on facilitating the operation of a series resonant inverter (SRI) by utilizing the recently introduced passive linear variable capacitor (LVC) structure. LVC utilizes the nonlinear parasitic capacitance of two back-to-back reverse-biased diodes to establish a voltage- or current-dependent linear capacitor. This research analyzes combining LVC and constant linear capacitors to dynamically change SRI's resonant frequency for varying load and, that way, reduce the frequency regulation band of the SRI. This article presents a complete analytical framework and describes a design procedure for an SRI with integrated LVC. The proposed framework is verified through simulations and experimentation. A control frequency band reduction of 39% and 37% is experimentally demonstrated for the two studied SRI designs. In addition, the effects of temperature variation and device heterogeneity on LVC characteristics are analyzed, along with their impact on SRI performance.**

***Index Terms*—Capacitors, integrated circuit modeling, passive components, resonant power converters, semiconductor diodes.**

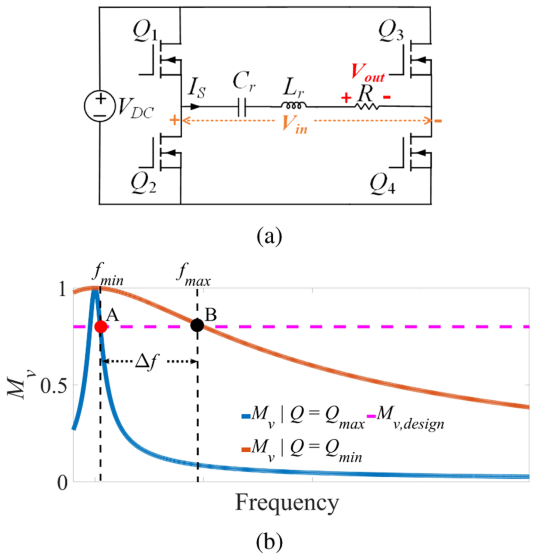

Fig. 1. Full bridge SRI. (a) Circuit diagram. (b) Voltage gain versus frequency characteristics for variable load.

I. Introduction

SERIES resonant inverters (SRIs) find application in many systems, either independently or as part of a series resonant converter (SRC). SRIs are commonly used for low and mid-power applications because of their high efficiency and power density resulting from high operating frequency. SRIs are often preferred because of their 1) low component count, 2) zero voltage switching (ZVS) operation over a wide range of loads, 3) ability to effectively integrate an isolation transformer, and 4) ability to integrate parasitic inductance (e.g., transformer's leakage inductance) into the circuit or even use them as a replacement for circuit elements [1], [2]. A full-bridge voltage-sourced SRI is shown in Fig. 1(a). Resistance R represents an electric load or an equivalent load of the isolation–rectification section of an SRC. Replacing the rectifier and isolation transformer with equivalent resistance $R = R_{L,\text{eq}}$ allows the same SRI analysis to be conducted, whether the SRI operates independently or as a part of a resonant converter.

Maintaining constant output voltage and efficient operation under fluctuating load R and input voltage V_{DC} is challenging for an SRI. Impedance transformation networks (ITN) are sometimes used to maintain soft switching conditions and reduce the effective range of load variation [3], [4]. However, an ITN increases circuit complexity and adds extra losses while not solving the problem entirely. Control of the output voltage can be accomplished by means of varying i) inverter's input voltage V_{DC}, ii) the SRI's operating frequency, or iii) the SRI's resonant frequency. Most reported approaches utilized sensing and active feedback control for load regulation [5], [6]. Control methods with constant frequency operation, including pulsewidth modulation (PWM) [7], [8], asymmetric PWM, phase-shift [7], and fixed on-time modulation [9] actively vary the first harmonic of the inverter's output voltage. However, these methods typically provide a suboptimal ZVS range and lower efficiency compared to other methods.

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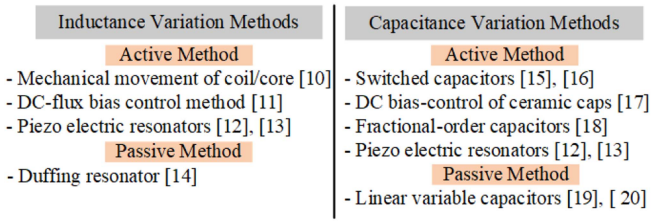


Fig. 2. Methods of adjusting resonant frequency based on varying SRI's reactive components (inductors or capacitors).

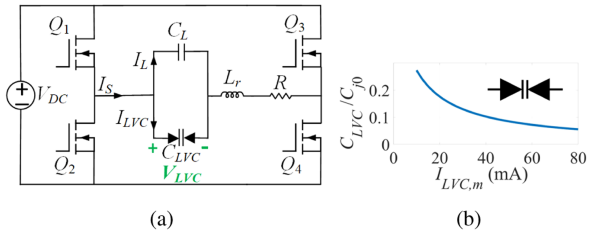


Fig. 3. LVC application in an SRI and a typical LVC characteristic. (a) SRI with a linear capacitor and an LVC in parallel. (b) Current-dependent capacitance model of an LVC made of RB238T150 at $f = 1$ MHz [21].

Frequency regulation (FR) is traditionally the preferred way to regulate SRI because of the simple control approach and ZVS operation above the resonant frequency. To maintain the required output voltage, a controller varies the operating frequency from $f_{\min}$ to $f_{\max}$ as operating conditions change, establishing a region of operation and frequency band illustrated in Fig. 1(b). The difference between $f_{\min}$ and $f_{\max}$ is defined as frequency band Δf. The main challenges of regulating an SRI with FR are as follows:

1) The frequency band requirement is theoretically infinite for a full load to no-load voltage regulation.
2) Conduction losses of many components increase at higher frequencies and may counteract the ZVS benefits.
3) Operating in a wide frequency range may lead to suboptimal magnetics design.

Alternative solutions based on varying SRI's reactive components (inductors or capacitors) to adjust the resonant frequency and indirectly regulate the output voltage are summarized in Fig. 2. Active inductance variations can be achieved using a mechanical actuator to move the core or inductor coil to change the airgap between the core and coil [10]. However, it is featured by slow dynamics, reliability issues, and design complexity. Flux-bias control adjusts inductance by biasing the core with dc flux, though the complexity of the bias circuit and additional flux losses hinder widespread adoption [11]. Piezoelectric resonators vary impedance based on vibration mode, but damping from connection resistance and nonlinear material properties limits their application [12], [13]. Nonlinear saturable inductors employ partial core saturation to introduce nonlinearity, but high-frequency core losses often limit their application to lower frequencies (tens of kHz) [14].

Researchers have also explored capacitance variation methods as capacitors generally have higher quality factors and lower volumetric footprint than inductors in the MHz range. The switched capacitors method is straightforward, but its implementation can be complex depending on the required capacitance resolution. They need a passive capacitor bank and an auxiliary switching circuit for capacitance control [15], [16]. DC-bias control of ceramic capacitors relies on the voltage-dependent capacitance behavior of Class II and Class III ceramics [17]. However, its implementation is challenging due to the need for auxiliary dc-bias circuitry. Fractional-order capacitors use phase-shift control on regular capacitors to achieve fractional-order dynamics, necessitating additional switching, sensing, and control circuitry for each component [18]. Recently introduced linear variable capacitor (LVC) consisting of back-to-back reverse-biased diodes [19], [20] demonstrates significant potential as a variable capacitance method. It utilizes the parasitic capacitance of back-to-back diodes to form a harmonic-less (linear) current-dependent capacitor. LVC operates as a simple passive component, without auxiliary circuitry and control, but requires a careful design and an integrated device maximizing parasitic capacitance for enhanced performance. The LVC capacitance profile and relevant characteristics have been studied in detail in [21]. An example of an LVC in an SRI is shown in Fig. 3(a), and the current-dependent capacitance model of an LVC made of diodes RB238T150 operating at 1 MHz is shown in Fig. 3(b) [21]. C_{j0} is the zero bias capacitance of diode and $I_{\mathrm{LVC},m}$ is the magnitude of peak LVC current. Passive operation (no biasing circuit needed), small size, high efficiency at high frequencies, and low cost make an LVC highly appealing for resonant power applications.

The authors in [19] and [20] utilized a polynomial approximation of the diode charge model and Duffing equation to describe an LVC and integrate into a wireless power transfer (WPT) system. In [19], they replaced the compensation capacitance on the transmitter side of an *LC–LC*-compensated WPT system with an LVC made of two Schottky diodes. The equivalent capacitance of the LVC acts as negative feedback to regulate output power for coupling variation. It is reported that the LVC doubled the acceptable misalignment range of the WPT system. Chai and Mortazawi [20] replaced both compensation capacitors of an *LC–LC*-compensated WPT system with LVCs. The results show that the minimum coupling coefficient required for power transfer has reduced by 60%.

While Class II and Class III ceramic capacitors, such as X7R capacitors, exhibit voltage-dependent capacitance due to high-permittivity dielectric materials like $BaTiO_3$, their suitability as substitutes for diode-based LVCs is limited. These capacitors are recognized by their ability to handle low-frequency ripple currents, but their performance diminishes at high frequencies (in the MHz range) due to a higher loss tangent, sometimes reaching 0.1 to 0.2 [22]. Temperature stability also presents a notable challenge– - Class II ceramic capacitors exhibit a temperature-dependent capacitance variation of $\pm$ 15%, while Class III models demonstrate even greater sensitivity, ranging from +22% to −82% [23]. Finally, the unique C-V profile of the *pn* junction with $m = 0.5$ results effectively in the harmonic-less

LVC operation. This is not the case with Class II and Class III ceramic capacitors, which generate harmonics even for sinusoidal excitations.

This study explores how an LVC can be integrated into a frequency-regulated SRI to improve its characteristics when operating under variable load or input voltage. The goal is to maintain the positive FR features (ZVS operation, high efficiency, and low current stress) while reducing the FR operation band Δf. As explained in the following sections, an LVC achieves this by a) reducing the network's natural resonant frequency at light load, b) increasing the slope of the gain curve in the inductive region, and c) facilitating ZVS for lower current phase lagging at light load despite lower operating frequency. This causes the operating region and frequency band to reduce. The paper employs power electronics methodology and accurate LVC models presented in [21] to derive an analytical model of an SRI with an LVC integrated in parallel to the linear capacitor. It describes the optimum LVC design procedure and derives boundaries of bifurcation-less converter operation. The key contributions of this research are as follows:

1) Deriving the analytical model of an SRI with an LVC added parallel to the constant capacitor in the resonant network.
2) Describing the relationship between LVC specifications and the reduction of the frequency band of frequency-regulated SRI for variable load and/or input voltage.
3) Deriving the maximum LVC participation to ensure a bifurcation-less operation of the control algorithm.
4) Analyzing the effects of temperature variation and device heterogeneity on LVC characteristics, along with their impact on the performance of an SRI.

The rest of this article is organized as follows. In Section II, an analytical model of an SRI with added LVC is presented. Section III presents the analysis of a frequency-regulated SRI with an LVC under variable load conditions, focused on deriving an expression for the frequency band. It also includes a comparative evaluation of the impact of LVC on SRI losses. Section IV discusses the same band but for the case when both the load and input voltage vary. Section V presents the experimental results obtained for two different LVCs, including detailed loss modeling, a comparative analysis of measured losses, and a discussion on overall system efficiency. Section VI discusses key considerations for a practical LVC implementation, including the effects of temperature and device heterogeneity. Finally, Section VII concludes this article.

II. Modeling and SRI With an LVC

This section derives an analytical model of an SRI with an LVC connected in parallel with a linear capacitor and verifies it through LTSpice simulations. The analysis starts from a conventional SRI with a linear capacitor and establishes an LVC-based SRI by adding an LVC in parallel with the linear capacitor, as illustrated in Fig. 3(a). In the two cases, the system is designed to achieve the same operating condition for the maximum load ($R = R_{\min}$), including the same output current, output voltage, and switching frequency. Therefore, the equivalent capacitance of both designs must be the same at the *common design point* (abbreviated as CDP in the text) designated by $f = f_{\min}$ and $R = R_{\min}$ ($Q = Q_{\max}$). The CDP is marked in Fig. 1(b) with a red dot and letter A. This should ensure fair comparison as the minimum operating frequency is the same. For a general SRI, voltage gain M_v between the first harmonic of the full-bridge switching nodes voltage V_{in} and the output load voltage V_{out} is given by

$$M_v = R/\sqrt{(\omega L_r - 1/\omega C_r)^2 + R^2}. \tag{1}$$

The phase of the SRI resonant network input impedance, which determines the switching behavior of the inverter, is

$$\phi = \arctan((\omega L_r - (1/\omega C_r))/R). \tag{2}$$

For a specified gain M_v at the CDP, the equivalent capacitance C_r is calculated using (1) as

$$C_r = ((\omega_{\min} L_r/R_{\min}) - \sqrt{1/{M_v}^2 - 1})/(\omega_{\min} R_{\min}). \tag{3}$$

For the SRI circuit with added LVC capacitor C_{LVC} shown in Fig. 3(a), the equivalent capacitance at the CDP is given by

$$C_{r,\text{eq}}(\omega_{\min}, I_{S,A,m}) = C_{\text{LVC}}(\omega_{\min}, I_{LVC,A,m}) + C_L \tag{4}$$

where $I_{S,A,m}$ and $I_{\text{LVC},A,m}$ are the magnitudes of total branch and LVC currents, respectively. Many C_L-C_{LVC} pairs can satisfy (4), each of them resulting in different $f_{\max}$ for light load $R = R_{\max}$. To analyze possible solutions, capacitance ratio k_{CP} is defined at a CDP A as

$$k_{\text{CP}} = C_{\text{LVC}}(\omega_{\min}, I_{\text{LVC},A,m})/C_{r,\text{eq}}(\omega_{\min}, I_{S,A,m}). \tag{5}$$

For a specified operating point with parameters $C_{r,\text{eq}}$ and k_{CP}, C_{LVC} and C_L can be calculated as

$$C_{\text{LVC}}(\omega_{\min}, I_{\text{LVC},A,m}) = k_{\text{CP}} C_{r,\text{eq}}(\omega_{\min}, I_{S,A,m}) \tag{6}$$

$$C_L = (1 - k_{\text{CP}}) C_{r,\text{eq}}(\omega_{\min}, I_{S,A,m}). \tag{7}$$

This study relies on the definition of the commonly used diode differential junction capacitance [21], [24], where

$$C_j(v_D) = C_{j0}(1 + v_D/V_B)^{-m} \quad -\frac{V_B}{2} \le v_D \le V_{BN} \tag{8}$$

1) C_{j0} is the zero-bias junction capacitance of a single diode. Accordingly, $C_{eq,j0} = nC_{j0}$ used in this article is the equivalent zero-bias capacitance of n identical parallel diodes constituting one LVC side;
2) V_B is the forward bias junction threshold voltage;
3) m is the grading exponent. For most power devices in the market, m is from 0.3 to 0.6, most frequently being at or near 0.5; and
4) V_{BN} is the diode breakdown voltage.

$C_{j\,0}$, m, and V_B can be derived using the capacitance model of p-type and n-type (PN) and Schottky diodes, as explained in [21] and [24]. The next step is to calculate $C_{eq,j0}$ for given diode parameters m and V_B to satisfy (6) at the CDP A.

The following set of equations (9)–(13) are solved to obtain $C_{eq,j0}$

$$C_{\text{LVC}}(\omega_{\min}, I_{S,A,m}) = I_{S,A,m}/(\omega_{\min} V_{\text{LVC},A,1m}) \tag{9}$$

where $V_{\mathrm{LVC},A,1m}$ is the magnitude of the first harmonic component of the LVC voltage v_{LVC} at the CDP A. v_{LVC} is expressed as derived in [21]

$$v_{\mathrm{LVC}} = V_B P^{1/(1-m)} \left([1 + P_S - \cos\theta]^{1/(1-m)} - [1 + P_S + \cos\theta]^{1/(1-m)} \right) \quad (10)$$

where

$$P = I_{S,A,m} (1-m) / (\omega_{\min} C_{eq,j0} V_B) \quad (11)$$

$$P_S = (1/P)/(1 - V_S/V_B)^{1-m}. \quad (12)$$

Fundamental voltage magnitude $V_{\mathrm{LVC},A,1m}$ is calculated as

$$V_{\mathrm{LVC},A,1m} = \frac{1}{\pi} \int_0^{2\pi} v_{\mathrm{LVC}}(\theta) \cos(\theta) d\theta. \quad (13)$$

The presence of harmonics in an SRI can result in control and EMI issues and additional losses. In [21], total harmonic distortion (THD) of the voltage of a sinusoidal current-supplied LVC is studied as a function of I_m and m. It is concluded that the THD is less than 2% for $m < 0.6$. However, for $m = 0.5$, the LVC operates as a linear device not producing harmonics, which makes diodes with $m = 0.5$ a preferred choice for designing/manufacturing LVCs. A generalized explicit solution of $C_{\mathrm{eq},j0}$ can be determined by solving (9)–(13) only for $m = 0.5$. For other values of m, (9)–(13) must be solved numerically to obtain $C_{\mathrm{eq},j0}$. After $C_{\mathrm{eq},j0}$ is obtained, which effectively decides the LVC, the next step is to establish a method of calculating circuit current and voltages for an arbitrary load and frequency (for operating points different than CDP A). Calculating C_{LVC} is a prerequisite for that, but C_{LVC} depends on I_{LVC}. The following equations are derived by applying simple circuit analysis to SRI in Fig. 3(a), and they have to be simultaneously solved to obtain C_{LVC} at every frequency and load

$$I_{S,m} = V_{\mathrm{in},m} / \sqrt{(\omega L_r - 1/\omega C_{r,\mathrm{eq}}(\omega, I_{S,m}))^2 + R^2} \quad (14)$$

$$C_{r,\mathrm{eq}}(\omega, I_{S,m}) = C_{\mathrm{LVC}}(\omega, I_{\mathrm{LVC},m}) + C_L \quad (15)$$

$$I_{S,m}/(\omega C_{\mathrm{eq}}(\omega, I_{S,m})) = I_{\mathrm{LVC},m}/(\omega C_{\mathrm{LVC}}(\omega, I_{\mathrm{LVC},m})) \quad (16)$$

$$C_{\mathrm{LVC}}(\omega, I_{S,m}) = I_{S,m}/(\omega V_{\mathrm{LVC},1}) \quad (17)$$

where $V_{\mathrm{in},m} = 4V_{\mathrm{DC}}/\pi$ is the magnitude of $V_{\mathrm{in},m}$, and $V_{\mathrm{LVC},1}$ is the fundamental voltage component of V_{LVC}. An explicit solution of (14)–(17) to obtain C_{LVC} is only feasible for $m = 0.5$, while numerical methods must be used to solve the equations for other m values. M_v is then calculated using (1).

A simplified approach, possible only for $m = 0.5$, is discussed here. For $m = 0.5$, C_{LVC} of an LVC is given by [21]

$$C_{\mathrm{LVC}}(\omega, I_{\mathrm{LVC},m}, m = 0.5) = \frac{C_{\mathrm{eq},j0}^2 \omega V_B}{I_{\mathrm{LVC},m} + 2\omega C_{\mathrm{eq},j0} V_S}. \quad (18)$$

For typical I_{LVC} currents, $I_{\mathrm{LVC},m}$ is significantly greater than $2\omega C_{\mathrm{eq},j0} V_S$ in (18), allowing the approximation

$$C_{\mathrm{LVC}}(\omega, I_{\mathrm{LVC}}, m = 0.5) = C_{eq,j0}^2 \omega V_B / I_{\mathrm{LVC},m}. \quad (19)$$

TABLE I
SRI TEST SETUP CHARACTERISTICS ($k_{\mathrm{CP}} = 0$)

Circuit Parameters	Baseline SRI/ SRI-1/ SRI-2
V_{DC} [V]	15 / 15 /30
M_V	0.8
V_{out} [V]	13.50 / 13.50 / 27
P_{out} at $R_{\min}$ [W]	23.3 / 23.3 / 93.2
$Q_{\max}, Q_{\min}$	8, 0.8
$R_{\min}, R_{\max}$ [Ω]	5, 50
f_r [MHz]	1
$f_{\min}$ [MHz]	1.048
L_r [μH]	6.36

Using (5), (16), and (19), $C_{\mathrm{eq},j0}$ can be calculated for CDP A (condition $I_{\mathrm{LVC},m} = I_{\mathrm{LVC},A,m}$ and $\omega = \omega_{\min}$) as

$$C_{\mathrm{eq},j0} = k_{\mathrm{CP}} \sqrt{I_{S,A,m} C_{r,\mathrm{eq}} / (\omega_{\min} V_B)}. \quad (20)$$

To calculate M_v for other operating frequencies and loads, the SRI is solved for steady-state values of circuit parameters. Therefore, substituting (1), (6), and (16) into (14) leads to quartic equation in terms of I_{LVC}

$$aI^4{}_{LVC}\mathrm{LVC} + bI^3{}_{LVC}\mathrm{LVC} + cI^2{}_{LVC}\mathrm{LVC} + dI_{LVC}\mathrm{LVC} + e = 0 \quad (21)$$

where

$$a = \omega^4 L_r^2 C_L^2 + 1 - 2L_r \omega^2 C_L + R^2 \omega^2 C_L^2$$

$$b = 2\omega^3 C_{\mathrm{eq},j0}^2 V_B \left(C_L \omega^2 L_r^2 - L_r + R^2 C_L \right)$$

$$c = \omega^6 L_r^2 C_{\mathrm{eq},j0}^4 V_B^2 + R^2 \omega^4 C_{\mathrm{eq},j0}^4 V_B^2$$

$$d = 0$$

$$e = -\omega^4 V_{\mathrm{in},m}^2 C_{\mathrm{eq},j0}^4 V_B^2.$$

Once $C_{\mathrm{eq},j0}$ is obtained from (20), (21) can be solved for specified ω and R. Finally, C_{LVC}, M_v, and $I_{S,m}$ can be calculated using (19), (1), and (14), respectively.

The baseline SRI system ($k_{\mathrm{CP}} = 0$) shown in Fig. 1(a) is designed as per Table I. A load range is selected to represent a battery charger's typical constant-voltage (CV) operation [25]. The L_r selection is essential to maintain an adequate loaded quality factor Q and apply the first harmonic approximation-based SRI analysis. This consideration becomes particularly important as the load often varies up to 10 times during a typical constant current (CC)–constant voltage (CV) charging operation [see Fig. 1(b)]. The adoption of a high Q factor effectively suppresses current harmonics but leads to a high voltage rating for reactive components and makes the system sensitive to variations in component values caused by component tolerance, aging, or changes in operating conditions. In contrast, a low Q could lead to harmonic generation, which can cause EMI issues and increased losses. In this study, Q is defined at the resonant frequency of 1 MHz, and its boundary values are calculated as $Q_{\max} = \omega_r L_r / R_{\min} = 8$ and $Q_{\min} = \omega_r L_r / R_{\max} = 0.8$. This range of Q allows the system to operate with mostly the

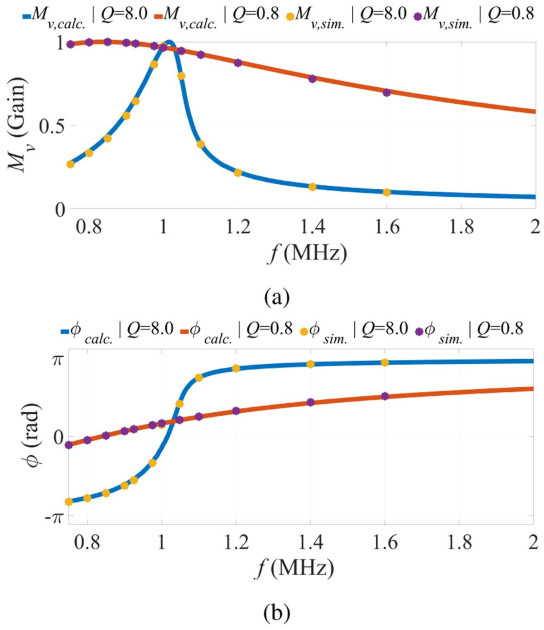


Fig. 4. Comparison of analytical and simulation results for $k_{CP} = 0.25$. (a) Gain plot. (b) Phase of the input impedance of the SRI resonant network as seen by the inverter.

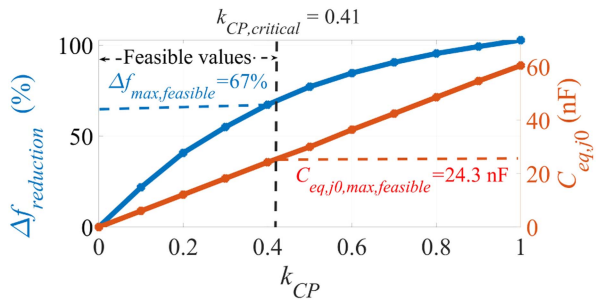


Fig. 5. Reduction in Δf as a function of k_{CP} for $M_v = 0.80$.

fundamental harmonics through the entire load range while still utilizing low-voltage-rated diodes.

An LTspice model is developed to verify the analysis for an LVC made of diodes RB238T150 for $k_{CP} = 0.25$. The simulation and analytically obtained voltage gain magnitude and phase values are presented in Fig. 4, demonstrating a close matching and verifying the proposed analytical model for $k_{CP} = 0.25$.

III. Analysis and Design of a Frequency-Regulated LVC-Based SRI for Variable R Conditions

This section describes the methodology and operational boundaries of integrating an LVC into a frequency-regulated SRI with varying load R. The role of FR is to maintain constant output voltage (voltage gain M_v) as the load varies, while the role of LVC is to reduce the required frequency band Δf. To solve for Δf, (21) is solved for $M_v = 0.8$ and $R = R_{max}$ to get f_{max} as f_{min} is maintained constant for all k_{CP} values.

The blue trace corresponding to the left y-axis plot in Fig. 5 describes the percentage of Δf reduction as k_{CP} changes from

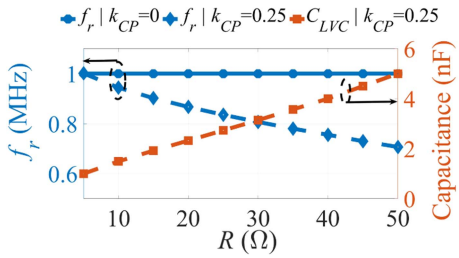


Fig. 6. f_r and C_{LVC} as a function of R in an SRI without ($k_{CP} = 0$) and with ($k_{CP} = 0.25$) an LVC for $M_v = 0.80$.

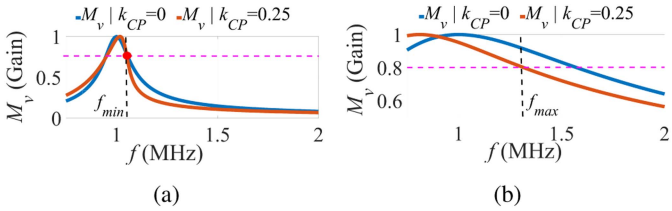


Fig. 7. SRI voltage gain for $k_{CP} = 0.25$. (a) $Q = 8$. (b) $Q = 0.8$.

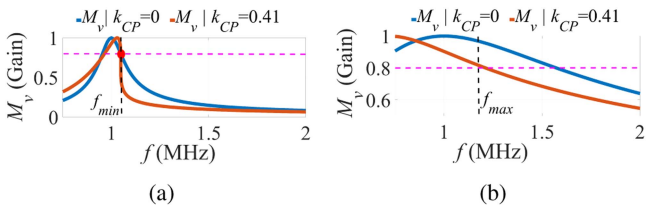


Fig. 8. SRI voltage gain for $k_{CP} = 0.41$. (a) $Q = 8$. (b) $Q = 0.8$.

zero (only linear capacitor) to one (only LVC). It can be observed that $\Delta f_{reduction}$ increases as k_{CP} increases. approaching 100% as the relative LVC contribution approaches $k_{CP} = 1$. The required $C_{eq,j0}$ as a function of k_{CP} is presented on the orange trace corresponding to the right y-axis in Fig. 5. It can be seen that the required $C_{eq,j0}$ increases with k_{CP}, demanding a larger silicon area or more discrete diodes. In Fig. 6, the effect of adding LVC capacitance to an SRI can be observed in the change of network resonant frequency f_r as a function of loading conditions for constant gain $M_v = 0.80$. While f_r is constant for $k_{CP} = 0$, as expected, it decreases by almost 30% at minimum load for $k_{CP} = 0.25$. f_r changes because C_{LVC} increases as I_{LVC} reduces for lighter loads. The LVC is designed to contribute 25% of total capacitance C_r at the CDP ($R = 5\ \Omega$). C_{LVC} increases by almost 500% at the minimum load $R = 50\ \Omega$, boosting C_{LVC} contribution to total capacitance $C_{eq,r}$ by 2.5 times to 62.5%. This increase in C_{LVC} reduces Δf and lowers operation frequency.

M_v curves using different C_{LVC} are plotted for cases $k_{CP} = 0.25$, 0.41, and 1 in Figs. 7 –9, respectively. In Figs. 7(a), 8(a), and 9(a), it is observed that the natural resonant frequency increases slightly for high load operation (Q=8) as k_{CP} increases. On the contrary, in Figs. 7(b), 8(b), and 9(b), it is observed that the natural resonant frequency reduces significantly for light load operation (Q=0.8) and that shift becomes even higher for

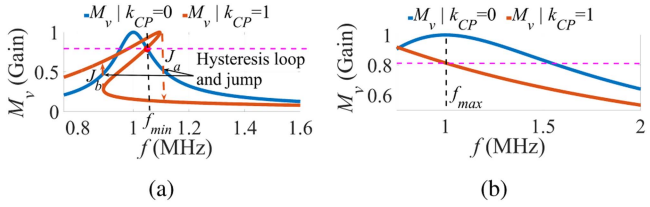


Fig. 9. SRI voltage gain for $k_{CP}=1$. (a) $Q=8$. (b) $Q=0.8$.

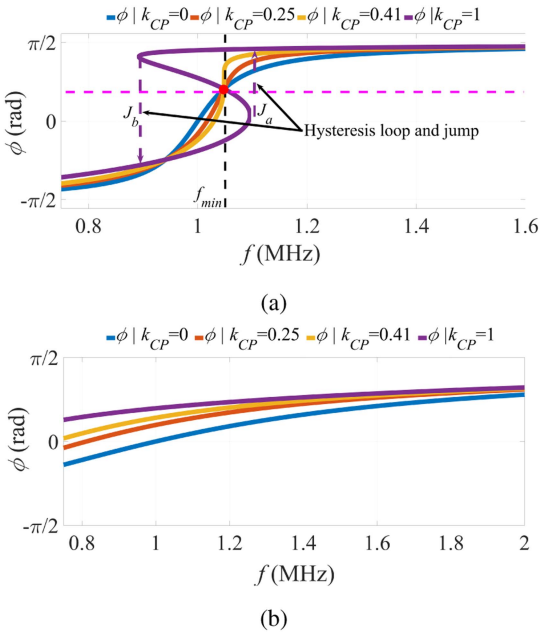


Fig. 10. Phase plot for $k_{CP}=0$, 0.25, 0.41, and 1. (a) $Q=8$. (b) $Q=0.8$.

larger k_{CP}. A lower natural resonant frequency leads to a lower f_{max}, reducing Δf.

As visible in Fig. 9(a), for higher k_{CP} values, the resonant peak bends, causing a hysteresis loop and jump phenomenon known in nonlinear systems [19], [20]. The arrows in Fig. 9(a) mark the jump transitions when moving along the frequency axis. The direction of frequency change determines the transition. If the frequency increases, transition J_a occurs, while J_b is observed if the frequency decreases. These "jumps" could cause high phase and gain transitions leading to instability.

A comparative phase plot is presented in Fig. 10 for $k_{CP}=0$, 0.25, 0.41, and 1. For Q=8, phase φ monotonously increases with frequency for $k_{CP}=0$, 0.25, and 0.41. The phase curve slope increases as k_{CP} increases up to the point when the hysteresis loop appears, as observed for $k_{CP}=1$ and marked by black arrows. The gain and phase plots for all k_{CP} values merge at higher frequencies. On the other hand, for Q=0.8, the phase monotonously increases for all cases, with the slope reducing for higher k_{CP}.

As the jump phenomenon is typically unwanted in control of power electronic systems, it is important to determine the maximum k_{CP} value that guarantees jump-less operation. The hysteresis occurs if all four solutions of (21) are real for any

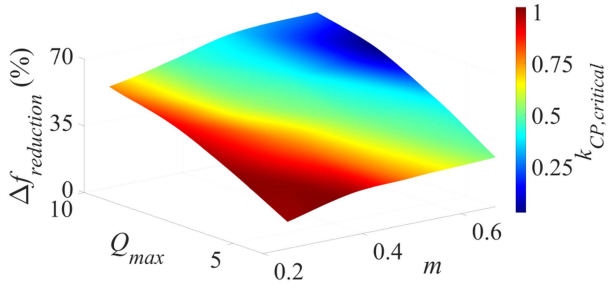


Fig. 11. Q_{max} and m impact on Δf and $k_{CP,critical}$.

ω between ω_{min} and ω_{max}, which, as per [26], will occur if conditions (22)–(25) are satisfied

$$\Delta > 0 \;\&P < 0 \;\&D < 0 \tag{22}$$

$$\begin{aligned}\Delta = {} & 256a^3e^3 - 192a^2bde^2 - 128a^2c^2e^2 + 144a^2cd^2e \\ & -27a^2d^4 + 144ab^2cd^2 - 6ab^2d^2e - 80abc^2de \\ & +18abcd^3 + 16ac^4e - 4ac^3d^2 - 27b^4e^2 + 18b^3cde \\ & -4b^3d^3 - 4b^2c^3e + b^2c^2d^2 - 4ac^3d^2 - 27b^4e^2\end{aligned} \tag{23}$$

$$P = 8ac - 3b^2 \tag{24}$$

$$D = 64a^3e - 16a^2c^2 + 16ab^2c - 16a^2bd - 3b^4. \tag{25}$$

In the studied system, the hysteresis occurs for $k_{CP,critical}$ greater than 0.41. However, the rate of Δf change reduces as k_{CP} increases, causing the zone above $k_{CP,critical}$ to contribute less to Δf reduction, as visible in Fig. 5. Therefore, a design with $k_{CP} \leq 0.41$ can still provide considerable Δf reduction without instigating the hysteresis behavior.

Therefore, the goal of an LVC-based SRI design would be to maximize LVC contribution by operating close to $k_{CP,critical}$ for a given system defined by Q_{max} and m. Fig. 11. illustrates the relationship between Q_{max}, $k_{CP,critical}$, m, and $\Delta f_{reduction}$. For simplicity, it is assumed that $Q_{min}=Q_{max}/10$. It is observed that $k_{CP,critical}$ values are higher for systems with lower Q_{max}, and m, but systems with higher Q_{max} and m result in more $\Delta f_{reduction}$. However, designing an SRI system with a higher Q_{max} leads to a high component rating and high design sensitivity, whereas a higher m greater than 0.5 introduces more harmonics. Moreover, Fig. 11 indicates that $k_{CP,critical}$ is relatively low when operating at high Q and m for the same Δf, i.e., capacitance contribution from LVC can be kept low if high Q and m values are used.

A. Comparing the Effect of LVC on the Losses in an SRI

Table II compares power losses in SRIs with and without an LVC, highlighting how frequency reduction affects efficiency at various loads. It examines inverter conduction and switching losses, inductor core and copper losses, and losses in resonant capacitors, focusing on LVC's role in reducing power loss and boosting efficiency. In the table, f_{min} denotes the switching frequency at CDP A, Δf_1 is the extra frequency bandwidth required to operate at $R > R_{min}$ for the SRI with constant

TABLE II
LOSS RATIO AS A FUNCTION OF FREQUENCY FOR SRIS WITH AND WITHOUT LVC FOR $R>R_{MIN}$ AND $m=0.5$

	Parameter	$P_{loss,\,k_{CP}\neq 0}/P_{loss,\,k_{CP}=0}$
Inverter	Conduction loss	1
	Switching loss	F_R
Inductor	Core loss	F_R^{α}
	Proximity loss	F_R^2
	Skin-effect loss	1
Capacitor	Combined linear capacitor and LVC loss	$\frac{r_{CL2}+\lambda^2 r_{LVC}}{r_{CL1}(\lambda+1)^2}$ $\lambda=\frac{I_{LVC}}{I_{CL}}=\frac{k_{CP}}{(1-k_{CP})}\frac{R}{R_{min}}F_R$

capacitor case, and $\Delta f_{reduction}$ is the reduction in bandwidth achieved when LVC is employed ($k_{CP}\neq 0$). Parameter F_R is the ratio between the SRI's operating frequencies with and without an LVC deployed

$$F_R=\frac{f_{\min}+\Delta f_1-\Delta f_{\text{reduction}}}{f_{\min}+\Delta f_1}. \tag{26}$$

Since the operating input voltage, voltage gain, and loads are the same for both systems, the conduction losses in inverter switches do not differ between the two designs. Switching losses are directly proportional to the switching frequency, favoring LVC-based designs operating at lower frequencies. For inductors, variations in core loss are attributed to the frequency-dependent Steinmetz term f^{α}, as $\Delta\beta$ is identical for both designs under identical load currents. Parameter α is the core material-dependent and typically ranges between 1.8 and 2 for high-frequency magnetic materials, such as PC200 [27]. Inductor copper loss is affected by both the skin and proximity effects. Since the inductor used in this research employed subskin-depth size Litz wire with a short twisting pitch length, the skin effect loss variation can be neglected at both strand and bundle levels. However, the strand level proximity effect varies with f^2 as described in [28], favoring the LVC SRI operating at a lower frequency. The resonant capacitor losses are a combination of losses inside the constant capacitor and the LVC. For any load $R>R_{\min}$, the circuit equation is to be solved to calculate C_{LVC} and then compute the total current through C_L and C_{LVC} for the LVC-based design. In the table, r_{CL1} is the equivalent series resistance (ESR) of the constant capacitor C_L used for the non-LVC design. $r_{CL2}$and r_{LVC} are the ESRs of C_L and C_{LVC} for the LVC-based design, respectively. The expressions are derived assuming m=0.5.

B. Analyzing the Effect of LVC on the ZVS Condition of an SRI

SRI systems with and without LVC are designed to maintain constant M_v for a specified load variation. Since both systems operate with identical input voltage, voltage gain, and load conditions, their net impedance seen by the inverter is the same. The key distinction is that the LVC system achieves the same impedance angle at a lower switching frequency than an equivalent non-LVC system. This allows LVC-based systems to facilitate ZVS for lower current phase lagging, thereby enabling soft switching at lighter loads, less circulating reactive power, and, consequently, higher efficiency.

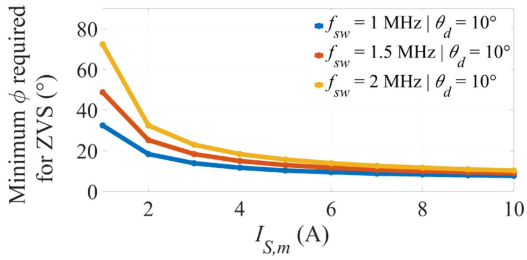


Fig. 12. Effect of switching frequency on required lagging phase under different load currents for V_{DC}=15 V, V_B=1 V, and $C_{oss}(V_{DC})$=200 pF.

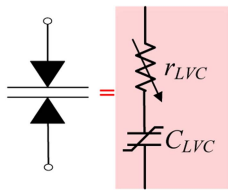


Fig. 13. Equivalent loss model of an LVC.

The charge that load current I_m can provide during dead time t_d for current commutation is:

$$Q_I = -\int_0^{\theta_d}\frac{I_{S,m}\sin(\theta-\phi)}{\omega}d\theta=-\frac{I_{S,m}}{\omega}(\cos\phi-\cos(\phi-\theta_d)) \tag{27}$$

where $I_{S,m}$ is the peak load current, ϕ is the lagging phase, and θ_d is the phase corresponding to dead time t_d. The charge needed to switch polarities of two output capacitors C_{oss} of two half-bridge switches between 0 and V_{DC} is

$$2Q_j(V_{\text{DC}})=2\left[2(V_{\text{DC}}+V_B)C_{\text{oss}}(V_{\text{DC}})\right] \tag{28}$$

where V_B is the body diode forward voltage drop, and $C_{oss}(V_{DC})$ is the switch output capacitance dependent on the blocking voltage V_{DC}. For the ZVS condition, the load current charge should be enough to charge/discharge the two capacitors, resulting in the inequality $Q_I>2Q_j(V_{DC})$.

A plot depicting the relationship between the required minimum ϕ and $I_{S,m}$ is presented in Fig. 12 for constant θ_d. It is observed that, under light load conditions, low-frequency systems can ensure ZVS with lower ϕ values. On the other hand, under high load conditions, the difference becomes almost negligible.

C. Equivalent Loss Model of an LVC

The equivalent loss model of an LVC is shown in Fig. 13, with r_{LVC} being the LVC equivalent series resistance. r_{LVC} represents the sum of the resistances of the undepleted active layers, spreading resistance, and ohmic contact resistance [29],

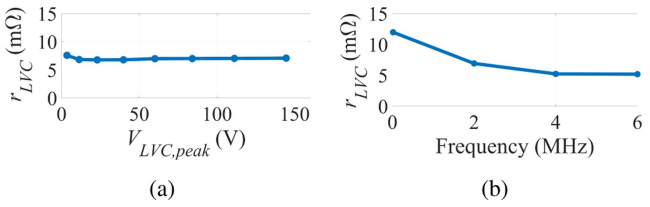


Fig. 14. R_{LVC} for an LVC made of two diodes RB238T150 (a) versuspeak voltage at 2 MHz and (b) versus frequency.

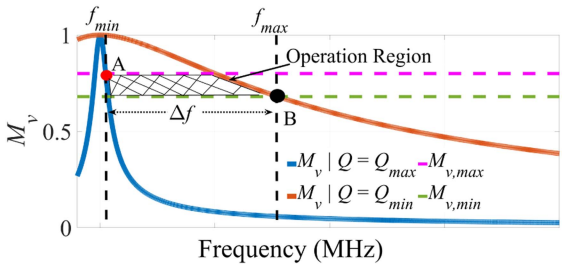


Fig. 15. Operation region of a full-bridge SRI with a linear capacitor for variable load and input DC voltage.

[30]. Measuring r_{LVC} presents a challenge due to significant junction reactance in series with r_{LVC} in the blocking state, making it difficult to measure through dc measurement techniques. Moreover, high reactance makes it challenging to estimate r_{LVC} with RF-based extraction methods [31].

LVC losses are simulated in LTspice with the LVC made of two RB238T150 diodes to characterize its high-frequency ac resistance for LVC applications. The resultant r_{LVC} values are shown in Fig. 14. It is observed that r_{LVC} is relatively small and reduces with higher frequency and applied voltage. A significant challenge with these results is that manufacturers rarely characterize diodes in the MHz range in blocking mode. Consequently, the existing simulation models may not accurately reflect loss modeling. Therefore, obtaining an accurate characterization of the LVC loss model remains a challenge.

IV. Analysis and Design of a Frequency-Regulated LVC-Based SRI for Variable R and V_{DC}

Often, an SRI is designed with the expectation to operate under a variable input voltage condition along with the load variation, demanding a more robust controller with a larger Δf to regulate V_{out}. The operating region for a full-bridge SRI with a constant capacitor under R and V_{DC} variation is illustrated in Fig. 15. Four lines bind the region: the two horizontal lines are the M_v values required for $V_{DC} = V_{DC,max}$ ($M_{v,min}$) and $V_{DC} = V_{DC,min}$ ($M_{v,max}$) operations, while the other two M_v side lines belong to gain plots derived for the minimum and maximum loads. Frequency band Δf is the difference between frequencies at point A (f_{min}) and point B (f_{max}).

This analysis compares conventional SRI with a constant capacitor and an LVC-based SRI with a parallel combination of a constant capacitor and an LVC, as illustrated in Fig. 3(a). In both cases, the system is designed to achieve the same output voltage

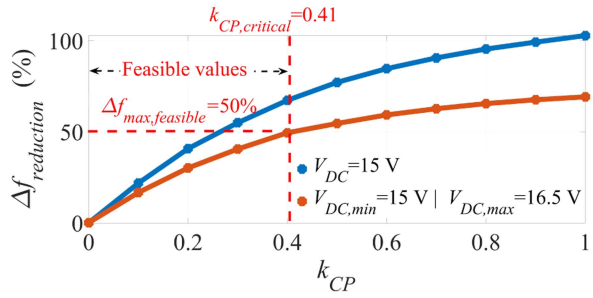


Fig. 16. Impact of V_{DC} variation on $\Delta f_{reduction}$.

and switching frequency at CDP (labeled with a red dot in Fig. 15) characterized by maximum load R_{min} and minimum input voltage $V_{DC,min}$. The equivalent capacitance of both designs must be the same at the CDP, and it can be expressed by rewriting (3) as

$$C_r = \left(\omega_{min} L_r / R_{min} - \sqrt{1/M_{v,max}^2 - 1}\right) / (\omega_{min} R_{min}). \tag{29}$$

The SRI circuit with constant capacitor described in Section II is analyzed considering a 10% variation of $V_{DC,min}$ (15–16.5 V), resulting in $M_{v,max}$ range between 0.80 and 0.72. CDP A remains the same as in the SRI circuit with a constant input voltage of 15 V. Maximum frequency f_{max} is obtained to be 1.668 MHz for $R_{max} = 50\ \Omega$ and $V_{DC,max}$ =16.5 V. Frequency band Δf is calculated to be 0.62 MHz.

For an SRI with an integrated LVC, the analysis is similar to the one described in Section II. Starting from the C_r value at CDP, $C_{eq,j0}$ is calculated using (4)–(13) for given diode parameters m and V_B. After $C_{eq,j0}$ is calculated, C_{LVC} is obtained for the operational frequency, load, and input voltage by solving (14)–(17). M_v is then calculated using (1) for the range of operating frequencies and loads. As already mentioned, an explicit solution of $C_{eq,j0}$ and C_{LVC} is possible only for $m = 0.5$, while for other LVCs, (4)–(17) must be solved numerically. $C_{eq,j0}$ for the harmonicless case of m=0.5 is calculated using (20) at the CDP A. To calculate M_v for different operating points, the SRI is solved using a quartic equation for steady-state values of circuit parameters (21).

An SRI with an integrated LVC made of diodes RB238T150 ($m = 0.5$, $V_B = 0.5$) is analyzed for k_{CP} varying from 0 to 1. Δf reduction for the SRI with 10% variation of V_{DC} and with constant V_{DC} is plotted in Fig. 16. It can be observed that achievable $\Delta f_{reduction}$ decreases from 67% to 50% for $k_{C,critical}$ for the SRI with 10% V_{DC} variation compared to the constant V_{DC} operation. Moreover, $\Delta f_{reduction}$ reduces more with the increase in V_{DC} variation, revealing a limitation of the LVC deployment in an SRI. However, $k_{C,critical}$ remains the same as the CDP is the same for both systems.

V. Experimental Setup and Validation

This section describes the experimental setup and presents experimental results to verify the analysis of an SRI with an added LVC. Two experimental SRI systems (SRI-1 and SRI-2)

TABLE III
SPECIFICATIONS OF SELECTED LVCS

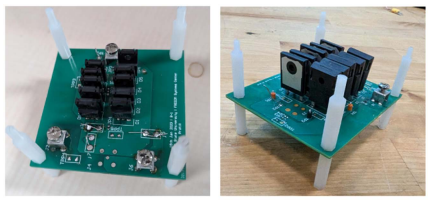
Diode Specifications	LVC-D1	LVC-D2
Part Number	RB238T150NZC9	C6D50065H
Voltage Rating	150 V	650 V
Number of Diodes	20	10

TABLE IV
EXPERIMENTAL SETUP FOR SRI TESTING

Equipment	Specification
Full-Bridge Inverter	Custom PCB built using two half-bridge evaluation boards GS-EVB-HB-61008P-ON (GaN devices GS61008P)
Capacitor | C_r,C_L	Johnson Technology | 1111 S42E-Series Capacitors
Variable Inductor | L_r	New England Litz Wire | Strand AWG 48 | No. of strands 2200
Resistor | R	OHMITE TGHM series | 300 W | 10 MHz

(a) (b) (c) (d)

Fig. 17. Experimental setup elements. (a) Full-bridge inverter. (b) Auxiliary board for the constant capacitor. (c) Air-core coaxial coupled inductor. (d) Resistive loads on a heat sink.



(a) (b)

Fig. 18. LVCs made from discreet diodes for SRI testing. (a) LVC-D1. (b) LVC-D2.

are designed to measure the control band Δf to validate the analysis. The circuit characteristics of the two testing setups are listed in Table I for the constant capacitor case $k_{\mathrm{CP}} = 0$. The two systems are designed to have the same f_r and Δf for $k_{\mathrm{CP}} = 0$, resulting in the same component values and load variation range. The difference is that SRI-2 is supplied by twice the voltage V_{DC} used for SRI-1, capable of delivering four times more P_{out}.

The specifications of an LVC selected for experimental testing are presented in Table III. The SRI-1 setup is tested for $k_{\mathrm{CP}} = 0.29$ using an LVC made of RB238T150NZC9 diodes (LVC-D1). The SRI-2 setup is tested for $k_{CP} = 0.35$ using an LVC made from higher rated C6D50065H diodes (LVC-D2). Circuit components used for experimental setups are listed in Table IV and shown in Fig. 17. The systems comprise a gallium nitride (GaN)-based full-bridge inverter, a variable air-core inductor used as a resonant inductor, and high-quality ceramic capacitors used as constant capacitors. A printed circuit board (PCB) is designed to combine multiple diodes to form LVC-D1, as shown in Fig. 18.

The high Q operating point determines the LVC voltage rating as

$$V_{\mathrm{LVC,max}} = V_{\mathrm{in},m} Q_{\max} M_V = \frac{4V_{\mathrm{DC}}}{\pi} Q_{\max} M_V. \tag{30}$$

For the LVC-D1 diode used in the SRI-1 setup, the maximum V_{LVC} is determined to be 122 V, while the chosen LVC diode has a rating of 150 V and m=0.5 capacitance profile. In the SRI-2 setup, the maximum V_{LVC} is calculated to be 244 V. The ideal LVC diode for this experiment would have a rating between 300 and 400 V. The 650-V LVC-D2 diode was selected due to its m=0.58 being far from the commonly found m=0.5 and to investigate the impact of larger package diodes.

In their operation, LVCs do not exhibit direct current conduction; instead, they conduct displacement current or, in other words, they capacitively couple current through the junction capacitance. Generally, diodes rated for higher direct current have a large junction area, leading to more junction capacitance. On the contrary, LVCs with smaller package discrete diodes and the same voltage requirements would demand more diodes to achieve the required $C_{eq,j0}$ capacitance and the displacement current rating. The assembly of a higher number of smaller package diodes for LVCs may lead to more parasitic losses. Therefore, an integrated LVC design is needed in the future, not optimized for direct current but rather for the *pn* junction capacitance value and voltage rating.

The experiment is conducted in three stages to obtain voltage gain plots as a function of frequency. At first, the SRI with the constant capacitor only ($k_{\mathrm{CP}} = 0$) is tuned to resonate at $f_r = 1$ MHz. Thereafter, the SRI is connected to a dc source and tested by varying the switching frequency for different resistive loads. The circuit parameters are noted, and voltage gains are calculated. Finally, the constant capacitor is replaced by the parallel combination of linear capacitors and the LVC, and power tests are repeated.

A. Experimental Results for SRI-1

The SRI circuit with the constant capacitance $C_r = 4$ nF and load $R = 5\ \Omega$ is tuned to 1 MHz using a vector network analyzer (VNA). The resonant inductance is tuned to $L_r = 6.33\ \mu$H, close to the design value of 6.36 μH. The SRI is then connected to a dc voltage source and tested by varying switching frequency between 0.75 and 2 MHz for resistive loads $R =$ 5, 10, 25, and 50 Ω. The experimental setup is shown in Fig. 19. The analytical $M_{v,\mathrm{Cal.}}$ and experimental $M_{v,\mathrm{Exp.}}$ voltage gains for four loads are presented in Fig. 20, and they match each other. The experimental gains are calculated by extracting the first harmonic of V_{in} and V_{out}.

Next, capacitor C_r is replaced by the C_L-LVC-D1 pair, resulting in $k_{\mathrm{CP}} = 0.29$. C_L is calculated to be 2.98 nF, and $C_{\mathrm{LVC}} = 1$nF is expected to be achieved at the CDP. Diode RB238T150NZC9 with experimentally characterized parameters $C_{j0} = 1.62$, $m = 0.51$, and $V_B = 0.74$ is selected for this LVC. LVC-D1 is designed with a total of 20 diodes (10 C_{j0}). The analytical and experimental M_v plots are presented in Fig. 21, and they closely follow each other. Analytically calculated Δf relative to the linear case as a function of load R is presented

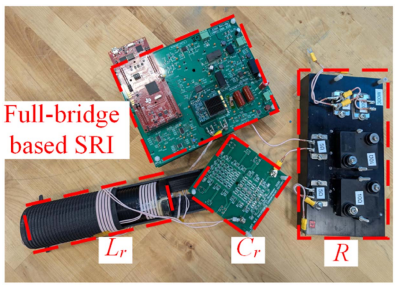


Fig. 19. Experimental setup used for tuning and testing SRI with a constant capacitor ($k_{CP} = 0$).

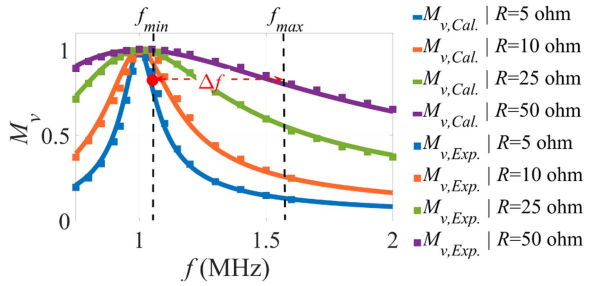


Fig. 20. $M_{v,\text{Cal.}}$ and $M_{v,\text{Exp.}}$ as a function of frequency in SRI-1 with a constant capacitor ($k_{CP} = 0$) and for four loads.

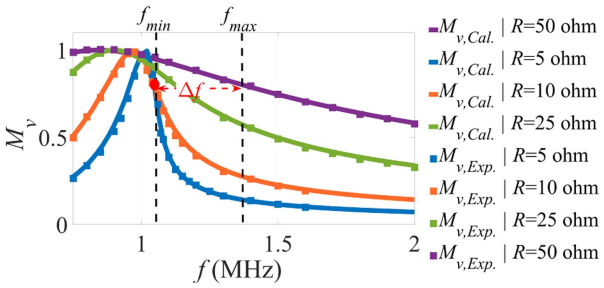


Fig. 21. $M_{v,\text{Cal.}}$ and $M_{v,\text{Exp.}}$ as a function of frequency in SRI-1 with LVC-D1 for $k_{CP} = 0.29$ and four different loads.

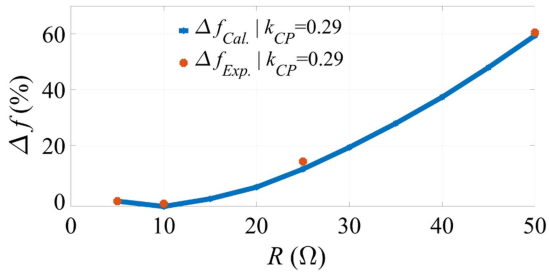


Fig. 22. Analytically calculated Δf relative to the benchmark linear case as a function of R and four experimental values measured in SRI-1 with LVC-D1.

in Fig. 22 together with four experimental values measured for four loads. The experimental points closely follow the analytical curve with a maximum error of 3% for $R = 25\ \Omega$. Calculated and experimentally measured $\Delta f_{\text{reduction}}$ are 40.6% and 39.50%, respectively. Simulated and experimentally measured phases between the inverter voltage and load current are shown in Fig. 23

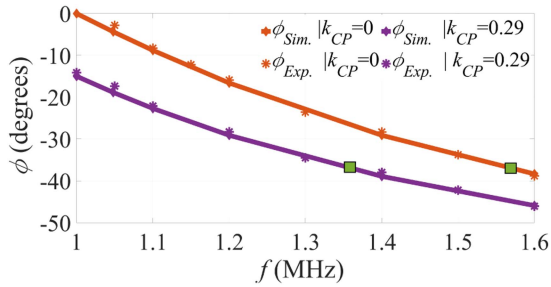


Fig. 23. Phase of the input impedance of SRI resonant network seen by the inverter for $R = 50\ \Omega$ and $k_{CP} = 0$ and 0.29 in SRI-1 with LVC-D1. The two green markers represent the two operating points.

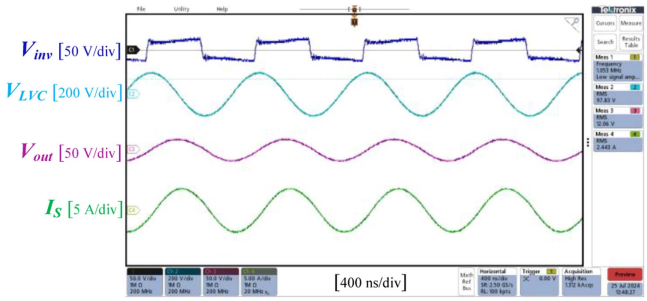


Fig. 24. Experimental waveforms of SRI-1 with LVC-D1 for $R = 5\ \Omega$ operating close to resonant frequency at 1.05 MHz.

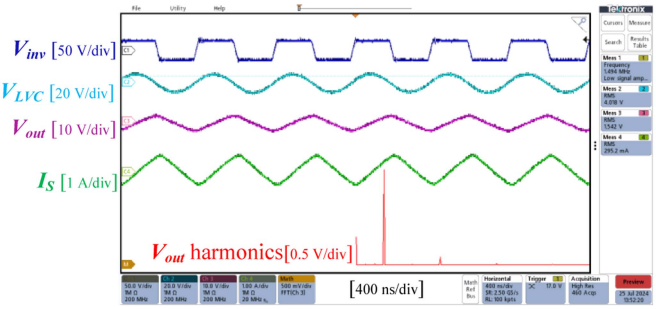


Fig. 25. Experimental waveforms of SRI-1 with LVC-D1 for $R = 50\ \Omega$ operating at 1.495 MHz.

for light load $R = 50\ \Omega$. It is observed that experimental and analytically calculated phase match well, and that the difference reduces with frequency.

The experimental waveform for full-bridge SRI with constant capacitor C_L and an LVC-D1 at rated load and light load conditions is shown in Figs. 24 and 25, respectively. Voltage and current waveforms are sinusoidal at the rated load, but harmonics appear at the light load. Therefore, the first harmonic of experimental voltages is calculated for fair comparison with analytical gain calculations.

In the following experimentation, V_{DC} is varied 10%, from 15 to 16.5 V. To maintain the same V_{out}, the voltage gain must be reduced by 10% to $M_v = 0.72$. The analytical SRI-1 model for $k_{CP} = 0$ and $k_{CP} = 0.29$ predicts this M_v to be achieved at 1.76 and 1.55 MHz, which is close to the experimentally measure

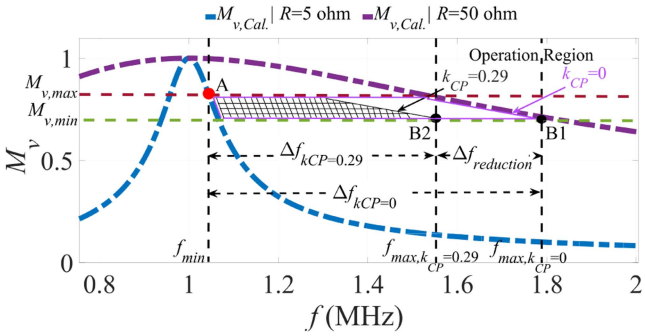


Fig. 26. SRI-1 operating region for $k_{CP}=0$ and $k_{CP}=0.29$ and V_{DC} varying between 15 and 16.5 V.

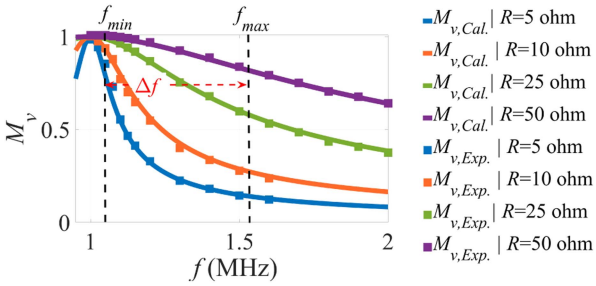


Fig. 27. $M_{v,\text{Cal.}}$ and $M_{v,\text{Exp.}}$ as a function of frequency in SRI-2 with a constant capacitor ($k_{\text{CP}}=0$) for four loads.

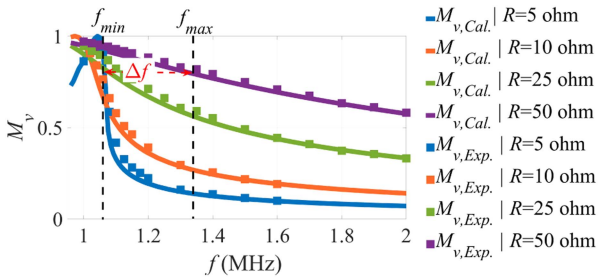


Fig. 28. $M_{v,\text{Cal.}}$ and $M_{v,\text{Exp.}}$ as a function of frequency in SRI-2 with LVC-D2 for $k_{\text{CP}}=0.35$ and four different loads.

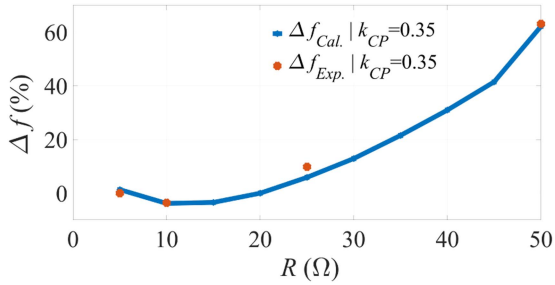


Fig. 29. Analytically calculated Δf relative to the linear case as a function of R and four experimental values measured in SRI-2 with LVC-D2.

values of 1.795 and 1.539 MHz, respectively. The experimental $\Delta f_{\text{reduction}}$ is calculated to be 34.3%, a reduction from 39.5% for the $V_{\text{DC}}=15$ V case. The SRI-1 operating region for $k_{\text{CP}}=0$ and $k_{\text{CP}}=0.29$ and variable load and V_{DC} is shown in Fig. 26. The analytical gain curves for R_{max} and R_{min} and experimental boundary points (A, B1) mark the operating zone for $k_{\text{CP}}=0$. When LVC is deployed, the operating region is bound by point B2, shrinking significantly from the case when only C_L is employed.

The parasitic inductance of the PCB and diode packages may influence the SRI operation at higher frequencies. The effect of parasitic PCB and package inductances is studied in [21]. The experimental results remain unaffected, as the frequency range is confined to 2 MHz, which is significantly below the 3 MHz where parasitics begin to have a more notable impact on LVC-D1 operation [21].

B. Experimental Results for SRI-2

The objective of this experimentation is to verify the validity of the model and the design procedure for another LVC (LVC-D2) and a different k_{CP} parameter ($k_{\text{CP}}=0.35$). Similar to the test procedure for SRI-1, the SRI-2 circuit with constant capacitor $C_r=4$ nF at $k_{\text{CP}}=0$ and $R=5\ \Omega$ is tuned to resonate at 1 MHz using a variable inductor and a VNA. SRI-2 is then tested by varying the switching frequency between 0.75MHz and 2MHz for the four resistive loads $R=5$, 10, 25, and 50 Ω. The analytically $M_{v,\text{Cal.}}$ and experimentally $M_{v,\text{Exp.}}$ derived voltage gains for four loads are presented in Fig. 27, closely matching each other. Next, capacitor C_r is replaced by the C_L-LVC-D2 pair, resulting in $k_{\text{CP}}=0.35$. C_L and C_{LVC} are calculated to be 2.6 and 1.4 nF at the CDP A, respectively. Diode C6D50065H used for LVC-D2 is experimentally characterized, and its parameters are $C_{j0}=3.3$ nF, $m=0.58$, and $V_B=3.4$ V. LVC-D2 is designed with a total of 10 diodes (5 C_{j0}), establishing $k_{\text{CP}}=0.35$. Analytical and experimental M_v plots are presented in Fig. 28. They mostly follow each other with a slight deviation at high load due to an imperfection in tuning the experimental setup. However, its effect on Δf is negligible as it affects both f_{min} and f_{max}. Analytically calculated Δf relative to the linear case as a function of load, together with four experimental points, are shown in Fig. 29. The experimental points reside on or close to the analytical curve. The calculated and experimental values of $\Delta f_{\text{reduction}}$ are 37.9% and 37%, respectively. Simulated and measured phase differences between V_{in} and V_{out} are shown in Fig. 30 for light load $R=50\ \Omega$, showing a good match.

SRI-2 is also tested while varying V_{DC} from 30 to 33 V. This requires the voltage gain M_v to be varied between 0.8 and 0.72 for the same output voltage. The calculated frequencies for $k_{\text{CP}}=0$ and $k_{\text{CP}}=0.35$ to achieve these gains are 1.76 and 1.57 MHz, close to the experimental values of 1.77 and 1.54 MHz, respectively. Experimental $\Delta f_{\text{reduction}}$ is found to be 31.6%, reduced from 37% for constant V_{DC}.

C. Experimental Efficiency of an SRI With an LVC

Theoretically, it is expected that an SRI with an LVC will demonstrate the same or better efficiency than a conventional SRI. This is because the inclusion of LVC reduces the operating frequency and extends the ZVS range at light load, reducing

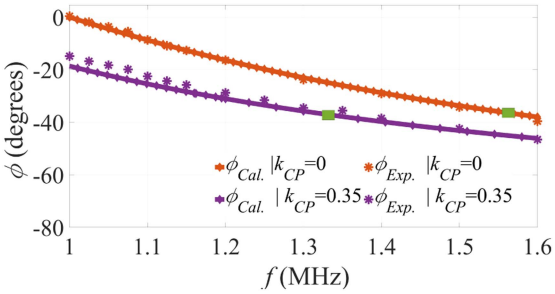


Fig. 30. Phase of the SRI resonant network impedance seen for $R = 50\ \Omega$ and $k_{CP} = 0$ and 0.35 in SRI-2 with LVC-D2. The two green markers represent the two operating points.

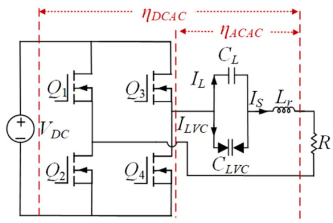


Fig. 31. Definition of η_{DCAC} and η_{ACAC} efficiencies.

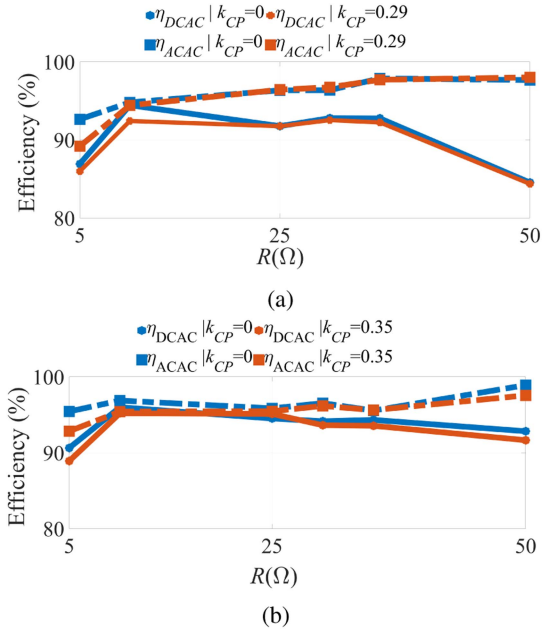


Fig. 32. Experimentally measured efficiencies η_{DCAC} and η_{ACAC} as a function of load. (a) SRI-1 with LVC-D1 for $k_{CP} = 0$ and $k_{CP} = 0.29$. (b) SRI-2 with LVC-D2 for $k_{CP} = 0$ and $k_{CP} = 0.35$.

switching losses. Moreover, the LVC itself is expected to have low losses and high-quality factors because of its dominant operation under reverse-biased conditions. Two efficiencies, η_{DCAC} and η_{ACAC}, are experimentally measured to compare losses in SRIs with and without LVC for a constant gain operation. The input and output ports for efficiency measurements are marked in Fig. 31. η_{DCAC} represents the overall SRI efficiency and is measured from the dc input power source to the load. η_{ACAC} represents the resonant network efficiency and is measured from the full-bridge output to the load. The experimental efficiencies of SRI-1 and SRI-2 with and without LVCs are presented in Fig. 32(a) and (b), respectively. It is observed that η_{ACAC} increases as the load decreases. The LVC-based resonant network is less efficient at CDP A than in the C_L-only case, but the difference between them significantly reduces as the load drops. Thermal images of PCBs containing LVC and C_L are shown in Fig. 33(a) and (b) for SRI-1 and SRI-2 systems, respectively. For the low-power SRI-1 system, almost no temperature change is observed in LVC-D1 diodes while operating at CDP A, but thermal hotspots are observed on the PCB. This is due to low current (only 63 mA) flowing through each of the 20 diodes with no exposed thermal cases. Similar thermal tests are conducted for the high-power SRI-2 system, and a 9°C temperature increase is observed on the exposed thermal cases of the LVC-D2 diodes and thermal hotspots on the PCB. This time, 300 mA flows through each of the 10 diodes of LVC-D2 with exposed thermal cases. The thermal hotspots on the PCB are attributed to the resistive jumpers and PCB trace resistances. This thermal analysis revealed that the difference in η_{ACAC} under high load could be attributed to PCB and package parasitics.

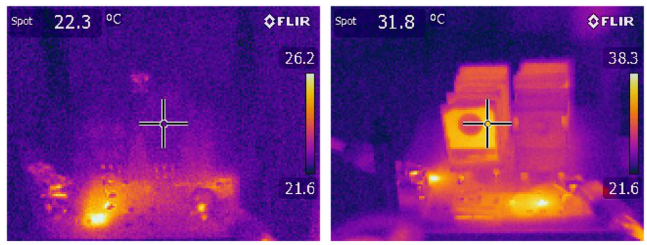


Fig. 33. Thermal images of the PCB containing LVC and C_L under operation at CDP A. (a) SRI-1 with LVC-D1 for $k_{CP} = 0.29$. (b) SRI-2 with LVC-D2 for $k_{CP} = 0.35$.

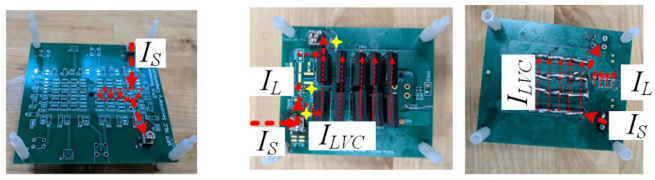


Fig. 34. Current conduction paths on PCBs used for SRI-2. (a) C_r. (b) LVC-D2 and C_L (top and bottom view).

Current conduction paths are marked on SRI-2 constant-capacitor and LVC-D2 PCBs, as shown in Fig. 34. The constant-capacitor PCB contains only traces for paralleled high-Q capacitors. On the other hand, the joint (LVC-D2)-C_L PCB contains three resistive jumpers along the current path, marked with yellow stars in the figure. The same jumpers are identified

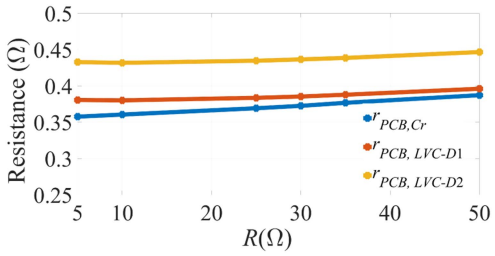


Fig. 35. Experimentally measured ESR of conduction paths of PCBs used for C_r, LVC-D1, and LVC-D2.

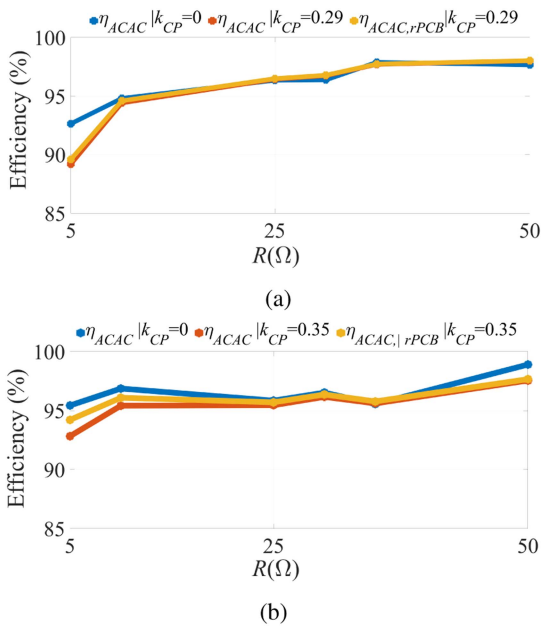


Fig. 36. Effect of PCB parasitic resistance on efficiency. (a) SRI-1. (a) SRI-2.

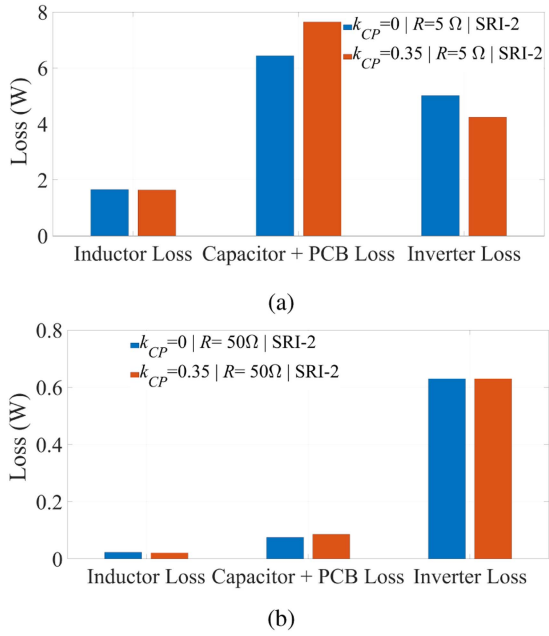


Fig. 37. Loss breakdown for SRI-2 design with and without LVC under (a) $R = 5\ \Omega$. (b) $R = 50\ \Omega$ loading conditions.

as hotspots in Fig. 33(b). To get an estimate of the elevated PCB's parasitic ESR, an impedance measurement with a VNA is conducted by shorting the LVC and C_L for the LVC-based design and shorting C_r for the constant capacitor design. The PCB parasitic resistances are plotted in Fig. 35, showing that the resistance of LVC-D1 PCB $r_{\text{PCB,LVC}-D1}$ and LVC-D2 PCB $r_{\text{PCB,LVC}-D2}$ are approximately 7% and 21% higher than the C_r $r_{\text{PCB},Cr}$ PCB resistance, respectively. The difference between the path resistances is analytically removed from experimentally measured values for a fair efficiency comparison. The resulting efficiency plots are shown in Fig. 36(a) and (b) for SRI-1 and SRI-2, respectively. It is observed that the PCB ESR has minimal effect on the efficiency of SRI-1 with LVC-D1, while they contribute to almost 50% of the loss difference for SRI-2 between the C_r and LVC-D2 systems. The remaining loss difference could be attributed to the loss inside the LVC diode packages. A major difference between constant-capacitor and LVC designs is the package itself. C_r capacitance is made of six parallel surface mount capacitors of the 1111 package intended for RF applications, while LVC diodes have large surface areas and long leads for power applications. LVC-D1 is made using 20 pieces of TO220FN package with 15-mm long leads. LVC-D2 is built using 10 pieces of TO-247-2 package with 20-mm long leads. The skin and eddy effect in the 1–2 MHz frequency range could be the source of extra losses. This problem can be resolved by manufacturing an integrated LVC with an RF package for MHz range operation. When comparing the overall efficiency of LVC and non-LVC designs, it is observed in Fig. 32 that η_{DCAC} increases and then decreases as a function of load in both SRI systems. The efficiency increase could be because of lower switching losses as the switching current is reduced to 50% at $R = 10\ \Omega$ compared to $R = 5\ \Omega$. The cause of the efficiency reduction for $R > 10\ \Omega$ might be because of the increased switching losses at higher frequencies. The overall LVC and non-LVC system efficiency is almost the same for light loads, as higher conduction losses in LVC diodes and PCB parasitics are offset by lower switching losses due to lower operating frequency. This leads to the same conclusion as above that an integrated LVC design would benefit the SRI+LVC efficiency. Fig. 37 illustrates the breakdown loss on the example of the SRI-2 design for two compensation cases (k_{CP}=0 and k_{CP}=0.35) and two loads (R=5 Ω and R=50 Ω). *Inductor losses* are calculated based on experimental load currents and ESR measurements at the operating frequency [32]. *Capacitor+PCB losses* were computed using experimental current measurements, measured PCB parasitics, and C_L capacitor quality factors obtained from its datasheet. Due to the C_L's high-quality factor, the *Capacitor+PCB losses* are dominated by PCB parasitics for k_{CP}=0 and PCB and LVC package parasitics for k_{CP}=0.35 designs. *Inverter losses* were measured utilizing the oscilloscope power calculation functionality.

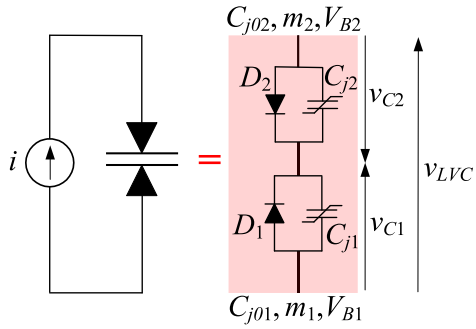


Fig. 38. Equivalent LVC circuit consisting of two diodes with different nonlinear capacitance parameters.

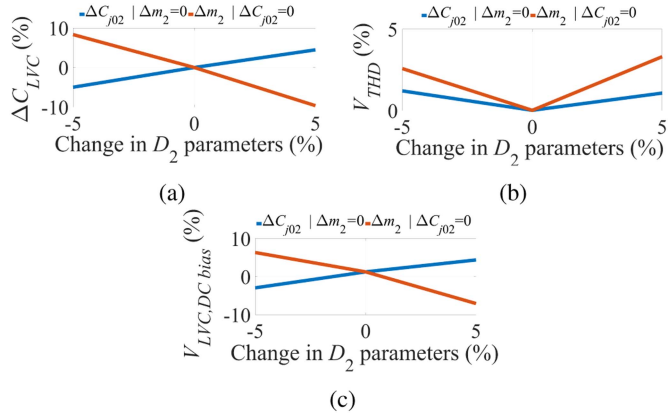


Fig. 39. Effect of D_2 parameter variation on a current-supplied LVC for $I_m = 0.5$ A and $f = 1$ MHz. The nominal D_1 and D_2 parameters are based on diode GD2 [21]. (a) Effect on the equivalent LVC capacitance. (b) Effect on the voltage signal THD. (c) Effect on the DC bias of the voltage signal.

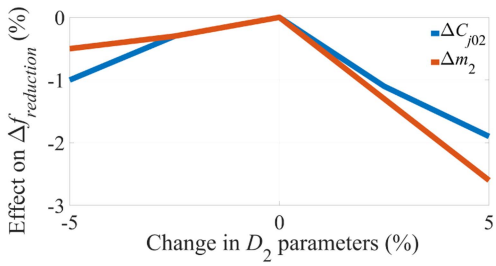


Fig. 40. Effect of nonhomogeneity on $\Delta f_{reduction}$ for variation of ΔC_{j02} and Δm_2.

VI. Considerations for Application of LVCs

This section discusses the impact of key application considerations, including device heterogeneity and temperature effects, as well as the limitations and research opportunities for integrating LVCs within the broader field of power electronics.

A. Effect of Heterogeneity on LVC and SRI Characteristics:

The LVC capacitance model used in this research is derived for homogeneous LVCs [21], i.e., the LVC is assumed to be composed of identical diodes D_1 and D_2 with the same nonlinear capacitance profiles, $C_{j1}(V)$=$C_{j2}(V)$, as shown in Fig. 38. However, manufacturing identical diodes may not be possible because of imperfections in the manufacturing process. An LTspice simulation model is built to vary the D_2 capacitance parameters C_{j02} and m_2 for analyzing their effect on the LVC connected to a current source. The nominal diode parameters are adopted as C_{j01}= C_{j02}=10 nF, m_1=m_2=0.5, and V_{B1}=V_{B2}=0.5 V. A current source supplies the LVC at I_m=0.5 A and f=1 MHz. D_1 parameters are fixed at the nominal values, while D_2 parameters C_{j02} and m_2 vary ±5% with respect to their nominal value. Two cases are considered: (a) varying C_{j02} while keeping m_2 at the nominal value and (b) varying m_2 while keeping C_{j02} at its nominal value. The relative change in the equivalent LVC capacitance with respect to the nominal value for the variation of D_2 parameters is presented in Fig. 39(a). It is observed that the change in C_{LVC} is linear but asymmetric across the nominal point as D_2 parameters vary. The total variation in C_{LVC} for the net 10% variation of the selected parameter is approximately 10% for ΔC_{j02} and 18% for Δm_2. It is observed that C_{j02} reduction causes the voltage magnitude across D_2 to be much greater than that across D_1. It is understood that a large voltage swing allows D_2 to create the same current for diodes with lower C_{j02}, resulting in higher THD and nonzero dc bias voltage. The THD of the voltage signal of a current-supplied LVC as a function of the relative change in D_2 parameters is presented in Fig. 39(b). Overall, THD increases as either m_2 or C_{j02} deviates from their nominal values in either direction, with m_2 impacting the THD more. Moreover, the D_2 parameter deviation leads to the appearance of a dc bias voltage across the LVC. The dc bias voltage of a current-supplied LVC as a function of a relative change in D_2 parameters is presented in Fig. 39(c) after being normalized with the peak value of V_{LVC} obtained for identical diodes. The total variation in $V_{LVC,DCbias}$ for the net 10% variation of the selected parameter is approximately 8% for ΔC_{j02} and 12% for Δm_2. The effect of a nonhomogeneous LVC on SRI operation is studied through LTspice simulations on the example of the baseline SRI system in Table I for k_C=0.25 and an LVC made with RB238T150 diodes. The analysis evaluates the impact of C_{j0} and m mismatch of up to ±5% on $\Delta f_{reduction}$ at boundary operating points A and B, and the results are shown in Fig. 40. It is observed that $\Delta f_{reduction}$ reduces by approximately 2.5% for the maximum LVC nonhomogeneity. The LVCs used in this research are constructed by paralleling multiple discrete diodes, helping average out individual nonuniformities and making a more homogeneous LVC.

B. Effect of Temperature on LVC Characteristics and Its Impact on SRI Operation:

When designing LVC applications for resonant converters, it is crucial to understand how junction temperature affects the resulting LVC capacitance. As no diode datasheet provides a temperature-dependent junction capacitance model, this effect can be analyzed using the known temperature dependence models of V_B and C_{j0} [24]. The $V_B(T)$ as a function of temperature

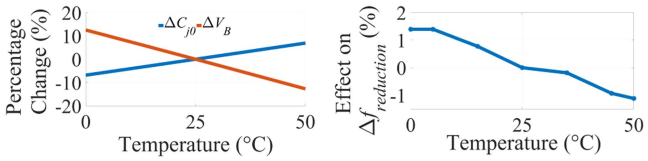


Fig. 41. Effect of temperature variation (a) on parameters of RB238T150 diode deployed in the LVC (C_{j0}=16.2 nF, m=0.5, V_B=0.5) and (b) on $\Delta f_{reduction}$ for the k_C=0.25 case.

is given by

$$V_B(T) = V_B(T_{\text{nom}})\frac{T}{T_{\text{nom}}} + \frac{2kT}{q}\ln\left(\frac{n_i(T_{\text{nom}})}{n_i(T)}\right) \tag{31}$$

where T is the junction temperature in Kelvin, T_{nom}=298 °K (25°C), k is Boltzmann's constant, q is the charge of an electron, and n_i is the intrinsic carrier concentration in cm^{-3}, which is itself temperature dependent. $n_i(T)$ is given by

$$n_i(T) = 1.45\cdot 10^{10}\left(\frac{T}{T_{\text{nom}}}\right)^{1.5} e^{\left\{\left[\frac{q}{2k}\right]\left[\frac{E_g(T_{\text{nom}})}{T_{\text{nom}}}-\frac{E_g(T)}{T}\right]\right\}} \tag{32}$$

where $E_g(T)$ is the energy gap temperature-dependent function (in eVs) for silicon. Based on experimental data, $E_g(T)$ is estimated as [24]

$$E_g(T) = 1.16 - \frac{7.02\cdot 10^{-4}\cdot T^2}{T+1108}. \tag{33}$$

The C_{j0} temperature dependence is calculated using m and V_B as [24]

$$C_{J0}(T) = C_{J0}(T_{\text{nom}})\left[\begin{array}{c}1+4*10^{-4}m(T-T_{\text{nom}})\\ +m\left(1-\frac{V_B(T)}{V_B(T_{\text{nom}})}\right)\end{array}\right]. \tag{34}$$

Fig. 41(a) shows the effect of temperature on normalized V_B and C_{j0} of the LVC made of RB238T150 diodes. In Fig. 41(a), V_B shows a negative temperature coefficient, while C_{j0} has a positive one. Equations (31) and (34) are then deployed to analyze the impact of temperature on $\Delta f_{reduction}$ of the SRI with the above LVC and for k_C=0.25, compared to the baseline SRI in Table I. The temperature effect on $\Delta f_{reduction}$ is calculated by determining $f_{\min}$ at $R_{\min}$ and $f_{\max}$ at $R_{\max}$. Fig. 41(b) illustrates the variation in $\Delta f_{reduction}$ relative to the nominal circuit parameters at 25°C. The total change in $\Delta f_{reduction}$ for the temperature variation between 0°C and 50°C is ∼2.5%.

C. Challenges in Implementing LVCs for Broader Power Electronics Applications and Future Research Directions:

1) *Integrated LVC design for parasitic mitigation and enhanced current capability:* The influence of PCB and diode package parasitic inductances is examined in [21]. Larger parasitics can cause self-resonance, which may obstruct the operation of resonant converters, including SRI. Therefore, an integrated LVC with maximum LVC capacitance and minimal parasitic inductance is essential for high-frequency applications. Furthermore, diodes designed to reduce parasitic capacitances result in the LVC current rating being a small fraction of the discrete diode current rating, even at MHz frequencies [21]. Integrated LVCs optimized for maximum junction capacitance and voltage rating can enable higher device utilization and improved power density.
2) *Harmonics and control challenges:* The presence of harmonics in a power topology, including SRI, can result in control and EMI issues and additional losses. In [21], THD of the voltage of a sinusoidal current-supplied LVC is studied as a function of I_m and m. It is concluded that the THD is less than 2% for m<0.6. However, for $m = 0.5$, the LVC operates as a linear device not producing harmonics, which makes diodes with m=0.5 a preferred choice for manufacturing LVCs. Despite aiming for m=0.5, realistic manufacturing processes may still lead to m not equal to 0.5, introducing harmonics.
3) *Effect of dc bias:* Given the scope of our study, we have focused on ac current flowing through LVC to demonstrate its capabilities. However, many applications in power electronics involve some degree of dc voltage that is blocked by the LVC, inserting a dc bias voltage across one of the LVC diodes. Unfortunately, the existing LVC model presented in [21] does not apply in that case, and a more comprehensive analysis incorporating dc bias is required.

VII. Conclusion

This study analyzed the integration of passive LVC devices into an SRI to reduce the frequency control band requirements under variable load and input voltage conditions. An analytical SRI-LVC model is derived and experimentally validated on two setups. It also discusses the impact of key application considerations, including device heterogeneity and temperature effects. The experimental results corroborate the theoretical analysis, demonstrating a frequency band reduction of 39% (37%) for variable load conditions and 34.3% (31.6%) for variable load and dc input voltage for two SRI setups, respectively. This application demonstrates the ability of an LVC to tune resonant circuits, compelling the need to further research and develop integrated LVC devices for improved characteristics and efficiency.

References

[1] J.-P. Vandelac and P. Ziogas, "A DC to DC PWM series resonant converter operated at resonant frequency," *IEEE Trans. Ind. Electron.*, vol. 35, no. 3, pp. 451–460, Aug. 1988.
[2] R. Steigerwald, "A comparison of half-bridge resonant converter topologies," *IEEE Trans. Power Electron.*, vol. 3, no. 2, pp. 174–182, Apr. 1988.
[3] Y. Guan et al., "Analysis and design of high-frequency converter with resistive matching network and spiral inductor," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5062–5075, Jun. 2018.
[4] Y. Han, O. Leitermann, D. A. Jackson, J. M. Rivas, and D. J. Perreault, "Resistance compression networks for radio-frequency power conversion," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 41–53, Jan. 2007.
[5] F. C. Lee, Q. Li, and A. Nabih, "High frequency resonant converters: An overview on the magnetic design and control methods," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 1, pp. 11–23, Feb. 2021.
[6] Y. Wei, A. Mantooth, Q. Luo, and D. Woldegiorgis, "Control strategies generation mechanism for LLC resonant converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2020, pp. 2892–2897.

[7] V. Sidorov, A. Chub, D. Vinnikov, and A. Bakeer, "An overview and comprehensive comparative evaluation of constant-frequency voltage buck control methods for series resonant dc–dc converters," *IEEE Open J. Ind. Electron. Soc.*, vol. 2, pp. 65–79, 2021.
[8] J. Kong, K. M. Smedley, and H. Cheng, "Full-range regulation method for half-bridge series resonant converter," *IEEE Trans. Ind. Electron.*, vol. 70, no. 2, pp. 1905–1915, Feb. 2023.
[9] V. Sidorov, A. Chub, and D. Vinnikov, "Performance improvement of PWM control methods for voltage step-down in series resonant dc–dc converters," *Energies*, vol. 13, no. 17, 2020, Art. no. 4569. [Online]. Available: https://www.mdpi.com/1996-1073/13/17/4569
[10] D. Thenathayalan and J.-H. Park, "Highly flexible high-efficiency multiple-resonant wireless power transfer system using a controllable inductor," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 3, pp. 1914–1930, Sep. 2019.
[11] Z. Zhang, F. Zhu, D. Xu, P. T. Krein, and H. Ma, "An integrated inductive power transfer system design with a variable inductor for misalignment tolerance and battery charging applications," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11544–11556, Nov. 2020.
[12] J. D. Boles, J. J. Piel, N. Elaine, J. E. Bonavia, J. H. Lang, and D. J. Perreault, "Piezoelectric-based power conversion: Recent progress, opportunities, and challenges," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2022, pp. 1–8.
[13] W.-C. B. Liu and P. P. Mercier, "A series/parallel magnetic-less step-down converter based on piezoelectric resonators," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2023, pp. 484–489.
[14] X. Yang, C. Jiao, J. Yang, J. Fan, D. Li, and B. Wang, "Bandwidth enhancement for wireless power transfer system employing non-linear resonator," *IEEE Access*, vol. 9, pp. 485–496, 2021.
[15] W. Zhong and S. Y. Hui, "Reconfigurable wireless power transfer systems with high energy efficiency over wide load range," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 6379–6390, Jul. 2018.
[16] J. Zhang, J. Zhao, Y. Zhang, and F. Deng, "A wireless power transfer system with dual switch-controlled capacitors for efficiency optimization," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6091–6101, Jun. 2020.
[17] L. Zhang et al., "Voltage-controlled capacitor—Feasibility demonstration in DC–DC converters," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 5889–5892, Aug. 2017.
[18] Y. Jiang and B. Zhang, "A fractional-order wireless power transfer system insensitive to resonant frequency," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 5496–5505, May 2020.
[19] O. Abdelatty, X. Wang, and A. Mortazawi, "Position-insensitive wireless power transfer based on nonlinear resonant circuits," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 9, pp. 3844–3855, Sep. 2019.
[20] R. Chai and A. Mortazawi, "A position-insensitive wireless power transfer system employing coupled nonlinear resonators," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 3, pp. 1752–1759, Mar. 2021.
[21] U. Pratik and Z. Pantic, "Comprehensive modeling of a back-to-back diodes-based linear variable capacitor," *IEEE Trans. Power Electron.*, vol. 39, no. 2, pp. 2489–2504, Feb. 2024.
[22] R. Fiore, "ESR losses in ceramic capacitors," Accessed: Jun. 4, 2025. [Online]. Available: https://rfs.kyocera-avx.com/userFiles/uploads/pdfs/esrlosses_appnote.pdf
[23] *Ceramic dielectric capacitors classes i, ii, iii and iv–part i: Characteristics and requirements* EIA Standard EIA-198-1-F, Electronic Industries Alliance (EIA) Nov. 2002, Part I.
[24] H. Russell, "The spice diode model," in *Rectifier Applications Handbook*, W. Rochr, Ed. Denver, Colorado, USA: ON Semiconductor, Nov. 2001, pp. 47–72. [Online]. Available: http://www.introni.it/pdf/Motorola%20-%20Rectifier%20Applications%20Handbook.pdf
[25] S.-H. Ryu, D.-H. Kim, M.-J. Kim, J.-S. Kim, and B.-K. Lee, "Adjustable frequency– Duty-cycle hybrid control strategy for full-bridge series resonant converters in electric vehicle chargers," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5354–5362, Oct. 2014.
[26] S. Neumark, *Solution of Cubic and Quartic Equations*. New York, NY, USA: Elsevier, 2014.
[27] TDK Electronics AG, "High-frequency, low-loss ferrite material PC200," Accessed: Jun. 6, 2025. [Online]. Available: https://product.tdk.com/en/techlibrary/productoverview/ferrite_pc200.html
[28] C. R. Sullivan and R. Y. Zhang, "Analytical model for effects of twisting on litz-wire losses," in *Proc. IEEE 15th Workshop Control Model. Power Electron.*, 2014, pp. 1–10.
[29] L. Dickens, "Spreading resistance as a function of frequency," *IEEE Trans. Microw. Theory Techn.*, vol. 15, no. 2, pp. 101–109, Feb. 1967.
[30] J. Stake, S. Jones, L. Dillner, S. Hollung, and E. Kollberg, "Heterostructure-barrier-varactor design," *IEEE Trans. Microw. Theory Techn.*, vol. 48, no. 4, pp. 677–682, Apr. 2000.
[31] J. Stake, "Planar heterostructure barrier varactor diodes for millimetre wave applications," Doctoral dissertation, 1999. [Online]. Available: https://publications.lib.chalmers.se/records/fulltext/879/879.pdf
[32] U. Pratik and Z. Pantic, "Design of variable air-core coupled co-axial solenoidal inductors," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2022, pp. 1–6.

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