Magnetized Dickson Charge Pump Inverters

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***Abstract*—A class of high step-up single-stage inverters based on magnetically coupled inductors and a Dickson charge pump (CP) technique is presented. Firstly, the magnetized Dickson charge pump inverter (MDCPI) is presented, producing a higher voltage gain with fewer components than its counterparts. Unlike conventional magnetically coupled impedance source networks, the suggested structure provides a substantial voltage boost at a meager shoot-through duty ratio range of 0 to 10%. Thus, it offers a high step-up ability with high modulation index and smaller number of winding turns. Hence, the proposed inverter can be an excellent choice for applications with space constraints where the high output voltage, high power quality, and fewer components are the main issues. However, in addition to drawing discontinuous input current from the dc source, the topology requires tight magnetic coupling to reduce the effect of the leakage inductance. In order to address the aforementioned drawbacks, an improved MDCPI (IMDCPI) is proposed. Although the IMDCPI employs more passive components, it delivers a higher output voltage with reduced dc-link voltage spikes across the inverter bridge. Compared with the existing voltage multipliers such as Dickson, Cockcroft–Walton, and Greinacher, the proposed structures do not require extension by adding extra stages and chains to obtain demanded high voltage. Additionally, the presented topologies solve the conventional voltage multipliers' drawbacks, including output voltage drop and significant voltage stress across the CP cells' capacitors. Input current ripple and flux density of the coupled transformer in IMDCPI is compared with its counterparts to demonstrate its improved features. Detailled experimental results are provided which verify the proposed inverters' performance.**

***Index Terms*—Charge pump (CP) cell, Cockcroft–Walton, Dickson, Greinacher, input current ripple, switched capacitor (SC), voltage multiplier.**

I. Introduction

HIGH step-up converters are operated in various applications, such as medical equipment, energy storage systems (ESSs), motor drives, electric vehicles, high-power electronics appliances, and flexible ac transmission systems (FACTS), to increase the voltage of the energy generated from renewable energy sources (RES) and ESSs, where the output voltage is often low and intermittent. Voltage multipliers and charge pump (CP) cells based on switched-capacitors (SC) circuits shown in Fig. 1, are widely employed for numerous high step-up converters [1], [2], [3]. Cockcroft–Walton and Greinacher voltage multipliers are assumed as one of the most successful step-up cells because of their high step-up ability, high density, low cost, and low voltage stress across the diodes and capacitors [4], [5]. However, using a utility source with a frequency of 50 or 60 Hz, creates a high ripple at the output voltage [3]. In addition, due to the series connection of the capacitors, increasing the number of stages leads to significant output voltage drop under heavy loads. Dickson CP, can overcome this concern by parallel connection of the coupling capacitors to the diode chains. However, Dickson cells still suffer from excessive voltage stress across the last coupling capacitors, equal to the CP output voltage [6], [7]. A hybrid structure illustrated in Fig. 1(i), was proposed to overcome this weakness by integrating Dickson CP and Cockcroft–Walton voltage multiplier [8]. To attain low voltage stress across the capacitors and low output voltage sag, it integrates both series and parallel capacitors simultaneously. Its significant drawback is the use of extra stages consisting of capacitors and diode chains for ultrahigh step-up applications, which makes the converter bulky and complex.

Applying high-frequency magnetically coupled transformers to power electronics converters is a superior approach to improve their performance and step-up ability and avoid adding extra stages. For instance, in [9], a coupled transformer has been exploited in a modified SEPIC dc–dc converter to reach a 400 V dc bus with a low input voltage and duty ratio of 29 V and 53%, respectively. In [10], [11], [12], diverse classes of coupled inductors have been used for ac–ac conversion, where higher gain and lower switching loss are demanded. In [13], coupled inductors is used in ac–dc conversion to improve the efficiency and performance of the rectifiers. By using coupled inductors in ac–dc conversion, the output voltage ripple and electromagnetic interference (EMI) can be reduced and the power factor correction capability can be improved. Additionally, the inductive properties of the coupled inductors can smooth out the rectified output waveform and reduce voltage ripple. In dc–ac inverters, it is desirable to use transformers with low leakage inductance in order to achieve a high modulation index and reduce electrical stresses on semiconductor devices [14].

Over the past decade, magnetically coupled impedance source networks have been implemented in diverse types of shapes such as Γ, FΓ, T, LCCT, Y, and Δ structures [15], [16], [17].

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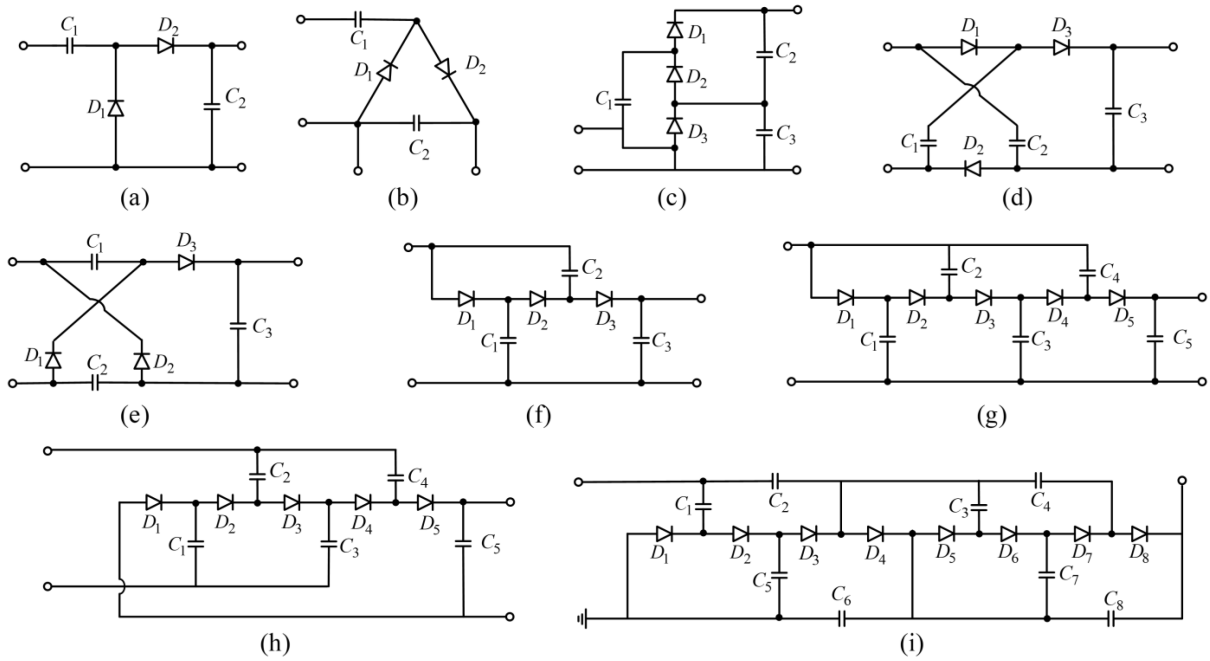


Fig. 1. Overview of various voltage multiplier circuits. (a) Greinacher. (b) Cockcroft–Walton. (c) ladder, (d) VM1. (e)VM2. (f) Original Dickson charge pump. (g) Extended Dickson charge pump. (h) Modified extended Dickson charge pump. (i) Hybrid Cockcroft–Walton and Dickson charge pump.

The critical issue in these networks is that the windings' coupling must be tight to secure minimal leakage inductance at their windings terminal. To eliminate the effects of the leakage inductance, some clamping circuits based on passive or active components have been proposed in [18], [19], [20], [21], [22], [23], [24], [25], and [26]. However, similar to the conventional magnetically coupled impedance source networks, they show a weak boost ability at small shoot-through duty ratio (STDR). It can be crucial for dc–ac conversion where there is a reverse relation between the STDR and modulation index. In [27], [28], and [29], two high-frequency transformers are exploited to induce the inverter to operate at very high modulation ratios. Nevertheless, applying four coupled inductors with two cores is a bulky and lossy approach. To reduce the number of coupled inductors and cores, three-winding switched coupled inductors are proposed in [30], [31], and [32]. Although they use three coupled inductors on the same core, the number of turns of the windings needs to be increased for higher voltage range, which makes the system oversized. Thus, dual-winding magnetically-coupled impedance source networks with high voltage transfer ratio are preferred because of their higher efficiency and density. In [32] and [33], tapped switched coupled-inductor networks based on quasi Z-source network and ΓSN, respectively are proposed. A modular structure of the extensible ZSN was suggested in [34] to get a higher gain. Yet for ultra-high gain applications, extended structures are required, including extra diodes, inductors, and capacitors in each expansion, which increase costs and reduce efficiency. To avoid extending the structures, integration of the voltage multiplier techniques such as Cockcroft–Walton cell and coupled transformer are proposed in [35] and [36].

In this article, two new magnetic coupling inverters named MDCPI and IMDCPI based on Dickson charge pump (DCP) circuits are proposed. Compared with the existing structures, IMDCPI can provide a higher voltage step-up ability, especially in short time STDR range.

This rest of this article is organized as follows. First direct dc–ac conversion concept of the proposed converters is presented in Section II. The operation modes along with theoretical analysis of the MDCPI is provided in Section III. In Section IV, the improved MDCP inverter is presented, where its working principle, circuit analysis, design guidelines, and comparative analysis are investigated in details. In Section V, evaluation results are given to verify the inverters' effectiveness. Finally, Section VI concludes this article

II. Direct DC–AC Conversion Concept

High step-up converters with direct dc–ac conversion are advantageous for RESs and ESSs applications. Fig. 2 illustrates various configurations based on SC structures and magnetic components, termed hybrid SC configurations. Fig. 2(a) depicts a ladder SC structure with a coupled inductor, while Fig. 2(b) shows a configuration using two SCs and one coupled inductor. Both structures utilize a single power switch on the dc side. Topologies shown in Fig. 2(c) and (d) include PWM resonant SC coupled transformers and SC-based active networks, both using two switches on the dc side. The SC-based active network specifically suffers from the additional disadvantage of an unshared ground between the input and output sides. Fig. 2(e) and (f) present two types of SC configurations with two switches on the dc side based on the DCP. As illustrated in Fig. 2, these conventional converters often necessitate an additional dc–dc stage before connecting to a half-bridge or full-bridge inverter, which involves one or two extra power switches. This additional stage increases complexity, component count, and reduces efficiency, while also exacerbating control

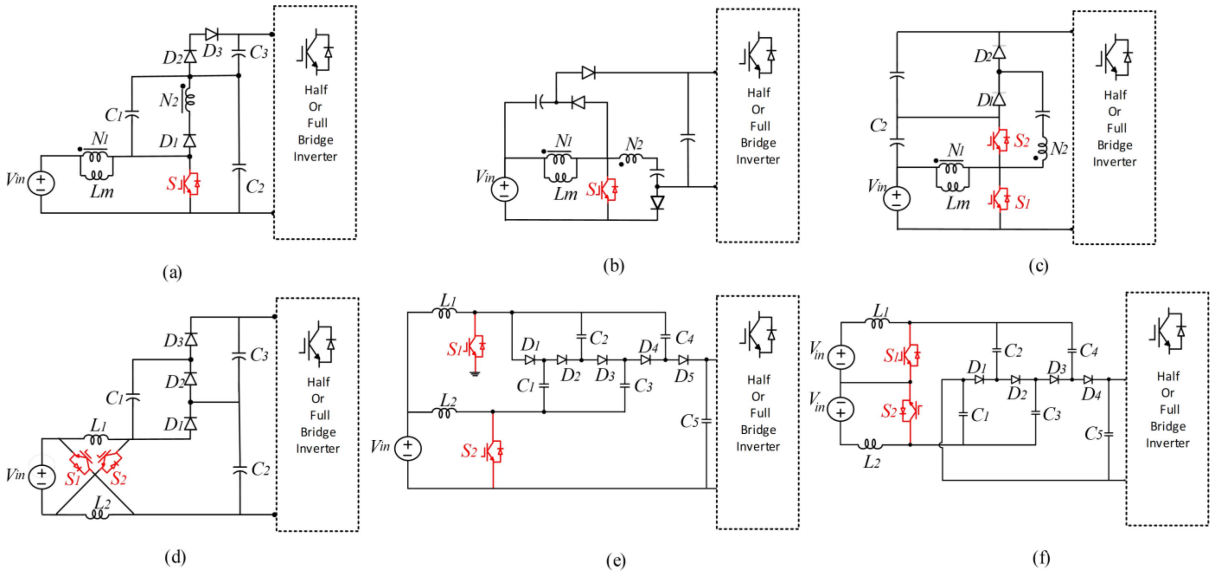


Fig. 2. Hybrid SC configuartion for DC–AC conversion. (a) magnetized SC ladder II. (b) Two SC coupled inductor converter. (c) PWM resonant SC coupled inductor converter. (d) SC-based active network. (e) double-switch Dickson charge pump converter. (f) Modified double-switch Dickson charge pump converter.

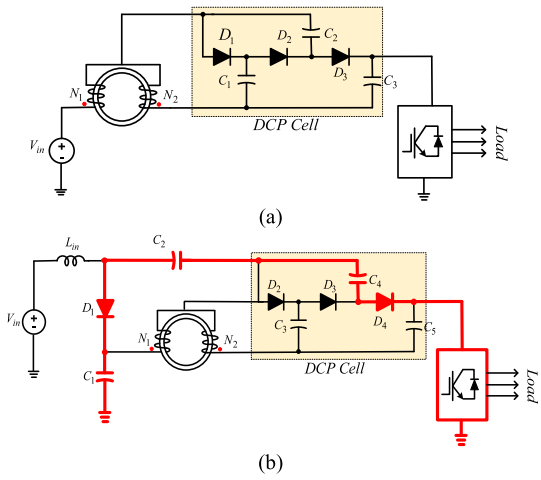


Fig. 3. Proposed hybrid SC inverters. (a) MDCPI. (b) IMDCPI with DC-rail voltage clamping.

challenges, switching losses, and heat generation. Moreover, for ultrahigh gain applications, conventional hybrid SC converters may require adding more SC cells, operating at higher duty cycles, or, in the case of magnetic coupling topologies, increasing the transformer turns ratio. These structures also face the issue of ST when capacitors become short-circuited due to both switches in one leg of a half/full bridge inverter being turned ON. This problem raises reliability concerns and increases the potential for issues in dc to ac conversion for conventional SC converters. Two hybrid SC converters based on a coupled transformer and DCP with direct dc–ac conversion capability are proposed, as shown in Fig. 3. The proposed converters offer several key features: they maintain a common ground between the dc input and ac output, eliminating the need for isolated sensing systems; they enable direct dc–ac conversion without additional power switches, making them suitable for RES and ESS applications; their transformer design allows for high voltage gain with a reduced turns ratio, achieving low STDR and high modulation index; the integration of DCP with coupled inductors eliminates shoot-through (ST) and open-circuit risks; capacitors mitigate leakage inductance and suppress voltage spikes during switching transitions, particularly in IMDCPI, where dc-link voltage clamping is achieved; and finally, IMDCPI ensures a continuous input current, while in MDCP, the series transformer placement helps suppress inrush current at start-up.

III. Magnetized Dickson Charge Pump Inverter

Fig. 3(a) shows the proposed MDCPI, which integrates a coupled transformer and a DCP cell. The DCP includes three capacitors and three diodes. The coupled transformer is connected in series with the input source, and its unavoidable leakage inductance can decrease the input current ripple. For steady-state analysis, the following assumptions are made: all power switches are ideal, and the coupled inductors' parasitic resistances and the ESR of the capacitors are ignored. The turns ratio of the coupled transformer is defined as $= \frac{N_1}{N_2}$. Because of the inductors-diodes-capacitors structure, the proposed inverter can operate in an extra mode named ST state along with the nonshoot-through (NST) state. In ST state two switches in one leg of the inverter are turned ON simultaneously, leading to a boost in the output voltage. Fig. 4(a), shows the equivalent circuit of the proposed MDCPI in ST mode. In this state, the inverter bridge is equivalent to a short circuit, diodes D_1 and D_3 are blocking, while D_2 conducts the current. In this mode, the windings N_1 and N_2 are energized by input source and capacitor C_3, and capacitor C_2 charges capacitor C_1. The coupling coefficient is $k = \frac{L_m}{L_m + L_k}$, where L_m and L_k represent the magnetizing inductance and leakage inductance of the coupled

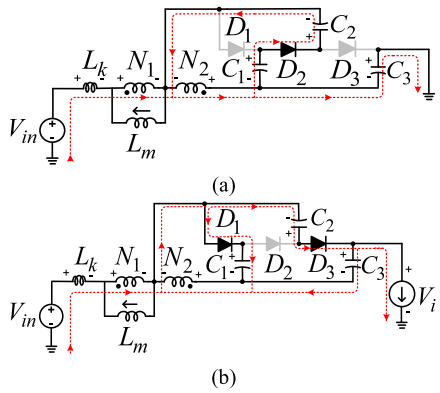


Fig. 4. Equivalent circuits of the proposed MDCPI in (a) ST mode and (b) NST mode.

transformer. By assuming $= \frac{L_k}{L_m}$, we have

$$\gamma = \frac{1-k}{k}. \tag{1}$$

From Fig. 2(a), by applying KVL we get

$$\begin{cases} V_{L_m} - V_{N_2} = V_{\text{in}} - V_{L_k} + V_{C_3} \\ V_{N_1} = V_{L_m} = V_{in} - V_{L_k} - V_{C_2} - V_{C_1} + V_{C_3} \\ V_{N_2} = -(V_{C_1} + V_{C_2}) \end{cases}. \tag{2}$$

In NST mode, the inverter bridge is equivalent to a current source. D_1 and D_3 conduct the current, and the windings release their energies into the loads and capacitors. From Fig. 4(b), we get

$$\begin{cases} V_{N_2} = -V_{C_1} \\ V_{N_2} = -(V_{C_2} + V_{C_3}) \\ V_{L_m} = -nV_{C_1} \\ V_{L_m} = -n(V_{C_2} + V_{C_3}) \\ V_i = V_{in} - V_{L_k} - V_{L_m} + V_{C_2} \end{cases}. \tag{3}$$

By applying the volt-second balance principle to the windings, we have

$$\int_0^{DTs} V_{Lm}dt + \int_{DTs}^{Ts} V_{Lm}dt = 0. \tag{4}$$

In (4), D and T_S represent the STDR and switching period, respectively. By solving (4), the voltages across capacitors are

$$\begin{cases} V_{C_1} = \frac{D}{n(\gamma+1)(1-D)-2} V_{\text{in}} \\ V_{C_2} = \frac{1}{n(\gamma+1)(1-D)-2} V_{\text{in}} \\ V_{C_3} = \frac{(1+D)}{n(\gamma+1)(1-D)-2} V_{\text{in}} \end{cases}. \tag{5}$$

From (3), the peak dc-link voltage (V_i) across the inverter bridge and the voltage boost factor (B) are given as

$$V_i = \frac{n(\gamma+1)-1}{n(\gamma+1)(1-D)-2} V_{\text{in}} \tag{6}$$

$$B = \frac{V_i}{V_{\text{in}}} = \frac{n(\gamma+1)-1}{n(\gamma+1)(1-D)-2}. \tag{7}$$

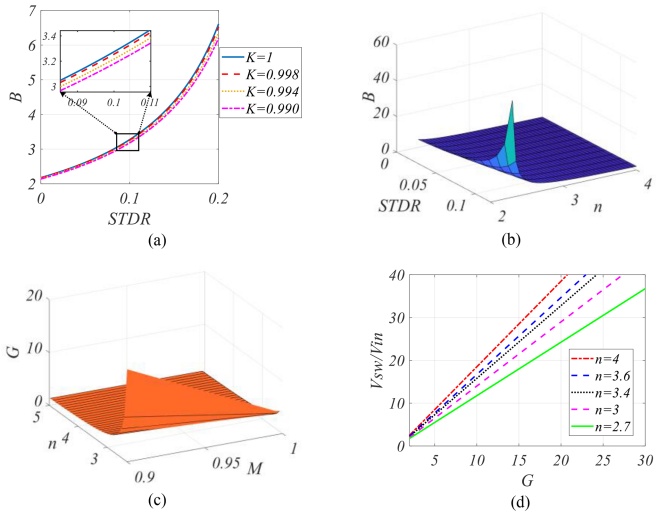


Fig. 5. Voltage plots of the proposed MDCPI. (a) Effect of leakage inductance on voltage boost factor. (b) Voltage boost factor versus D and n. (c) Voltage gain versus M and n. (d) Normalized voltage stress across the power switches for different n.

Fig. 5(a) shows B versus the STDR for various coupling k values. It can be seen that the effects of the leakage inductance on B is negligible. Hence, for the ideal case when $k = 1$ or $\gamma = 0$, we obtain

$$B = \frac{n-1}{n(1-D)-2}. \tag{8}$$

Fig. 5(b), shows B versus the STDR and N. The figure shows that the proposed MDCPI generates a high voltage gain for smaller N. Likewise, the peak value of the output phase voltage is given by (9), where M is modulation index

$$\hat{v}_{\text{ph}} = \frac{\text{MBV}_{\text{in}}}{2} = \frac{M(n-1)}{2n(1-D)-4} V_{\text{in}}. \tag{9}$$

Then, the output voltage gain (G) is obtained as

$$G = \frac{2\hat{v}_{\text{ph}}}{V_{\text{in}}} = \frac{M(n-1)}{(nM-2)}. \tag{10}$$

Fig. 5(c) depicts G versus M and n. It can be seen that G is increased by lowering the turn ratio. According to Fig. 4(a) and (b), the voltage stresses across the diodes are as follows:

$$V_{D_1} = V_{D_2} = V_{D_3} = \frac{1}{n(\gamma+1)(1-D)-2} V_{\text{in}}. \tag{11}$$

The voltage stresses across the switches are calculated in (12). From Fig. 5(d), it is clear that the lower turns ratio results in a lower voltage stress across the switches

$$V_{\text{sw}} = V_i = \frac{(n-1)}{(nM-2)} V_{\text{in}}. \tag{12}$$

Table I gives a brief comparison between the proposed MDCP structure and the selected magnetic-coupled voltage multipliers. The number of switches (N_S) in the dc side of the proposed topology, input and output ground state, trans-inverse feature, and voltage boost factor of MDCP and selected structures are investigated. Fig. 6(a) indicates that the proposed

TABLE I
COMPARISON WITH SELECTED MAGNETIC-COUPLED VOLTAGE MULTIPLIERS

Ref.	N_S in dc side	Common ground	Trans-inverse	B
Wu et al. [1]	1	×	×	$\frac{n+2}{1-D}$
Ye et al. [2]	2	✓	×	$\frac{n+2}{1-D}$
da Silva Bernardo Loureiro et al. [3] (I and III)	1	✓	×	$\frac{nD+2}{1-D}$
da Silva Bernardo Loureiro et al. [3] (II)	1	✓	×	$\frac{n-nD+1}{1-D}$
da Silva Bernardo Loureiro et al. [3] (IV)	1	✓	×	$\frac{nD+1}{1-D}$
da Silva Bernardo Loureiro et al. [3] (V)	1	✓	×	$\frac{n+2}{1-D}$
MDCPI	0	✓	✓	$\frac{n-1}{n-2-nD}$

TABLE II
COMPARISON WITH MAGNETIC-COUPLED INVERTERS

Ref.	Num. of				B	G	V_{sw}/V_{in}
	L	CL	C	D			
Aleem and Hanif [18]	1	2	2	2	$\frac{n-1}{n-1-2nD-D}$	$\frac{M(n-1)}{-2-n+M+2nM}$	$\frac{G+2nG-n+1}{n+2}$
Ma et al. [19]	2	2	4	2	$\frac{1}{1-2D-nD}$	$\frac{M-1}{-n+2M+nM}$	$\frac{2G+nG-1}{n+1}$
Liu et al. [21]	2	2	4	2	$\frac{1}{1-3D-nD}$	$\frac{M}{-2-n+3M+nM}$	$\frac{3G+3nG-1}{n+2}$
Reddivari and Jena [23]	0	2	1	1	$\frac{n-1}{n-nD-1}$	$\frac{M(n-1)}{nM-1}$	$nG\text{-}n+1$
Aleem et al. [27]	0	4	2	2	$\frac{n-1}{n-2nD-1}$	$\frac{M(n-1)}{-N+2nM-1}$	$\frac{-n+2nG+1}{n+1}$
Sharifi and Monfared [32]	1	2	3	2	$\frac{n+1}{n-2nD-D}$	$\frac{M(n+1)}{-1-n+M-2nM}$	$\frac{2nG+G--1}{n+1}$
Ding et al. [35]	0	2	2	2	$\frac{n-1}{n-2-nD+D}$	$\frac{M(n-1)}{-1-M+nM}$	$nG\text{-}G\text{-}n+1$
MDCPI	0	2	3	3	$\frac{n-1}{n-2-nD}$	$\frac{M(n-1)}{-2+nM}$	$\frac{nG-n+1}{2}$

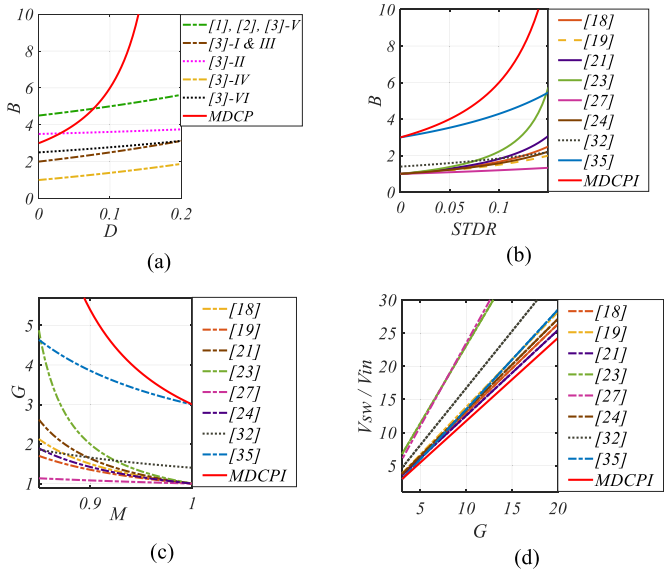


Fig. 6. Comparative plots. (a) Voltage boost factor versus duty cycle among voltage multipliers and MDCP. (b) Voltage boost factor versus duty cycle. (c) Voltage gain versus M. (d) Normalized switch voltage stress versus voltage gain among magnetic coupling inverters and MDCPI.

MDCP converter offers a higher voltage boost factor when compared with its counterparts. Table II gives a comparison between the MDCPI and selected magnetic- coupled impedance source networks. The voltage boost factors versus the STDR between the MDCPI and selected topologies are compared in Fig. 6(b). Furthermore, Fig. 6(c) demonstrates a comparison of the voltage gain versus the modulation index. It can be seen that for the same transformer turns ratio, the proposed MDCPI offers a higher voltage gain with smaller STDR and higher modulation index. Additionally, the proposed MDCPI has lower switch voltage stress as shown in Fig. 6(d).

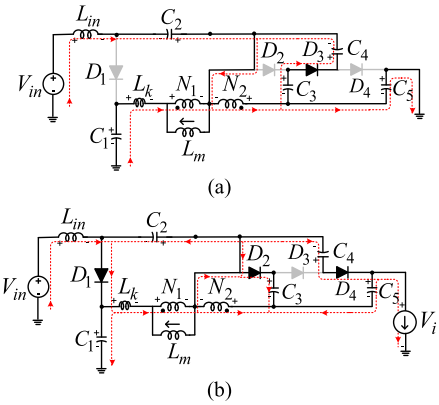


Fig. 7. Equivalent circuits of the proposed IMDCPI in (a) ST mode and (b) NST mode.

IV. IMPROVED MAGNETIZED DICKSON CHARGE PUMP INVERTER

To improve the performance of the proposed MDCPI, IMDCPI is presented in this section. Fig. 3(b) shows the configuration of the proposed IMDCPI. Compared with the

MDCPI, the IMDCPI has one extra input inductor, two capacitors, and one diode. This modification provides some features for the improved topology such as smooth input current

with limited inrush current at start up, higher voltage boost ability, and reduced voltage spikes across the inverter bridge. To carry out the steady-state analysis of the IMDCPI, the same assumptions as the first topology are considered.

A. Working Principle and Leakage Inductance Effect

The proposed IMDCPI also has two operating states. In ST mode as shown in Fig. 7(a), D_3 is conducting, while other diodes are reverse-biased. In this mode, the input inductor is charged by input source and C_2, and C_1 and C_5 energize the windings N_1 and N_2. Additionally, C_4 is charged by C_3. According to Fig. 7(b), in NST mode, D_1 is conducting the current; hence, the

input inductor discharges its saved energy into C_1. D_1 creates a loop, while C_2 receives energy from winding N_1 and absorbs the stored energy of the leakage inductance. N_2 charges C_3 though D_2, and its leakage inductance is clamped. In this state, C_4 is charging, while C_5 releases its stored energy into the loads. In Fig. 3(b), the capacitive high-frequency loop of the IMDCPI is highlighted in red.The proposed MDCPI and IMDCPI prevent current mismatches by minimizing differences in inductor currents through mutual inductance. The capacitors serve as energy storage elements and absorb leakage currents, which helps balance transients and ensure stable current distribution. The high-frequency loop in the IMDCPI topology provides a path for high-frequency currents flow, and the dc-link voltage is clamped to C_1, C_2, and C_4, mitigating oscillations that could lead to mismatches or voltage spikes. These design features ensure stable operation under inductive loads, preventing current mismatches.

B. Voltage Analysis

By applying KVL to Fig. 7(a) in ST mode, we get

$$\begin{cases} V_{L_{\text{in}}} = V_{\text{in}} + V_{C_2} - V_{C_3} + V_{C_4} + V_{C_5} \\ V_{N_1} = V_{L_m} = V_{C_1} - V_{L_k} - V_{C_3} + V_{C_4} + V_{C_5} \\ V_{N_2} = -V_{C_3} + V_{C_4} \end{cases}. \tag{13}$$

In NST mode, from Fig. 7(b) we get

$$\begin{cases} V_{L_{\text{in}}} = V_{\text{in}} - V_{C_1} \\ V_{N_1} = -(V_{C_1} + V_{L_k}) \\ V_{N_2} = -V_{C_3} = -(V_{C_4} + V_{C_5}) \end{cases}. \tag{14}$$

By applying the volt-second balance principle to the windings, and input inductor, the voltage stresses across the capacitors can be obtained as

$$\begin{cases} V_{C_1} = \frac{n(\gamma+1)(1-D)-2}{n(\gamma+1)-2nD(\gamma+1)-2} V_{\text{in}} \\ V_{C_2} = \frac{nD(\gamma+1)}{n(\gamma+1)-2nD(\gamma+1)-2} V_{\text{in}} \\ V_{C_3} = \frac{D}{n(\gamma+1)-2nD(\gamma+1)-2} V_{\text{in}} \\ V_{C_4} = \frac{1}{n(\gamma+1)-2nD(\gamma+1)-2} V_{\text{in}} \\ V_{C_5} = \frac{1+D}{n(\gamma+1)-2nD(\gamma+1)-2} V_{\text{in}} \end{cases}. \tag{15}$$

The maximum value of the dc-link voltage (V_i) and the voltage boost factor *(B)* are calculated as

$$V_i = \frac{n(\gamma+1)-1}{n(\gamma+1)-2nD(\gamma+1)-2} V_{\text{in}} \tag{16}$$

$$B = \frac{V_i}{V_{\text{in}}} = \frac{n(\gamma+1)-1}{n(\gamma+1)-2nD(\gamma+1)-2}. \tag{17}$$

Similar to the MDCPI, the effects of the leakage inductance on *B* is insignificant for IMDCPI, which is shown in Fig. 8(a). For the ideal case, substituting $\gamma = 0$ into (17) we get

$$B = \frac{n-1}{n-2nD-2}. \tag{18}$$

Similar to the MDCPI, the proposed IMDCPI offers a strong voltage boost factor for smaller turns ratios, which is depicted in Fig. 8(b). The peak output phase voltage and voltage gain are obtained as

$$\hat{v}_{\text{ph}} = \frac{\text{MBV}_{\text{in}}}{2} = \frac{M(n-1)}{2(n-2nD-2)} V_{\text{in}} \tag{19}$$

$$G = \frac{2\hat{v}_{\text{ph}}}{V_{\text{in}}} = \frac{M(n-1)}{(2nM-n-2)}. \tag{20}$$

The output voltage gain versus the modulation index and transformer turn ratio for the proposed IMDCPI is plotted in Fig. 8(c). It is clear that the voltage gain is raised by reducing the turns ratio.

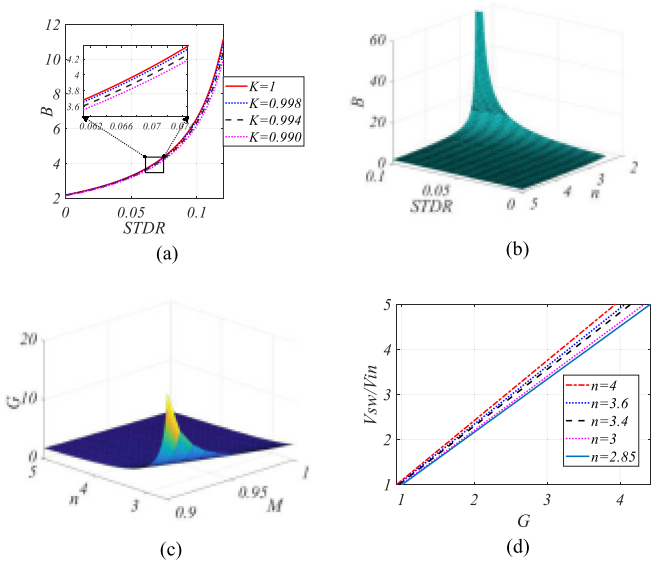


Fig. 8. Voltage plots of the proposed IMDCPI. (a) Effect of leakage inductance on voltage boost factor. (b) voltage boost factor versus *D* and *n*. (c) Voltage gain versus *M* and *n*. (d) Normalized voltage stress across the power switches among different n.

C. Current Analysis

By applying Kirchhoff's current law to Fig. 7(a), we get

$$\begin{cases} I_{C_1} = I_{L_m} - I_1 \\ I_{C_2} = -I_{\text{dc}} \\ I_{C_3} = I_1 - I_{L_m} + I_{\text{dc}} - nI_1 \\ I_{C_4} = I_{L_m} - I_1 - I_{\text{dc}} + nI_1 \\ I_{C_5} = I_{L_m} - I_1 - I_{\text{dc}} \end{cases}. \tag{21}$$

From Fig. 7(b), the current equations in NST can be written as

$$\begin{cases} I_{C_1} = I_{\text{dc}} - I_i \\ I_{C_2} = I_1 - I_{L_m} - I_i \\ I_{C_3} - I_{C_4} = -nI_1 + I_i \\ I_{C_3} + I_{C_5} = nI_1 \end{cases}. \tag{22}$$

By applying the current-second balance principle to capacitors

$$\int_0^{DT} i_{Ci}dt + \int_{DT}^{T} i_{Ci}dt = 0 \tag{23}$$

where $i = 1, 2, \ldots$, and 5, represent the capacitors' indexes. Substituting (21) and (22) in (23), yields

$$\begin{cases} i_1 = \frac{1+2D}{n(1+D)}\, I_{\rm dc} \\ i_{N2} = \frac{1+2D}{1+D}\, I_{\rm dc} \\ i_{Lm} = \frac{2D-n-Dn+1}{n(1+D)}\, I_{\rm dc} \\ i_i = \frac{nD-1}{D-1}\, I_{\rm dc} \end{cases}. \tag{24}$$

D. Design Guidelines of the Proposed IMDCPI

In this section design and component selections for the proposed IMDCPI is presented.

1) Magnetic Components Selection

The magnetic parameters of the proposed IMDCPI are determined by considering the maximum current ripple and voltage in the ST interval. As a result, the following equations are derived, where x% represents the maximum permissible current ripple for the inductors, which is set to 20% in the design process

$$\begin{cases} L_1 \geq \frac{{V_{\rm in}}^2(n-nD)D}{x\%(n-2nD-2)Po.f_{sw}} \\ L_m \geq \frac{{V_{\rm in}}^2(n-nD)(n+nD)D}{x\%(n-2nD-2)(1+2D-nD-n)Po.f_{\rm sw}} \end{cases}. \tag{25}$$

2) Capacitors Selection

The capacitive components of the proposed inverter are designed based on their voltage ripple, maximum current, switching frequency, and ST duty ratio. Accordingly, the following equations are derived, where $y\%$ denotes the maximum allowable voltage ripple, which is set to 1% during the design process

$$\begin{cases} C_1 \geq \frac{(n-2nD-2)DPo}{y\%(n-nD-2)\ {V_{\rm in}}^2 f_{\rm sw}} \\ C_2 \geq \frac{i_{C2}.D}{\Delta V_{C2}.f_{\rm sw}} = \frac{(n-2nD-2)DPo}{y\%nD{V_{\rm in}}^2 f_{\rm sw}} \\ C_3 \geq \frac{(n-2nD-2)DPo}{y\%D(1+D){V_{\rm in}}^2 f_{\rm sw}} \\ C_4 \geq \frac{(n-2nD-2)DPo}{y\%(1+D){V_{\rm in}}^2 f_{\rm sw}} \\ C_5 \geq \frac{2(-n+2nD+2)DPo}{y\%\ (1+D){V_{\rm in}}^2 f_{\rm sw}} \end{cases}. \tag{26}$$

3) Semiconductors Selection

To select the semiconductors in the proposed IMDCPI, we need to obtain the maximum voltage and current stress of the diodes and power switches. From Fig. 7(a), the voltage stress across the diodes D_1, D_2, and D_4 can be obtained, and from Fig. 7(b), the voltage stress across D_3 can be attained as

$$\begin{cases} V_{D1-\max} = \frac{n}{n-2nD-2}\, V_{\rm in} \\ V_{D2-\max} = V_{D3-\max} = V_{D4-\max} = \frac{1}{n-2nD-2}\, V_{\rm in} \end{cases}. \tag{27}$$

The peak current stress of the diodes D_1, D_2, D_4 can be derived in NST mode, while D_3 is conducting in ST mode, therefore we can obtain the maximum current stress on the diodes from (28). It should be noted that $I_{D\text{-}\max}$ denotes the highest current that flows through I_{D2} and I_{D4}

$$\begin{cases} I_{D1-\max} = 2\, I_{\rm dc} \\ I_{D3-\max} = I_{C_3} = \frac{1}{(1+D)}\, I_{\rm dc}. \\ I_{D-\max} = \frac{2D}{1-D^2}\, I_{\rm dc} \end{cases} \tag{28}$$

The maximum value of the voltage stress across the switches is obtained from (29), and demonstrated in Fig. 8(d)

$$V_{\rm sw} = \frac{(n-1)}{(-n+2nM-2)}\, V_{\rm in}. \tag{29}$$

The maximum current stress of the switches is attained based on the dc-link current as

$$I_{\rm sw-max} = \frac{2-2D}{(-1+2D)}\, I_i. \tag{30}$$

E. Comparative Analysis: The proposed inverters offers significant advantages over traditional boost converters commonly used for dc–dc–ac conversion. While boost converters use minimal components (a single switch and diode), their voltage gain is limited to 1/(1−D), requiring impractically high duty cycles for large voltage gains, leading to high conduction losses, increased component stress, and reduced efficiency. Additionally, boost converters rely on a two-stage process (dc–dc and dc–ac conversion), increasing complexity and reducing efficiency. In contrast, the proposed inverters eliminate the dc–dc stage, achieving direct dc–ac conversion with significantly higher voltage gain, reduced component stress, simplified control, and improved overall efficiency, making it ideal for high-voltage, high-power applications. The proposed IMDCPI also provides distinct benefits compared to traditional CP topologies. Generally, CP structures require additional components to attain higher voltage levels, which can increase complexity and cost [6], [7], [8]. Thanks to the magnetic structure of the IMDCPI, it provides a high voltage gain without the need for extensive additions or modifications. In contrast to conventional Cockcroft–Walton CP structures, the proposed topology does not suffer from output voltage drop, guaranteeing that the expected voltage level is maintained without considerable losses. Unlike other DCP structures, the proposed topology does not have high voltage stress across its capacitors. Additionally, for three-phase dc–ac power conversion, traditional CP structures need two stages: a dc–dc conversion stage and a dc–ac conversion stage. The proposed direct dc–ac CP converter eliminates the requirement for auxiliary power switches associated with the intermediate dc–dc stage, which brings some advantages including enhanced efficiency, simplified control, and reduced volume and component count. Notably, the proposed topologies eliminates the risk of capacitor short circuits, which can occur in traditional configurations, and reduces stress on the dc-link capacitor by distributing the voltage across multiple capacitors.

Conventional magnetic-coupled impedance networks such as Δ-source, Y-source and Γ-source networks [16], [17] exhibit discontinuous input current behavior that causes high stress on the input source. Furthermore, they suffer from high inrush current at start-up, which leads to instability, and potential damage to components. The proposed IMDCP structure draws a full smooth and continuous input current from the dc source with a

TABLE III
COMPARISON OF THE IMDCPI WITH SELECTED INVERTERS

Ref.	Yazdani et al. [16] (ΓSI)	Ma et al. [19] DW-TISI	Ahmed et al. [30]	Ding et al. [35]	Esmaeili et al. [36]	IMDCPI
L.I.C.R	×	✓	✓	✓	✓	✓
Trans-inv	✓	×	×	✓	✓	✓
DC-LVC	×	✓	✓	✓	✓	✓
B	$\frac{n-1}{n-1-nD}$	$\frac{1}{1-2D-nD}$	$\frac{1+2n}{n-D-3nD}$	$\frac{n-1}{n+2D-2nD-2}$	$\frac{n-1}{n+D-2nD-2}$	$\frac{n-1}{n-2nD-2}$
G	$\frac{M(n-1)}{-1+nM}$	$\frac{M}{-n+2M+nM-1}$	$\frac{M(2n+1)}{-2n+M+3nM-1}$	$\frac{M(n-1)}{-n-2M+2nM}$	$\frac{M(n-1)}{-n-M+2nM-1}$	$\frac{M(n-1)}{-n+2nM-2}$
V_{Sw}/V_{in}	$1-n+nG$	$\frac{-1+nG+2G}{n+1}$	$\frac{-1-2n+3nG+G}{2n+1}$	$\frac{1-n-2G+2nG}{n}$	$\frac{1-n-G+2nG}{n+1}$	$\frac{1-n+4nG}{2n+4}$
STDR	$\frac{(n-1)G-n+1}{nG-n+1}$	$\frac{G-1}{(2+n)G-1}$	$\frac{nG-2n-1}{(3n+1)G-2n-1}$	$\frac{(n-2)G-n+1}{(2n-2)G-n+1}$	$\frac{(n-2)G-n+1}{(2n-1)G-n+1}$	$\frac{(n-2)G-n+1}{2nG-n+1}$
$(V_{L_{in}}/V_{in})^*$	NA	G	G	G	$\frac{nG}{n-1}$	$\frac{nG}{n-1}$
$\Delta i_{Lin}/V_{in}$	NA	$\frac{(G-1)G}{((2+n)G-1)L_1 f_{sw}}$	$\frac{(nG-2n-1)G}{((3n+1)G-2n-1)L_1 f_{sw}}$	$\frac{((n-2)G-n+1)G}{((2n-2)G-n+1)L_1 f_{sw}}$	$\frac{((n-2)G-n+1)nG}{((2n-1)G-n+1)(n-1)L_1 f_{sw}}$	$\frac{((n-2)G-n+1)nG}{(2nG-n+1)(n-1)L_1 f_{sw}}$
$\Delta B_{L_{in}}$	NA	$\frac{(G-1)G}{((2+n)G-1)N A_c f_{sw}}$	$\frac{(nG-2n-1)G}{((3n+1)G-2n-1)N A_c f_{sw}}$	$\frac{((n-2)G-n+1)G}{((2n-2)G-n+1)N A_c f_{sw}}$	$\frac{((n-2)G-n+1)nG}{((2n-1)G-n+1)(n-1)N A_c f_{sw}}$	$\frac{((n-2)G-n+1)nG}{(2nG-n+1)(n-1)N A_c f_{sw}}$
$(V_{N1,2}/V_{in})^*$	G	G	$\frac{nG}{1+2n}$	$\frac{nG}{n-1}$	G	$\frac{nG}{n-1}$
$\Delta B_{N1,2}$	$\frac{((n-1)G-n+1)G}{(nG-n+1)N A_c f_{sw}}$	$\frac{(G-1)G}{((2+n)G-1))N A_c f_{sw}}$	$\frac{(nG-2n-1)nG}{((3n+1)G-2n-1)(1+2n)N A_c f_{sw}}$	$\frac{((n-2)G-n+1)nG}{((2n-2)G-n+1)(n-1)N A_c f_{sw}}$	$\frac{((n-2)G-n+1)G}{((2n-1)G-n+1)N A_c f_{sw}}$	$\frac{((n-2)G-n+1)G}{(2nG-n+1)N A_c f_{sw}}$

*In ST mode, L.I.C.R: low input current ripple, Trans-inv: Trans-inverse, DC-LVC: DC-link voltage clamping.

low inrush current at start-up. Hence, the system's reliability is enhanced and the lifespan of the components will be extended. Likewise, several existing magnetic-coupled impedance source networks encounter challenges related to leakage inductance effects and switching voltage spikes during their switching transitions, which may damage the circuit components or affect the overall system performance [15], [16], [17]. As it was mentioned, the proposed IMDCPI overcomes these issues by exploiting a capacitive high-frequency loop that serves to clamp the dc link voltage and suppress switching voltage spikes. Table III gives a brief comparison between the proposed IMDCPI and selected topologies. Voltage boost ability, output quality, voltage stress across the switches, and input current ripple are evaluated in the following sub-sections. For a fair comparison, the windings (*N1* and *N2*) turns number are assumed 57 and 20 in the proposed inverter and the selected topologies.

1) Voltage Boost Ability: A comparison between the proposed IMDCPI topology and other selected topologies in terms of the voltage boost factor and STDR is shown in Fig. 9(a). The trend in Fig. 9(a) demonstrates that the proposed IMDCPI inverter offers a greater capacity for voltage boosting than the selected topologies under similar conditions. Furthermore, it can be seen that the proposed network offers a considerable voltage boost capability at extremely low STDR values. In contrast, conventional impedance source networks present a steeper slope at small STDR values, posing challenges in circuit control.

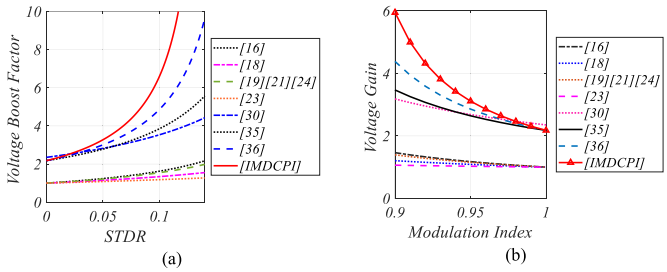


Fig. 9. Comparison of the (a) voltage boost factor and (b) voltage gain among IMDCPI and selected topologies.

2) Output Quality: The modulation index represents the ratio of the modulating signal's peak amplitude to the carrier signal's peak amplitude in a simple boost control. Fig. 9(b) illustrates the voltage gain versus modulation index for the proposed IMDCPI and its counterparts. It is obvious that the proposed inverter can deliver a similar voltage gain with a higher modulation index. Operating with a high modulation index in a dc–ac inverter can have significant advantages. A higher modulation index improves the ac output voltage quality by allowing finer control over the output waveform, more accurately replicating the desired ac voltage and better tracking of reference signals. This leads to a more sinusoidal output waveform with reduced harmonic distortions.

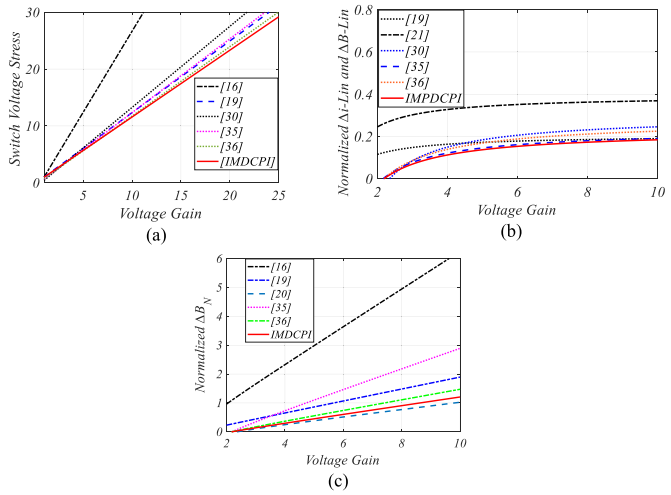


Fig. 10. Comparison of (a) switch's voltage stress. (b) Input current ripple and input inductor's flux density swing. (c) Coupled inductors' flux density swing among IMDCPI and selected topologies.

3) Voltage Stress Across the Switches: We can rewrite (29) based on the voltage gain as follows:

$$V_{\text{sw}} = \frac{1 - n + 4nG}{2n + 4}\, V_{\text{in}}. \tag{31}$$

By substituting $N_1/N_2 = 57/20$ in (31), the voltage stress on the switches can be obtained as

$$V_{\text{sw}} = \frac{-1.85 + 11.4G}{9.7}\, V_{\text{in}}. \tag{32}$$

The maximum voltage stress of the switches in other converters can be given in Table III. Fig. 10(a) shows a comparison between the proposed IMDCPI topology and other selected topologies in terms of the voltage gain. It shows that the proposed IMDCPI has a lower voltage stress across its switches. Hence, the

IMDCPI operates using switches with lower voltage ratings. Lower voltage stress across the switches leads to enhanced reliability and longevity of the system. Likewise, lower voltage stress contributes to the improved overall efficiency of the inverter by decreasing losses and enhancing the power conversion process. Also, using lower-rated switches is generally more economical compared to higher-rated ones.

4) Input Current Ripple: The input current is equal to the current of the input inductor. Thus, the ripple of the input current can be obtained as

$$\Delta i_{L1} = \frac{D\, V_{L1}}{L_1\, f_{\text{sw}}}\,. \tag{33}$$

From (13), the voltage across the input inductor during the ST mode can be rewritten as

$$V_{L_{\text{in}}} = \frac{n\,(1 - D)}{n - 2nD - 2} = \frac{nG}{n - 1}\, V_{\text{in}}. \tag{34}$$

Hence, the input current ripple is derived from (33) as

$$\Delta i_{L\text{in}} = \frac{nDG}{L_1\ (n - 1)\, f_{\text{sw}}}\, V_{\text{in}}. \tag{35}$$

Table III gives the input current ripple expressions for the proposed and similar selected topologies. Assuming the same values for input inductance, input source voltage, turns ratio, and switching frequency, the input current ripple of the proposed and selected topologies relies on STDR. Consequently, these expressions allow for a fair comparison of the input current ripple among the topologies. For the proposed inverter, the STDR is determined as

$$D = \frac{1.85G - 1.85}{1.7 - 11.4G}. \tag{36}$$

By putting STDR obtained from (36) into (35), regarding the assumptions mentioned earlier, and applying the same procedure to the chosen inverters, we can plot the relationship between the normalized input current ripple and the voltage gain. Fig. 10(b) shows the normalized current ripple of the input inductor for different voltage gains in the proposed IMDCPI and the selected topologies. A lower input current ripple results in improved power quality, ensuring the stable and reliable operation of the inverter, and smaller size of input inductor.

5) Flux Density Swing of Magnetic Components: The flux density swing of the magnetic components can be written as

$$\Delta B = \frac{D\, V_M}{N\, A_e\, f_{\text{sw}}} \tag{37}$$

where V_M, N, and A_e represent the voltage stress on magnetic components, number of turns, core cross-sectional area of the magnetic components. By substituting (34) into (37), the flux density swing of the input inductor can be rewritten as

$$\Delta B_{L_{\text{in}}} = \frac{nDG}{(n - 1)\ N\, A_e\, f_{\text{sw}}}\, V_{\text{in}}. \tag{38}$$

Therefore, for the same values for input dc voltage, turns ratio, number of turns, core cross-sectional area, and switching frequency, the input inductor flux density of the proposed and selected topologies depend on STDR. The same method can be applied for the magnetic- coupled inductors. In the proposed IMDCPI, the voltage stress across the windings is obtained as

$$V_{N_{1,2}} = \frac{nM}{(-n + 2nM - 2)}\, V_{in} = \frac{n}{(n - 1)}\, \text{GV}_{\text{in}}. \tag{39}$$

Thus, the flux density swing of the coupled inductors is given

$$\Delta B_{N_{1,2}} = \frac{nDG}{(n - 1)\ N_1\, A_e\, f_{\text{sw}}}\, V_{\text{in}}. \tag{40}$$

Again, by considering the mentioned assumptions, and substituting STDRs in (35) and Table III into (38) and (40), we can plot the normalized flux density swing of the input inductor and coupled inductors for the proposed IMDCPI and selected topologies in Fig. 10(c). It is clear the proposed inverter has a lower magnetic component flux density compared with its counterparts, which leads to improved efficiency, reliability, and power density.

V. Evaluation Results

The proposed inverters have been built in laboratory as shown in Fig. 11. The electrical specifications of the experimental prototype are given in Table IV. The C055866A2 toroidal core,

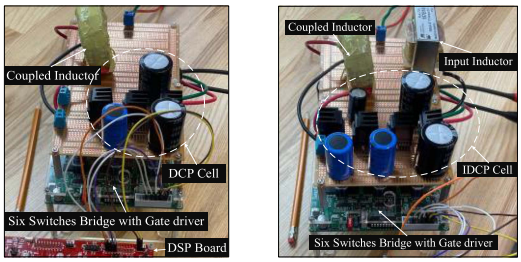


Fig. 11. Prototype of (a) MDCPI and (b) IMDCPI.

TABLE IV
COMPONENTS ELECTRICAL SPECIFICATIONS

Components	Values
Input voltage (V_{in})	100 V
Switching and fundamental ac frequency	50 kHz, 60 Hz
Diodes	STTH12R06
Controller	TMS320F280049C
Inductors (L_{in}), Capacitors	0.5 mH, 470 μF
Transformer coupling coefficient, k	0.994
Transformer magnetizing inductance	0.528 mH
Transformer core	C055866A2
Transformer windings, N_1 and N_2	57 and 20 turns
STDR for MDCPI and IMDCPI	10% and 5%
Modulation index for MDCPI and IMDCPI	0.9, 0.95
LC filter, Y connected resistive load	1 mH , 50 μF, 50 Ω

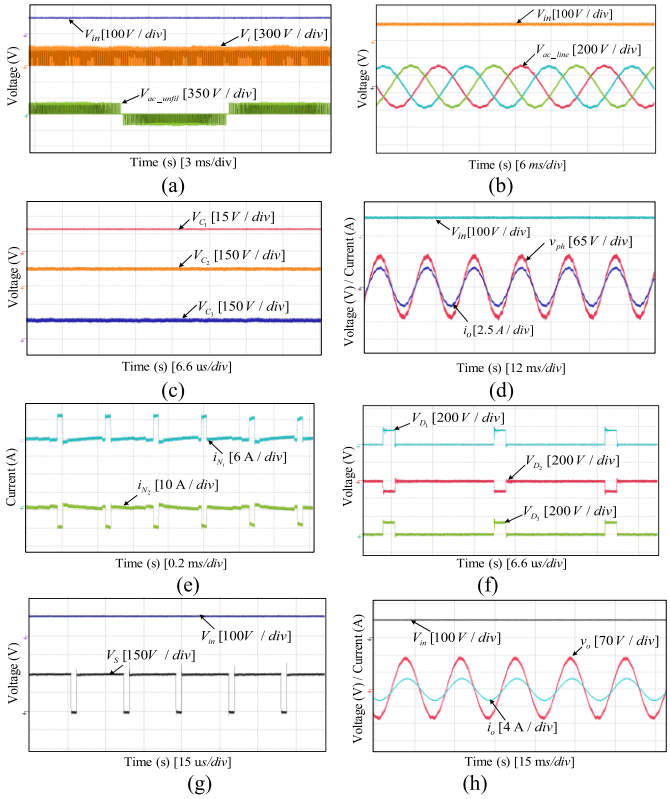


Fig. 12. Experimental results of the proposed MDCPI. (a) DC-link voltage and unfiltered AC voltage. (b) Line-to-line AC voltages. (c) Voltage stress across the capacitors. (d) AC phase voltage and output current. (e) Windings' currents. (f) Voltage stress across the diodes. (g) Voltage stress across the switches. (h) AC phase voltage and output current under *RL* load.

with an outer diameter of 78.94 mm, an inner diameter of 48.21 mm, and a height of 13.84 mm, was selected for its permeability of 125 nH/T^2 and low core losses in high-frequency applications. AWG 15 copper wire is used for the windings, offering adequate current capacity and low resistance. First, the results of the MDCPI with STDR of 10% are presented in Fig. 12. From (6), the peak value of the inverter bridge's input voltage is 327 V. Fig. 12(a), shows that the dc link voltage is about 300 V. The difference comes from the power losses within the active and passive components. Also, it can be seen that the voltage spikes across the inverter bridge is reached to about 400 V. Despite this, the SC structure of the proposed MDCPI ensures this value remains significantly lower than that of conventional magnetic coupling inverters. Fig. 12(b) illustrates the line-to-line ac voltages with a peak value of 230 V, which is close to the theoretical calculation of 255 V. Low distortion is observed from these waveforms. Fig. 12(c) shows the voltage stress across the capacitors in the DCP cell. The voltages across C_1, C_2, and C_3 are approximately 17, 160, and 175 V**,** respectively, which are close to the theoretical values of 17, 177, and 194 V**.** From Fig. 12(d), the peak ac phase voltage and output current are 130 V and 2.6 A, respectively, which are consistent with the theoretical values of 147 V and 2.9 A. Fig. 12(e) shows the windings' current. It is seen that due to the effect of leakage inductance, the peak currents do not reach huge levels. From Fig. 12(f), the voltages across the diodes D_1, D_2, and D_3 have the same value of 160 V, which are in agreement with the theoretical values of 177 V. Fig. 12(g) shows the voltage stress across the power switches. Because of the presence of the DCP cell, the voltage spikes across the switches is lower than conventional magnetically coupled inductors inverters. The proposed MDCPI was under RL loads with inductance of 5 mH has been tested. Fig. 12(h) demonstrates that the output current and output voltage exhibit sine waves with low THD. This validation confirms that the proposed inverter operates stably under inductive loads without experiencing current mismatch or severe voltage spikes. Fig. 13 shows the experimental results of the proposed IMDCPI. In Fig. 13(a), it is evident that the dc link voltage increased to 315 V, which is reasonably consistent with the theoretical calculation of 327 V. The inclusion of a clamping circuit has substantially reduced voltage spikes across the inverter bridge, with the maximum spike reaching 335 V. Unlike the MDCPI topology, the proposed IMDCPI consistently draws continuous input current from the dc source, as confirmed by Fig. 13(a). According to (35), the input current ripple is about 0.95 A, which is verified by Fig. (13)(g). Fig. 13(b) reveals that the peak ac line-to-line voltage is approximately 250 V, which is reasonably consistent with the theoretical value of 269 V derived from mathematical equations, demonstrating improved performance compared to the MDCPI even with a lower STDR. In Fig. 13(b) and (c), the voltage stresses across capacitors C_1, C_2, C_3, C_4, and C_5 are approximately 125, 24, 8, 150, and 160 V, respectively, while the theoretical calculations yield 125, 24, 8, 177, and 185 V. From theoretical calculations, the peak ac phase voltage and current of the proposed IMDCPI are 155 V and 3.1 A, respectively. Fig. 13(d) illustrates the ac phase voltage and current, with

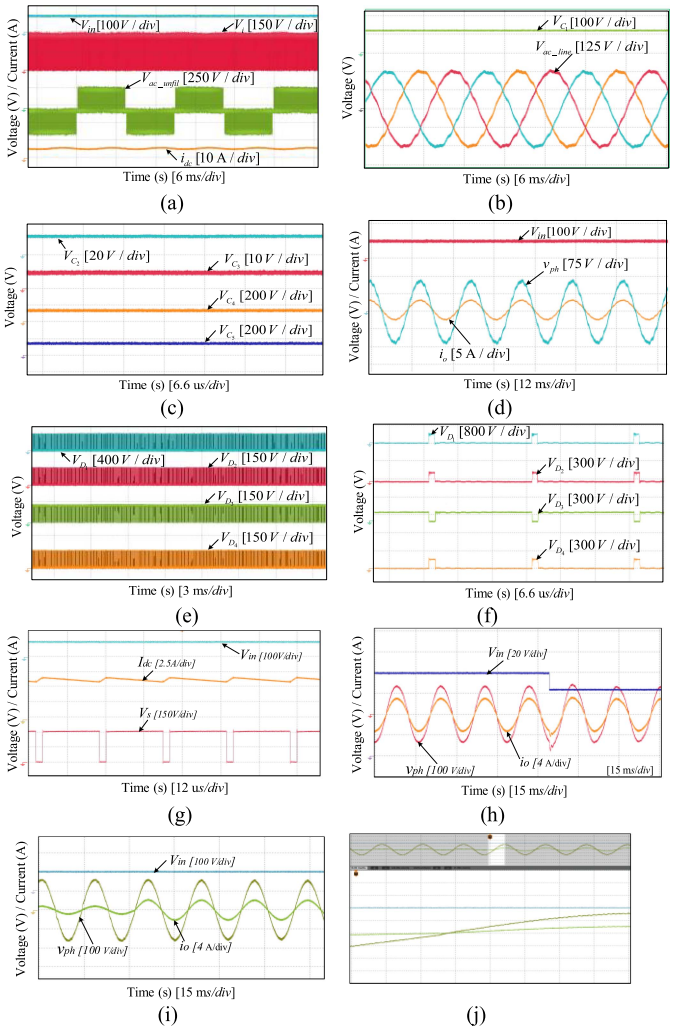


Fig. 13. Experimental results of the proposed IMDCPI. (a) DC-link voltage, unfiltered AC voltage, zoomed-out input current. (b) Line-to-line AC voltages. (c) Voltage stress across the capacitors. (d) AC phase voltage and output current. (e) Zoomed-out voltage stress across the diodes. (f) Zoome-in voltage stress across the diodes. (g) Voltage stress across the switches and zoomed-in input current. (h) Closed-loop response to a step change in input voltage. (i) Response to a step change in load. (j) Expnded view of Fig. 13(i).

measured peak values of 143 V and 2.85 A, demonstrating good agreement with the theoretical predictions. The output voltage and current waveforms demonstrate the effective maintenance of the output phase angle by both proposed inverters. Finally, the zoom-in and zoom-out voltage stress on the diodes are depicted in Fig. 13(e) and (f). From (27), the peak voltage blocking on the input diode is approximately 504 V, while for the other diodes, it is 177 V. According to the experimental results, the voltage on the input diode is measured at 450 V, whereas the other diodes in the DCP cell exhibit a peak value of 150 V. The observed variations are primarily due to practical factors such as voltage drops across parasitic resistances and diode reverse recovery characteristics. Fig. 13(g) shows that the voltage spikes across the switches are significantly reduced due to the dc-rail voltage clamping circuit. Details of the transient experimental results of the proposed IMDCPI are shown in Fig. 13(h), (i), and (j). Fig. 13(h) illustrates the results depicting the closed-loop

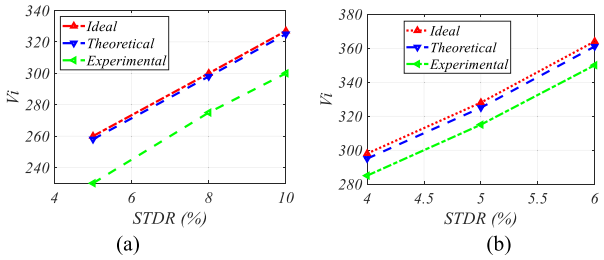


Fig. 14. DC link voltage in ideal, theoretical, and practical cases among different STDR for (a) MDCPI and (b) IMDCPI.

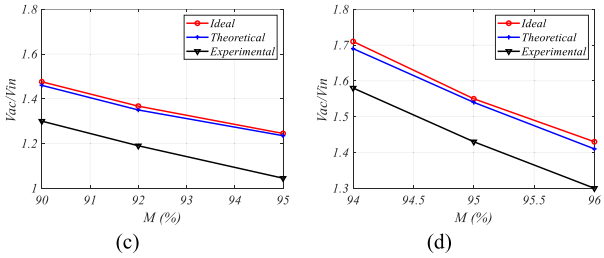


Fig. 15. AC voltage boost ratios in ideal, theoretical, and practical cases among different STDR for (a) MDCPI and (b) IMDCPI.

response of step change in input voltage while maintaining a steady output. Fig. 13(i) shows the the response of the proposed IMDCPI to a step change in load. Fig. 13(j) gives an expanded view of the time response shown in Fig. 13(i). The experiments have been repeated with different STDR for both inverters. The peak value of dc link voltage and ac voltage boost ratio for ideal case (excluding the effects of leakage inductance), theoretical calculations (including the effects of leakage inductance), and experimental observation are shown in Figs. 14(a) and (b), and Figs. 15(a) and (b).The discrepancies between experimental and theoretical results arise from component parasitic, switching losses, and thermal effects. Real-world nonidealities, such as parasitic resistances and inductances, slightly affect the dc-link voltage and ac voltage boost ratios. However, the experimental values remain close to the theoretical predictions, validating the proposed inverters' effectiveness. To provide a fair and insightful evaluation of the proposed IMDCPI converter, a comprehensive comparison has been conducted with several recent topologies based on experimental data, as given in Table V. All topologies have been evaluated under consistent conditions ($V_{\text{in}} = 100$ V, turn ratio $= 2.85$) to ensure a fair and reliable comparison. The analysis focuses on the achieved dc-link voltage, the corresponding overshoot during the transition from the ST to the NST state, and the required STDR and modulation ratio to reach a consistent ac output voltage level of 140–155 V. While most referenced converters require STDR values around 10% and lower modulation indices (e.g., $M = 0.9$) to achieve this voltage range, the IMDCPI demonstrates the ability to reach target dc-link voltage with a significantly reduced STDR (5%) and a higher modulation index ($M = 0.95$). Furthermore, the measured overshoot in the IMDCPI remains substantially lower than that of other designs, reducing switching stress and improving system reliability.

TABLE V
EXPERIMENTAL VALUES OF DC-LINK VOLTAGE AND VOLTAGE OVERSHOOT FOR AC OUTPUT OF 140–155 V WITH CORRESPONDING STDR AND M SETTINGS

Ref.	STDR (%)	M	V_i (V)	Overshoot (V)
Zhang et al. [28]	10	0.9	320	+90
Ding et al. [29]	10	0.9	316	+25
Ding et al. [35]—Topo 1	10	0.9	240	+720
Ding et al. [35]—Topo 2	10	0.9	320	+100
MDCPI	10	0.9	300	+100
IMDCPI	5	0.95	315	+20

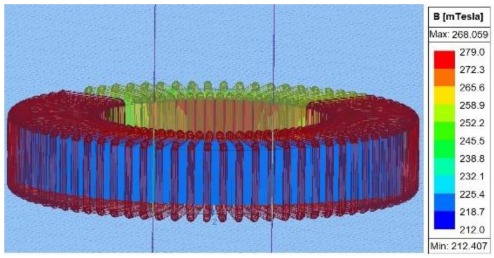


Fig. 16. Flux density of the coupled transformer in the proposed IMDCPI via FEM simulation.

To verify the theoretical equations for flux density, first the flux density of the proposed IMDCPI at the operating point of the experimental test is calculated. The flux density can be derived from the magnetic flux and core cross-sectional area [37], using the parameters $N_1 = 57$, $A_e = 176$ mm^2, $L_m = 0.528$ mH

$$B = \frac{\Phi}{A_e} = \frac{L_m . I_{Lm}}{A_e . N_1} \cong 0.220 \text{ T}. \tag{41}$$

Next, using the flux density swing equation, we have

$$\Delta B_N = \frac{nDG}{(n-1)\ N_1\ A_e\ f_{\text{sw}}} V_{\text{in}} \cong 48 \text{ mT}. \tag{42}$$

To verify this theoretical calculation, ANSYS Maxwell software has been used. The coupled transformer is first designed in PEmag, and the proposed converter is simulated in Simplorer using the experimental parameters. Finally, a FEM simulation is conducted in ANSYS Maxwell to obtain the flux density in the transformer core. As shown in Fig. 16, the simulation results indicate a flux density ranging from 212.407 to 268.059 mT. The calculated theoretical value of 0.220 T falls within this range, confirming the theoretical calculation. Moreover, the flux density swing from the simulation is 55.652 mT, which closely aligns with the theoretical value of 48 mT. To analyze the effect of switching frequency on magnetizing inductance, L_m is plotted versus various switching frequencies at different output power levels. Fig. 17 illustrates the magnetizing inductance variation with switching frequency under experimental test parameters. Fig. 18 shows the FFT breakdown analysis of the proposed IMDCPI converter, highlighting the ac voltage and output current characteristics. According to this figure, the recorded THD of 2.704% and 2.679% per phase at the rated

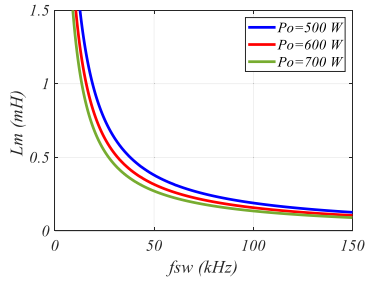


Fig. 17. Magnetizing inductance versus switching frequency at different powers.

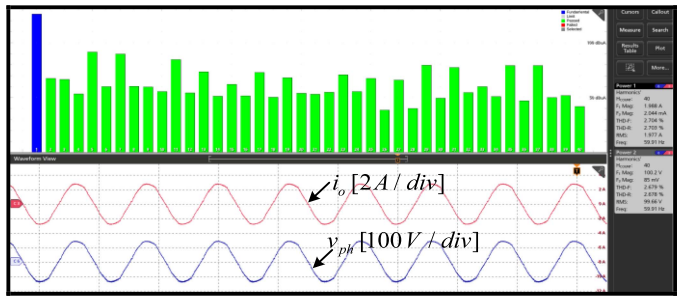


Fig. 18. Harmonic analysis of the proposed IMDCPI converter.

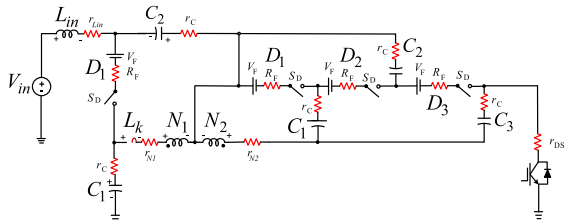


Fig. 19. Equivalent circuit of the proposed IMDCPI for power loss calculation.

power of the converter, indicating a clean output waveform suitable for various applications.

The efficiency analysis of the proposed IMDCPI is presented in this section. The primary sources of power losses can be attributed to magnetic components, the equivalent series resistance (ESR) of the capacitors, and semiconductors [38]. Fig. 19 shows the equivalent circuit of the proposed inverter with parasitic components. Both the inductor and transformer components play pivotal roles in power loss generation. These losses can be primarily attributed to ESR losses associated with inductor and coupled transformer, core losses, and copper losses. The ESRs of the magnetic elements generate the power losses [38], which can be obtained as

$$P_{\text{ESR}-L} = r_{L1}\ {I_{\text{dc-rms}}}^2 + r_{N1}\left(\frac{2D - n - nD}{n\,(1+D)}\ I_{\text{dc-rms}}\right)^2 + r_{N2}\left(\frac{1+2D}{(1+D)}\ I_{\text{dc-rms}}\right)^2. \tag{43}$$

The input inductor and coupled transformer copper losses are calculated as

$$P_{cu-L1} = \frac{(\text{MLT}).\rho.{I_{\text{dc-rms}}}^2}{K_u.W_A} \tag{44}$$

$$P_{cu-T} = \frac{(\text{MLT}).\rho.\left(\frac{N_1(2D-n-nD)I_{\text{dc-rms}}}{n(1+D)} + \frac{N_2(1+2D)I_{\text{dc-rms}}}{(1+D)}\right)^2}{K_u.W_A}. \tag{45}$$

Then, the total magnetic copper loss is calculated as

$$P_{\text{cu-tot}} = P_{\text{cu}-L1} + P_{\text{cu}-T} = \frac{(\text{MLT}).\rho.{I_{\text{dc-rms}}}^2}{K_u.W_A} + \frac{(\text{MLT}).\rho.\left(\frac{N_1(1+2D)I_{\text{dc-rms}}}{n(1+D)} + \frac{N_2(1+2D)I_{\text{dc-rms}}}{(1+D)}\right)^2}{K_u.W_A} \tag{46}$$

where ρ, MLT, W_A, K_u, $I_{\text{dc-rms}}$, N_1, N_2, $i_{N1-\text{rms}}$, $i_{N2-\text{rms}}$, are wire effective resistivity, mean length per turns, core window area, winding fill factor, input inductor's RMS current, primary winding turns number, secondary winding turns number, RMS current of primary winding, and RMS current of the secondary winding, respectively. Furthermore, the coupled transformer's core loss of the coupled transformer is calculated from (47), where l_m, A_e, K_{fe}, $B_{\max}$, and β, represent mean magnetic path length, core cross-sectional area, core loss coefficient, peak ac flux density, and core loss exponent, respectively,

$$P_{fe} = l_m.A_e.K_{fe}.{B_{\max}}^{\beta}. \tag{47}$$

Therefore, the total power loss of the magnetic elements is

$$P_{\text{Magnetic-tot}} = P_{\text{ESR}-L} + P_{\text{cu-tot}} + P_{\text{fe.}} \tag{48}$$

By considering $r_{L1} = 0.046\Omega$, $r_{N1} = 0.131\Omega$, $r_{N2} = 0.046\Omega$, $\rho = 2.21\times10^{-8}\Omega\cdot$m, MLT = 0.2 m, $W_A = 1.77\times10{-}4$ m^2, $K_u = 0.4$, $l_m = 0.2$ m, $A_e = 1.77\times10^{-4}$m^2, K_{fe}= 1.2×10^{-3}W/cm^3, $B_{\max}$= 0.22T, $\beta = 2.5$, the total magnetic loss is obtained 15.99 W. The power loss of the capacitors is attributable to their ESRs as

$$P_{C-\text{tot}} = P_{ESR-C} = \sum_{i=1}^{5} r_{Ci}.{I_{Ci-\text{rms}}}^2. \tag{49}$$

The rms equations of capacitors' currents are obtained as

$$\begin{cases} I_{C1-\text{rms}} = \sqrt{\frac{n^2D(1+D)^2}{(1-n-2D-nD)^2} + \frac{(1-D)^3}{(nD-1)^2}}\, I_{\text{dc}} \\ I_{C2-\text{rms}} = \sqrt{D + \frac{(1-D)n^2(1+D)^2}{(1+2D+n)^2}}\, I_{\text{dc}} \\ I_{C3-\text{rms}} = \\ \quad \sqrt{\frac{n^2D(1+D)^2}{(2D+n-2nD)^2} + \left(\frac{(1-D)n(1+D)}{n(1+2D)} + \frac{(1-D)(D-1)}{nD-1}\right)^2}\, I_{\text{dc}} \\ I_{C4-\text{rms}} = \\ \quad \sqrt{\frac{n^2D(1+D)^2}{(1-n-2D-nD+2nD)^2} + \left(\frac{(1-D)(D-1)}{nD-1} - \frac{(1-D)(1+D)}{n^2(1+2D)^2}\right)^2}\, I_{\text{dc}} \\ I_{C5-\text{rms}} = \sqrt{\frac{n^2D(1+D)^2}{(1-n-2D-nD)^2} + \frac{(1-D)(1+D)^2}{(1+2D)^2}}\, I_{\text{dc}} \end{cases} \tag{50}$$

From (50) and subtititing $r_c = 50$ mΩ in (49), the theoretical power loss of the capacitors is calculated to be approximately 3.74 W**.** The power losses in the power switches are a result of switching and conduction losses. The switching power loss of the IGBTs in the inverter is given by (51), where C_{CE} is the IGBTs junction capacitance and V_{sw} is from (32).

$$\begin{aligned} P_{\text{sw}} &= P_{\text{turn-off}} + P_{\text{turn-on}} \\ &= \frac{1}{2}.\left(\frac{3}{2}C_{\text{CE}}\right).f_{\text{sw}}.{V_{\text{sw}}}^2 + \frac{1}{2}.\left(\frac{3}{2}C_{\text{CE}}\right).f_{\text{sw}}.{V_{\text{sw}}}^2 \\ &= \frac{3}{2}C_{\text{CE}}.f_{\text{sw}}.\left(\frac{-1.85+11.4G}{9.7}V_{\text{in}}\right)^2 \\ &= \frac{3}{2}C_{\text{CE}}.f_{\text{sw}}.\left(\frac{(-1.85+11.4G)P_O}{9.7\,I_{\text{dc}}}\right)^2. \end{aligned} \tag{51}$$

The RMS value of the ST current is

$$i_{\text{ST-rms}} = \sqrt{\frac{1}{T}.\int_0^T {i_{\text{ST}}}^2\,dt} = 2\sqrt{D}\,I_{\text{dc.}} \tag{52}$$

The conduction loss of the IGBTs is given by (53), where r_S represents the ON-resistance of the IGBTs

$$P_{\text{con}} = 6.r_S.\left(\frac{i_{\text{ST-rms}}}{3}\right)^2 = \frac{8}{3}.r_S.\left(\frac{D\,Po^2}{{V_{\text{in}}}^2}\right). \tag{53}$$

From [39], the total power loss of the switches is obtained as

$$P_{S-\text{tot}} = \frac{3}{4}.C_{\text{CE}}.f_{\text{sw}}.\left(\frac{(-1.85+11.4G)P_O}{9.7\,I_{\text{dc}}}\right)^2 + \frac{8}{3}.r_S.\left(\frac{D\,Po^2}{{V_{\text{in}}}^2}\right). \tag{54}$$

According to the datasheets, C_{CE}= 2.1 nF, $r_S = 0.025\,\Omega$. The conduction loss is calculated as 9.92 W, while the switching loss is 10.08 W. Therefore, the total power loss of the switches is approximately 20 W. The loss of the diodes because of their forward voltage drop (V_{Fd}) is attained as

$$P_{V_{Fd}} = \sum_{i=1}^{4} V_{Fd}.I_{Di} = V_{Fd}\,I_{\text{dc}}\left(\frac{2}{\pi} + \frac{(1+D)}{\pi} + \frac{(2D)}{\pi(1-n^2)}\right) \tag{55}$$

where I_D represents the diodes average currents. The loss from the diodes parasitic resistances is

$$P_{R_{sd}} = \sum_{i=1}^{4} R_{sd}.{I_{Di-\text{rms}}}^2 \tag{56}$$

where R_{sd} presents the diodes' parasitic resistance. Additionally, the diodes' reverse recovery losses are calculated from (57), where Q_{rr} and V_{rrD} represent the reverse recovery charge and voltage of the diodes, respectively,

$$P_{rrd} = \sum_{i=1}^{4} Q_{rr}.f_{\text{sw}}.V_{rrDi}. \tag{57}$$

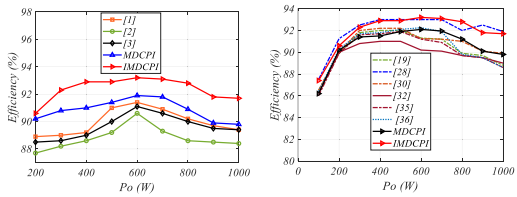


Fig. 20. Comparison of the estimated efficiency at $f_{\rm sw} = 10$ kHz, STDR = 10%, and M = 0.9 for the proposed converters.(a) Selected DC—DC–AC magnetically coupled SC topologies. (b) Magnetically coupled impedance source topologies.

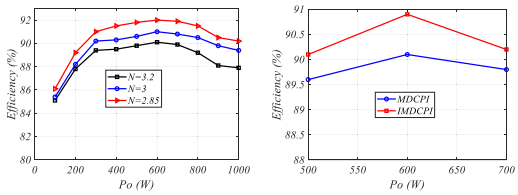


Fig. 21. (a) Efficiency of the proposed inverters at at $f_{\rm sw} = 50$ kHz and different turns ratios. (b) Measured efficiency of the proposed inverters from experimental tests.

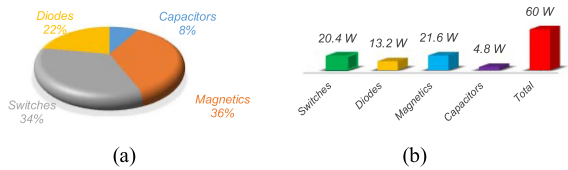


Fig. 22. Power loss distribution of the proposed IMDCPI at $Po \cong 600$ W. (a) Percentage. (b) In watts.

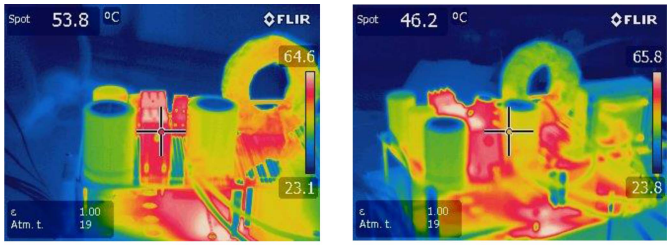
Thus, the diodes' total power loss can be represented by

$$P_{D-tot} = \sum_{i=1}^{4} (V_{Fd} \,.I_{Di}) + \left(R_{sd}.I_{Di-\rm rms}{}^2\right) + (Q_{rr}.f_{\rm sw}.V_{rrDi})\,. \tag{58}$$

According to the diode datasheets, we have $V_{Fd} = 1.4$ V, R_{sd} = 53 mΩ, Q_{rr} = 30nC. The final diode loss is approximately 12 W. Finally, the theoretical total power loss of the proposed IMDCPI is approximately 51.7 W, resulting in an estimated efficiency of around 92% at an output power of 600 W. The efficiency of the proposed inverters have been compared with its counterparts under the same windings turns number, switching frequency, STDR, and modulation index. Additionally, some of the selected topologies have been designed based on dc–dc converters. For a fair comparison, their efficiencies in a dc–ac three-phase inverter configuration have been investigated. By using the simulation, datasheets, and equations to obtain the efficiency, we can plot Fig. 20. Fig. 20(a) shows the efficiency comparison between the proposed inverters and selected SC-based dc–dc–ac converters with coupled inductors. To evaluate efficiency, we conducted simulations in PSIM, comparing the proposed IMDCPI and MDCPI inverters with three selected switched-capacitor-based dc–dc converters proposed in [1], [2], and [3] connected to a full-bridge inverter. In [3], a family of converters is presented. Among the topologies discussed, we have selected the best one, referred to as topology V. Furthermore, a conventional PWM technique was applied to these converters to address their short-circuit considerations. Fig. 20(a) shows that, the proposed IMDCPI and MDCPI inverters demonstrate superior efficiency across the evaluated power range. This improvement is attributed to the higher voltage boost capability of the proposed inverters, resulting in lower output current and minimized conduction losses. Additionally, the direct dc–ac conversion eliminates the need for redundant power processing stages, while the absence of dc-side switches further reduces switching and conduction losses. Fig. 20(b) shows the efficiency comparison between the proposed inverters and selected magnetically coupled impedance source converters. It can be seen that the proposed IMDCPI exhibits higher efficiency compared to its counterparts, except for the proposed topology in [28]. This is due to the higher voltage and lower output current of the proposed inverter. However, it demonstrates higher or equal efficiency in the range of 500–800 W. The lower efficiency at lower output powers is attributed to power loss in the one additional diode compared with the topology in [28]. Additionally, the proposed MDCPI shows higher efficiency in the range of 600–800 W compared with its counterparts. The lower efficiency of the MDCPI, compared to the IMDCPI and the converter in [28], is due to its discontinuous input current, despite having a lower number of components. Fig. 21(a) shows the efficiency of the proposed IMDCPI at different turns ratios. It can be observed that the proposed converter exhibits higher efficiency at lower turns ratios. Fig. 21(b) illustrates the efficiency of the proposed inverters from experimental tests at three operating points of output power: 500; 600; and 700 W. The experimental power loss distribution of the proposed IMDCPI is illustrated in Fig. 22(a) and (b). The total power loss is approximately 60 W, and the power loss distribution closely matches the values obtained from the theoretical power loss analysis. The observed differences primarily stem from non-idealities in the experimental setup. It is noted that the cumulative losses of the diodes are lower than those of the IGBTs. This is mainly because the diodes are fast-recovery types and are fewer in number compared to the six IGBTs in the inverter bridge. The estimated junction temperature is calculated based on the standard thermal relation:

$$\mathrm{T}j = \mathrm{T}_{\rm case} + (\mathrm{P}_{\rm loss} \times \mathrm{R}_{\theta \rm JC}) \tag{59}$$

where $R_{\theta\,\rm JC}$ represents the junction-to-case thermal resistance. For the STTH12R06 diodes, $R_{\theta\,\rm JC} = 2$°C/W with a maximum allowable junction temperature of 150°C, and for the IGBTs, $R_{\theta\,\rm JC} = 0.63$°C/W with a maximum junction temperature of 175°C. The thermal images of both proposed inverters are shown in Fig. 23(a) and (b), highlighting that the highest heat generation occurs in the IGBTs and diodes. However, the recorded temperatures remain below 65°C, which is well within safe operating limits for power electronics converters under this operating range. From Fig. 23, the case temperatures ranged between 40°C and 65°C. Even under the worst-case assumption (65°C case



(a) (b)

Fig. 23. Thermal image of (a) MDCPI and (b) IMDCPI.

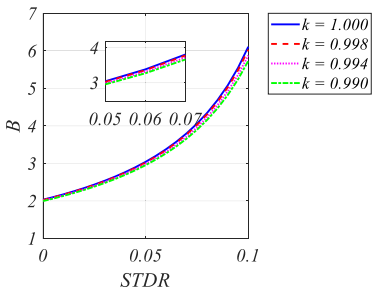


Fig. 24. Boost factor with winding and inductor resistances.

temperature), the calculated junction temperatures remain well within safe operating limits. Winding resistance can introduce additional voltage drops, impacting the dc-link voltage. By considering these resistances and applying KVL to equivalent circuits of the proposed IMDCPI, and then using volt-second balance principle to the windings, and input inductor, the voltage across inverter bridge can be updated as

$$Vi=\frac{n(\gamma+1)+i_{\rm dc}.(r_{L_{\rm in}}-r_{N_1})-n(\gamma+1)\,i_{N_2}.r_{N_2}-1}{n(\gamma+1)-2nD(\gamma+1)-2}\,V_{\rm in}. \tag{60}$$

According to experimental parameters and (60), the voltage boost factor versus STDR is plotted, as shown in Fig. 24. As depicted in the plots, these resistances result in a slight reduction of the boost factor. Table VI gives the component count and estimated cost for the proposed converters compared to similar voltage multiplier converters. The table demonstrates that the proposed MDCPI has a lower cost and fewer components, leading to reduced complexity. Meanwhile, the IMDCPI, though slightly higher in cost, maintains a reasonable component count and offers advantages such as ultrahigh voltage gain, dc-link voltage clamping, and continuous input current without the need for an input filter. To compare the proposed inverters with state-of-the-art converters, Fig. 25 presents a normalized bar chart based on eleven key performance indicators. Structural or qualitative features, including low input current ripple (L.I.C.R), ST immunity, trans-inverse structure, direct dc–ac conversion, and common ground—are binary and scored as either 1 or 5, with 5 denoting a desirable attribute. The L.I.C.R score for converters [1], [2], [3] and MDCPI is set to 2, as their input current is discontinuous but not subject to inrush current due to the series-connected coupled inductors. Quantitative metrics

TABLE VI
COMPARISON OF THE PROPOSED INVERTERS WITH SELECTED TOPOLOGIES IN TERMS OF ESTIMATED COST

Ref.	Num. of				Estimated Cost
	C	L +CL	D+S	Total	
Wu et al. [1]	3	0 + 1 (DW)	3 + 7	14	$170
Ye et al. [2]	5	0 + 1 (TW)	4 + 8	19	$210
da Silva Bernardo Loureiro et al. [3]	3	0 + 1 (DW)	3 + 7	14	$170
Baddipadiga and Ferdowsi [6]	5	2 + 0	4 + 8	18	$230
Prabhala et al. [7]	5	2 + 0	5 + 8	19	$235
Ding et al. [29]	5	1 + 2 (DW)	5 + 6	20	$320
MDCPI	3	0 + 1 (DW)	3 + 6	13	$160
IMDCPI	5	1 + 1 (DW)	4 + 6	17	$225

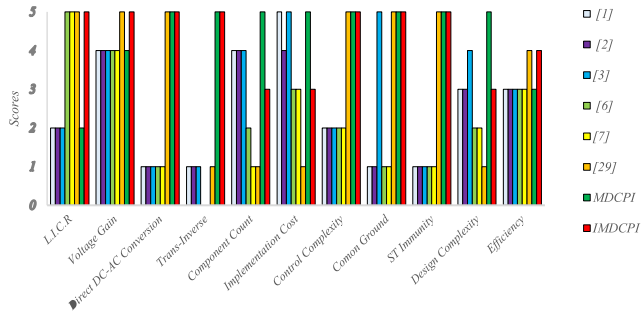


Fig. 25. Grouped bar chart comparing key performance indicators across various converters (higher scores indicate better performance).

like voltage gain, efficiency, cost, and component count are rated based on reported or calculated values, with higher scores reflecting better performance. Fig. 25 shows that MDCPI suits applications prioritizing low component count, simplicity, and cost, while IMDCPI is preferable for continuous input current, reduced voltage spikes, and very high gain. Both also help reduce control complexity in direct dc–ac conversion.

VI. CONCLUSION

In this article, a class of magnetically coupled inverters based on the DCP structure was proposed. Compared to conventional CP topologies, the proposed converters achieve high voltage gain without requiring additional stages, and avoid output voltage drop and excessive capacitor stress. They offer improved performance with lower transformer turns ratio, reduced STDR, and higher modulation index. The IMDCPI structure also demonstrates a better input current profile and lower magnetic flux swing, as confirmed by PEmag simulations. A detailed power loss analysis and 600 W experimental validation show agreement with theory, confirming the effectiveness of the proposed topologies for high-gain renewable and grid-connected applications.

REFERENCES

[1] G. Wu, X. Ruan, and Z. Ye, "High step-up DC–DC converter based on switched capacitor and coupled inductor," *IEEE Trans. Ind. Electron.*, vol. 65, no. 7, pp. 5572–5579, Jul. 2018.

[2] Y. Ye, K. W. E. Cheng, and S. Chen, "A high step-up PWM DC–DC converter with coupled-inductor and resonant switched-capacitor," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7739–7749, Oct. 2017.

[3] P. H. C. da Silva Bernardo Loureiro, T. M. K. Faistel, A. Toebe, and A. M. S. S. Andrade, "Generation and comparative analysis of high voltage gain non-isolated DC-DC converters with ladder switched capacitor and coupled inductor," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 6742–6753, Dec. 2022.

[4] B. Andres, L. Romitti, A. M. S. S. Andrade, L. Roggia, and L. Schuch, "Comprehensive analysis of voltage step-up techniques for isolated SEPIC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 10, pp. 4298–4311, Jul. 2022.

[5] R. Wang et al., "Modeling and analysis of MHz-frequency PRC-LCLC resonant converter utilizing only parasitic capacitance from planar transformer and Cockcroft–Walton voltage multiplier as parallel capacitor," *IEEE Trans. Power Electron.*, vol. 40, no. 4, pp. 5400–5411, Apr. 2025.

[6] B. P. Baddipadiga and M. Ferdowsi, "A high-voltage-gain dc-dc converter based on modified Dickson charge pump voltage multiplier," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7707–7715, Oct. 2017.

[7] V. A. K. Prabhala, P. Fajri, V. S. P. Gouribhatla, B. P. Baddipadiga, and M. Ferdowsi, "A DC–DC converter with high voltage gain and two input boost stages," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4206–4215, Jun. 2016.

[8] S. Park, J. Yang, and J. Rivas-Davila, "A hybrid Cockcroft– Walton/Dickson multiplier for high voltage generation," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2714–2723, Mar. 2020.

[9] S. Esmaeili, M. Shekari, M. Rasouli, S. Hasanpour, A. A. Khan, and H. Hafezi, "High gain magnetically coupled single switch quadratic modified SEPIC DC-DC converter," *IEEE Trans. Ind. Appl.*, vol. 59, no. 3, pp. 3593–3604, May–Jun. 2023.

[10] S. M. J. Mousavi, E. Babaei, M. Sahabi, and H. Komurcugil, "A class of bidirectional single-phase Z-source AC-AC converter with continuous input current and reduced component count," *IEEE Trans. Power Electron.*, vol. 38, no. 5,pp. 6311–6318, May 2023.

[11] S. Esmaeili, E. Azimi, H. Hafezi, A. Mahmoudi, M. Jamil, and A. A. Khan, "Magnetically coupled single-phase AC-AC converter with reduced number of passive components," *IEEE Access*, vol. 10, pp. 79628–79643, Jul. 2022.

[12] H. M. F. Younis, S. Esmaeili, and A. A. Khan, "Autotransformer Incorporated single-phase AC–AC converter," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 6, no. 2, pp. 754–767, Apr. 2025.

[13] F. Liu, J. Wan, Y. Li, and K. Z. Liu, "A new soft-switching AC-DC converter based on coupled inductors for onboard charging applications," *IEEE Trans. Power Electron.*, vol. 38, no. 3,pp. 3433–3443, Mar. 2023.

[14] S. Konar, P. K. Gayen, and S. S. Saha, "A new variant of turns-ratio independent shoot-through current based magnetically-coupled Z-source inverter with smooth DC-link voltage and enhanced high-gain," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 72, no. 6, pp. 858–862, Jun. 2025.

[15] M.M. Rezazadeh, A. Nikbahar, and S. Sharifi, "A family of high voltage gain quasi-Δ-source impedance networks," *IET Power Electron.*, vol. 14, pp. 807–820, Dec. 2020.

[16] S. Yazdani, A. Rajaei, and A. Rahideh, "Speed control and maximum efficiency operation of three-phase squirrel cage induction motors supplied by modified impedance source inverter," *IET Power Electron.*, vol. 17, pp. 2878–2889, 2024, doi: 10.1049/pel2.12802.

[17] Y. Ji, S. Ji, L. Geng, J. Mo, and Y. Liu, "Voltage-doubler reverse coupled-inductor impedance network inverter with continuous and discontinuous inductor current operation," *IEEE Trans. Ind. Electron.*, vol. 13, no. 1, pp. 230–243, Feb. 2025, doi: 10.1109/TIE.2025.3460123.

[18] Z. Aleem and M. Hanif, "Operational analysis of improved Γ-Z-source inverter with clamping diode and its comparative evaluation," *IEEE Trans. Ind. Electron.*, vol. 64, no. 12, pp. 9191–9200, Dec. 2017.

[19] J. Ma, H. Liu, J. Chen, Y. Li, and P. C. Loh, "A Family of coupled dual-winding impedance-source inverters with continuous input currents and No DC-link voltage spikes," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 7904–7914, Dec. 2022.

[20] H. Liu, Y. Li, Z. Zhou, W. Wang, and D. Xu, "A family of low-spike high-efficiency Y-source inverters," *IEEE Trans. Ind. Electron.*, vol. 66,no. 12, pp. 9288–9300, Dec. 2019.

[21] H. Liu et al., "A family of high step-up coupled-inductor impedance-source inverters with reduced switching spikes," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9116–9121, Nov. 2018.

[22] M. S. Mahmoodabadi, M. Monfared, and A. Mahdavi, "A family of high-boost active-switched impedance networks with low shoot-through current using coupled-inductor," *IEEE Trans. Ind. Electron.*, vol. 72, no. 3, pp. 2576–2587, Mar. 2025.

[23] R. Reddivari and D. Jena, "A negative embedded differential mode Γ-source inverter with reduced switching spikes," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 10, pp. 2009–2013, Oct. 2020.

[24] S. Esmaeili, A. Mahmoudi, S. Kahourzadeh, and A. Mostaan, "Dual winding magnetically coupled impedance-source inverters with DC-rail voltage clamping circuits," in *Proc. IEEE 12th Energy Convers. Congr. Expo.*, 2021, pp. 2286–2291.

[25] A. Nikbahar and M. Monfared, "A family of high step-up magnetically coupled impedance source inverters with clamped DC-link voltage and low shoot-through current," *IEEE Trans Power Electron.*, vol. 38, no. 1, pp. 107–111, Jan. 2023.

[26] A. Nikbahar and M. Monfared, "Smooth DC-link Y-source inverters: Suppression of shoot-through current and avoiding DC magnetism," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 12357–12369, Oct. 2022.

[27] Z. Aleem, H. K. Yang, H. F. Ahmed, and J. W. Park, "Quasi-clamped ZSI with two transformers," *IEEE Trans. Ind. Electron.*, vol. 68, no. 10, pp. 9455–9466, Oct. 2020.

[28] M. Zhang, H. Li, Y. Hao, K. Li, and X. Ding, "A modified switched-coupled-inductor quasi-Z-source inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 3, pp. 3634–3646, Jun. 2021.

[29] X. Ding, K. Li, Y. Hao, H. Li, and C. Zhang, "Family of the coupled inductor multiplier voltage rectifier quasi-Z-source inverters," *IEEE Trans. Ind. Electron.*, vol. 68, no. 6, pp. 4903–4915, Jun. 2021.

[30] H. F. Ahmed, H. Cha, S. H. Kim, and H. G. Kim, "Switched-coupled-inductor quasi-Z-source inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1241–1254, Feb. 2016.

[31] S. Sharifi, Y. Chulaee, H. A. Zarchi, and M. Monfared, "Generalized three-winding switched-coupled-inductor impedance networks with highly flexible gain," *IEEE Trans. Ind. Electron.*, vol. 68, no. 3, pp. 2130–2141, Mar. 2021.

[32] S. Sharifi and M. Monfared, "Modified series and tapped switched coupled-inductors quasi-Z-source networks," *IEEE Trans. Ind. Electron.*, vol. 66, no. 8, pp. 5970–5978, Aug. 2019.

[33] S. Esmaeili and A. A. Khan, "Ultrahigh step-up switched-capacitors-coupled-inductor inverter," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 5, no. 3, pp. 974–984, Jul. 2024.

[34] X. Ding, Y. Hao, K. Li, H. Li, Z. Wei, and W. Wu, "Extensible Z-source inverter architecture: Modular construction and analysis," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1742–1763, Feb. 2021.

[35] X. Ding, Y. Liu, D. Zhao, and W. Wu, "Generalized cockcroftwalton multiplier voltage Z-source inverters," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7175–7190, Jul. 2020.

[36] S. Esmaeili, M. J. A.A.Khan, U. A. Khan, H. F. Ahmed, and S.. Ahmed, "Improved high step-up Cockcroft-Walton magnetic coupling inverter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 6, pp. 1981–1985, Jun. 2023.

[37] H. Li, Y. Chen, and T. Jin, "A soft-switched SEPIC-based high voltage gain DC–DC converter for renewable energy applications," *IEEE Trans. Ind. Electron.*, vol. 72, no. 4, pp. 3746–3757, Apr. 2025.

[38] J. Cai, M. Fu, and X. Zhang, "A generalized voltage gain model of the asymmetric Γ-source converter with typical parasitic parameters considered," *IEEE Trans. Power Electron.*, vol. 40, no. 7, pp. 9577–9587, Jul. 2025.

[39] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Norwell, MA, USA: Kluwer, 2001.

[40] M. K. Kazimierczuk, "Boost PWM DC-DC converter," in *Pulse-Width Modulated DC-DC Power Converters*, 2nd Ed.. Chichester, U.K.: Wiley, 2016, pp. 98–106.