Hybrid Commutation-Based Active Loss-Balancing Control Scheme for Si/SiC Hybrid Three-Level ANPC Inverters

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***Abstract*—The hybrid utilization of silicon (Si) and silicon carbide (SiC) devices is an effective way to improve the efficiency and power density of three-level active neutral-point-clamped (3L-ANPC) inverters while the hardware cost is not significantly increased. However, the unbalanced power loss between SiC devices reduces the inverter lifespan and increases the complexity of the cooling system design. A hybrid commutation-based active loss-balancing control (HC-ALBC) scheme is proposed for Si/SiC hybrid 3L-ANPC inverters. First, the loss distribution of different commutation processes in the 4SiC-III hybrid 3L-ANPC inverter is analyzed. Then, three different commutation processes are utilized with an optimized usage ratio to actively control the power loss difference between SiC devices. As a result, the balanced power loss is achieved under different output power and modulation indices. Finally, a 6-kW Si/SiC hybrid inverter prototype is built, and experimental results show that the proposed HC-ALBC scheme achieves balanced power loss between SiC devices. Besides, both high efficiency and excellent harmonic performance are achieved.**

***Index Terms*—Active neutral-point-clamped inverter, commutation, power loss balancing control, Si/SiC hybrid, three-level inverter.**

I. Introduction

THREE-LEVEL active neutral-point-clamped (ANPC) inverters are widely used in photovoltaic power generation and electric transportation due to their lower voltage stress and lower harmonic distortion [1], [2]. To achieve higher power density, reducing the filter size of the ANPC inverter is desired by increasing the switching frequency [3], [4]. However, more switching loss is generated as well. Compared with silicon (Si) devices, silicon carbide (SiC) devices such as SiC metal-oxide-semiconductor field-effect transistors (MOSFET) feature lower switching loss and higher thermal conductivity [5], [6]. Thus, ANPC inverters using SiC devices could operate with higher switching frequency and temperature, resulting in higher power density. However, as illustrated in Fig. 1, SiC devices are more expensive than their Si counterparts in similar specifications [7]. Thus, full-SiC ANPC inverters significantly increase hardware costs.

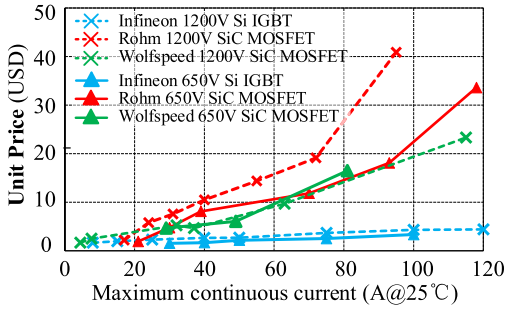

Fig. 1. Unit prices of Si and SiC devices according to http://www.mouser.cn/.

To achieve the tradeoff between the inverter performance and the hardware cost, the hybrid utilization of SiC MOSFETs and Si IGBTs is studied [8], [9], [10]. Five different Si/SiC hybrid ANPC inverters and their optimized driving signals are presented in Fig. 2. In Fig. 2(a), two SiC MOSFETs are employed to achieve the high-frequency switching of the bridge-leg voltage, and four Si IGBTs only operate in fundamental frequency [11]. Thus, the switching loss can be reduced while only two SiC MOSFETs are utilized. Fig. 2(b) presents the topology of another 2-SiC hybrid solution [12]. All devices operate with high-frequency switching during half of the fundamental period. The switching loss of four Si IGBTs is reduced by optimizing the modulation scheme. Therefore, the switching loss is mainly generated by two SiC MOSFETs as well. These 2-SiC hybrid topologies feature low hardware cost and high efficiency, but suffer from excessive thermal stress on the two SiC devices due to concentrated power losses, thereby limiting the power rating. 4-SiC hybrid topologies are proposed to lower the switching loss of each SiC MOSFET, leading to higher output power and power density, as depicted in Fig. 2(c)–(e). By optimizing the

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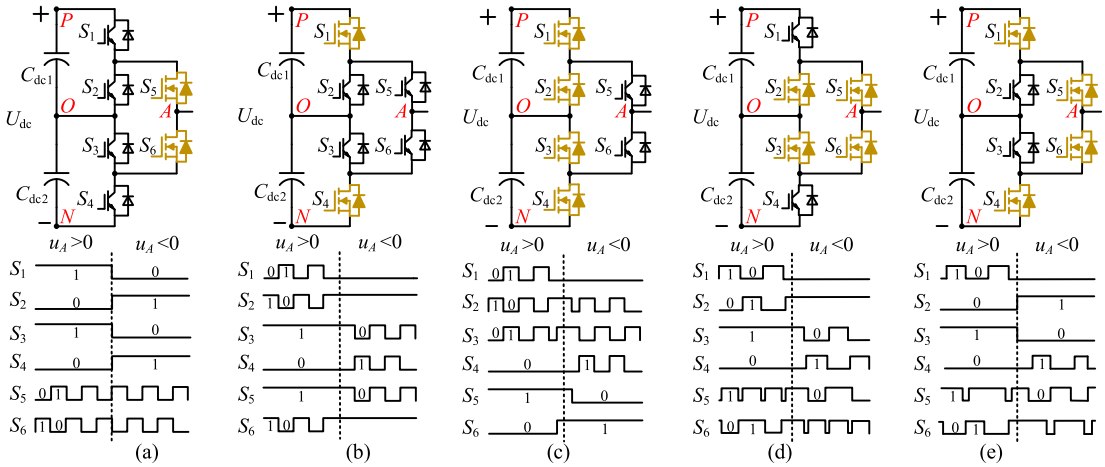


Fig. 2. Topologies with their switching signal sequences of SiC/Si hybrid 3L-ANPC inverters. (a) 2SiC-I hybrid topology [11]. (b) 2SiC-II hybrid topology [12]. (c) 4SiC-I hybrid topology [13]. (d) 4SiC-II hybrid topology [14]. (e) 4SiC-III hybrid topology [15].

modulation scheme and adopting zero-current switching (ZCS) for the Si IGBTs, the switching loss is generated by four SiC MOSFETs, achieving a more averaged loss distribution compared with 2-SiC hybrid topologies [13], [14], [15]. Compared to the 2SiC-I topology, the 4SiC-I topology increases the output power by a factor of 1.47 [16]. In the 4SiC-II hybrid topology, the ZCS of Si devices and dual current paths for all O states are achieved at all PF conditions, which can further improve the efficiency. However, the switching losses of inner and outer SiC MOSFETs still have a significant difference [16], resulting in excessive thermal stress on some SiC MOSFETs. This uneven thermal distribution leads to great difficulty in heat sink design [17], [18], limits the output power, and accelerates device aging, thereby limiting both the power density [19], [20], [21] and lifespan of the inverter [22], [23], [24].

Improving the modulation scheme can effectively achieve balanced power loss between each switching device in Si/SiC hybrid 3L-ANPC inverters. A doubling switching frequency (DF) scheme is proposed in [25], where the modulation wave is compared with two opposite carrier signals to enable two different current paths for O-level within a switching period. As a result, the switching losses are evenly distributed between inner and outer switching devices. A similar scheme is proposed in [26], where three sinusoidal modulation signals with different amplitudes are compared with one carrier signal to enable different current paths for the O-level. In [27], by modifying the commutation process, the outer switching devices generate the turn-OFF losses, and turn-ON losses are generated by the inner switching devices. As a result, the switching losses are distributed in outer and inner switching devices. However, these schemes only balance the switching losses between the inner and outer switching devices, and the conduction loss is not considered. Jiao and Lee [28] introduced a dual current path scheme for O levels, further reducing the conduction losses of inner switching devices. Unfortunately, these schemes use fixed current paths at the O level under varying operating conditions. Thus, the power losses of the switching devices cannot be balanced under different output power or modulation indices.

To actively balance the power loss under varying operation conditions, the hybrid utilization of different switching frequencies and redundant O levels with different current paths are combined according to calculated power loss or estimated junction temperature. Based on the DF scheme, Deng et al. [29] introduced an adaptive doubled frequency scheme, which balances the power loss by controlling the duty cycles of redundant O levels with different current paths within a switching period. However, the switching times are increased. To avoid the additional switching times in each switching period, different current paths for O-level can be hybrid utilized within a fundamental period by adjusting the amplitudes of the modulation signals [30]. Similarly, in [21], the redundant O levels are hybrid utilized within ten fundamental periods, and an offline power loss calculation module is employed to control the ratio of redundant O levels. However, this scheme leads to significant fluctuations in junction temperature. In [20], the switching device with the maximum junction temperature is detected, and the current path of the O level is optimized to reduce the junction temperature of the dedicated switching device. Although the maximum device temperature is controlled, all switching devices operate in high-frequency switching, which increases the switching loss of Si devices and thus reduces the efficiency of Si/SiC hybrid inverters [31]. An active thermal control (ATC) scheme is introduced in [32], where the high and low switching frequencies are mixed based on instantaneous current values to improve efficiency. Meanwhile, different current paths of O level are applied with different switching frequencies to achieve balanced power loss distribution. However, reducing switching frequencies degrades the harmonic performance and the power density. Therefore, the existing active loss-balancing schemes cannot achieve low current total harmonic distortion (THD) and high efficiency while actively balancing the power loss.

A hybrid commutation-based active loss-balancing control (HC-ALBC) scheme is proposed for Si/SiC hybrid 3L-ANPC inverters. First, the power loss distribution of different commutation processes in the 4SiC-III hybrid 3L-ANPC inverter is analyzed. Then, three commutation processes with different loss

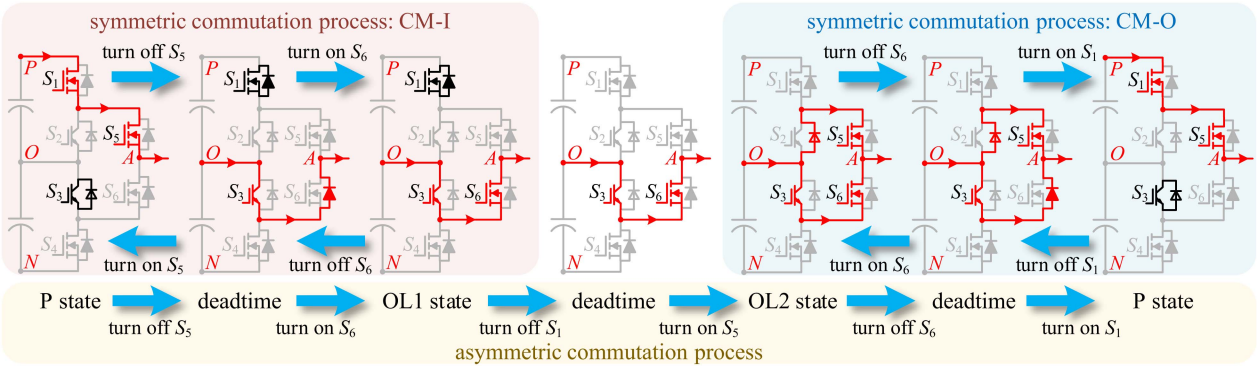


Fig. 3. Different commutation processes at the positive half period.

TABLE I
SWITCHING STATES OF THE 4SIC-III HYBRID 3L-ANPC INVERTER

Switching states	S_1	S_2	S_3	S_4	S_5	S_6	Voltage
P	1	0	1	0	1	0	$0.5U_{dc}$
OL1	1	0	1	0	0	1	0
OL2	0	0	1	0	1	1	0
OL3	0	0	1	0	0	1	0
OU1	0	1	0	1	1	0	0
OU2	0	1	0	0	1	1	0
OU3	0	1	0	0	1	0	0
N	0	1	0	1	0	1	$-0.5U_{dc}$

distribution characteristics are utilized in a hybrid manner. The usage ratio of different commutation processes is optimized by calculating the power loss in real time to achieve balanced loss distribution under different operating conditions. The rest of this article is structured as follows: Section II analyzes the power loss distribution in detail by using different commutation processes. In Section III, the proposed HC-ALBC scheme is presented. In Section IV, a three-phase 4SiC-III hybrid 3L-ANPC inverter prototype was built to conduct experiments. Section V concludes this article.

II. POWER LOSS ANALYSIS OF THE 4SIC-III HYBRID 3L-ANPC INVERTER

The 4SiC-III hybrid 3L-ANPC inverter shown in Fig. 2(e) is the previous work reported in [15]. In this section, the power loss distribution of a 4SiC-III hybrid 3L-ANPC inverter with different commutation processes is analyzed to explore the active power loss control method of each switching device.

A. Topology and Switching States Analysis

In ANPC inverters, the switching devices S_1 to S_6 of each bridge leg are categorized as outer switching devices (S_1 and S_4), inner switching devices (S_5 and S_6), and clamping switching devices (S_2 and S_3). In the 4SiC-III Hybrid 3L-ANPC inverter, the SiC MOSFETs are used for the inner and outer switching devices, while Si IGBTs are used for the other switching devices. The switching states of the 4SiC-III hybrid 3L-ANPC inverter are listed in Table I, where "0" and "1" represent the off and on states of switching devices, respectively. U_{dc} is the dc-link voltage. With different switching states, the 3L-ANPC inverter can output three different voltages, including P state ($+0.5U_{dc}$), O state (0 V), and N state ($-0.5U_{dc}$). From Table I, it is obvious that O state can be realized by six redundant switching states (OL1, OL2, OL3, OU1, OU2, and OU3).

B. Analysis of Power Loss Distribution With Different Commutation Processes

Three different commutation processes of the 4SiC-III hybrid 3L-ANPC inverter at the positive half period are shown in Fig. 3. The inner commutation process (CM-I) and the outer commutation process (CM-O) have a symmetric commutation process. The OL1 and OU1 states are utilized by using CM-I, while the OL2 and OU2 states are utilized by using CM-O. The asymmetric commutation process can be considered as a combination of CM-I and CM-O within a switching period. The positive half period is utilized to analyze the power loss distribution of different commutation processes. The switching losses (E_{sw}) consist of turn-ON loss (E_{on}), turn-OFF loss (E_{off}), and the reverse recovery loss of the body diode (E_{rr}). The conduction loss (E_{con}) is also divided into three parts: the conduction loss with the P state (E_{con_P}), the conduction loss with the O state (E_{con_O}), and the conduction loss of the body diode (E_{Dcon}).

1) Loss Distribution With CM-I: As shown in Fig. 3, by using CM-I, S_5 and S_6 operate at high frequency to achieve different output voltages. During this process, S_1 has the conduction loss with the P state. S_3 has the conduction loss with the OL1 state. When the switching state is changed between the P state and OL1 state, S_5 is turned off and on, generating the turn-OFF and turn-ON losses. With the P state, S_5 also has the conduction loss. Since the inductor current flows through the body diode of S_6 in the dead time, turning on and off S_6 results in zero-voltage switching (ZVS) with no turn-ON or turn-OFF losses. S_6 has the conduction loss with the O state, and its body diode has both the conduction loss and reverse recovery loss in the dead time.

2) Loss Distribution With CM-O: By using CM-O, S_1 and S_6 operate at switching frequency at the positive half period. When the switching state is changed between the P state and OL2 state, S_1 is turned off and on, generating the turn-OFF and turn-ON losses. During this process, the conduction loss with the

TABLE II
LOSS DISTRIBUTION UNDER DIFFERENT COMMUTATION PROCESSES AT THE POSITIVE HALF PERIOD

	Symmetric commutation process: CM-I						Symmetric commutation process: CM-O						Asymmetric commutation process					
	E_{sw}			E_{con}			E_{sw}			E_{con}			E_{sw}			E_{con}		
	E_{on}	E_{off}	E_{rr}	E_{con_P}	E_{con_O}	E_{Dcon}	E_{on}	E_{off}	E_{rr}	E_{con_P}	E_{con_O}	E_{Dcon}	E_{on}	E_{off}	E_{rr}	E_{con_P}	E_{con_O}	E_{Dcon}
S_1				√			√	√		√			√			√		
S_2									√			√					√	√
S_3					√						√						√	
S_4																		
S_5	√	√		√						√	√			√		√	√	
S_6			√		√	√			√		√	√			√		√	√

P state is also generated by S_1. The conduction loss and reverse recovery loss are generated by the body diode of S_2. S_3 has the conduction loss during the OL2 state. S_5 has the conduction loss during both the P state and O state. Similar to the CM-I, turning on and off S_6 achieves ZVS. The body diode of S_6 has conduction loss and reverse recovery loss. Compared with CM-I, CM-O employs dual current paths for O state, which reduces the conduction loss.

3) Loss Distribution With the Asymmetric Commutation Process: By using the asymmetric commutation process, S_1, S_5, and S_6 operate at high frequency at the positive half period. During this process, S_1 has the conduction loss during the P state. There is no current flowing through the S_1 when the switching state is changed from the OL1 state to the OL2 state. Thus, turning off S_1 achieves zero-current switching (ZCS) with no turn-OFF loss. Due to the asymmetric commutation process, when the switching state is changed from the OL2 state back to the P state, turning ON S_1 cannot achieve ZCS, and the turn-ON loss is generated. The body diode of S_2 has conduction loss and reverse recovery loss. S_3 has the conduction loss during the O states. When the switching state is changed from the P state to the OL1 state, S_5 is turned OFF. Thus, S_5 has the turn-OFF loss. Besides, while turning on the S_5, the body diode of the S_2 will not be conducted before the drain–source voltage of S_5 is decreased to about zero [15]. Thus, turning ON S_5 achieves ZCS without turn-ON loss. Since the inductor current flows through the body diode of S_6, turning ON and OFF S_6 also achieves ZVS with no turn-ON and turn-OFF losses.

The loss distribution by using different commutation processes at the positive half period is summarized in the Table II. The loss distribution at the negative half period can be analyzed similarly and is not mentioned here for brevity. It can be seen that the CM-I generates the turn-ON and turn-OFF losses on the inner switching devices, while CM-O generates these losses on the outer switching devices. In the asymmetric commutation process, the turn-ON and turn-OFF losses are generated by outer and inner switching devices, respectively. As a result, further control of power loss distribution can be achieved by utilizing different commutation processes with different loss distribution characteristics.

III. HYBRID COMMUTATION-BASED ACTIVE LOSS-BALANCING CONTROL SCHEME

In this section, an HC-ALBC scheme is proposed, which is a hybrid that utilizes three different commutation processes with an adjustable usage ratio. As a result, the switching loss of the inner and outer SiC devices can be actively controlled. Then, the total loss can be further balanced by optimizing the ratio coefficients based on the real-time calculation of power losses under varying operating conditions.

A. Proposed HC-ALBC Scheme

The modulation signals and the driving signals of the proposed HC-ALBC scheme at the positive half period are shown in Fig. 4. u_m and u_{zP} represent the modulation signal and the positive triangular carrier signal, respectively. u_{gs1}–u_{gs6} represent the driving voltages for switching devices S_1–S_6, while u_{AO} represents the voltage between points A and O. u_k is a newly introduced modulation signal that is compared with the positive carrier signal u_{kP} to determine the commutation process in each switching period. At the positive half period, S_2 and S_4 are clamped at OFF-state, while S_3 is clamped at on-state. As shown in Fig. 4, with the proposed HC-ALBC scheme, three different commutation processes are hybrid utilized with a specific ratio within every N switching periods. These N switching periods are divided into N-1 switching periods with the symmetric commutation process and one switching period with the asymmetric commutation process. In these switching periods with symmetric commutation processes, the CM-I and CM-O schemes are hybrid utilized across different switching periods at a ratio of n_{01}: n_{02}. The switching period with the asymmetric commutation process is also shown in Fig. 4. t_O represents the duration of the O state in a switching period. In this asymmetric commutation period, the OL1 state and OL2 state are hybrid utilized. k_{11} and k_{12} represent the ratio of the duration of the OL1 and OL2 states to the t_O, respectively. By adjusting the k_{11} and k_{12}, the conduction loss can be further controlled within a switching period, enabling a more precise loss balancing control

$$\begin{cases} N = n_{01} + n_{02} + k_{11} + k_{12} \\ 1 \leqslant N \leq 0.5N_s, N \in Z \\ k_{11} + k_{12} = 1, 0 \leqslant k_{11}, k_{12} \leqslant 1 \\ 0 \leqslant n_{01}, n_{02} \leqslant N - 1, n_{01}, n_{02} \in Z \end{cases} \tag{1}$$

$$N_s = \frac{f_s}{f_g}. \tag{2}$$

By using the proposed HC-ALBC scheme, the relationship between N, n_{01}, n_{02}, k_{11}, and k_{12} is given by (1). The N_s represents the total switching periods in a fundamental period,

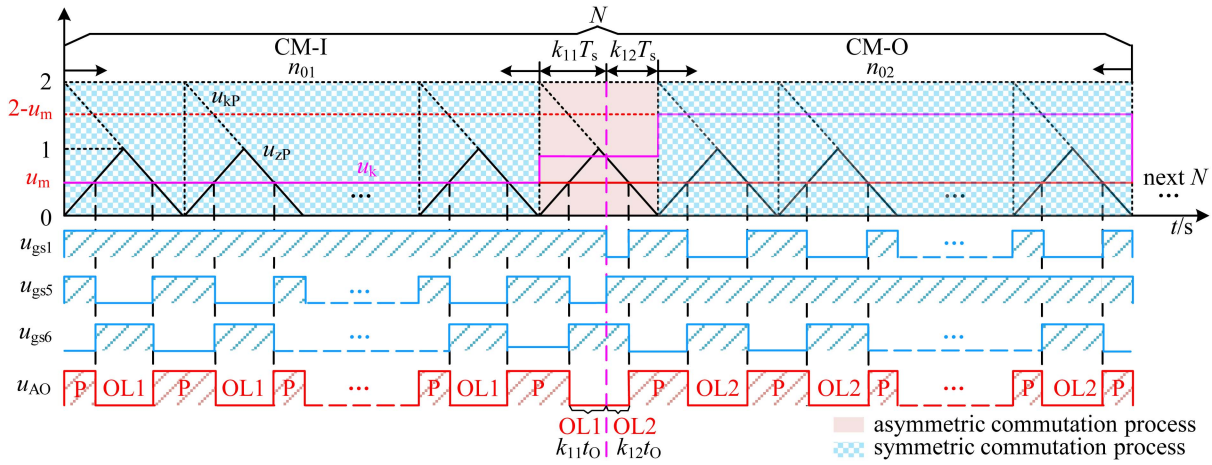


Fig. 4. Modulation signals and the driving signals of the proposed HC-ALBC scheme at the positive half period.

which is calculated by (2), where f_s is the switching frequency and f_g is the fundamental frequency. In (1), every N switching periods can be divided into n_{01} switching periods with CM-I, n_{02} switching periods with CM-O, and one switching period with the asymmetric commutation process. This asymmetric commutation period can be divided into $k_{11}T_s$ and $k_{12}T_s$. To ensure symmetrical loss distribution between the positive and negative half period, N is limited to be lower than $0.5N_s$.

As shown in Fig. 4, the commutation process in the HC-ALBC scheme can be determined by a set of ratio coefficients (N, n_{01}, n_{02}, k_{11}, k_{12}). From (1), it can be found that only three of the five ratio coefficients (N, n_{01}, k_{11}) are independent. As a result, within every N switching periods, u_k for the ith switching cycle can be calculated by (3) according to the specific ratio coefficients (N, n_{01}, k_{11}). For example, in the positive half period ($u_m>0$), the asymmetric commutation is

$$u_k(i)=\begin{cases} u_m(i) & u_m(i)\neq 0, 1\leqslant i\leqslant n_{01} \\ (2k_{11}-1)\,u_m(i)+2-2k_{11} & u_m(i)>0, i=n_{01}+1 \\ 2-u_m(i) & u_m(i)>0, (n_{01}+1)<i\leqslant N \\ (2k_{11}-1)\,u_m(i)-2+2k_{11} & u_m(i)<0, i=n_{01}+1 \\ -2-u_m(i) & u_m(i)<0, (n_{01}+1)<i\leqslant N \end{cases} \tag{3}$$

applied at the $(n_{01}+1)$th switching period within the total of N switching periods ($i=n_{01}+1$). As shown in Fig. 4, the value of u_k can be calculated based on the principle of triangle similarity using k_{11} and u_m, resulting in $(2k_{11}-1)u_m+2-2k_{11}$. The values of u_k in the other switching periods can be calculated similarly.

It is worth noting that Si IGBT in the 4SiC-I and 4SiC-II topology will have switching loss with CM-I and CM-O, respectively. Thus, the proposed HC-ALBC scheme is not suitable for these two conventional hybrid topologies. Since the 4SiC-III can be combined with the proposed HC-ALBC scheme to achieve highly balanced power loss, it is advantageous in reducing the thermal stress of SiC devices.

B. Optimal Ratio Coefficients

Based on Table II, the power loss of each switching device within every N switching periods at the positive half period is presented in Table III. Thanks to the SiC materials, the reverse recovery losses of the diodes of SiC MOSFETs can be ignored. In Table III, E_{con_O} and E'_{con_O} represent the conduction loss during the O state with a single current path and a dual current path, respectively. A similar analysis can also be conducted at the negative half period. From Table III, it can be found that the power loss distribution can be actively balanced by optimizing the ratio coefficients N, n_{01}, and k_{11}.

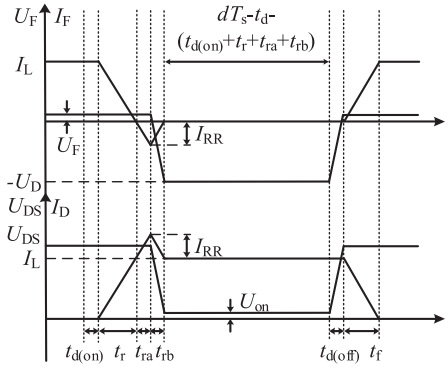


Fig. 5. Switching process of MOSFET and its body diode.

S_1 and S_5 are selected to calculate the power loss of the outer and inner SiC MOSFET, respectively. From Table III and the specific N, n_{01}, and k_{11}, the total loss generated by the S_1 and S_5 can be calculated in (4) and (5) shown at the bottom of next page, where i represents the ith switching period, j and k denote the jth set of every N switching periods and the kth switching period during a set of every N switching periods, respectively. v is defined as the remainder when $0.5N_s$ is divided by N. $e_1(v)$ and $e_5(v)$ represent the remaining losses generated by the S_1 and S_5 during the v switching periods. The detailed calculations are shown in the Appendix.

A power loss model is established to calculate the power loss in (4) and (5), referring to paper [33]. The switching characteristic of switching devices is assumed to be a linear process. Fig. 5 illustrates the switching process of a MOSFET and its body diode in a switching period. In Fig. 5, d represents the duty cycle corresponding to the on-state, while T_s and t_d represent

TABLE III
LOSS DISTRIBUTION BY USING THE PROPOSED HC-ALBC SCHEME WITHIN EVERY N SWITCHING PERIODS AT THE POSITIVE HALF PERIOD

	E_{sw}	E_{con}
S_1	$\sum_{i=n_{01}+2}^{N} E_{off}(i) + \sum_{i=n_{01}+1}^{N} E_{on}(i)$	$\sum_{i=1}^{N} E_{con\_P}(i)$
S_2	$\sum_{i=n_{01}+1}^{N} E_{rr}(i)$	$(1-k_{11})E'_{Dcon}(n_{01}+1) + \sum_{i=n_{01}+2}^{N} E'_{Dcon}(i)$
S_3	0	$\sum_{i=1}^{n_{01}} E_{con\_O}(i) + k_{11}E_{con\_O}(n_{01}+1) + (1-k_{11})E'_{con\_O}(n_{01}+1) + \sum_{i=n_{01}+2}^{N} E'_{con\_O}(i)$
S_4	0	0
S_5	$\sum_{i=1}^{n_{01}} E_{on}(i) + \sum_{i=1}^{n_{01}+1} E_{off}(i)$	$(1-k_{11})E'_{con\_O}(n_{01}+1) + \sum_{i=n_{01}+2}^{N} E'_{con\_O}(i) + \sum_{i=1}^{N} E_{con\_P}(i)$
S_6	0	$k_{11}(E_{con\_O}(n_{01}+1) + E_{Dcon}(n_{01}+1)) + (1-k_{11})(E'_{con\_O}(n_{01}+1) + E'_{Dcon}(n_{01}+1))$ $\sum_{i=1}^{n_{01}}(E_{con\_O}(i) + E_{Dcon}(i)) + \sum_{i=n_{01}+2}^{N}(E'_{con\_O}(i) + E'_{Dcon}(i))$

the switching period and the dead time. $t_{d(on)}$, t_r, $t_{d(off)}$, and t_f represent the turn-ON delay time, rise time, turn-OFF delay time, and fall time, respectively. t_{ra} and t_{rb} denote the reverse recovery time of the diode. I_L represents the inductor current, while U_F and U_D denote the body diode's forward voltage drop

$$E_{1total} = \sum_{i=1}^{0.5N_s} E_{con\_P}(i) + \sum_{j=1}^{\frac{0.5N_s}{N}} \left[\sum_{k=n_{01}+2}^{N} E_{off}(j,k) + \sum_{k=n_{01}+1}^{N} E_{on}(j,k) \right] + e_1(v) \tag{4}$$

and reverse voltage, respectively. U_{DS} denotes the drain–source voltage during the turn-OFF transition. In ON-state, the MOSFET is modeled as an equivalent ON-state resistance $R_{ds(on)}$, and U_{on} denotes the voltage drop across this resistance. I_{RR} denotes the reverse recovery current, which depends on the rate of current rise and the reverse recovery time. For 3L-ANPC inverters, U_{DS} equals to $0.5U_{dc}$. The parameters related to the switching characteristics of switching devices can be found in their datasheets.

Then, the turn-ON loss of the MOSFET during a single switching period can be calculated as follows:

$$E_{on} = \frac{1}{2}U_{DS}(I_L + I_{RR})(t_r + t_{ra}) + \frac{1}{2}U_{DS}I_L t_{rb} + \frac{1}{3}U_{DS}I_{RR}t_{rb}. \tag{6}$$

The turn-OFF loss of the MOSFET can be calculated as follows:

$$E_{off} = \frac{1}{2}U_{DS}I_L\left(t_{d(off)} + t_f\right). \tag{7}$$

The conduction loss of the MOSFET can be calculated as follows:

$$E_{con} = I_L^2 R_{ds(on)}\left(dT_s - t_{dead} - t_{d(on)} - t_r - t_{ra} - t_{rb}\right). \tag{8}$$

The conduction loss of the body diode can be calculated as follows:

$$E_{Dcon} = 2U_F I_L\left(t_{dead} - t_{d(ff)} - t_f + t_{d(on)}\right). \tag{9}$$

Since the power losses generated by S_2 and S_3 are symmetric at positive and negative half periods, the power loss between Si IGBTs is already balanced. Therefore, the power loss calculation of Si IGBT is not presented

$$\begin{cases} f(N, n_{01}, k_{11}) = |E_{5total} - E_{1total}| \\ 1 \leqslant N \leqslant 0.5N_s \; N \in Z \\ 0 \leqslant n_{01} \leqslant N-1 \; n_{01} \in Z \\ 0 \leqslant k_{11} \leqslant 1. \end{cases} \tag{10}$$

The loss balancing objective function $f(N, n_{01}, k_{11})$ is defined by (10). The $f(N, n_{01}, k_{11})$ represents the absolute total power loss difference between the inner and outer SiC MOSFETs. Based on the power loss model and operating conditions, the value of $f(N, n_{01}, k_{11})$ can be calculated under different N, n_{01}, and k_{11} values. Minimizing the $f(N, n_{01}, k_{11})$ determines the optimal ratio coefficients. Especially since the power loss distribution is different but symmetric at the positive and negative half period, the coefficient N is limited to be lower than $0.5N_s$. The flow chart and the calculation process of the optimal ratio coefficients by using the proposed HC-ALBC scheme is depicted in Fig. 6(a). First, reading the instantaneous value of the inductor current i_L, U_{dc}, and the modulation signal u_m. Then, search the optimal ratio coefficients with minimum $f(N, n_{01}, k_{11})$ by using an exhaustive method. Finally, (3) is used to enable different commutation processes in each switching cycle. Fig. 6(b) shows the system

$$E_{5total} = \sum_{i=1}^{0.5N_s} E_{con\_P}(i) + e_5(v) \sum_{j=1}^{\frac{0.5N_s}{N}} \begin{pmatrix} \sum_{k=1}^{n_{01}} (E_{on}(j,k) + E_{con\_O}(j,k) + E_{Dcon}(j,k)) \\ + \sum_{k=1}^{n_{01}+1} E_{off}(j,k) + \sum_{k=n_{01}+2}^{N} \left(2E'_{con\_O}(j,k) + E'_{Dcon}(j,k)\right) \\ + k_{11}\left(E_{con\_O}(j, k=n_{01}+1) + E_{Dcon}(j, k=n_{01}+1)\right) \\ + (1-k_{11})\left(2E'_{con\_O}(j, k=n_{01}+1) + E'_{Dcon}(j, k=n_{01}+1)\right) \end{pmatrix} \tag{5}$$

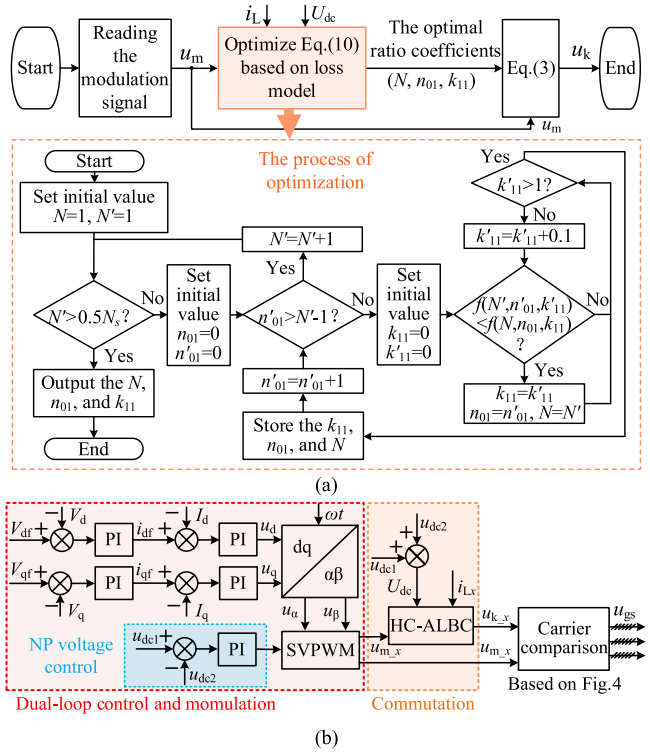


Fig. 6. Flowchart and the system control diagram under the proposed HC-ALBC scheme. (a) Flowchart of the proposed HC-ALBC scheme. (b) Overall system control diagram.

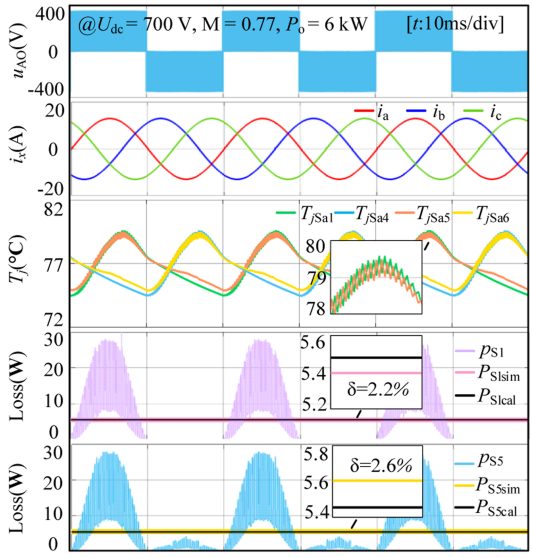


Fig. 7. Steady-state simulation waveforms of the proposed HC-ALBC scheme at the rated power.

TABLE IV
PARAMETERS OF THE 4SiC-III HYBRID 3L-ANPC INVERTER

Parameters	Value
Rated DC-link voltage (U_{dc})	700 V
Rated output voltage/ frequency	220 V/ 50 Hz
Rated modulation index	0.77
Rated output power	6000 W
Filter inductor (L_{fa}, L_{fb} and L_{fc})	622 μH
Filter capacitor (C_{fa}, C_{fb} and C_{fc})	4.7μF
SiC MOSFETS	IV1Q06060T3G
Si IGBTs	IKW30N60H3
Switching frequency	48 kHz

control diagram under the proposed HC-ALBC scheme. V_{df} and V_{qf} represent the d-axis and q-axis reference output voltages, while V_d and V_q represent the d-axis and q-axis components of three phase output voltage, respectively. Similarly, i_{df} and i_{qf} represent the d-axis and q-axis reference current, while I_d and I_q represent the d-axis and q-axis components of three phase inductor current, respectively. u_d and u_q are modulation signals in dq-coordinate and from the output of the dual-loop control. u_α and u_β represent modulation signals of α-axis and β-axis, respectively. u_{dc1} and u_{dc2} represent the upper and lower dc-link capacitor voltages, respectively. i_{Lx} represents the inductor current of phase x. From Fig. 6(b), the modulation signal of phase x u_{m_x} is calculated by the traditional seven-segment space vector pulsewidth modulation (SVPWM) based on the neutral point (NP) control and the dual-loop control. Then, based on the proposed HC-ALBC scheme shown in Fig. 6(a), the commutation modulation signal of phase x u_{k_x} is calculated. Finally, the driving voltages u_{gs} can be obtained through comparing u_{m_x} and u_{k_x} with the carrier signals (x = a, b, c).

C. Simulation Verification and Loss Distribution Comparison

A Simulink/PLECS cosimulation is also conducted to further verify the consistency between the calculated and actual losses under the proposed scheme, as shown in Fig. 7. The utilized specifications of the 4SiC-III hybrid 3L-ANPC inverter are shown in Table IV. u_{AO} represents the bridge leg voltage of phase A. i_x represents the output current of phase x (x = a, b, c). T_j represents the junction temperature of the SiC devices. p_{S1}, P_{S1sim}, and P_{S1cal} represent the instantaneous power loss within one switching period, the simulated average power loss and the calculated average power loss within one fundamental period of the outer SiC devices, respectively. Similarly, p_{S5}, P_{S5sim}, and P_{S5cal} represent the corresponding power losses for the inner SiC devices. As shown in Fig. 7, the calculated losses of the inner and outer switching devices are nearly the same as the simulated values, with the difference δ remaining below 3%.

To evaluate the impact of parameter differences caused by the parameter difference between devices, Fig. 8 presents the calculated power loss of each SiC MOSFET when the devices have different parameters. In operating condition 2, each SiC MOSFET is set with different ON-state resistances, and the loss balancing performance of the proposed scheme is only slightly degraded. Thus, the proposed HC-ALBC can still be utilized when the parameter is inconsistent between devices.

The calculated power losses and the simulated junction temperatures of the inner and outer SiC MOSFETs by using CM-I, CM-O, HC-ALBC, and the existing ATC scheme proposed in paper [32] are compared under different operating conditions, as shown in Fig. 9. Since the asymmetric commutation process can be considered as a combination of the CM-I and CM-O

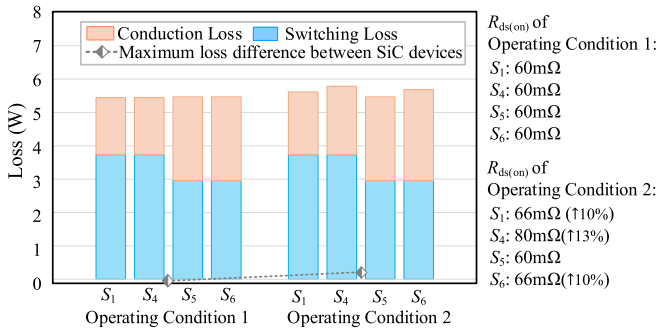


Fig. 8. Comparison of loss distribution when the devices have consistent and inconsistent performance.

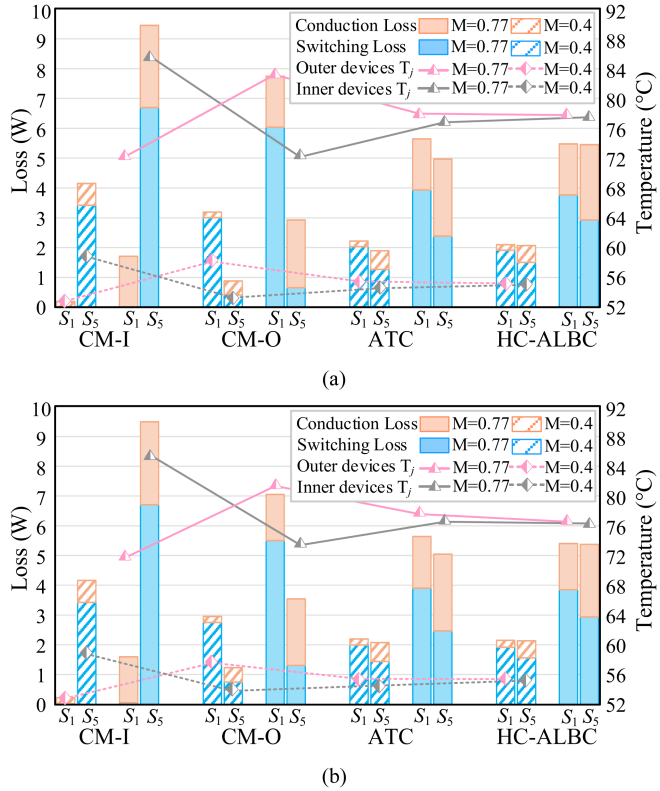


Fig. 9. Loss distribution and junction temperature comparison of different schemes under different modulation index (M) and power factor (PF) conditions. (a) PF = 1. (b) PF = 0.8.

schemes during a single switching period, the power loss by using the asymmetric commutation process is not compared with the proposed HC-ALBC scheme. It can be seen from Fig. 9 that, compared with the CM-I and CM-O schemes, the ATC scheme and the proposed HC-ALBC scheme significantly reduce the loss difference between the inner and outer switching devices. Besides, the power loss difference by using the proposed HC-ALBC scheme is much less than that of using the ATC scheme. Since the power loss between SiC MOSFETs is balanced by the proposed HC-ALBC scheme, the junction temperature difference between the inner and outer devices is also reduced to within 0.5 °C, resulting in a balanced thermal stress. Therefore,

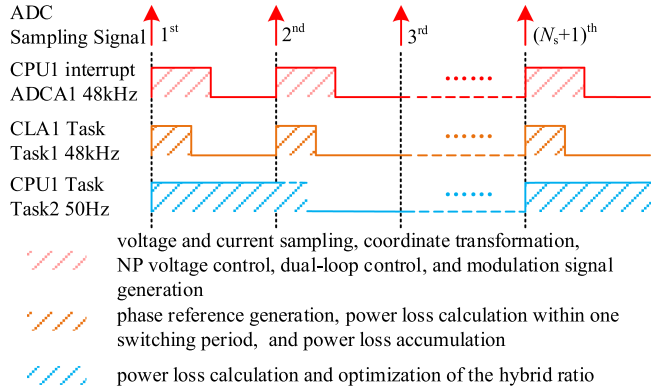


Fig. 10. Software implementation diagram of the proposed HC-ALBC scheme.

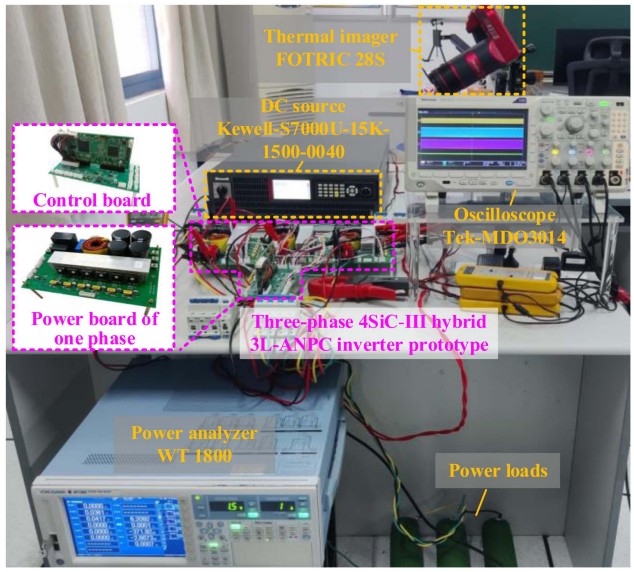


Fig. 11. Overall experimental setup and photograph of the three-phase 4SiC-III hybrid 3L-ANPC inverter prototype.

the proposed HC-ALBC scheme features the best loss-balancing performance compared to the other schemes under different operation conditions.

D. Software Implementation of the Proposed Scheme

Fig. 10 presents the software implementation of the proposed HC-ALBC scheme in a TMS320F28379D controller, which features dual-CPUs and dual control law accelerators (CLAs) architecture. The CPU1 interrupt and CLA1 task operate in parallel within one switching period to complete the voltage and current sampling, coordinate transformation, neutral-point voltage control, dual-loop control, and real-time loss calculation. Besides, a Task process with a period of 20 ms is set in CPU1 to optimize the hybrid ratio of different commutation processes in the next grid period. With these software design, although the proposed HC-ALBC scheme increases the complexity of the commutation program, it can still be executed efficiently in real-time.

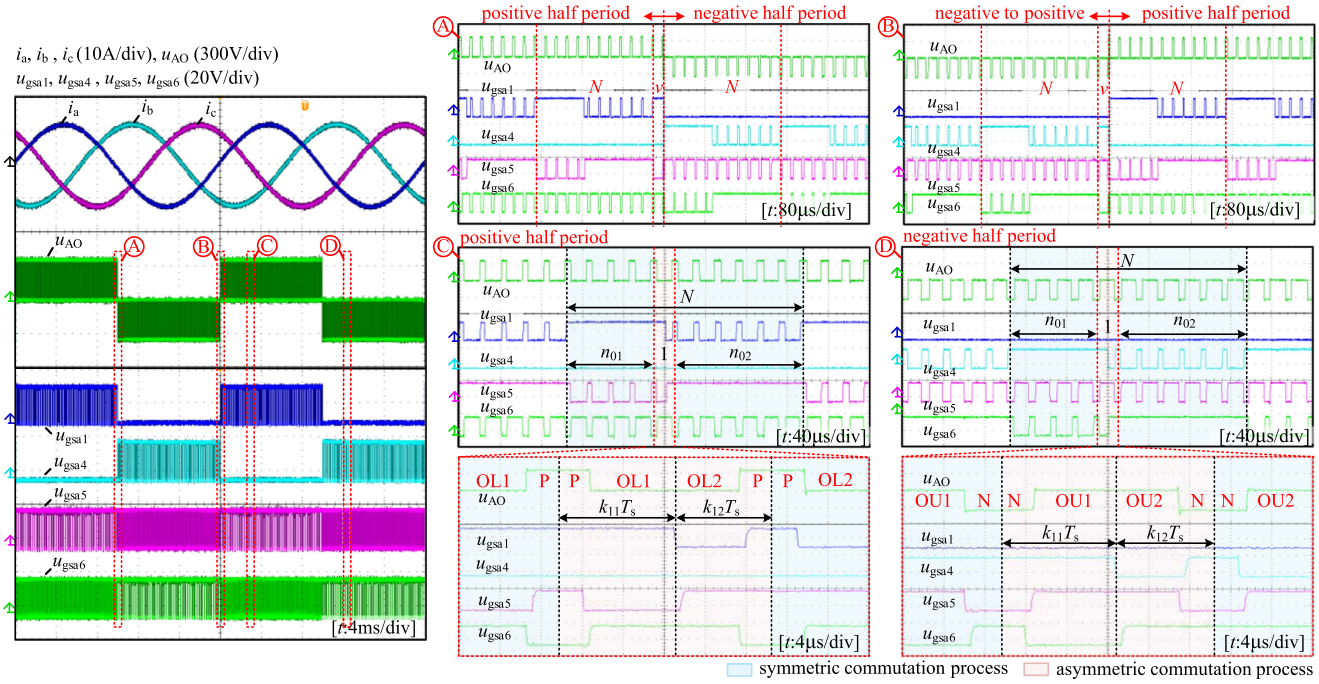


Fig. 12. Experimental steady-state waveforms of the proposed HC-ALBC scheme.

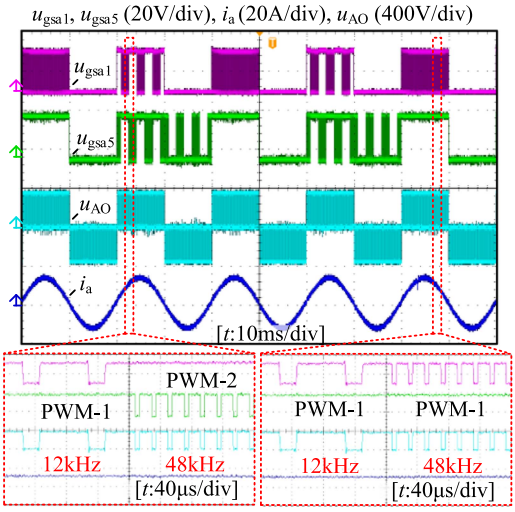


Fig. 13. Experimental steady-state waveforms by using the ATC scheme proposed in paper [32].

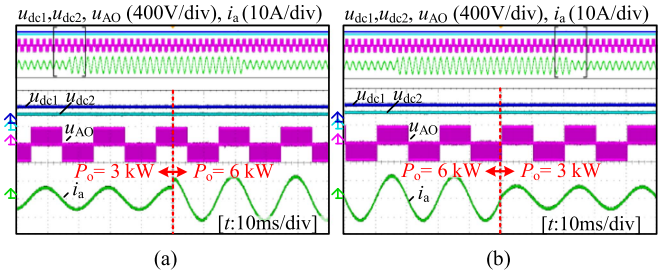


Fig. 14. Dynamic waveforms of the proposed HC-ALBC under different output power (P_o). (a) 3 to 6 kW. (b) 6 to 3 kW.

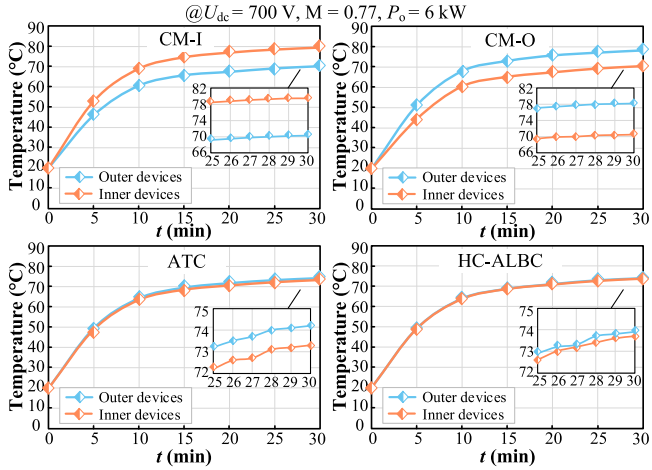
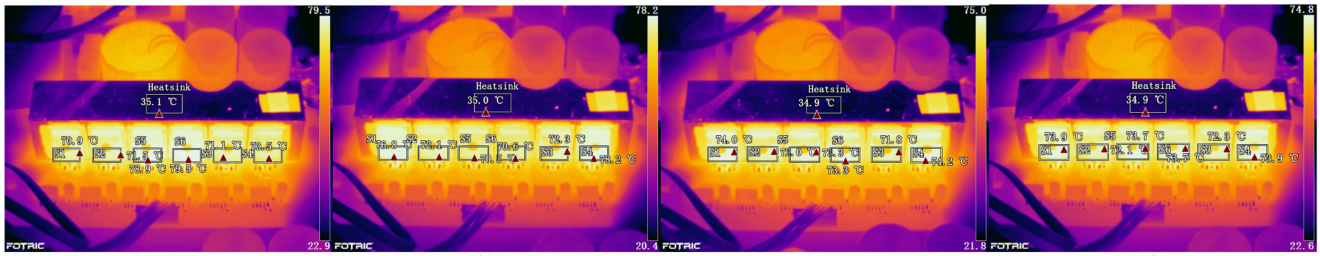


Fig. 15. Case temperature rising process of different schemes at rated output power when the modulation index is 0.77.

IV. Experimental Results

A three-phase 4SiC-III hybrid 3L-ANPC inverter prototype was built, and parameters are listed in Table IV. The prototype is controlled by a DSP TMS320F28379D and a field programmable gate array EF2L45GL144B. A Kewell dc source S7000U-15K-1500-0040 is used to power the prototype. All the waveforms are recorded by an oscilloscope (Tek-MDO3024). Both the THDs and efficiencies are measured by a YOKOGAWA power analyzer WT 1800. All the thermal images are captured using a thermal imaging camera FOTRIC 285 under natural air-cooling conditions and a consistent ambient temperature of



(a) (b) (c) (d)

Fig. 16. Thermal images of different schemes under rated output power when the modulation index is 0.77. (a) CM-I. (b) CM-O. (c) ATC. (d) HC-ALBC.

20 °C. Fig. 11 shows the overall experimental setup and photograph of the three-phase 4SiC-III hybrid 3L-ANPC inverter prototype. The SVPWM scheme is used in the experiment.

Fig. 12 shows the experimental steady-state waveforms of the proposed HC-ALBC scheme. $i_{\rm a}$, $i_{\rm b}$, $i_{\rm c}$, and $u_{\rm AO}$ represent the three-phase output current and the bridge-leg voltage of phase A, respectively. $u_{\rm gsa1}$, $u_{\rm gsa4}$, $u_{\rm gsa5}$, and $u_{\rm gsa6}$ represent driving voltages for S_1, S_4, S_5, and S_6 in phase A, respectively. In Fig. 12, it can be seen that there is no apparent alternating output current distortion by using the proposed HC-ALBC scheme, and three different commutation processes are hybrid utilized to achieve active balanced loss distribution. Within every N switching periods, the commutation process begins with the CM-I, which lasts for n_{01} switching periods. An asymmetric commutation process is utilized during the next switching period, when the commutation process is changed from the CM-I to CM-O. During this process, the OL1 state is enabled by turning off $S_{\rm a5}$. After k_{11} of the switching period, $S_{\rm a1}$ is turned off. After the dead time, $S_{\rm a5}$ is turned ON to enable the OL2 state. Within the next n_{02} switching periods, the CM-O scheme is employed. At the beginning of the positive and negative half periods, the commutation process of the proposed HC-ALBC scheme resets to the CM-I to ensure the symmetric loss distribution between the positive and negative half periods. It can be seen that the commutation process is consistent with that shown in Section III.

Experimental steady-state waveforms by using the ATC scheme are shown in Fig. 13. It can be seen that the ATC scheme balances the power loss by hybrid utilizing different switching frequencies and employing different modulation schemes for different switching frequencies. Fig. 14 shows the experimental dynamic waveforms of the proposed HC-ALBC. It can be seen that the NP voltage remains balanced with varying load conditions.

The measured case temperature curves of each switching device with rated operation conditions by using the CM-I, CM-O, HC-ALBC, and the existing ATC scheme proposed in paper [32] are shown in Fig. 15. The steady-state thermal image of different schemes is shown in Fig. 16. It can be seen that the maximum temperature difference between SiC devices ($\Delta T_{\rm SiC}$) by using the CM-I, CM-O, and the ATC scheme reaches 9.2, 7.7, and 0.9 °C, respectively. However, the $\Delta T_{\rm SiC}$ by using the HC-ALBC scheme is only 0.2 °C, resulting in a 97% reduction compared to the CM-I and CM-O schemes, and a 77% reduction compared to the existing ATC scheme. Thanks to the decrease of $\Delta T_{\rm SiC}$, the maximum device temperature ($T_{\rm max}$) can be reduced to 73.9 °C by using the HC-ALBC scheme, while the $T_{\rm max}$ under the CM-I, CM-O, and ATC schemes reaches 79.5, 78.2, and 74.2 °C, respectively. Therefore, the HC-ALBC scheme achieves the best loss-balancing performance compared to the other schemes. The maximum device junction temperature is also reduced. Figs. 17 and 18 present the steady-state thermal images with different modulation indices and output power. In Figs. 17 and 18, the HC-ALBC scheme also achieves the lowest $\Delta T_{\rm SiC}$ of 0.2 °C, with a reduction of 95% compared to the CM-I and CM-O schemes and a reduction of 66% compared to the existing ATC scheme. It is clear that the HC-ALBC scheme can effectively balance the power losses under different output power and modulation indices.

Fig. 19 shows the measured efficiencies of different schemes under different modulation indices. It can be seen that, compared to the CM-I scheme, the CM-O scheme has lower efficiency due to the additional reverse recovery losses of the Si devices [34]. Since the CM-I and CM-O schemes are hybrid utilized, the efficiency of the proposed HC-ALBC scheme is slightly lower than that of the CM-I and higher than that of the CM-O scheme. The proposed HC-ALBC scheme achieves maximum efficiency of 98.7% with $M = 0.77$, which is approximately 0.06% higher than the CM-O and only about 0.06% lower than CM-I. Since the ATC scheme employs a lower average switching frequency in some grid periods, it features the highest efficiency among these commutation processes. The maximum efficiency by using the proposed HC-ALBC also reaches 97.4%, which is only slightly lower than the maximum efficiency. When the modulation index is set at 0.4, the maximum efficiency by using the proposed HC-ALBC scheme is 97.4%, which is 0.13% higher than the CM-O scheme, and only 0.1% lower than the CM-I scheme. The efficiency of the ATC scheme remains the highest, approximately 0.13% higher than the proposed HC-ALBC scheme. Additionally, the efficiency of HC-ALBC achieves 98.6% under the rated condition. Therefore, high efficiency is also achieved by the proposed HC-ALBC scheme.

The measured output current THDs of different schemes under different output powers and modulation indices are compared in Fig. 20. It can be seen that the THD performance with the HC-ALBC scheme is similar to that of the CM-I and CM-O schemes. Although the ATC scheme improves efficiency by reducing the switching frequency at a high instantaneous current value, it also introduces more harmonics. Therefore, the

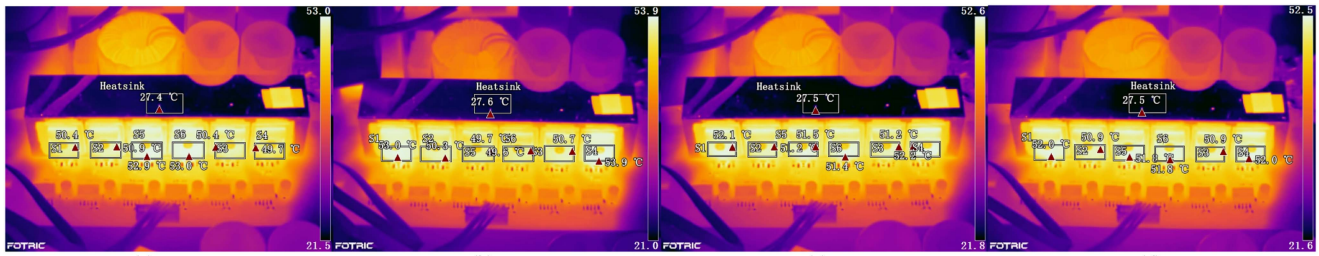


Fig. 17. Thermal images of different schemes under half of the rated output power with modulation index 0.77. (a) CM-I. (b) CM-O. (c) ATC. (d) HC-ALBC.

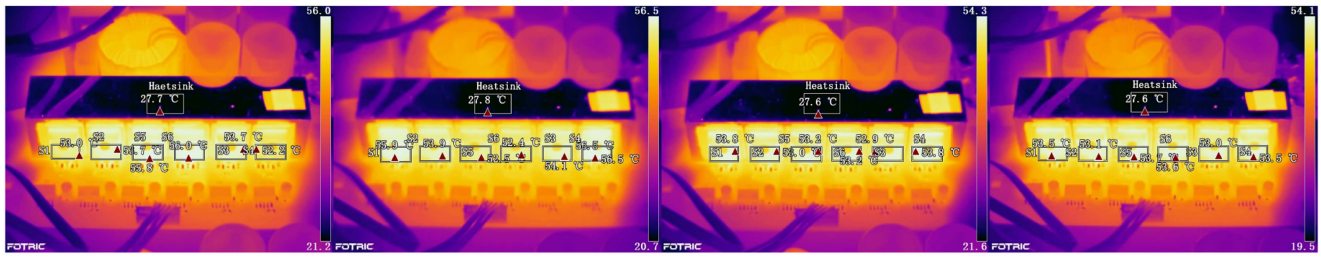


Fig. 18. Thermal images of different schemes under half of the rated output current with the modulation index 0.4. (a) CM-I. (b) CM-O. (c) ATC. (d) HC-ALBC.

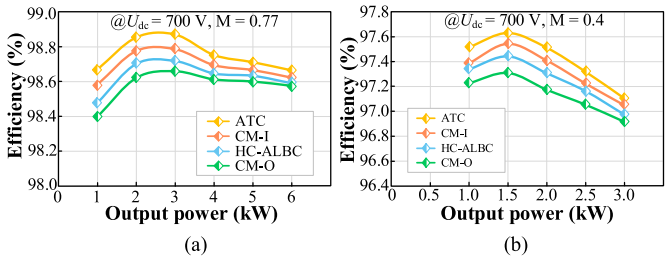


Fig. 19. Measured efficiencies of different schemes under different modulation indices. (a) $M = 0.77$. (b) $M = 0.4$.

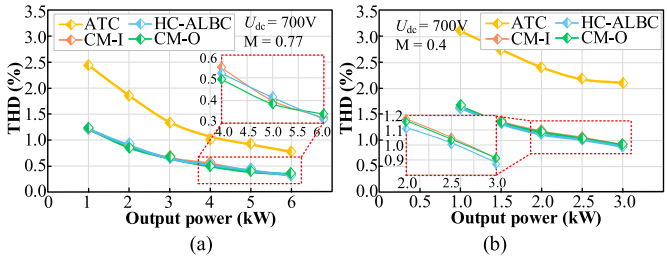


Fig. 20. Measured output current THDs of different schemes under different modulation indices. (a) $M = 0.77$. (b) $M = 0.4$.

proposed HC-ALBC scheme achieves actively balanced power loss while maintaining low current THDs compared with the ATC scheme.

It is also worth noting that although the simulation and experiment are based on a 6 kW inverter, the proposed HC-ALBC scheme can still effectively balance the power loss in different power levels by regulating the hybrid ratio of different commutation processes.

V. Conclusion

An HC-ALBC scheme for Si/SiC hybrid 3L-ANPC inverters is proposed. Commutation processes with different loss distribution characteristics are hybrid utilized with optimized usage ratios, which are actively controlled based on the real-time calculation of power losses. Analysis and experimental results highlight the following advantages:

1) The power loss distribution between SiC devices is effectively balanced under various operation conditions by using the proposed HC-ALBC scheme. Both the high efficiency and low harmonic performance are achieved as well.
2) Compared with the traditional CM-I and CM-O schemes, the proposed HC-ALBC scheme significantly balances the distribution of power losses. The maximum temperature difference between the SiC devices is reduced to 0.2 °C, with a reduction of over 95%. The maximum device temperature is also reduced by 7%.
3) Compared with the ATC scheme proposed in paper [32], the proposed HC-ALBC scheme also reduces the maximum temperature difference between the SiC devices by 77%. Besides, the proposed HC-ALCB scheme reduces the current THD by 50%, resulting in a smaller filter size and further improvement in power density.

Therefore, the proposed HC-ALBC scheme is an excellent commutation scheme for Si/SiC hybrid ANPC inverters, and can also be utilized by full-SiC high-power-density ANPC inverters.

Appendix

This Section presents the detailed calculations of $e_1(v)$ and $e_5(v)$ in (14). Depending on the value of v, $e_1(v)$ and $e_5(v)$ can

$$e_1(v)=\begin{cases}0, 0<v<n_{01}+1\\ E_{\text{on}}\left(\frac{0.5N_s}{N}+1, n_{01}+1\right), v=n_{01}+1\\ \sum_{k=n_{01}+2}^{v}\left(E_{\text{off}}\left(j=\frac{0.5N_s}{N}+1,k\right)+E_{\text{on}}\left(\frac{0.5N_s}{N}+1,k\right)\right)+e_1(n_{01}+1), v>n_{01}+1\end{cases} \tag{A1}$$

$$e_5(v)=\begin{cases}\sum_{k=1}^{v}\left[E_{\text{on}}\left(\frac{0.5N_s}{N}+1,k\right)+E_{\text{off}}\left(j=\frac{0.5N_s}{N}+1,k\right)+E_{\text{con\_}O}\left(\frac{0.5N_s}{N}+1,k\right)+E_{\text{Dcon}}\left(\frac{0.5N_s}{N}+1,k\right)\right], & 0<v<n_{01}1\\ +E_{\text{off}}\left(j=\frac{0.5N_s}{N}+1,n_{01}+1\right)+k_{11}[E_{\text{con\_}O}\left(j=\frac{0.5N_s}{N}+1,k=n_{01}+1\right) & \\ +E_{\text{Dcon}}\left(j=\frac{0.5N_s}{N}+1,k=n_{01}+1\right)]+(1-k_{11})\left[2E'_{\text{con\_}O}\left(j=\frac{0.5N_s}{N}+1,k=n_{01}+1\right), & v=n_{01}+1\\ +E'_{\text{Dcon}}\left(j=\frac{0.5N_s}{N}+1,k=n_{01}+1\right)\right]+e_5(n_{01}) & \\ \sum_{k=n_{01}+2}^{v}\left[2E'_{\text{con}_O}\left(j=\frac{0.5N_s}{N}+1,k\right)+E'_{\text{Dcon}}\left(j=\frac{0.5N_s}{N}+1,k\right)\right]+e_5(n_{01}+1) & v>n_{01}+1.\end{cases} \tag{A2}$$

be calculated by (A1) and (A2) shown at the top of this page, respectively.

REFERENCES

[1] J. Li, J. Liu, D. Boroyevich, P. Mattavelli, and Y. Xue, "Three-level active neutral-point-clamped zero-current-transition converter for sustain able energy systems," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3680–3693, Dec. 2011.

[2] L. Zhang, X. Yuan, X. Wu, C. Shi, J. Zhang, and Y. Zhang, "Performance evaluation of high-power SiC MOSFET modules in comparison to Si IGBT modules," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1181–1196, Feb. 2019.

[3] S. J. Bader et al., "Prospects for wide bandgap and ultrawide bandgap CMOS devices," *IEEE Trans. Electron Devices*, vol. 67, no. 10, pp. 4010–4020, Oct. 2020.

[4] D. Barater, C. Concari, G. Buticchi, E. Gurpinar, D. De, and A. Castella, "Performance evaluation of a three-level ANPC photovoltaic grid-connected inverter with 650-V SiC devices and optimized PWM," *IEEE Trans. Ind. Appl.*, vol. 52, no. 3, pp. 2475–2485, May/Jun. 2016.

[5] X. She et al., "High performance silicon carbide power block for industry applications," *IEEE Trans. Ind. Appl.*, vol. 53, no. 4, pp. 3738–3747, Jul./Aug. 2017.

[6] A. Anthon, Z. Zhang, M. A. E. Andersen, D. G. Holmes, B. McGrath, and C. A. Teixeira, "The benefits of SiC MOSFETs in a T-type inverter for grid-tie applications," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2808–2821, Apr. 2017.

[7] L. Zhang et al., "A Si/SiC hybrid five-level active NPC inverter with improved modulation scheme," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 4835–4846, May 2020.

[8] C. Li et al., "A SiC MOSFET and Si diode hybrid three-phase high-power three-level rectifier," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6076–6087, Jul. 2019.

[9] T. Yin, C. Xu, L. Lin, and K. Jing, "A SiC MOSFET and Si IGBT hybrid modular multilevel converter with specialized modulation scheme," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 12623–12628, Dec. 2020.

[10] D. Woldegiorgis, Y. Wu, Y. Wei, and H. A. Mantooth, "A high efficiency and low cost ANPC inverter using hybrid Si/SiC switches," *IEEE Open J. Ind. Appl.*, vol. 2, pp. 154–167, 2021.

[11] Q.-X. Guan et al., "An extremely high efficient three-level active neutral-point clamped converter comprising SiC and Si hybrid power stages," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8341–8352, Oct. 2018.

[12] S. Belkhode, A. Shukla, and S. Doolla, "Enhanced hybrid active-neutral-point-clamped converter with optimized loss distribution-based modulation scheme," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 3600–3612, Mar. 2021.

[13] D. Zhang, J. He, and D. Pan, "A megawatt-scale medium-voltage high efficiency high power density 'SiC+Si' hybrid three-level ANPC inverter for aircraft hybrid-electric propulsion systems," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 5971–5980, Nov./Dec. 2019.

[14] S. Belkhode, A. Shukla, and S. Doolla, "A highly efficient Si-/SiC-based hybrid active NPC converter with a novel modulation scheme," *IEEE Trans. Ind. Appl.*, vol. 58, no. 6, pp. 7445–7456, Nov./Dec. 2022.

[15] X. Lou, L. Zhang, Y. Chen, Z. Shen, and Z. Zheng, "A dedicate modulation scheme for 4-SiC 3L-ANPC inverter with loss balanced distribution and efficiency improvement," *Proc. CSEE*, vol. 42, no. 5, pp. 1925–1933, Mar. 2022.

[16] L. Zhang et al., "Evaluation of different Si/SiC hybrid three-level active NPC inverters for high power density," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8224–8236, Aug. 2020.

[17] M. Andresen, K. Ma, G. Buticchi, J. Falck, F. Blaabjerg, and M. Liserre, "Junction temperature control for more reliable power electronics," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 765–776, Jan. 2018.

[18] D. Andler, E. Hauk, R. Álvarez, J. Weber, S. Bernet, and J. Rodríguez, "New junction temperature balancing method for a three-level active NPC converter," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–9.

[19] X. Wang, H. Xiao, Y. Ren, and M. Cheng, "A novel modulation strategy for split-inductor active NPC inverter with loss distribution balancing and thermal stress reduction," *IEEE Trans. Power Electron.*, vol. 38, no. 6, pp. 7296–7307, Jun. 2023.

[20] A. Poorfakhraei, M. Narimani, and A. Emadi, "Improving power density of a three-level ANPC structure using the electro-thermal model of inverter and a modified SPWM technique," *IEEE Open J. Power Electron.*, vol. 3, pp. 741–754, 2022.

[21] J. Chen, Y. Pei, L. Wang, Y. Zhao, and S. Chen, "Loss equalization strategy of 3L active neutral point clamped inverter based on optimization algorithm," in *Proc. IEEE 10th Int. Power Electron. Motion Control Conf.*, 2024, pp. 3620–3625.

[22] A. Chanekar, N. Deshmukh, A. Gangwar, and S. Anand, "Thermal stress balancing for lifetime improvement of H6 solar inverter," in *Proc. 25th Eur. Conf. Power Electron. Appl.*, 2023, pp. 1–9.

[23] J. Ruthardt, J. Woelfle, M. Zehelein, and J. Roth-Stielow, "A new modulation technique to control the switching losses for single phase three-level active-neutral-point-clamped-inverters," in *Proc. PCIM Europe Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Manage.*, 2017, pp. 1–8.

[24] K. Ma and F. Blaabjerg, "Modulation methods for neutral-point clamped wind power converter achieving loss and thermal redistribution under low-voltage ride-through," *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 835–845, Feb. 2014.

[25] D. Floricau, E. Floricau, and M. Dumitrescu, "Natural doubling of the apparent switching frequency using three-level ANPC converter," in *Proc. 1st Int. Sch. Nonsinusoidal Curr. Compensation*, 2008, pp. 2375–1428.

[26] Y. Guo, X. Gao, J. Tan, P. Li, and H. Sun, "Research on loss balance modulation strategy based on single-phase half-bridge TL-ANPC inverter," in *Proc. 5th Int. Conf. Energy, Elect. Power Eng.*, 2022, pp. 375–382.

[27] G. Zhang, Y. Yang, F. Iannuzzo, K. Li, F. Blaabjerg, and H. Xu, "Loss distribution analysis of three-level active neutral-point-clamped (3L-ANPC) converter with different PWM strategies," in *Proc. IEEE 2nd Annu. Southern Power Electron. Conf.*, 2016, pp. 1–6.

[28] Y. Jiao and F. C. Lee, "New modulation scheme for three-level active neutral-point-clamped converter with loss and stress reduction," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5468–5479, Sep. 2015.

[29] Y. Deng, J. Li, K. H. Shin, T. Viitanen, M. Saeedifard, and R. G. Harley, "Improved modulation scheme for loss balancing of three-level active NPC converters," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2521–2532, Apr. 2017.

[30] L. Ma, T. Kerekes, P. Rodriguez, X. Jin, R. Teodorescu, and M. Liserre, "A new PWM strategy for grid-connected half-bridge active NPC converters with losses distribution balancing mechanism," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5331–5340, Sep. 2015.
[31] M. Novak, V. Ferreira, F. Blaabjerg, and M. Liserre, "Evaluation of carrier-based control strategies for balancing the thermal stress of a hybrid SiC ANPC converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2021, pp. 2077–2083.
[32] W. Song, W. He, Z. Zhang, C. Ma, and J. Li, "Active thermal control and power loss reduction scheme for three-level Active neutral-point-clamped inverters with hybrid modulation," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 2, pp. 1629–1640, Apr. 2024.
[33] L. Zhang, K. Sun, Y. Xing, and J. Zhao, "A family of five-level dual-buck full-bridge inverters for grid-tied applications," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7029–7042, Oct. 2016.
[34] X. Lou, G. Chen, L. Zhang, F. Zhao, and F. Wu, "An improved modulation scheme for 'Si&SiC' Hybrid 3L-active NPC rectifiers with low conduction losses," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2020, pp. 2004–2009.

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