# High-Efficiency Nonisolated Boost Converter Using *LC* Resonance for Quasi Soft Switching Operation in PV Applications

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***Abstract*—This article presents a high-efficiency nonisolated boost converter leveraging *LC* resonance for quasi soft switching operation. Conventional nonisolated dc/dc boost converters often suffer from efficiency degradation due to high switching operation during turn-ON and turn-OFF events. These losses necessitate bulky heat sinks, increasing the system's size and cost. To address these limitations, alternative solutions such as interleaved boost converters and coupled inductor designs with soft switching techniques have been proposed. However, these approaches often require multiple active and passive components, resulting in increased system complexity and reduced power density. The proposed converter employs a single SiC MOSFET to achieve cost reduction and design simplicity in a 10 kW power system, operating at a switching frequency of 100 kHz. By integrating an *LC* resonance design, the switching occurs at a specific point in the resonance waveform, enabling quasi soft switching and significantly reducing switching losses. Simulations and experimental results validate the proposed converter's performance, demonstrating a high efficiency of 99.0% at 10 kW output, compared to the conventional boost converters. Furthermore, the converter's integration into a dual-active-bridge and back-to-back system confirms its superior power density and efficiency compared to conventional methods.**

***Index Terms*—*LC* resonance, nonisolated boost converter high efficiency, photovoltaic (PV) dc/dc converter, quasi soft-switching, resonant converters, turn-OFF zero-voltage-switching (ZVS), turn-ON zero-current-switching (ZCS).**

## I. INTRODUCTION

THE excessive reliance on fossil fuels such as coal and oil has escalated environmental pollution and global warming, necessitating the development of sustainable energy solutions.

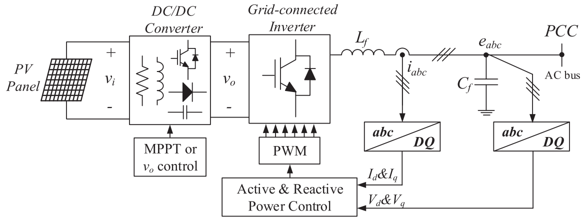

Fig. 1. Topology of converters and Inverters for PV applications.

In response, renewable energy sources such as solar, wind, and fuel cells have gained significant attention worldwide. A critical challenge in these systems is improving the efficiency of dc/dc converters, as their inefficiency can increase power generation costs by necessitating additional equipment to compensate for energy losses. Enhancing converter efficiency directly contributes to reducing the levelized cost of energy by maximizing power delivery from the same infrastructure.

In photovoltaic (PV) systems, dc/dc converters play a pivotal role in ensuring efficient power delivery to the grid, as illustrated in Fig. 1. These systems generally comprise three key components: the PV panel to harness renewable energy, the dc/dc converter to adjust the voltage level appropriately, and the grid-connected inverters to transfer renewable energy to the grid. Achieving high-efficiency power conversion in the dc/dc converter is particularly critical for optimizing the performance and cost-effectiveness of these systems.

Traditional nonisolated dc/dc boost converters [1], [2], [3], while offering simplicity and compactness, often suffer from significant switching losses and heat dissipation challenges, which limit their applicability in high-power systems. With the growing adoption of renewable energy sources, multiport converters integrating PV systems with energy storage systems (ESSs) and batteries have been proposed [4], [5], [6], [7], [8]. These configurations can include non-isolated three-port [4] or four-port [5] converters, as well as isolated multiport bidirectional converters [6], [7], [8]. While such multiport converters provide flexibility in combining PV with ESS, they tend to involve complex circuitry and require many active and passive components, leading to increased system cost and size.

To address the limitations of traditional boost converters, various converter topologies have been developed for PV applications [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21]. Interleaved boost converters [12], [13], [14], widely

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used for their scalability, reduce inductor size by increasing the effective switching frequency. Other notable designs include multilevel converters [15], buck-boost converters [16], flyback converters [17], [18], boost-SEPIC converters [19], and resonant converters [20], [21]. Furthermore, to achieve the high boost gain necessary for stepping up PV's low voltage to higher levels, advanced high-gain converter topologies have been proposed [22], [23], [24], [25]. These include coupled inductors, switched capacitor configurations, and quasi-resonance techniques. Despite their innovations, these designs often face challenges such as limited soft-switching ranges, increased device count, and inefficiencies under varying load and input conditions. As a result, parasitic ringing, electromagnetic interference (EMI), and lower power density become critical bottlenecks.

To mitigate these drawbacks, single-switch-based PV converters have emerged as promising solutions [26], [27], [28], [29], [30], [31], [32]. Various implementations, including active inductor-capacitor networks [26], [27], single-switched impedance networks [28], and switched capacitor-inductor networks [30], provide compact designs with reduced component count. However, these designs, while achieving high gain, may suffer from hard switching under load variations, leading to increased size and reduced efficiency due to excessive use of passive components.

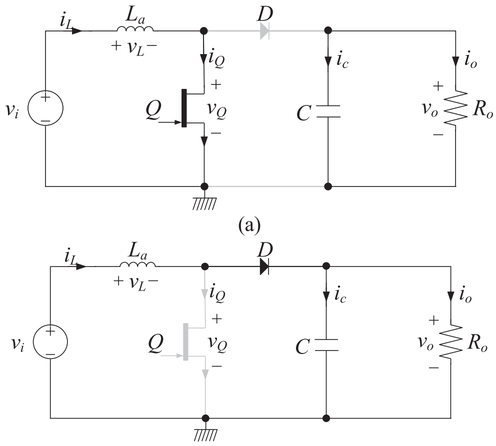
To overcome these challenges, this article proposes a novel non-isolated boost converter leveraging *LC* resonance to achieve quasi-soft switching. The proposed converter utilizes a single switching device, two inductors, two diodes, and two capacitors to create an *LC* quasi-resonant phenomenon. This enables soft switching for the switching device, ensuring high efficiency and cost-effectiveness in PV applications. The key features of the proposed converter are:

1) *Wide ZVZCS Range*: Zero-voltage turn-OFF and zero-current turn-ON soft-switching (ZVZCS) operation is ensured across a wide duty cycle range and varying input and output voltage conditions, offering superior performance compared to conventional boost converters. In this article, quasi resonant phenomena are utilized so that the ZVS turn-OFF operation is possible.
2) *Low Voltage Stress:* The voltage stresses of all components, except the output diode, are suppressed to levels dictated by the output voltage, regardless of operating conditions, enhancing reliability and efficiency.
3) *Minimal Component Usage*: The proposed converter employs only one active switch, along with two inductors, two capacitors, and three diodes. This reduces the overall cost and ensures a compact design for the PV converter.

By addressing the limitations of existing solutions and offering a high-efficiency, cost-effective alternative, the proposed converter represents a significant advancement in the design of dc/dc converters for PV applications. The detailed analysis, design, and experimental results are presented in the subsequent sections of this article.

## II. CIRCUIT ANALYSIS OF THE PROPOSED CONVERTERS

The conventional dc/dc boost converter, as depicted in Fig. 2, operates by turning the main active switch ON and OFF [1], [2], [3]. During the turn-ON phase, energy is stored in the inductor, while during the turn-OFF phase, the stored energy is transferred to the load. However, due to the large voltage and current stresses experienced by the switch at the moments of turn-ON and turn-OFF, hard-switching operation occurs. This results in significant switching losses and EMI, particularly in high-power applications. The hard-switching nature also increases thermal stress on components, thereby reducing overall system efficiency and reliability. In contrast, the proposed ZVZCS tapped boost converter, illustrated in Fig. 3, incorporates design features to mitigate these challenges. The converter comprises two inductors—a main inductor $L_a$ and an auxiliary inductor $L_b$ —an active switch $Q$, a snubber diode $D_1$, a snubber capacitor $C_s$, a recovery capacitor $C_r$, a clamp diode $D_3$, an output diode $D_2$, an output capacitor $C_o$, and an output resistor $R_o$. It is noted that the output resistor $R_o$ represents the effective resistance dictated by the operation of the grid-connected inverter in Fig. 1.



(a)
(b)

Fig. 2. Operation mechanism for conventional boost converters. (a) Turn-ON operation. (b) Turn-OFF operation.

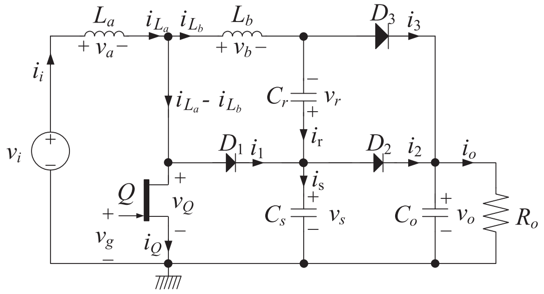


Fig. 3. Proposed resonant ZVZCS boost converters.

The proposed converter operates in the boundary conduction mode (BCM) for this analysis, as described in Fig. 4, which minimizes turn-ON losses due to ZCS. It is worth noting that the converter can also function in continuous conduction mode (CCM), as the time-domain analysis remains the same across these modes, although not described in this article. The analysis assumes negligible parasitic effects, such as line inductances, stray capacitances, and internal resistances, to simplify the discussion. Fast recovery diodes are employed, ensuring minimal switching and conduction losses as well as reduced reverse

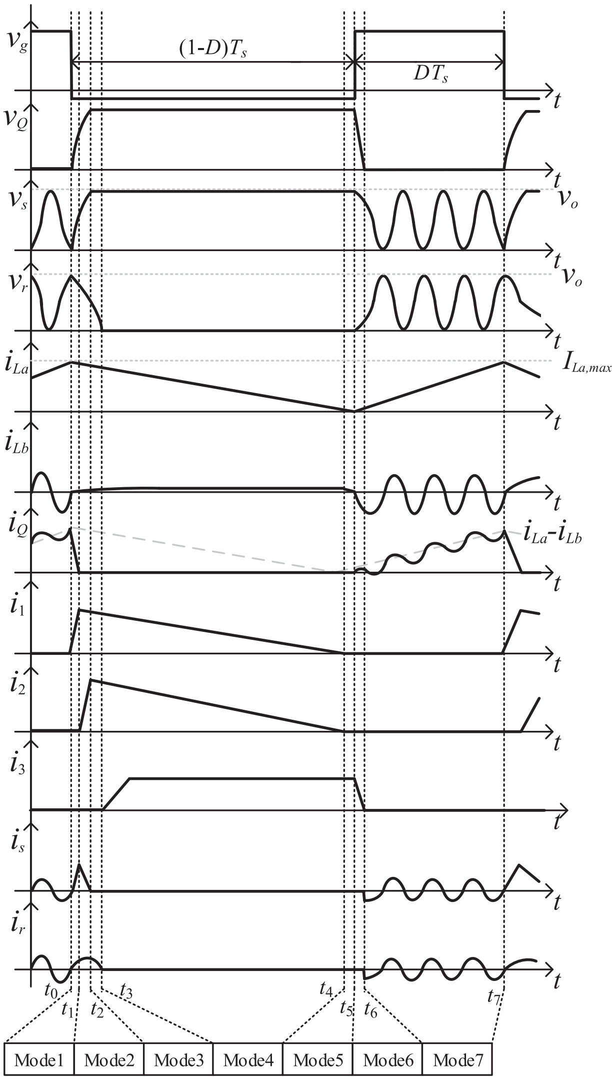


Fig. 4. Operating waveforms of proposed boost converters (BCM).

recovery times. The active switch is assumed to have finite turn-ON and turn-OFF times to calculate turn-ON and turn-OFF switching losses in this section. Furthermore, the input voltage $v_i$ and output voltage $v_o$ are treated as constant dc levels without ripple, given the large capacitance of $C_o$.

The operating modes of the proposed converter within one switching period $T_s$ are categorized into seven distinct phases, as shown in Fig. 5. During modes 1–5, the active switch is turned OFF, while during modes 6 and 7, it is turned ON.

The averaged static characteristics of the proposed converter in both BCM and CCM modes can be determined by the averaged duty cycle $D$, similar to a conventional boost converter [1], [2], [3]. The governing equation is expressed as follows:

$$G_V = \frac{V_o}{V_i} = \frac{1}{1-D}. \tag{1}$$

From now on, a detailed circuit analysis for each mode will be made, where the mode starts with the turning-OFF process.

*Mode 1* ($t_0 < t \leq t_1$): Mode 1 begins at the moment $t_0$ when the switching device $Q$ is turned OFF, as depicted in Fig. 5(a). At this stage, the switch current $i_Q$ starts to decrease sharply. This mode is crucial for reducing the turn-OFF losses of the switch. During Mode 1, the main inductor current $I_{La}$ begins to discharge from its peak value and gradually decreases.

In this mode, the snubber circuit, consisting of the diode $D_1$ and snubber capacitor $C_s$, becomes active. Diode $D_1$ conducts, ensuring that the switch voltage $v_Q$ is equal to the snubber capacitor voltage $v_s$. The snubber capacitor slowly charges, reducing the rate of voltage rise across the switch $dv_Q/dt$ and enabling ZVS during turn-OFF, as illustrated in Fig. 6(a). The voltage across the snubber capacitor $v_s$ during this mode is as follows:

$$C_s \frac{dv_s(t)}{dt} = i_s(t) \approx i_{La}(t)$$

$$\to v_s(t) = v_Q(t) = \frac{1}{C_s}\int_{t_0}^{t} i_s(t)dt \approx \frac{1}{C_s}\left(i_{La}(t) - i_{La}(t_0)\right). \tag{2}$$

Since $t_0$ marks the beginning of the switch turn-OFF, analyzing the turn-OFF switching losses $P_{\text{sw,off}}$ is critical. These losses are determined by the overlap between the switch voltage $v_Q$ and current $i_Q$ during turn-OFF and can be expressed as

$$P_{\text{sw,off}} = f_s \int_{t_0}^{t_1} \left(v_Q(t) \cdot i_Q(t)\right) dt \tag{3a}$$

$$\because i_Q(t_0) = i_{La}(t_0) - i_{Lb}(t_0) \approx i_{La}(t_0) = I_{La,\max}. \tag{3b}$$

For mode 1, the current $i_Q(t_0)$ can be approximated as the peak current of the main inductor $L_a$, as the auxiliary inductor $L_b$ current is nearly zero during this mode. Consequently, the turn-OFF switching losses can be calculated using (3).

Increasing the capacitance of $C_s$ slows the rate of voltage rise $dv_Q/dt$, thereby effectively reducing turn-OFF losses, as described in (2) and (3). However, excessively large $C_s$ decreases the *LC* resonance frequency $f_r$ during turn-ON, which limits the duty cycle resolution. This topic will be further elaborated in the next subsection. Therefore, selecting an optimal $C_s$ value is crucial to balancing duty cycle resolution and switching loss, as these two criteria are in a tradeoff relationship. Mode 1 concludes when the switch current $i_Q$ reaches zero. The duration of this mode is influenced by the $di_Q/dt$ characteristics of the switch current, which depend on the properties of the semiconductor switch.

*Mode 2* ($t_1 < t \leq t_2$): Mode 2 in Fig. 5(b) continues from the point where the snubber capacitor voltage $v_s$ equals the output voltage $V_o$ and lasts until the snubber capacitor current $i_s$ reaches 0 A. During this mode, the inductor current and the recovery capacitor discharge current simultaneously supply power to the load while charging the snubber capacitor. In this mode, the circuit dynamics can be analyzed using Kirchhoff's current law at the node shared by the snubber and recovery capacitors, leading to the following relationship:

$$i_{La}(t) = i_{Lb}(t) + i_1(t) = i_s(t) + i_o(t). \tag{4}$$

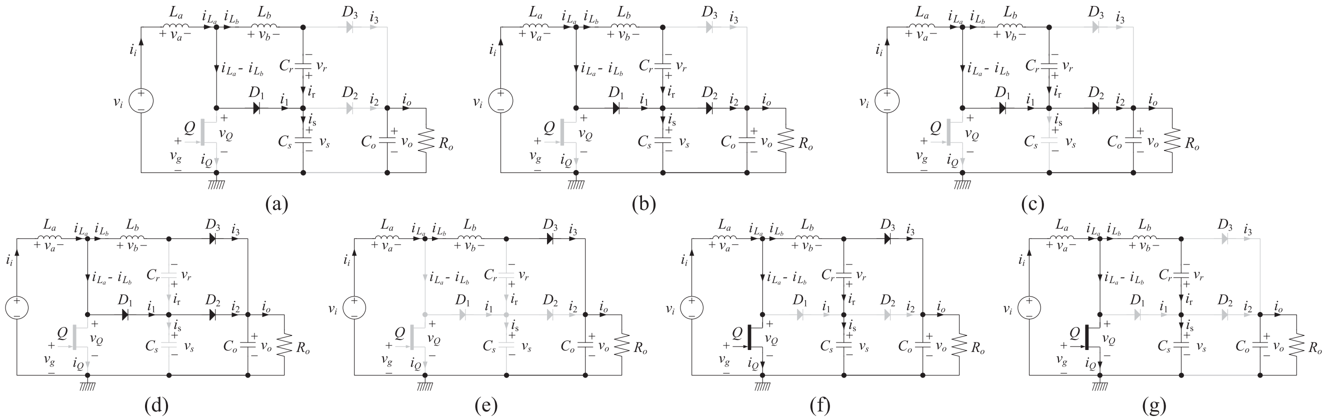


Fig. 5. Operating modes of the proposed converter. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7.

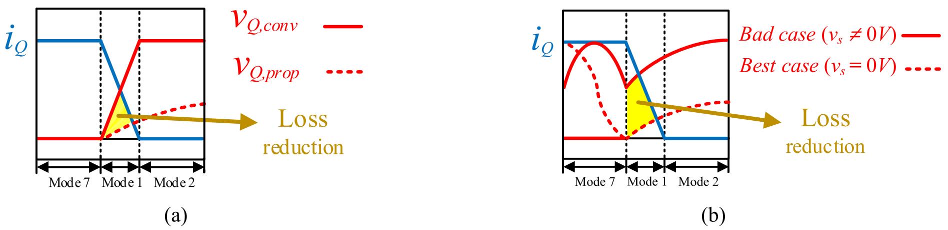


Fig. 6. Turn OFF ZVS operation for Quasi soft switching of the proposed converter in Mode 1. (a) Conventional versus Proposed approach. (b) Bad case versus Best case.

Assuming that Mode 1 is relatively short, mo2de 2's interval can be approximated as $t_{20} \approx t_{21} = t_2$ - $t_1$. This highlights the point at which the snubber capacitor voltage aligns with the output voltage, completing the charging phase. Thus, the duration of this mode $t_{21}$ can be determined by finding the time at which the snubber capacitor voltage equals the output voltage, as follows:

$$\therefore t_{21} = \frac{C_s}{i_Q(t_0)}\left(v_s(t_2) - v_s(t_1)\right) \approx \frac{C_s V_o}{I_{La,\max}}. \tag{5}$$

*Mode 3* ($t_2 < t \leq t_3$): Mode 3 in Fig. 5(c) begins at $t_2$, the point where the charging of $C_s$ is complete, resulting in $i_s(t) = 0$ A. This mode continues until $C_r$ is fully discharged, with the recovery capacitor current $i_r$ reaching 0 A and the recovery capacitor voltage $v_r$ becoming 0 V. The voltage-current relationship of the recovery capacitor during this mode is expressed as follows:

$$C_r\frac{v_r(t_3) - v_r(t_2)}{t_3 - t_2} = i_r(t_3) - i_r(t_2) \rightarrow i_r(t_2) = C_r\frac{V_o}{t_{32}}, \tag{6a}$$

$$\because v_r(t_3) \approx 0, i_r(t_3) \approx 0, v_r(t_2) \approx V_o. \tag{6b}$$

Based on these conditions of (6), the relationship between $i_r(t_2)$ and $t_{32}$ can be derived. To determine the values of these two parameters, i.e., $i_r(t_2)$ and $t_{32}$, an additional equation is required.

During this mode, the auxiliary inductor $L_b$ and the recovery capacitor $C_r$ form a series connection. This $L_b$-$C_r$ network is short-circuited through diode $D_1$, resulting in the following relationship:

$$v_r(t_3) - v_r(t_2) - L_b\frac{i_r(t_3) - i_r(t_2)}{t_{32}} = 0 \rightarrow V_o = L_b\frac{i_r(t_2)}{t_{32}}. \tag{7}$$

Using the two equations presented in (6a) and (7), the duration of this mode, $t_{32}$, and the recovery current $i_r$ can be determined, as expressed in the following equations:

$$\therefore t_{32} = \sqrt{L_b C_r}, i_r(t_2) = V_o\sqrt{\frac{C_r}{L_b}}. \tag{8}$$

From (8), the duration of this mode is determined by the resonant period of the auxiliary inductor $L_b$ and the recovery capacitor $C_r$.

*Mode 4* ($t_3 < t \leq t_4$): Mode 4 in Fig. 5(d) begins at $t_3$, the point where the discharge of $C_r$ is completed. In this mode, only the inductors $L_a$ and $L_b$ are responsible for power transfer. This mode continues while $i_{La}(t) > i_{Lb}(t)$, and ends when $i_{La}(t_4) = i_{Lb}(t_4)$. By considering these characteristics and utilizing the equation for inductor $L_a$, the duration $t_{43}$ can be derived as follows:

$$L_a\frac{i_{La}(t_4) - i_{La}(t_3)}{t_{43}} \approx V_i - V_o \rightarrow \therefore t_{43} \approx \frac{I_o}{V_o - V_i}. \tag{9}$$

*Mode 5* ($t_4 < t \leq t_5$): In this mode, the currents flowing through the main inductor $L_a$ and the auxiliary inductor $L_b$ are identical, i.e., $I_{La}(t) = I_{Lb}(t)$. This mode continues until just before the switch is turned ON and operates in the same manner as the turn-OFF phase of a conventional boost converter. At the end of mode 4, denoted as $t_4$, $i_{La}$ and $i_{Lb}$ become equal, and the current state persists until the switch turns ON.

(a) (b)

Fig. 7. Turn ON ZCS operation for Quasi soft switching of the proposed converter in Mode 6. (a) Conventional versus Proposed approach. (b) BCM case versus CCM case.

*Mode 6* ($t_5 < t \leq t_6$): Mode 6 in Fig. 5(f) begins at $t_5$, the moment the switch turns ON, and ends at $t_6$, when the conduction of diode $D_3$ is completed. During this interval, the circuit enables turn-ON ZCS soft switching, unlike a conventional boost converter. This is achieved because, when the switch turns on, the switch current flows from the inductor current. The principle behind this operation is illustrated in Fig. 7(a). The low $di_Q/dt$ characteristic of the current induced by the main inductor $L_a$ reduces the current slope during turn-ON, enabling ZCS operation. It is noteworthy that when the proposed converter operates in CCM, the switch current $i_Q$ ($=i_{La}$) includes a positive offset current component at the moment of turn-ON, which tends to increase ZCS turn-ON losses. Therefore, operating in BCM is most advantageous for achieving ZCS turn-ON, as illustrated in Fig. 7(b).

Additionally, the termination of mode 6 at $t_6$ can be adjusted by the value of $L_b$. The duration of this mode, which corresponds to the conduction time of $D_3$, is determined by the rate of decrease in $i_{Lb}$, which depends on $i_{Lb}$(t5) and $L_b$. The current decrease of $i_{Lb}$ after $t_5$ is described, as follows:

$$i_{Lb}(t) = i_{Lb}(t_5) + \frac{v_{Lb}(t)}{L_b}(t - t_5) \approx i_{Lb}(t_5) - \frac{V_o}{L_b}(t - t_5). \tag{10}$$

The time $t_6$ corresponds to the point where $i_{Lb}(t_6) = 0$ A. Using this, the time interval of mode 6 $t_{65}$ can be calculated as follows:

$$\therefore t_{65} \approx L_b \frac{i_{Lb}(t_5)}{V_o}. \tag{11}$$

In (10) and (11), the analysis of turn-ON switching losses during mode 6 can be calculated as follows:

$$P_{sw,on} = f_s \int_{t_5}^{t_6} v_Q(t) \cdot i_Q(t) dt = f_s \int_{t_5}^{t_6} \left( V_i - L_a \frac{di_{La}(t)}{dt} \right) \cdot i_Q(t) dt \approx f_s V_i \int_{t_5}^{t_6} i_Q(t) dt \tag{12a}$$

$$\because i_Q(t) = \frac{1}{L_a} \int_{t_5}^{t} v_{La}(t) dt - \frac{1}{L_b} \int_{t_5}^{t} v_{Lb}(t) dt. \tag{12b}$$

From (12), increasing the inductance of $L_a$ and decreasing the inductance of $L_b$ can effectively reduce turn-ON switching losses, enabling high-efficiency power conversion.

*Mode 7* ($t_6 < t \leq t_7$): This mode in Fig. 5(g) represents the interval between the end of $D_3$'s conduction and just before the switch turns OFF. During this period, the current flowing through the switch exhibits resonance within the *LC* network, which consists of $L_b$, $C_r$, and $C_s$. The resonant frequency of this *LC* network is given by the following equation:

$$f_r = \frac{1}{2\pi \sqrt{L_b \left( \frac{C_s C_r}{C_s + C_r} \right)}}. \tag{13}$$

As described in (13), sinusoidal resonance occurs at this resonant frequency. It is more favorable to turn ON the switch when $v_Q$, the voltage across the switch, aligns with the same potential as $v_s$, resulting in $v_s = 0$ [V]. This condition, illustrated in Fig. 6(b), better satisfies the requirements for ZVS operation of the switch. If the switch is turned ON under the condition $v_Q$(t) $> 0$, switching losses will occur proportional to the magnitude of $v_Q$(t). Ideally, switching under the condition $v_Q(t) = 0$ minimizes turn-ON switching losses, as this represents the optimal condition for reducing turn-OFF switching loss.

As explained in (2) and (3) in mode 1, increasing $C_s$ improves turn-ON ZVS losses. However, as identified from (13), an increase in $C_s$ reduces the resonant frequency, which lengthens the period during which $v_Q = 0$. In such cases, the duty resolution performance of this converter, which requires turn-ON switching at $v_Q = 0$, is degraded. Therefore, an appropriate $C_s$ value must be selected by considering the tradeoff relationship between duty resolution and turn-ON ZVS losses.

## III. DESIGN OF THE PROPOSED CONVERTERS

### A. *Optimal Duty Selection Strategy*

In this section, as discussed in the previous sections, the objective is to optimize the values of $L_b$, $C_s$, and $C_r$ for the proposed boost converter to stabilize thermal characteristics by minimizing switching losses. Specifically, the losses occurring during the turn-ON and turn-OFF of the switching devices significantly affect the efficiency of the converter, making the optimal selection of inductance and capacitance values used in the proposed converter essential for effective management.

In the previous section, it was demonstrated that the ZVS operation is achieved by turning OFF the switch when $v_s = 0$ V during the sinusoidal resonant waveform in mode 7, as described in detail in Fig. 8. Turn-OFF switching when $v_s$ is not zero fails to achieve the desired level of loss reduction. Consequently, a higher frequency of the sinusoidal waveform in mode 7 allows for more instances where $v_s = 0$ V, providing an advantage in duty cycle variability and improving resolution. While selecting lower values of $L_b$, $C_s$, and $C_r$ is advantageous for increasing the

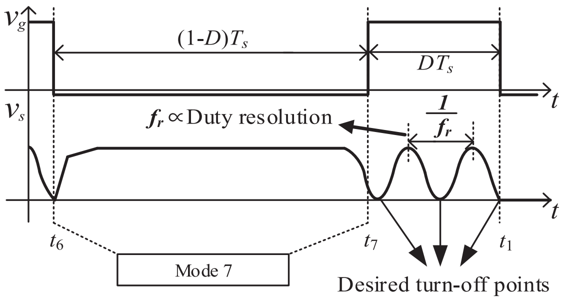


Fig. 8. Detailed operating waveforms of the proposed converter during turn-OFF ZVS operation.

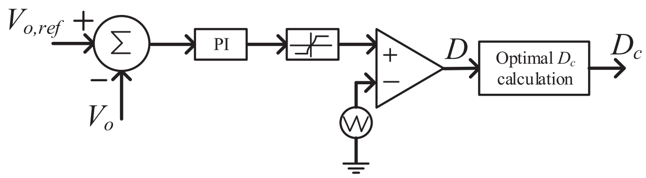


Fig. 9. Proposed voltage regulation controller.

TABLE I
DUTY OPERATING POINT $D_c$, ACHIEVING TURN-OFF ZVS AS $D$ VARIES

| $D$ range | Selected $D_c$ |
|---|---|
| $0.215 < D \leq 0.305$ | 0.26 |
| $0.305 < D \leq 0.395$ | 0.35 |
| $0.395 < D \leq 0.485$ | 0.44 |
| $0.485 < D \leq 0.575$ | 0.53 |
| $0.575 < D \leq 0.665$ | 0.62 |
| $0.665 < D \leq 0.755$ | 0.71 |
| $0.755 < D \leq 0.845$ | 0.80 |

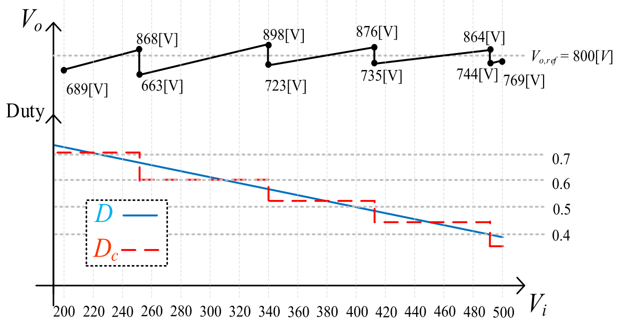


Fig. 10. Design results of $D$ and $D_c$ for $V_o \approx V_{o,\text{ref}}$.

frequency of the resonant waveform, as identified from (2)–(3), (13), it forms a tradeoff with the reduction in switching losses proportional to the increase in the values of $L_b$ and $C_s$.

In this article, the switching duty cycle is maintained below 0.1, enabling high-resolution voltage conversion in units of $0.1 \times N$ (where $N$ is an integer). For a switching frequency of 100 kHz, this implies that the turn-ON *LC* resonant frequency $f_r$ must exceed 1 MHz, although this value may vary depending on the operating frequency and the designer's objectives. To achieve the goal of this article, i.e., $V_i = 200 \sim 500$ V and $V_o \approx$ 800 V for 10 kW power delivery in Fig. 3, the proposed converter must satisfy these requirements while ensuring soft switching operations during both turn-ON and turn-OFF. The duty $D$ satisfying $v_s = 0$V assumes efficient switching operations at 0.089 cycles, based on the turn-ON *LC* resonant frequency of $f_r = 1.12$ MHz designed in the following chapter. The boost converter was evaluated under conditions where the input voltage increases linearly from 200 to 500 V, simulating a scenario in PV systems where shadows gradually clear. These input voltage variations demonstrate the broad applicability of the proposed converter to diverse input voltage fluctuations. When the grid-connected inverter system, as shown in Fig. 1, is connected to a three-phase 380 V grid, the output voltage of the proposed converter, which is also the input voltage of the grid-connected inverter, is tried to be maintained at $V_o = 800$ V. For this function, a feedback control method, as shown in Fig. 9, was adopted to regulate $D$, ensuring this output. However, the proposed boost converter must operate with an appropriate $D_c$ value, satisfying specific high-efficiency operating conditions within the input voltage range. To do this one, optimal dc calculation in Fig. 9 is required and these values are specified in Table I. The output voltage implemented through the proposed control method exhibits an average variation of approximately ±10% around 800 V, as shown in Fig. 10. This level of variation may be acceptable if the grid-connected inverters in Fig. 1 operate with a sufficient modulation index; a range of approximately 30% –60% is feasible under a 220 V/60 Hz grid condition. Furthermore, boost converters inherently provide robust small-signal stability against variations in input parameters, and such variations are generally minimal due to gradual weather changes [36]. Therefore, the observed voltage variation at the output of the boost converters—and consequently at the input of the grid-connected inverter—is considered acceptable.

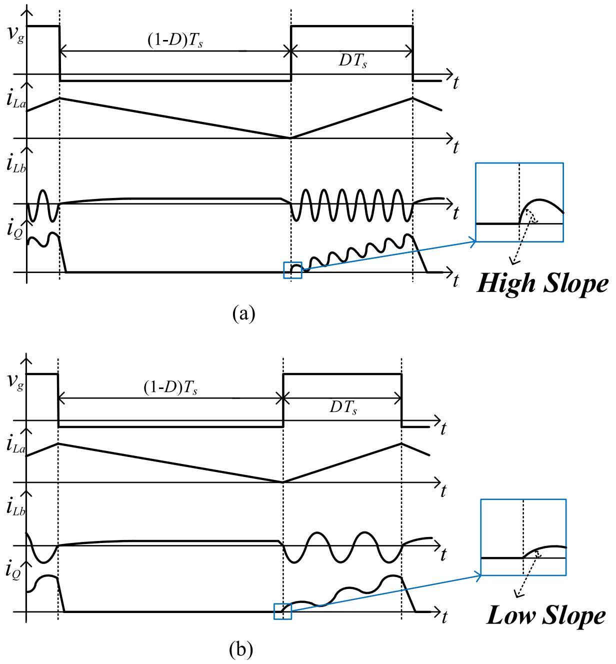
## B. *Optimal Parameter Selection*

To operate appropriate duty $D_c$ with turn-ON ZCS and turn-OFF ZVS operations, according to the characteristics presented in Fig. 10, optimal selection of passive component parameters is required. The parameters $L_b$, $C_s$, and $C_r$ used in this article should be determined, considering the tradeoff between the following two perspectives:

1) *Resonant Frequency* $f_r$: Higher $f_r$ provides higher duty switching resolution.
2) *Switching Loss* ($P_{\text{sw,on}}$ *&* $P_{\text{sw,off}}$): Higher $f_r$ results in higher switching losses.

In essence, duty resolution and switching loss exhibit a tradeoff relationship.

As $L_b$ decreases, $f_r$ increases, as identified from (13). However, the rising slope of the sinusoidal waveform also decreases, reducing the turn-ON ZCS effect and thereby increasing switching losses, as detailed in Fig. 11. It can be observed that the resonant waveform frequency during turn-ON and the current slope of the switch during turn-ON are both affected by the value of $L_b$. Conversely, as $C_s$ increases, the capacitor charges more slowly, favoring turn-OFF ZVS operation. However, $f_r$ in (13) decreases, reducing duty switching resolution.



(a)

(b)

Fig. 11. Comparison of two different cases of $L_b$. (a) Low $L_b$ case. (b) High $L_b$ case.

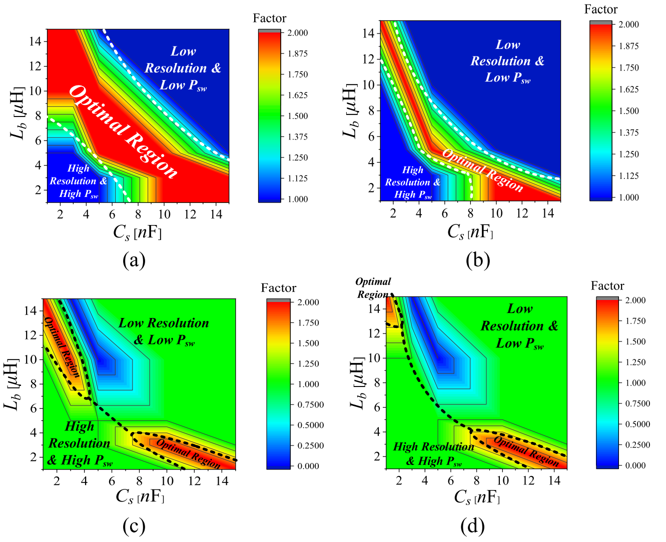
TABLE II
MAJOR CHARACTERISTICS OF THE PROPOSED CONVERTERS

| Classification | Resonant frequency $f_r$ | Switching loss $P_{sw,Q}$ |
|---|---|---|
| High $L_b$ and $C_s$ | Low (Bad) | Low (Good) |
| Low $L_b$ and $C_s$ | High (Good) | High (Bad) |

Ultimately, Table II highlights the tradeoff between resonant frequency $f_r$ and switching loss $P_{\mathrm{sw},Q}$ [$= P_{\mathrm{sw,on}}$ in (12) + $P_{\mathrm{sw,off}}$ in (3)]. In this article, the region, satisfying the following two criteria, is identified and presented in Fig. 12 as a 2D graph.

1) $f_r > 1$ MHz, considering the operating frequency of 100 kHz.
2) $P_{sw,Q} < 20$ W, considering the loss characteristics of applied SiC switch device.

As shown in Fig. 12, the region satisfying the tradeoff point varies depending on the ratio of $C_r$ to $C_s$, denoted as $\alpha_c$. The results indicate that as $\alpha_c$ approaches 1.0, the region satisfying both criteria expands. It is noteworthy that when $\alpha_c < 1.0$, the recovery capacitor becomes smaller than the snubber capacitance. This can cause malfunctions in the proposed mechanism, which relies on storing energy in the snubber capacitor and transferring it to the load. Thus, this condition is not considered in this article. The loss characteristics as a function of $\alpha_c$ are shown in Fig. 13. As $\alpha_c$ increases, turn-OFF switching losses increase. Considering the wider region in Fig. 12, it is determined that $\alpha_c = 1.0$ is the most suitable. Consequently, the optimal parameters, satisfying the criteria presented in this article, are determined to be $L_b = 3.0$ $\mu$H, $C_s = 16.0$ $n$F, and $C_r = 16.0$ $n$F in Fig. 3, achieving $P_{\mathrm{sw},Q} = P_{\mathrm{sw,on}} + P_{\mathrm{sw,off}} < 20$ W and $f_r > 1.0$ MHz under $f_s = 100$ kHz.



(a)

(b)

(c)

(d)

Fig. 12. 2D-plot results for optimized parameter selection. (a) $\alpha_c = 1.0$. (b) $\alpha_c = 2.0$. (c) $\alpha_c = 3.0$. (d) $\alpha_c = 4.0$.

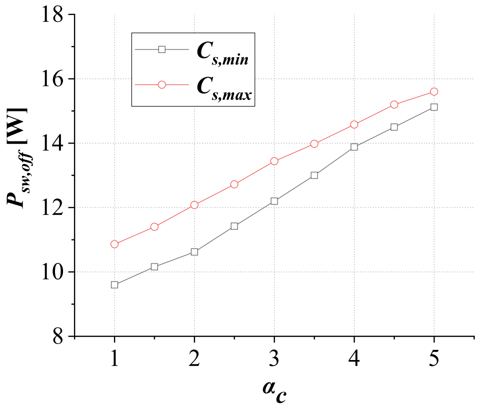


Fig. 13. Turn-OFF switching loss characteristics w.r.t. $\alpha_c$ (=$C_r$/$C_s$).

The inductors $L_a$ and $L_b$ applied in this article were designed considering the required inductance and current capacity. Core size, number of turns, and air gaps were selected by conventional inductor design processes in [37] and this is illustrated in Fig. 14. A finite-element method (FEM) based simulation analysis confirmed that the flux density B was appropriately designed to remain below 0.15 T during rated operation, and the temperature characteristics were well maintained below 40 °C during rated operation.

### *C. Comparison Between Conventional and Proposed One*

To compare the efficiency and loss characteristics of the proposed boost converters, the parameters are appropriately selected, as given in Table III. Based on the parameters derived in the previous section, a circuit simulation was conducted, and the losses and peak component ratings of the proposed converters were comparatively evaluated, as illustrated in Fig. 15 and Table IV. As discussed in Section II, all components operate below their output voltage ratings, ensuring that the proposed

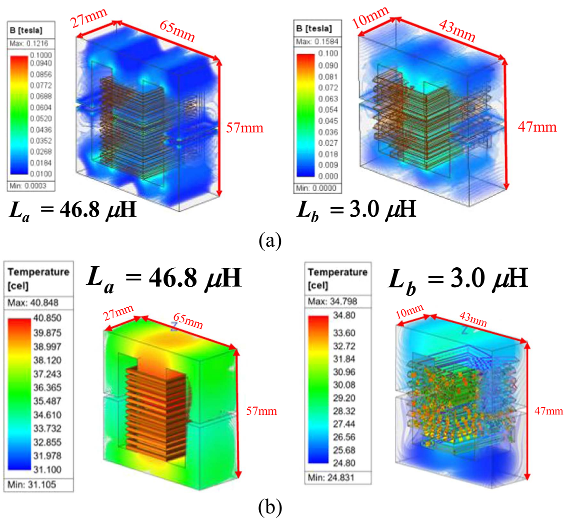


Fig. 14. FEM simulation results for applied inductors $L_a$ & $L_b$. (a) Magnetic characteristics. (b) Temperature characteristics.

TABLE III
PARAMETER SELECTION FOR CONVENTIONAL AND PROPOSED CONVERTERS

| Classification | Conventional | Proposed |
|---|---|---|
| $V_i$ | 200–500 V | |
| $V_o$ | 800 V | |
| $f_s$ | 100 kHz | |
| $L_a$ | 47.0 μH | |
| $L_b$ | - | 3.0 μH |
| $C_s$ | - | 16.0 *n*F |
| $C_r$ | - | 16.0 *n*F |
| $f_r$ | - | 1.12 MHz |

TABLE IV
PEAK COMPONENT RATINGS OF THE PROPOSED CONVERTERS

| | Peak voltage [V] | Peak current [A] |
|---|---|---|
| $Q$ | $V_o$ | $I_{La}$- $I_{Lb}$ |
| $D_1$ | $V_b$ - $V_r$ | $i_{La}(t_0)$ - $i_{Lb}(t_0)$ |
| $D_2$ | $V_b$ - $V_r$ | $I_{La,\max}$ |
| $D_3$ | $V_b$ + $V_r$ | $I_{Lb}$ |
| $C_s$ | $V_o$ | $I_{La,\max}$ |
| $C_r$ | $V_o$ | $I_{Lb}$ |

converters are compact and cost-effective. Notably, the switching loss of the active switch $Q$ is significantly reduced when using the proposed converter shown in Fig. 3, compared to the conventional converter depicted in Fig. 2, where the switching loss of $Q$ is approximately five times higher. For the conventional converter, the switch loss constitutes 68.8% of the total loss, while for the proposed converter, it is reduced to only 40.3% due to the implementation of the proposed soft-switching operations. Thus, the total losses for the conventional and proposed converters are 177.3 W and 93.1 W, respectively. The reduction in total loss is primarily attributed to the decrease in switching loss, which improves the reliability of the converter's switching operation. As identified from Fig. 6, variations in the resonant-tank components ($L_a$, $L_b$, $C_r$, and $C_s$) can compromise the turn-OFF ZVS operation of the proposed converter. Because *a* ±10% manufacturing tolerance is typical for these components, a Monte Carlo analysis of vendor-supplied samples is applied to evaluate the soft-switching performance of the proposed converters, as shown in Fig. 16 [38]. The results show that a ±10% tolerance can shift the resonant frequency by up to ±10%, thereby eliminating turn-OFF ZVS. Under this worst-case scenario, the predicted efficiency declines to 98.82%, approximately 0.30% lower than under ideal ZVS conditions. Accordingly, tighter manufacturing tolerances for the resonant-*LC* network are recommended to preserve the high efficiency of the proposed converter.

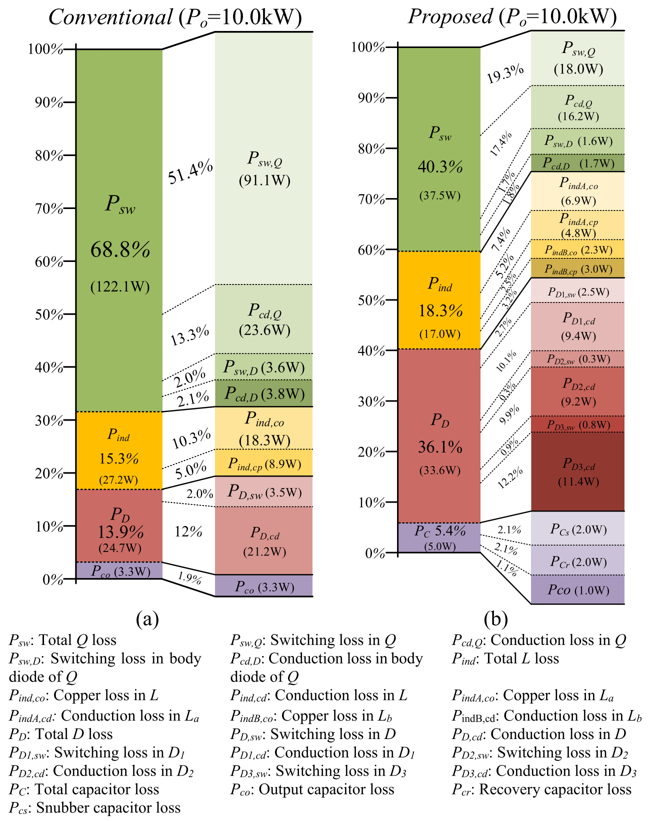


Fig. 15. Breakdown loss analysis for $P_o = 10$ kW. (a) Conventional one. (b) Proposed one.

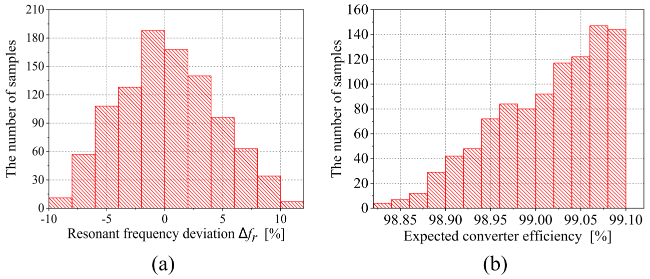
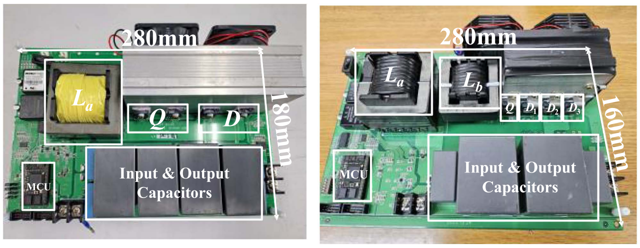


Fig. 16. Expected converter performance under ±10% resonant *LC* manufacturing variations. (a) Resonant frequency deviation. (b) Expected converter efficiency.



(a) (b)

Fig. 17. Fabricated prototypes for the boost converters. (a) Conventional one. (b) Proposed one.

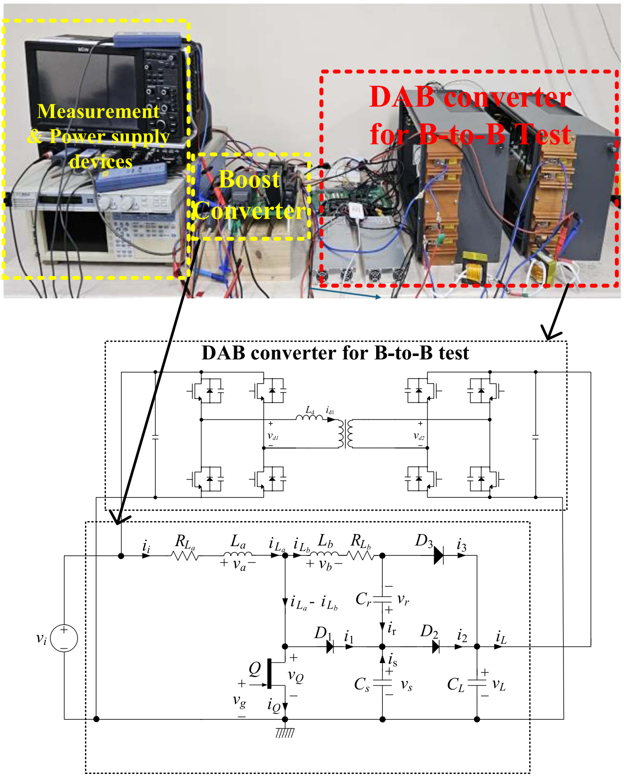
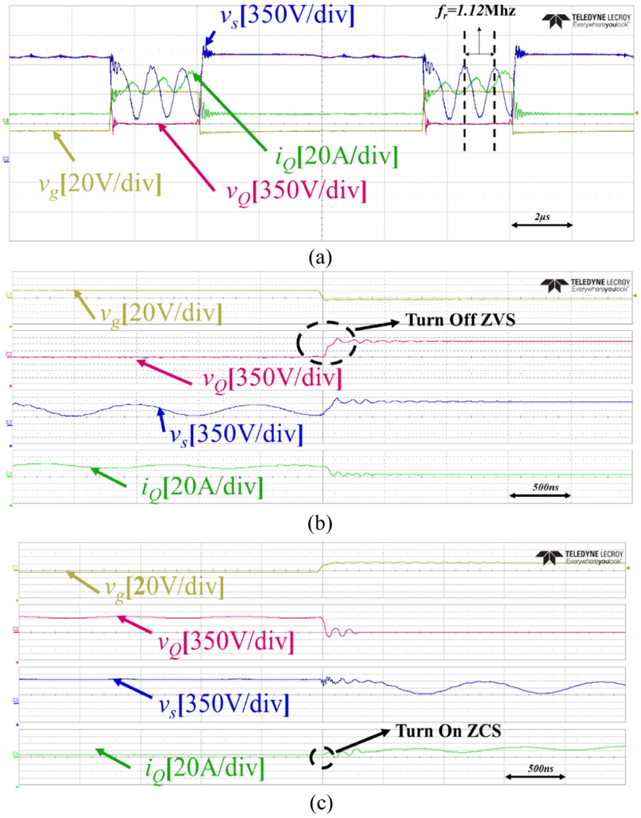


Fig. 18. Back-to-back system to test 10 kW output power delivery.



(a)

(b)

(c)

Fig. 19. Experimental waveforms of the proposed converters. (a) Overall waveforms (Time scale: 2 $\mu$s/div). (b) Turn OFF ZVS waveforms (Time scale: 500 ns/div). (c) Turn ON ZCS waveforms (Time scale: 500 ns/div).

## IV. EXPERIMENTAL VERIFICATIONS

The design principles outlined in the previous section have been applied to a prototype ZVZCS boost converter operating at a switching frequency of 100 kHz, with nominal input and output voltages of 500 and 800 V, respectively. A SiC MOSFET (C3M0016120D) with a 1200 V voltage rating, switching times $t_r$ and $t_f$ of 28 ns, and a conduction loss resistance of 16 m$\Omega$, along with a SiC diode (C4D40120D) rated at 1200 V and 40 A, have been utilized in this article [39]. The variation of selected parameters may happen in this case; thus, precisely manufactured inductors and capacitors having ±1∼3% parameter tolerance are recommended for the turn-OFF ZVS operation of the proposed converters. It is noted that two active switches are used in parallel for large current capacity in this article. Based on these switching device selections, 10 kW PV boost converters, both conventional and proposed, were fabricated, as shown in Fig. 17 . The dimensions of the fabricated converters are 180 mm × 280 mm for the conventional design and 160 mm × 280 mm for the proposed design, making the proposed converter 12% more compact. Consequently, the power density of the proposed converter, including all components (e.g., fan, controller, heat sink), is 1200 W/in$^3$. To evaluate the performance under a 10 kW load, a back-to-back converter system was implemented, as shown in Fig. 18 [40]. A high-power dual-active-bridge (DAB) converter was connected to the proposed converters, enabling circulating power control by modulating the phase shift of the DAB converter. This approach ensures that only the active power loss components are supplied from the source, allowing precise output power delivery control without requiring a high-capacity power supply or load bank.

The experimental waveforms of the prototype are illustrated in Fig. 19, where various output power delivery conditions including $P_o = 10$ kW were evaluated to evaluate the ZVS turn-ON and ZVS turn-OFF operations. The voltage and current stresses of the components are also well mitigated in accordance with the analyses. As a result, ZCS turn-ON and ZVS turn-OFF operations of the main switch are achieved through the proposed operating concept, as described in Figs. 9 and 10. Although not all cases are presented in this article due to the high similarity of the operating waveforms, the proposed concept also ensures ZVZCS operation under various other duty cycle conditions. The key characteristics of the proposed converters are illustrated in Fig. 20, showing good agreement with the simulation results

TABLE V
FAIR COMPARISON BETWEEN THE CONVENTIONAL AND PROPOSED BOOST CONVERTERS

| References | Voltage Gain (CCM) | Switching frequency | Max voltage on Switch | Max voltage on Diode | Soft-switching | The number of passive components | Measured efficiency @ rated power |
|---|---|---|---|---|---|---|---|
| Kumar et al. [26] | $\frac{1}{(1-D)^3}$ | 50 kHz | $V_o$ | $V_o$ | Turn-ON hard switching<br>Turn-OFF hard switching | Inductor: 3<br>Capacitors: 2<br>Diode: 5, SW: 1 | 91.6 % @ 250W |
| Karthikkumar et al. [27] | $\frac{(3-D)}{(1-D)^2}$ | 20 kHz | $V_o$ | $V_o$ | Turn-ON hard switching<br>Turn-OFF hard switching | Inductor: 3<br>Capacitors: 3<br>Diode: 6, SW: 1 | 94.3 % @ 300W |
| Shanthi et al. [28] | $2\frac{1+D}{1-D}$ | 50 kHz | $V_o/2$ | $V_o/2$ | Turn-ON hard switching<br>Turn-OFF hard switching | Inductor: 2<br>Capacitors: 4<br>Diode: 6, SW: 1 | 91.4 % @ 500W |
| Diwakar Naik and Vinatha [29] | $\frac{1+D}{(1-D)^2}$ | 50 kHz | $V_o/(1+\mathrm{D})$ | $V_o/(1+\mathrm{D})$ | Turn-ON hard switching<br>Turn-OFF hard switching | Inductor: 3<br>Capacitors: 3<br>Diode: 4, SW: 1 | 95.4 % @ 110W |
| Kumar et al. [30] | $\frac{2-D}{(2-D)^2}$ | 50 kHz | $V_i/(1+\mathrm{D})$ | $\left(\frac{V_o}{V_s(1-D)}-1\right)\frac{V_s}{1-D}$ | Turn-ON hard switching<br>Turn-OFF hard switching | Inductor: 2<br>Capacitors: 2<br>Diode: 4, SW: 1 | 91.2 % @ 500W |
| Barbosa et al. [31] | $\frac{2-N}{(1-N)(1-\mathrm{D})}$ | 50 kHz | $V_{\mathrm{in}}/(1\text{-}\mathrm{D})$ | $\left(\frac{V_o}{V_s(1-D)}-1\right)\frac{V_s}{1-D}$ | Turn-ON Quasi ZCS<br>Turn-OFF hard switching | Inductor: 2<br>Capacitors: 3<br>Diode: 3, SW: 1 | 96.6 % @ 300W |
| Mahmood et al. [32] | $\frac{2(2-D)}{(1-D)^2}$ | 40 kHz | $\frac{(2-D)}{(1-D)^2}$ | $V_o/2$ | Turn-ON Quasi ZCS<br>Turn-OFF hard switching | Inductor: 2<br>Capacitors: 4<br>Diode: 6, SW: 1 | 95.0 % @ 300W |
| Sankaranarayanan et al. [33] | $\frac{1}{1-D}$ | 110kHz | $V_o$ | $V_o$ | Turn-ON ZVS-QSW<br>Turn-OFF ZCS | Inductor: 1<br>Capacitors: 2<br>Diode: 0, SW: 2 | 98.3% @ 7 kW |
| Bi et al. [34] | $\frac{3}{1-D}$ | 50 kHz | $V_o/3$ | $2V_o/3$ | Turn-ON hard switching<br>Turn-OFF hard switching | Inductor: 3<br>Capacitors: 4<br>Diode: 3, SW: 2 | 97.9% @ 1 kW |
| Chandra Mouli et al. [35] | $\frac{1}{1-D}$ | 47 kHz | $V_o$ | $V_o$ | Turn-ON hard switching<br>Turn-OFF hard switching | Inductor: 4<br>Capacitors: 1<br>Diode: 3, SW: 3 | 98.0% @ 10 kW |
| Proposed | $\frac{1}{1-D}$ | 100 kHz | $V_o$ | $V_{\mathrm{b}}+V_{\mathrm{r}}$ | Turn-ON Quasi ZCS<br>Turn-OFF Quasi ZVS | Inductor: 2<br>Capacitors: 2<br>Diode: 3, SW: 1 | 99.0% @ 10kW |

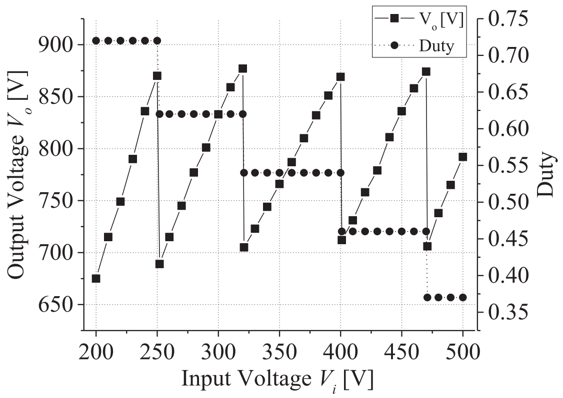


Fig. 20. Measured results of $V_o$ and duty w.r.t. $V_i$.

presented in Fig. 10. Although a ±12% variation in output voltage occurs, as previously discussed in Fig. 10, this phenomenon can be considered acceptable for ac/dc inverters. These inverters can continue to operate by injecting active and reactive currents into the grid, as depicted in Fig. 1, as long as the dc-link voltage of the inverter $V_o$, which is the output voltage of the proposed converter, remains sufficiently higher than the grid voltage $V_g$. In this case, the modulation index of the grid-side inverter remains in the range of approximately 35%–50%, which is adequate to deliver the required active and reactive power.

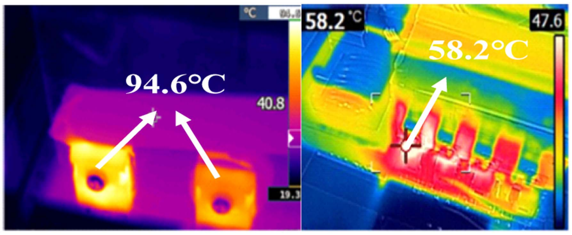


Fig. 21. Thermal measurement of the switching device $Q$ after 1 hour for the conventional (left) and proposed (right) converters.

For a 10 kW rated output power delivery, the temperature of the active switch was measured, as shown in Fig. 21. The measured temperature of the conventional converter reached approximately 95 °C, while the proposed converter maintained a temperature below 60 °C after 1 h of operation. The measured efficiencies under various load conditions and input voltages are shown in Fig. 22. The proposed converter achieved a maximum efficiency of 99.2% at $P_o = 2.0$ kW and 99.0% at $P_o = 10.0$ kW, compared to the conventional converter shown in Fig. 22(a), which achieved a maximum efficiency of 98.2% at $P_o = 2.0$ kW and 97.7% at $P_o = 10.0$ kW. This demonstrates an efficiency improvement of over 1.0%, consistent with the theoretical and simulation results shown in Fig. 16. Moreover, as shown in Fig. 22(b), the proposed converter maintains an efficiency improvement of approximately 1.0% or more over

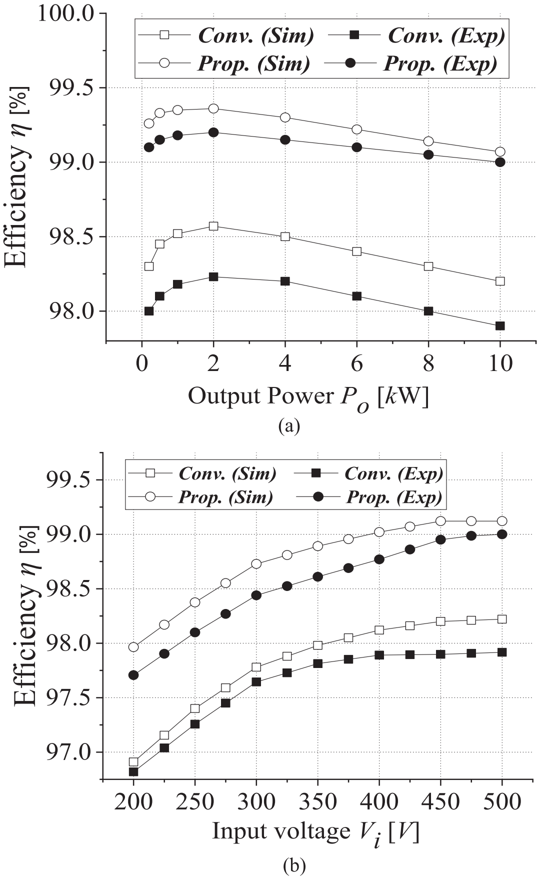


Fig. 22. Efficiency comparison between two converters. (a) Efficiency versus output power $P_o$ ($V_i = 500$ V, $R_o$ varies). (b) Efficiency versus input voltage $V_i$ ($R_o = 25\ \Omega$, $P_o$ varies).

the conventional converter even under varying input voltages. The slight discrepancy between the simulated and experimental results is attributed to the assumption of constant loss terms for the switching devices in the simulation, whereas the actual devices exhibit loss components that vary with operating current, voltage, and temperature.

Table V compares the key performance metrics of representative boost-type PV converters, excluding the input and output smoothing capacitors. When only a single active switch is employed—cases [26], [27], [28], [29], [30], [31], [32]—a relatively large number of passive components (inductors, capacitors, and diodes) is necessary to achieve the desired voltage gain, which in turn increases volume, cost, and conduction loss. To alleviate these penalties, converters in [33], [34], and [35] introduce two or three active switches and implement partial soft-switching schemes; nevertheless, they still rely on several passive components and their measured efficiencies remain below 99% .

In contrast, the proposed converter in Table V operates with lower voltage stress on both the main switch and the output diode, while requiring the fewest passive elements among all candidates. This reduction directly translates into higher power density and improved cost-effectiveness. As a result, its experimentally verified efficiency (99.0% at 10 kW) surpasses that of the conventional counterparts, highlighting its suitability for high-power PV applications.

## V. CONCLUSION

The proposed high-efficiency non-isolated boost converter leveraging *LC* resonance for quasi soft-switching operation has demonstrated remarkable performance in both theoretical and experimental validations. Key findings include a significant reduction in switching losses through quasi soft-switching operations, resulting in a peak efficiency of 99.0% at 10 kW output. The proposed converter also achieved a 15% reduction in size compared to conventional designs, showcasing its high power density and cost-effectiveness. By employing a single SiC MOSFET, the converter achieves both design simplicity and operational reliability, making it an ideal solution for high-power PV applications.

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