Dual-Layer SVM-Based Power Flow Control of ANPC-Type Multiport Inverter in Multisource Electric Vehicles

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***Abstract*—The active-neutral-point-clamped (ANPC) multiport inverter can serve as a high-efficiency interface for multisource electric vehicles by eliminating the need for intermediate dc–dc converters. However, achieving precise power flow control between dc sources, while ensuring satisfactory motor control becomes challenging, particularly under unbalanced dc port voltages. To address this issue, this article proposes a dual-layer space vector modulation (SVM)-based control strategy for ANPC-type multiport inverters to enable simultaneous power flow control between dc sources and motor drive regulation, even under unbalanced dc port conditions. In the proposed scheme, the asymmetrical three-level SVM is decomposed into symmetrical upper and lower layers based on the switching state of the low-frequency cell, simplifying the calculation of dwell time under unbalanced dc-link voltages. And a direct power control scheme is applied in the upper-layer SVM to realize the desired power flow between the dc sources. In addition, the proposed dual-layer SVM ensures that the low-frequency cell operates at the fundamental frequency, even in the presence of dc-link imbalance. The power distribution range of the proposed scheme is also analytically discussed. Experimental results confirm the effectiveness of the proposed dual-layer SVM-based power flow control scheme.**

***Index Terms*—Hybrid electric vehicle (EV), multiport inverter, permanent-magnet synchronous motor (PMSM), single-stage conversion, space vector modulation (SVM).**

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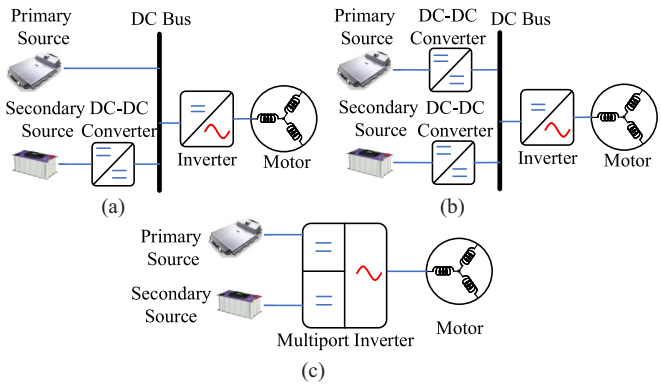

Fig. 1. Various configurations for MEVs. (a) Semi-active configuration. (b) Active configuration. (c) Multiport inverter configuration.

I. Introduction

ELECTRIC vehicle (EV) is considered a promising solution to deal with the fossil fuel depletion and environmental issues introduced by the internal combustion engine. Among the various types of electric vehicles, multisource EVs (MEVs) combining the power output of two or more energy sources with complementary characteristics have become a preferred choice due to their advanced features in terms of range per charge, initial investment, efficiency, lifespan, and reliability [1], [2], [3], [4], [5], [6].

As a key enabler for MEVs, the power electronic interfaces determine the power distribution and motor drive control performance and should be properly designed. The typical configurations are shown in Fig. 1(a) and (b), where extra dc–dc converters are required to integrate the secondary energy sources. Among the various types of interfaces, multiport inverters, which allow dc sources to be directly connected to each dc port of the inverter, have drawn attention due to their significant advantages [7], such as high efficiency without an intermediate dc–dc power conversion stage, high power density with improved integration level, and superior output waveform with multilevel output features. At present, multiport inverters, which evolved from multilevel inverters by replacing dc-link capacitors with dc sources, are the dominant options because of their mature hardware design and modulation schemes inherent

in their corresponding multilevel counterparts [8]. Its typical configuration is presented in Fig. 1(c).

The topologies of multiport inverters can be easily transplanted from the existing multilevel converters, such as neutral-point-clamped (NPC) converters [9], [10], [11], active-NPC (ANPC) type [12], [13], cascaded H-bridge (CHB) converters [14], [15], [16], and modular multilevel converters (MMC) [17], [18], etc. The CHB- and MMC-type multiport inverters are constantly employed in large-scale energy source integration, such as centralized renewable energy power generation. Meanwhile, NPC and ANPC forms are usually employed in small-scale scenarios, such as EVs with two complementary energy sources. Compared to other topologies, the ANPC-type multiport inverter, which inherent all the salient advantages of the ANPC converter, such as reasonable component utilization with few passive components and sufficient control degree of freedom with the capability of fundamental frequency operation of partial power switches [19], [20], [21], has been an attractive solution in industrial or commercial applications to enhance system efficiency and reliability for MEVs.

Despite these advantages, ANPC-type multiport inverters suffer from the unbalanced dc-link voltages introduced by the direct energy source connections, which leads to an asymmetric voltage vector diagram and a heavy computational burden for modulation scheme design. Besides, compared with the ANPC converters, ANPC-type multiport inverters should achieve the desired power distribution between the dc sources while maintaining satisfactory motor control.

Given this, substantial research efforts have been conducted to deal with the unbalanced dc-link voltages of ANPC converters. An equivalent two-level space vector modulation (SVM) of ANPC converters was proposed in [22] to achieve a high-quality ac current. In [23], a carrier-based modulation was proposed to balance the flying capacitor without reducing the quality of ANPC converter output. In [24], an optimized carrier-based pulsewidth modulation (PWM) method for 5L-ANPC converters was proposed to achieve a tradeoff between neutral-point potential balance performance and harmonic performance. A simplified PWM strategy with unbalanced dc links was proposed in [25] to achieve high-quality line-to-line output voltages and to maximize the linear modulation range. A two-stage model predictive control (MPC) was proposed in [26] to realize undistorted stator current under both balanced and unbalanced dc-link scenarios. Although these methods effectively realize high-quality ac current under the unbalanced dc-link scenario, power distribution between the dc ports, which is mandatory in ANPC-type multiport inverters, is not discussed in these works.

Regarding the power distribution between the dc ports in ANPC multiport inverters, to the best of our knowledge, no investigation has been reported. Several modulation schemes in NPC-type multiport inverters were reported in recent years [27], [28], [29], [30] to concurrently realize power distribution on the dc side and stator current tracking on the ac side. Although these methods are effective in NPC-type multiport inverters, they are not applicable to ANPC-type multiport inverters, as the number of switching states in the ANPC-type multiport inverter is much larger than that of the NPC-type one. Besides, the fundamental-frequency operation of the low-frequency cell (LFC) in the ANPC-type multiport inverter should also be guaranteed for high-efficiency operation, even under unbalanced dc-link voltages.

In view of this, this article proposed a dual-layer SVM-based power flow control of ANPC-type multiport inverter to simultaneously realize power flow control between the dc sources and motor drive control under the unbalanced dc port voltage with the fundamental-frequency operation of LFC. In the proposed scheme, the asymmetrical three-level SVM is decomposed into symmetrical upper-layer and lower-layer SVMs according to the switching state of the LFC to simplify the dwell time calculation under unbalanced dc-link voltages. Subsequently, the dc-port power model in the upper layer SVM is put forward to achieve the desired power flow control between the dc sources. In addition, the fundamental-frequency operation of the low-frequency cell is also guaranteed with the proposed dual-layer SVM, even under unbalanced dc-link voltages. In addition, the power distribution range for the proposed scheme is also discussed analytically. The steady-state and dynamic performances confirm the effectiveness of the proposed method.

The main contributions of this article are as follows:

1) The asymmetrical three-level SVM is decomposed into symmetrical upper-layer and lower-layer SVMs according to the switching state of the LFC to simplify the dwell time calculation and reduce switching losses under unbalanced dc-link voltages.
2) An instantaneous dc port power model in the upper layer SVM and the corresponding modulation scheme are put forward to achieve the flexible power flow and motor drive control. Moreover, the power distribution capability of the ANPC-type multiport inverter with the proposed scheme is also analytically revealed.
3) The fundamental-frequency operation of the low-frequency cell is also guaranteed with the proposed dual-layer SVM, even under unbalanced dc-link voltages.

The rest of this article is organized as follows. Section II presents the system topology and system modeling of the ANPC-type multiport inverter. The proposed dual-layer SVM-based power flow control of the ANPC-type multiport inverter is illustrated in Section III. The effectiveness of the proposed scheme is experimentally evaluated in Section IV. Finally, Section V concludes this article.

II. Modeling of ANPC-Type Multiport Inverters

The topology of the ANPC-type multiport inverter for MEVs is illustrated in Fig. 2. The high-voltage port is connected to the primary source, and the low-voltage port is connected to the secondary source. Unlike a traditional ANPC converter, the ANPC-type multiport inverter has no neutral point. Therefore, the modulation and control schemes cannot be transplanted directly from the ANPC converter. Both sources are connected to the motor directly, enabling single-stage power conversion from the sources to the motor. The permanent-magnet synchronous motor (PMSM), mainly used in MEVs because of its high efficiency and compactness, is employed to investigate ANPC-type multiport inverters for MEVs.

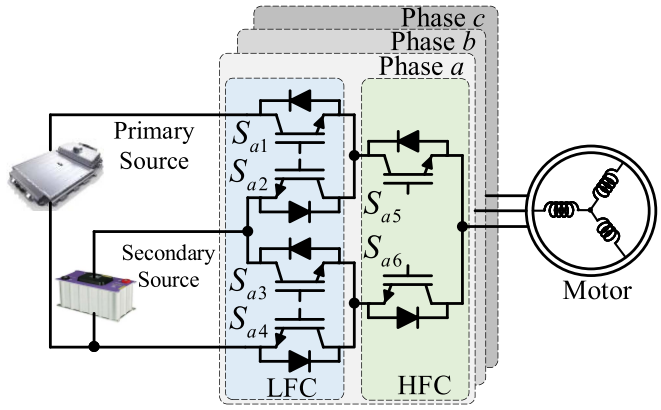

Fig. 2. Topology of an ANPC-type multiport inverter.

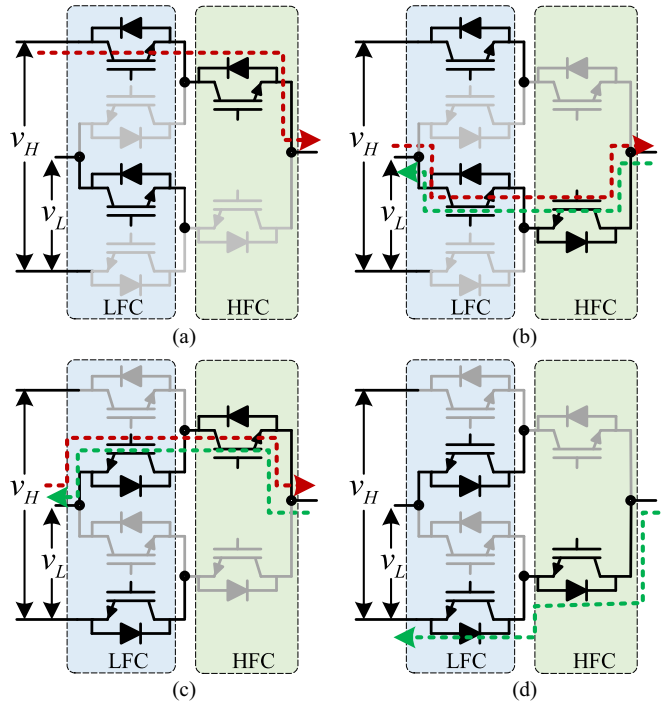

Fig. 3. Current paths of ANPC-type multiport inverters. (a) $S_{x1}S_{x5} = 11$. (b) $S_{x1}S_{x5} = 01$. (c) $S_{x1}S_{x5} = 10$. (d) $S_{x1}S_{x5} = 00$. ($x \in \{a, b, c\}$).

Each phase of the ANPC-type multiport inverters consists of six active switches $S_{x1} \sim S_{x6}$, ($x \in \{a, b, c\}$), where $S_{x1}S_{x2}$, $S_{x3}S_{x4}$, and $S_{x5}S_{x6}$ are complementary switching states, respectively, which can prevent shoot through within the inverter circuit [8]. This type of converter can operate simultaneously at two different frequencies: fundamental frequency (i.e., 0$\sim$ 50 Hz) for $S_{x1} \sim S_{x4}$, denoted as low-frequency cell (LFC) and PWM frequency (i.e., 10 kHz) for S_{x5} and S_{x6}, denoted as the high-frequency cell (HFC). S_{x1} and S_{x3} have the same switching signals.

As shown in Fig. 3, the power flow paths among the primary source, secondary source, and motor are determined by the switching states of S_{x1}, S_{x3}, and S_{x5}. All the switching states, their corresponding output voltage levels, and the power sources supplying the motor of ANPC-type multiport inverters

TABLE I
SWITCHING STATES OF ANPC-TYPE MULTIPORT INVERTERS

Gating signals S_{x1}/S_{x3}	Gating signals S_{x5}	Voltage v_{xN}	Power source
1	1	v_H	Primary source
1	0	v_L	Secondary source
0	1	v_L	Secondary source
0	0	0	None of the sources

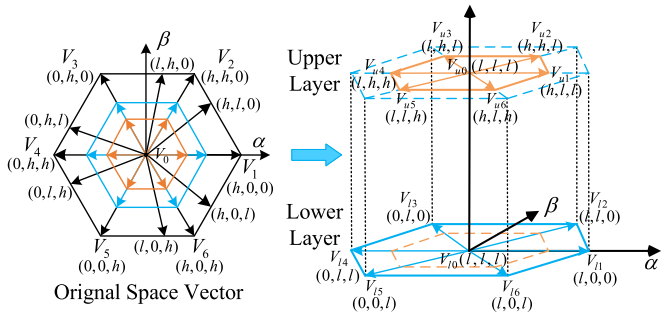

Fig. 4. Space vector diagrams for the original asymmetrical one and layer decomposed one.

are presented in Table I. As shown, the switching state not only determines the output voltage, but also the power source that supplies the motor. Therefore, the modulation design of the ANPC-type multiport inverters is challenging since the desired power distribution between the dc sources, together with the motor drive control, should be achieved simultaneously under the unbalanced dc ports. Besides, the fundamental-frequency operation of the LFC should be guaranteed to enhance the power conversion efficiency.

When S_{x1}/S_{x3} is ON, the output voltage of phase x is v_L or v_H, while when S_{x1}/S_{x3} is OFF, the output voltage of phase x is 0 or v_L. It is seen that the output power/voltage can be determined by the switching states of LFC. To ease dc power flow control together with ac voltage modulation, the decomposition of the ANPC-type multiport inverters is developed in this article, where the SVM of the ANPC-type multiport inverter is decomposed into upper-layer and lower-layer according to the switching state of LFC, as shown in Fig. 4. The dc-link voltage of the upper layer is $v_H - v_L$, while that of the lower layer is v_L. To maintain the fundamental-frequency operation of LFC, zero voltage vector (l, l, l) is always employed, and (h, h, h) is abandoned for voltage vector synthesis in the upper-layer SVM. Besides, zero voltage vector (l, l, l) is always employed, and (0,0,0) is abandoned for voltage vector synthesis in the lower-layer SVM. In this way, the zero vectors on both layers are consistent. With fewer voltage vectors employed, the number of switching times can be reduced.

Due to the direct energy source integration configuration, the dc port voltage is unbalanced with the state of charge of the energy sources. As shown in Fig. 4, the voltage vector diagram is asymmetrical, and voltage vector synthesis using these asymmetrical voltage vectors results in a heavy computational burden. In addition, similar to an ANPC converter, the original space vector diagram of the multiport inverter has 64 available voltage

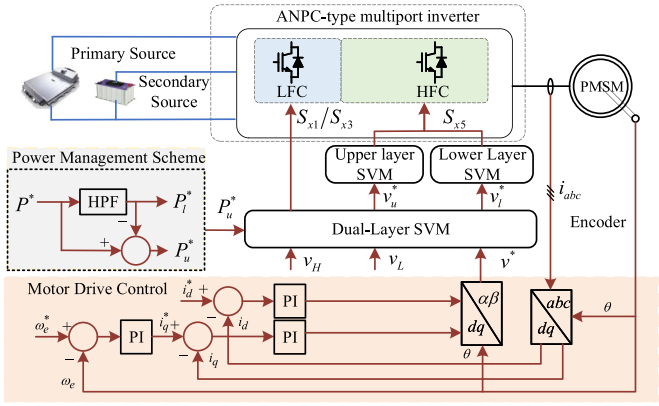

Fig. 5. Overall control diagram of the ANPC-type multiport inverters.

vectors. By the layer decomposition, the space vector diagram in each layer is symmetrical, and the number of available voltage vectors is sharply reduced to 7 in each layer. Therefore, the voltage vector synthesis in the proposed dual-layer SVM can be simplified in a symmetrical space vector diagram with seven voltage vectors.

III. Dual-Layer SVM-Based Power Flow Control

The overall control scheme for the ANPC-type multiport inverters is depicted in Fig. 5. It comprises four parts: ac voltage reference calculation by classical field-oriented control, dc port power reference calculation by a frequency splitter, power flow control by the proposed dual-layer SVM, and dwell time calculation in each layer. Detailed descriptions of each part are given in the following text.

A. Motor Drive Control and Power Management

The output of the motor controller is the voltage vector reference v^*. As long as the voltage-second value for the active voltage vector remains unchanged, the motor drive control is achieved. For simplification, the voltage vector reference v^* is calculated by assuming the ANPC-type multiport inverter as a two-level inverter with a dc-link voltage of v_H. The vector synthesis of v^* in Sector I is illustrated

$$v^* = \frac{(V_1 t_1 + V_2 t_2)}{T_s} \tag{1}$$

where V_1 and V_2 are basic vectors in Sector I, respectively. t_1 and t_2 are the dwell time for V_1 and V_2, respectively. T_s is the sampling period.

The sum of the voltage vectors in the dual-layer SVM satisfies

$$\boldsymbol{v}^* = \boldsymbol{v}_{\boldsymbol{u}}^* + \boldsymbol{v}_{\boldsymbol{l}}^* \tag{2}$$

where $\boldsymbol{v}_{\boldsymbol{u}}^*$and $\boldsymbol{v}_{\boldsymbol{l}}^*$ are the desired voltage vectors for the upper and lower layers, respectively. Considering $\boldsymbol{v}^* \in [0, v_H]$, $\boldsymbol{v}_{\boldsymbol{u}}^* \in [0, v_H - v_L]$, and $\boldsymbol{v}_{\boldsymbol{l}}^* \in [0, v_L]$, it can easily be obtained that $\boldsymbol{v}_{\boldsymbol{u}}^* + \boldsymbol{v}_{\boldsymbol{l}}^* \in [0, v_H]$. Therefore, the layer decomposition process will not affect the feasible range of the synthesized voltage vector in the original space vector diagram.

To fully explore the potential of the different energy sources, the power management scheme is inevitable in HEVs [31], [32], [33]. In this article, a simple frequency splitter is employed for power management, where the load power demand is split into low- and high-frequency components. The load demand frequency decoupling is achieved through a high-pass filter [34]. The high-frequency component is fed into the fast-acting power sources (secondary source in this article), noted as P_l^*, such as the supercapacitor, and the rest of the components are fed into the slow-acting sources (primary source in this article), noted as P_u^*, such as fuel cells or batteries.

B. Direct Power Control in the Upper-Layer SVM

According to the above analysis of the power flow paths, the sources connected to the high-voltage and low-voltage dc ports can be modeled as two separate units to support the ac side independently, which can be written as follows:

$$\begin{cases} P_u = v_H i_H \\ P_l = v_L i_L \end{cases} \tag{3}$$

where P_u and P_l are the output power of the high-voltage and low-voltage dc ports, respectively. i_H and i_L are their corresponding currents, which can be obtained in a switching period as follows:

$$\begin{cases} i_H = \sum_{x=a,b,c} i_x d_{x1} \\ i_L = \sum_{x=a,b,c} i_x (d_{x2} - d_{x1}) \end{cases} \tag{4}$$

where d_{x1} and d_{x2} are the duty cycles of S_{x1} and S_{x2}, respectively, and i_x is the inverter phase current of the each phase $(x \in a, b, c)$.

The required power for the motor can be calculated as

$$P^* = \frac{3}{2}\mathrm{Re}\left(\boldsymbol{i}\bar{v}^*\right) \tag{5}$$

where $\bar{\boldsymbol{i}}$ denotes the conjugate of current vector $\boldsymbol{i}$.

However, due to $v^* = v_1^* + v_2^*$ and the instantaneous stator current i for each port being the same in each sampling period, the relation between the total demand power and the upper layer and lower layer power can be written as

$$P^* = P_u^* + P_l^* \tag{6}$$

$$P_u^* = \frac{3}{2} Re(v_u^* \bar{i}) \tag{7}$$

$$P_l^* = \frac{3}{2} Re(v_l^* \bar{i}). \tag{8}$$

As the dc port voltage of the primary source is v_H, the output power of the upper layer P_u^* should be corrected as

$$P_u^* = \frac{3}{2}\varepsilon\mathrm{Re}\left(\boldsymbol{i}\bar{v}_u^*\right) \tag{9}$$

where correction coefficient $\varepsilon = \frac{v_H}{v_H - v_L}$.

In Sector I, the switching states for LFC could be (100) and (110). Based on the switching states of LFC, voltage vector decomposition can be categorized into two cases, and each is clarified as follows:

1) Case I: When the switching states for LFC are (100), the output power from the high-voltage port is determined by the output voltage of phase a. Besides, $\boldsymbol{v}_{\boldsymbol{u}}^*$ is aligned with the basic vector $\boldsymbol{V_{u1}}/\boldsymbol{V_1}$ in this case. The voltage vector decomposition process in this case is shown in Fig. 6(a) and (b). As

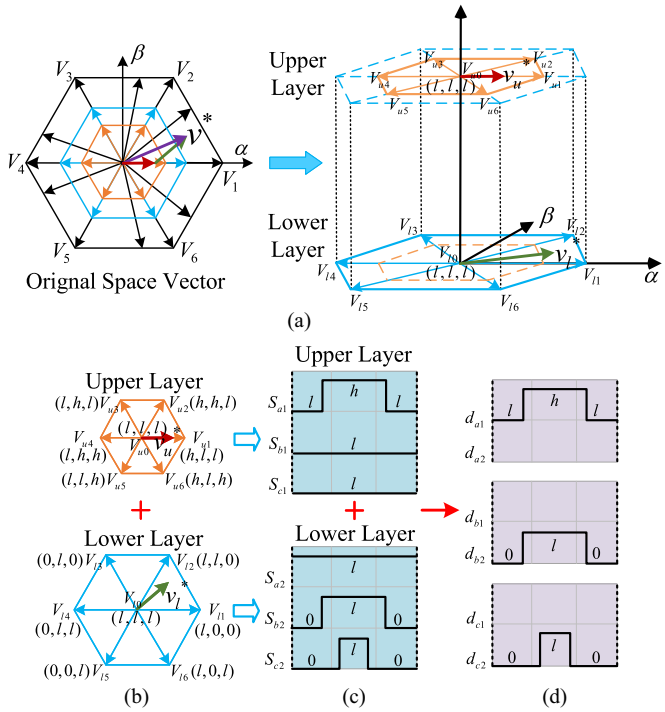

Fig. 6. Case I: vector decomposition in Sector I when $S_{a1}S_{b1}S_{c1} = (100)$. (a) Desired voltage vector for the ANPC-type multiport inverter. (b) Voltage vector decomposition in dual-layer SVM-based diagrams. (c) PWM in each layer SVM-based diagram. (d) Synthesized pulse train for the ANPC-type multiport inverter.

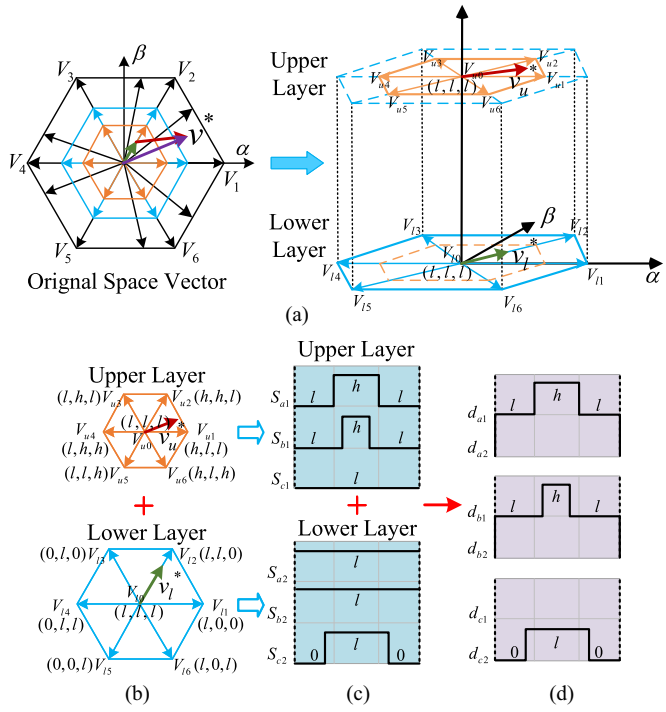

Fig. 7. Case II: vector decomposition in Sector I when $S_{a1}S_{b1}S_{c1} = (110)$. (a) Desired voltage vector for the ANPC-type multiport inverter. (b) Voltage vector decomposition in dual-layer SVM-based diagrams. (c) PWM in each layer SVM-based diagram. (d) Synthesized pulse train for the ANPC-type multiport inverter.

observed in Fig. 6(c), the upper-layer SVM requires only one switching operation, while the lower-layer SVM requires two. Consequently, the total switching operations for the ANPC-type multiport inverter under the proposed dual-layer SVM-based method amount to three, with the corresponding pulse train depicted in Fig. 6(d).

To satisfy the condition that $\boldsymbol{v}_{\boldsymbol{u}}^*$ is aligned with the basic vector $\boldsymbol{V_{u1}}/\boldsymbol{V_1}$, $\boldsymbol{v}_{\boldsymbol{u}}^*$ can be denoted using the basic vector

$$\boldsymbol{v}_{\boldsymbol{u}}^* = \lambda_1 \frac{\boldsymbol{V_1} t_1}{T_s} \tag{10}$$

where $\lambda_1 \in [0, 1]$ is the coefficient for vector decomposition in case I. Combining (9) and (10), λ_1 can be obtained.

2) Case II: When the switching states for LFC are (110), the output power from the low-voltage port is determined by the output voltage of phase c. Besides, $\boldsymbol{v}_{\boldsymbol{l}}^*$ is aligned with the basic vector V_{l2}/V_2. The voltage vector decomposition process in this case is shown in Fig. 7(a) and (b). As observed in Fig. 7(c), the lower-layer SVM requires only one switching operation, while the upper-layer SVM requires two. Consequently, the total number of switching operations for the ANPC-type multiport inverter under the proposed dual-layer SVM-based method is three, with the corresponding pulse train depicted in Fig. 7(d) .

To satisfy the condition that $\boldsymbol{v}_{\boldsymbol{l}}^*$ is aligned with the basic vector V_{l2}/V_2, $\boldsymbol{v}_{\boldsymbol{u}}^*$ can be denoted using the basic vector

$$\boldsymbol{v}_{\boldsymbol{u}}^* = \frac{\boldsymbol{V_1} t_1}{T_s} + \lambda_2 \frac{\boldsymbol{V_2} t_2}{T_s} \tag{11}$$

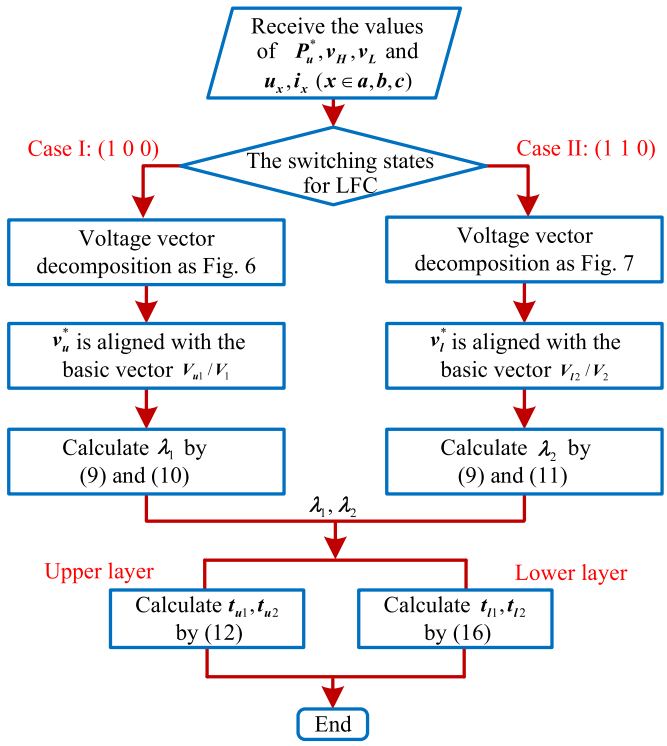

Fig. 8. Flowchart of the proposed dual-layer SVM-based power flow control scheme .

where $\lambda_2 \in [0,1]$ is the coefficient for vector decomposition in case II. Combining (9) and (11), λ_2 can be obtained. The flowchart diagram of the proposed dual-layer SVM-based power flow control scheme is depicted in Fig. 8.

C. Dwell Time Calculation in Each Layer

With the solving of λ_1 and λ_2, the desired voltage vectors $\boldsymbol{v_u^*}$ and $\boldsymbol{v_l^*}$ in each layer can be obtained. The dwell time calculation in Sector I is illustrated as an example to show the implementation process of dual-layer SVM.

The dwell time of the upper layer can be obtained from

$$\boldsymbol{v_u^*} = \lambda_1 \frac{\boldsymbol{V_1} t_1}{T_s} + \lambda_2 \frac{\boldsymbol{V_2} t_2}{T_s} = \frac{\boldsymbol{V_{u1}} t_{u1}}{T_s} + \frac{\boldsymbol{V_{u2}} t_{u2}}{T_s} \tag{12}$$

where

$$\frac{|\boldsymbol{V_1}|}{|\boldsymbol{V_{u1}}|} = \frac{|\boldsymbol{V_2}|}{|\boldsymbol{V_{u2}}|} = \frac{v_H}{(v_H - v_L)} = \varepsilon. \tag{13}$$

Solving (12), t_{u1} and t_{u2} can be obtained as

$$t_{u1} = \lambda_1 \varepsilon t_1 \tag{14}$$

$$t_{u2} = \lambda_2 \varepsilon t_2 \tag{15}$$

where t_{u1} and t_{u2} are the dwell time for $\boldsymbol{V_{u1}}$ and $\boldsymbol{V_{u2}}$, respectively.

The dwell time of the lower layer can be obtained from

$$\boldsymbol{v_l^*} = (1-\lambda_1) \frac{\boldsymbol{V_1} t_1}{T_s} + (1-\lambda_2) \frac{\boldsymbol{V_2} t_2}{T_s} = \frac{\boldsymbol{V_{l1}} t_{l1}}{T_s} + \frac{\boldsymbol{V_{l2}} t_{l2}}{T_s} \tag{16}$$

where

$$\frac{|\boldsymbol{V_1}|}{|\boldsymbol{V_{l1}}|} = \frac{|\boldsymbol{V_2}|}{|\boldsymbol{V_{l2}}|} = \frac{v_H}{v_L} = \frac{\varepsilon}{1-\varepsilon}. \tag{17}$$

Solving (16), t_{l1} and t_{l2} can be obtained as

$$t_{l1} = (1-\lambda_1) \frac{\varepsilon}{1-\varepsilon} t_1 \tag{18}$$

$$t_{l2} = (1-\lambda_2) \frac{\varepsilon}{1-\varepsilon} t_2 \tag{19}$$

where t_{l1} and t_{l2} are the dwell time for $\boldsymbol{V_{l1}}$ and $\boldsymbol{V_{l2}}$, respectively.

D. Power Distribution Range Analysis

By adopting the proposed dual-layer SVM, the ANPC-type multiport converter can achieve flexible power distribution between the dc sources. However, this capability depends on the load current $\boldsymbol{i}$ and the voltage vector associated with each port. To address this, an analytical framework is provided for evaluating the power distribution range of the dual-layer SVM.

The power distribution range η, represents the ratio of the power delivered by the primary source P_u to the total output power P, is provided as

$$\eta = \frac{P_u}{P} = \varepsilon \frac{|\boldsymbol{v_u^*}|}{|\boldsymbol{v^*}|}. \tag{20}$$

Only the linear modulation range is considered, the ranges of the voltage vectors can be calculated as $\boldsymbol{v_u^*} \in [0, \frac{v_H - v_L}{\sqrt{3}}]$, $\boldsymbol{v_l^*} \in [0, \frac{v_L}{\sqrt{3}}]$, and $\boldsymbol{v^*} \in [0, \frac{v_H}{\sqrt{3}}]$.

The lower boundary of η can be calculated as follows. When $|\boldsymbol{v^*}| \le \frac{v_L}{\sqrt{3}}$, all the power can be supplied by the secondary source, and the minimum value of $\boldsymbol{v_u^*}$ can be 0. When $|\boldsymbol{v^*}| > \frac{v_L}{\sqrt{3}}$, the power cannot be supplied by the secondary source. The minimum value of $\boldsymbol{v_u^*} = |\boldsymbol{v^*}| - \frac{v_L}{\sqrt{3}}$.

The upper boundary of η can be calculated as follows. When $|\boldsymbol{v^*}| \le \frac{v_H - v_L}{\sqrt{3}}$, all the power can be supplied by the primary source, and the maximum value of the $|\boldsymbol{v_u^*}| = |\boldsymbol{v^*}|$. When $|\boldsymbol{v^*}| > \frac{v_H - v_L}{\sqrt{3}}$, the power cannot be supplied by the primary source. The maximum value of $\boldsymbol{v_u^*} = \frac{v_H - v_L}{\sqrt{3}}$.

Combining the analysis of the upper and lower boundary for η, the theoretical power distribution range can be calculated as

$$\left\{0, \varepsilon\left(1 - \frac{v_L}{\sqrt{3}|\boldsymbol{v^*}|}\right)\right\}_{\max} \le \eta \le \left\{\frac{v_H}{\sqrt{3}|\boldsymbol{v^*}|}, \varepsilon\right\}_{\min} \tag{21}$$

where $|\boldsymbol{v^*}|$ is determined by the modulation index, while ε is determined by the voltage ratios.

Fig. 9(a) shows the power distribution range η versus different voltage ratios ε. The high-voltage dc port can support the motor independently when $\varepsilon = 1$, i.e., $\eta = 1$ can be achieved, and the lower-voltage dc port is able to supply the ac motor independently when $\eta = 0$. When $1 < \varepsilon < 2.5$, the range of the high-voltage dc port power ratio increases with the rise in the port voltage ratio, which means an enhanced output power capability on the high-voltage dc port. When $\varepsilon > 2.5$, the power distribution range decreases with the increase of the port voltage ratio. In the ANPC-type multiport inverter system, a wider power distribution range implies an expanded scope of applicability. Considering this, the port voltage ratio is recommended to be set at 1.5–3 for a wider power distribution range for the ANPC-type multiport inverter system.

Fig. 9(b) shows the power distribution range η versus different modulation indexes m_I. As shown in Fig. 9(b), when the modulation index is set to a small value, the ANPC-type multiport inverter with the proposed scheme can achieve full-range power distribution, and the primary and secondary source units can supply the ac side independently. When $\eta = 0$, the lower-voltage dc port is able to supply the ac motor independently. However, as the modulation index m_I increases, the range of port power distribution decreases. The essential reason is that the degree of freedom provided by the zero-sequence component decreases with the increase of the modulation index m_I. When the modulation index $m_I > 1$, the port power distribution range is limited to a small range. As the modulation index m_I continues to increase, the system will produce an over-modulation effect, introducing numerous harmonics that will affect the power flow control of the system and motor control. Hence, the tradeoff between power distribution range and utilization rate of dc-side voltage should be considered.

IV. Experimental Results

To verify the effectiveness of the proposed dual-layer SVM, an experimental prototype of the ANPC-type multiport inverter was constructed in the laboratory, as shown in Fig. 10. The experimental parameters are listed in Table II. Two programmable dc sources are adopted for dc-port energy sources, where the

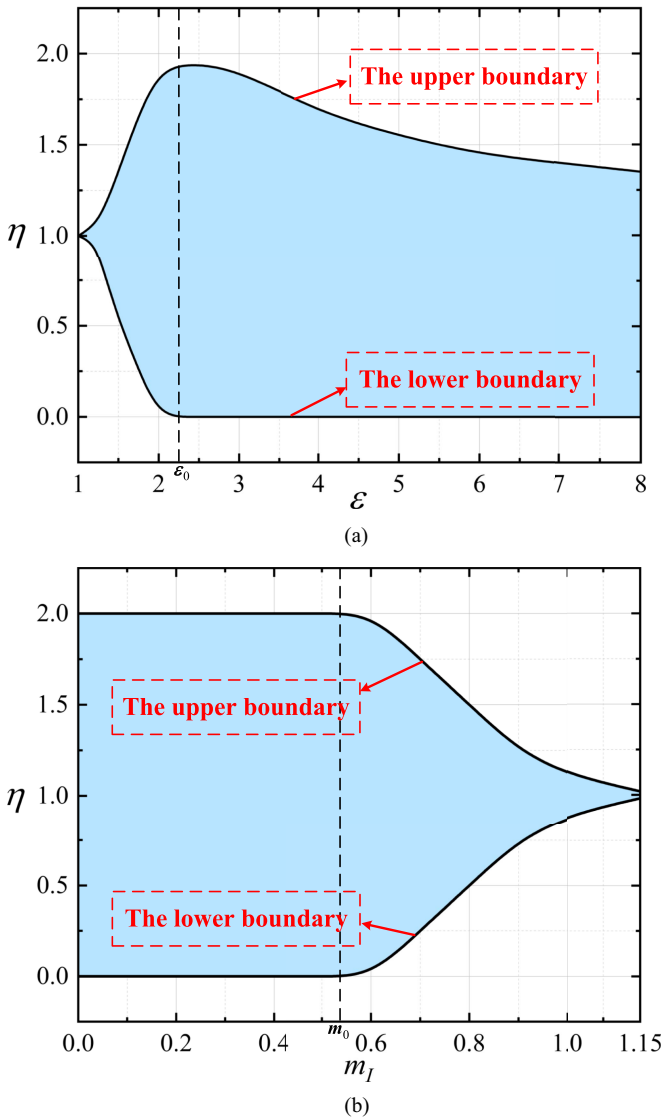

Fig. 9. Theoretical curves of the power distribution range η. (a) Under different voltage ratios ε. (b) Under different modulation indexes m_I.

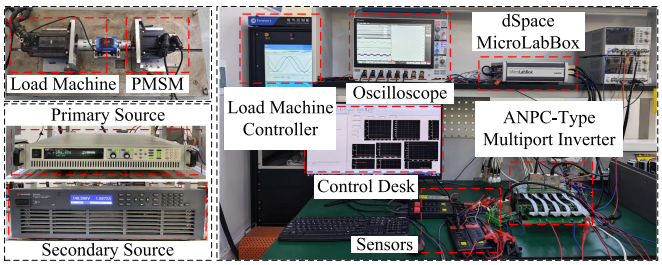

Fig. 10. Experimental test rig.

primary source is used to emulate a high-energy density source, while the secondary source is used to emulate a high-power density source. The voltage of the primary source is chosen as 300 V, and the voltage of the secondary source varies from 125 to 175 V to emulate the scenario of dc-port voltage varying with the state of charge. In addition, a commercial software-driven induction motor can operate in torque mode to simulate loads in practical applications. The digital control functionality was implemented using a dSPACE MicroLabBox DS1202 to generate gate signals for the switches. Rotor speed and position were measured using a 5000-pulse incremental encoder.

TABLE II
SYSTEM PARAMETERS

Parameters	value	Parameters	value
Primary Source voltage	300 V	Secondary Source voltage	125 V∼175 V
Rated power	900 W	Rated torque	8 Nm
Rated speed	1000 r/min	Rated current (RMS)	5 A
Rotor flux	0.41 Wb	Pole pairs	4
Stator inductance	3.54 mH	Stator resistance	2.5 Ω
Sampling period	50 μs	Dead time	1.5 μs

A. Steady-State Performance

The effectiveness of the proposed dual-layer SVM-based power flow control for the ANPC-type multiport inverter is first evaluated through steady-state tests.

1) Steady-State Performance Under Unbalanced Port Voltage: To account for dc source voltage variation in practical scenarios, the proposed scheme is initially evaluated under varying voltage ratios. The steady-state performance of the proposed dual-layer SVM-based power flow control scheme under different voltage ratios is illustrated in Fig. 11, where v_H is fixed at 300 V, and v_L is set to 125, 150, and 175 V, respectively. The experimental results were obtained under rated torque and speed conditions, demonstrating that the proposed scheme achieves satisfactory control performance across varying voltage ratios. As shown, the sinusoidal waveform of the stator current can be observed, and the fundamental-frequency operation of the switching state S_{a1} is also realized in all scenarios. Despite the unbalanced input voltages, the tracking performance of the d- and q-axes current references remains unaffected, indicating that the proposed dual-layer SVM-based power flow control scheme ensures stable and accurate motor drive regulation under varying dc-link voltage conditions.

The differences in the line-to-line voltage v_{ab} under different input voltage conditions are shown in Fig. 15: (a) $v_H = 300$ V, $v_L = 125$ V and (b) $v_H = 300$ V, $v_L = 175$ V. Even under conditions of unequal input voltages, the system maintains precise tracking of the d- and q-axes current references, while the motor continues to operate steadily at its rated speed. The experiment results further indicate that the proposed scheme is effective under variable dc-link voltage. To further evaluate the control performance of the proposed dual-layer SVM across varying voltage ratios, a fast Fourier transformation (FFT) analysis of the stator current was performed, with the resulting harmonic spectrum displayed in Fig. 12. The data, captured at a 1 MHz sampling rate using an oscilloscope and analyzed in MATLAB, reveal that the current THD values are 3.76%, 3.73%, and 3.75% for the tested voltage ratios. It is evident that the total harmonic distortion of phase a current shows negligible variation across these conditions, indicating that the current quality remains stable despite changes in the voltage ratio within a given range.

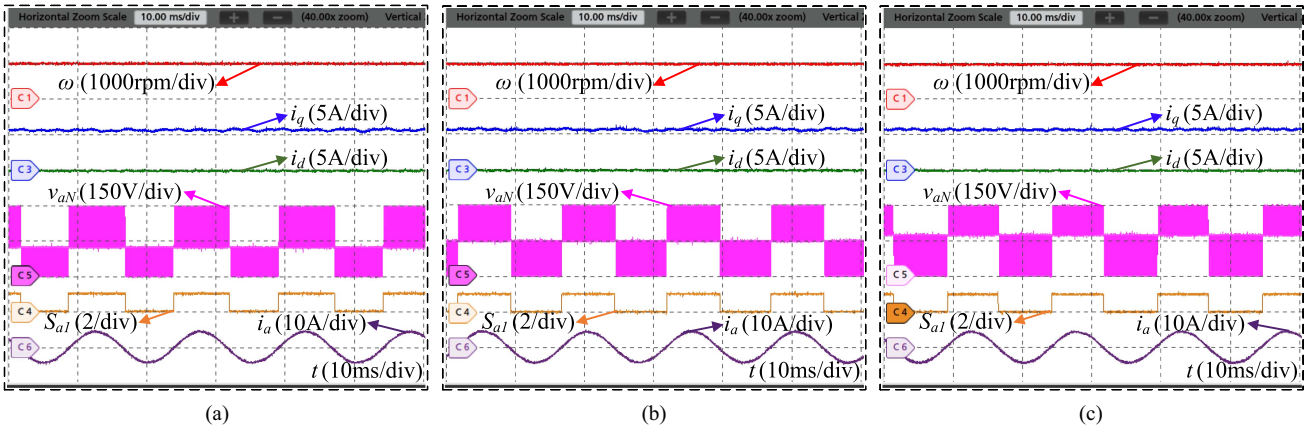

Fig. 11. Steady-state performance of the proposed dual-layer SVM-based power flow control at unbalanced DC links and the rated speed with the rated load torque. (a) $v_H = 300$ V, $v_L = 125$ V. (b) $v_H = 300$ V, $v_L = 150$ V. (c) $v_H = 300$ V, $v_L = 175$ V. From top to bottom, the waveform is rotor speed ω, q-axis current i_q, d-axis current i_d, the switching state of S_{a1}, phase a voltage v_{aN}, and phase a current i_a, respectively.

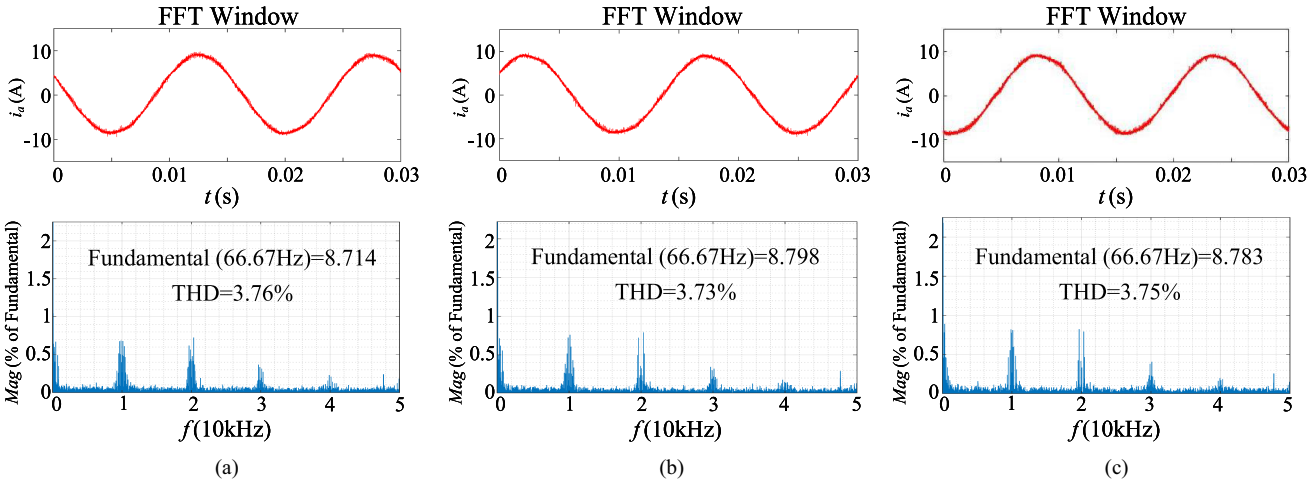

Fig. 12. Phase a current and its harmonics spectrum at unbalanced DC links and the rated speed with the rated load torque. (a) $v_H = 300$ V, $v_L = 125$ V. (b) $v_H = 300$ V, $v_L = 150$ V. (c) $v_H = 300$ V, $v_L = 175$ V.

2) Steady State Performance Under Different Power Flow Scenarios: According to the power supply scenarios of the secondary source, the power supply can be categorized into three scenarios: Primary and secondary source supply together, primary source supply only, and primary source supply power while the secondary source absorbs power. All three scenarios are verified below to verify the power distribution capability of the proposed scheme, as shown in Fig. 13. In the test, the motor operates at rated speed and torque, and the output power is around 900 W. In the first scenario, the desired power of the upper layer P_u^* is set to 600 W, as shown in Fig. 13(a). In the second scenario, the desired power of the upper layer P_u^* is set to 900 W, as shown in Fig. 13(b). In the third scenario, the desired power of the upper layer P_u^* is set to 1200 W, as shown in Fig. 13(c). In scenarios 1–3, the output power of the upper layer can track its references well. In addition, sinusoidal stator current tracking can be observed, and the fundamental frequency operation of the switching state S_{a1} is also realized in all scenarios. It can be concluded that the proposed dual-layer SVM-based power flow control scheme can simultaneously achieve flexible power distribution control and motor drive control, while maintaining the fundamental operation of the LFC.

By decoupling the power demand into high- and low-frequency components, the power management scheme assigns a constant value as the power reference for the primary source. As shown in the analyzed three scenarios, the primary source consistently delivers steady output power, while the secondary source dynamically responds to and tracks high-frequency fluctuations in power demand.

B. Dynamic Performance

The dynamic response of the system when the speed reference changes abruptly from half the rated speed to the full rated speed of 1000 r/min, with the primary source output fixed at 1000 W, is shown in Fig. 14(a). During this transition, the motor

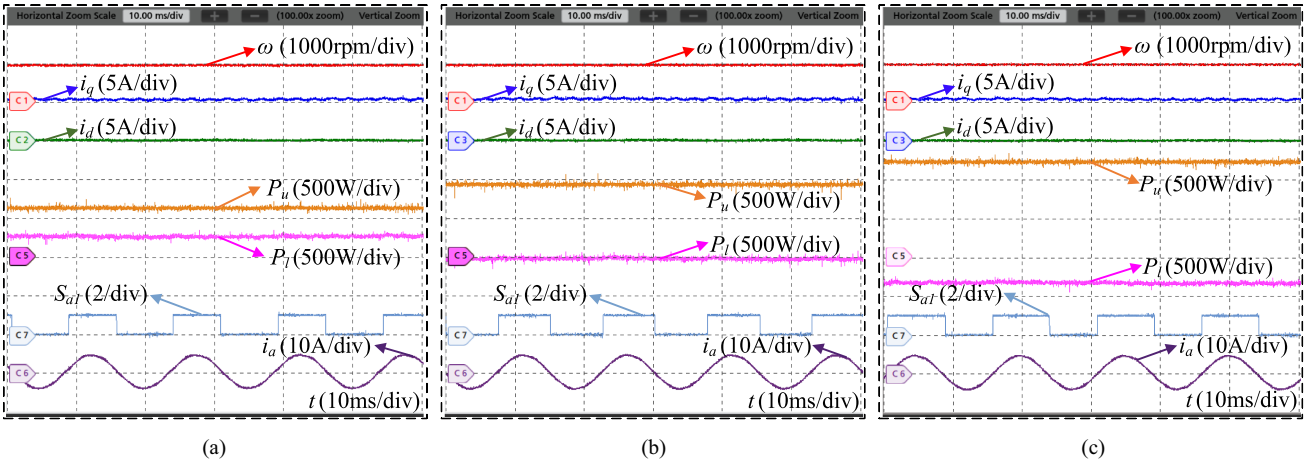

Fig. 13. Steady-state performance of the proposed dual-layer SVM-based power flow control at three power flow modes with the rated speed and rated load torque. (a) $P_u^* = 600$ W. (b) $P_u^* = 900$ W. (c) $P_u^* = 1200$ W. From top to bottom, the waveform is rotor speed ω, q-axis current i_q, d-axis current i_d, the output power of primary and secondary sources P_u and P_l, the switching state of S_{a1} and phase a current i_a, respectively.

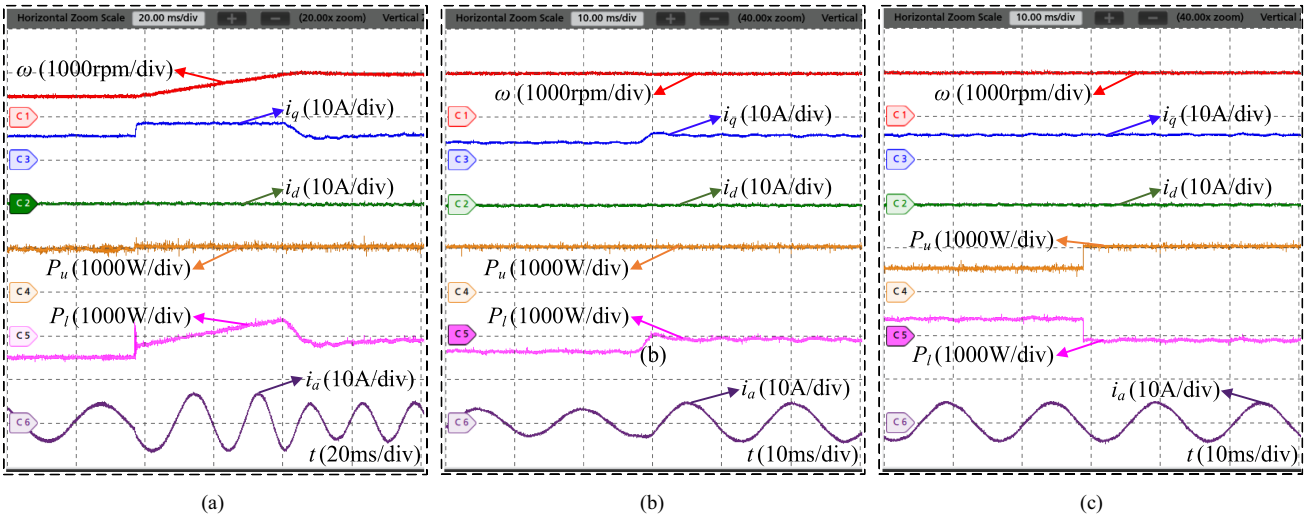

Fig. 14. Dynamic performance of the proposed dual-layer SVM-based power flow control. (a) Speed change from 500 to 1000 r/min at rated torque. (b) Load torque step change from 5 to 8 Nm at rated speed. (c) Port power distribution stepped change with P_u reference stepped from 500 to 1000 W. From top to bottom, the waveform is rotor speed ω, d- and q- axes current, the output power of primary and secondary sources P_u and P_l, and phase a current, respectively.

accelerates with maximum torque, while the primary source maintains a constant power output. Meanwhile, the secondary source dynamically adjusts its power output to accommodate the changing speed. Throughout the process, the d–q currents remain stable, confirming the effectiveness of the proposed dual-layer SVM-based power flow control scheme in handling sudden operating point transitions steadily.

The dynamic response of the system to a step increase in load torque from 5 to 8 Nm, with the rotor operating at a constant rated speed of 1000 r/min, is shown in Fig. 14(b). Despite the torque adjustment, the system maintains stable operation, with well-regulated i_d and i_q currents and consistent rotor speed. The primary source continues to deliver a fixed output, while the secondary source compensates for the increased torque demand by varying its power output. This demonstrates the reliability of the power management strategy during torque variations.

The dynamic response to a step change in the primary source power reference is shown in Fig. 14(c). During this test, conducted at rated speed and torque, the reference power of the primary source is initially set to 500 W and then increased to 1000 W. The primary source adjusts its output power fast within a single control period while the motor drive remains unaffected. These results validate the ability of the proposed dual-layer SVM to perform fast and precise power distribution control under dynamic conditions.

To test the control performance of the proposed dual-layer SVM-based power distribution scheme during significant and rapid changes in the availability of the energy source, dynamic

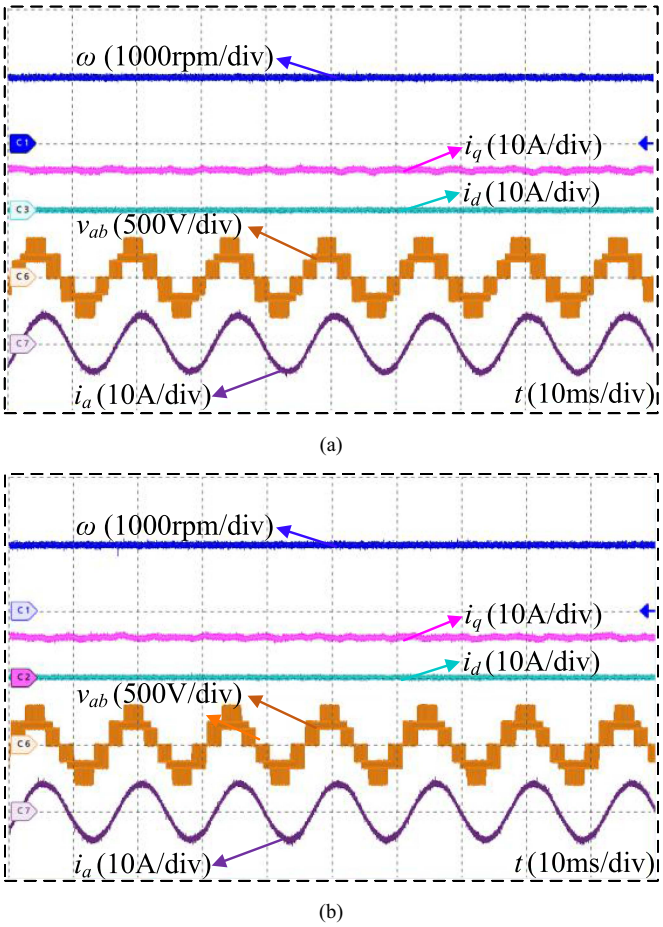

Fig. 15. The line voltages of the proposed structure under unbalanced DC port voltage. (a) $v_H = 300$ V, $v_L = 125$ V. (b) $v_H = 300$ V, $v_L = 175$ V. From top to bottom, the waveform is rotor speed ω, d-axis current i_d, q-axis current i_q, the line voltage v_{ab}, phase a current i_a, respectively.

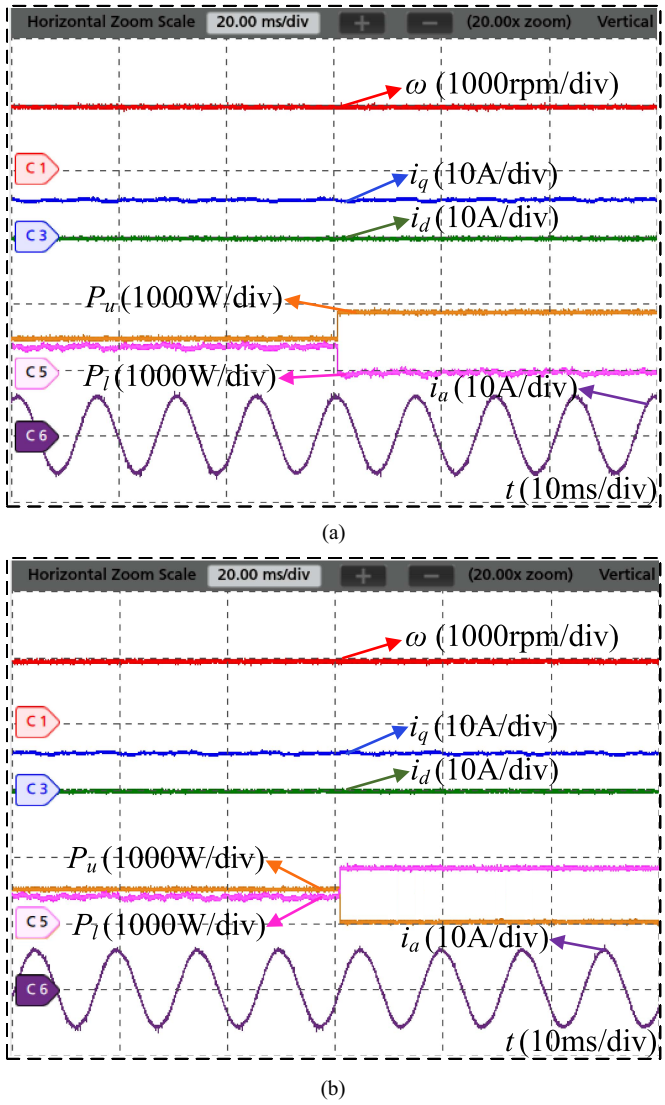

Fig. 16. Dynamic performance under the practical case of the unavailability of one source. (a) Primary source supplies only. (b) Secondary source supplies only. From top to bottom, the waveform is rotor speed ω, d-axis current i_d, q-axis current i_q, the output power of primary and secondary sources P_u and P_l, phase a current i_a, respectively.

experiments under a practical case of unavailability of one source are presented. The dynamic performance changes from the simultaneous supply of the primary source and secondary source to the independent supply of the primary source, as shown in Fig. 16(a). The performance changes to an independent supply of the secondary source, as shown in Fig. 16(b). From the experiment results of Fig. 16, it can be seen that the proposed dual-layer SVM can perform fast and precise power distribution control, while the motor drive remains unaffected during the unavailability of one source in extreme conditions.

C. Power Distribution Range Verification

Based on the analysis in Section III-D, the power distribution range is related to the voltage ratio and modulation index, as shown in (21). To validate the power distribution between the dc sources, the theoretical and experimental tests of the power distribution range for the ANPC-type multiport inverter are illustrated in Figs. 17 and 18, respectively. As shown, the tested experimental results are consistent with the theoretical analysis, which verifies the correctness of the power distribution range analysis. Besides, the voltage ratio ε is suggested to be set around 1.5∼3, while the modulation index is suggested to be set around 0.6∼0.8 to realize a wide power distribution range of the ANPC-type multiport inverter.

D. Comparison With Existing Scheme

To highlight the benefits of the proposed dual-layer SVM-based power distribution control of ANPC-type multiport inverter, a theoretical comparison is carried out against existing power distribution methods used in MEVs, with the findings summarized in Table III. As shown, the strategies outlined in [35], [36], and [37] rely on the NPC-type multiport inverter to achieve flexible power distribution on the dc sides, enabling direct power control through the converters. However, Zhou et al. [35] and Liu et al. [36] introduced extra switching losses with increased switching times in each control period. Zhou et al.

TABLE III
COMPARISON WITH THE EXISTING SCHEMES

Schemes	The type of topology	Total switching times	Power distribution range in dc Sides	Stator current/ Voltage performance	Computational burden	Power conversion efficiency
[35]	NPC	4	Flexible	Medium	Medium	Medium
[36]	NPC	4	Flexible	Medium	Medium	Medium
[37]	NPC	3	Flexible	Good	Large	Medium
[19]	ANPC	3	Fixed	Medium	Medium	Medium
[21]	ANPC	3	Fixed	Medium	Medium	Medium
Proposed	ANPC	3	Flexible	Good	Small	High

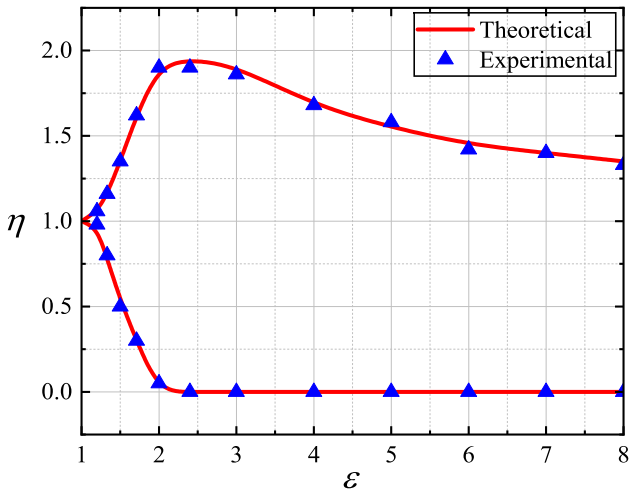

Fig. 17. Curve of the power regulation ratio versus voltage ratio ε at rated torque and speed.

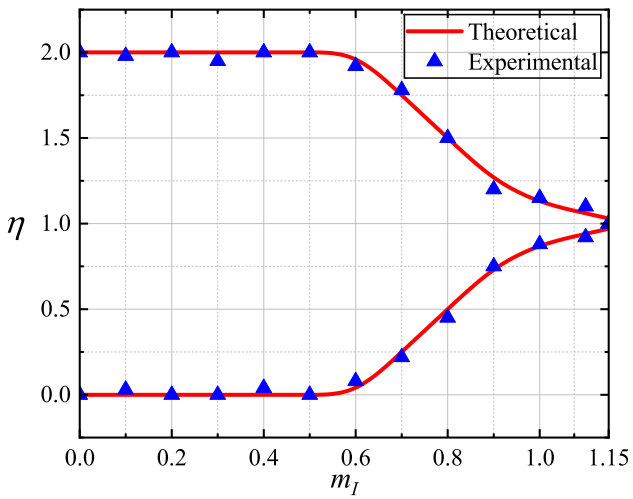

Fig. 18. Curve of the power regulation ratio versus modulation index m_I at rated torque and speed.

[37] inevitably gave rise to the heavy computational burden due to the complex control structure.

On the other hand, the schemes, which rely on the ANPC-type multiport inverters, are outlined in [19] and [21]. The fundamental frequency of the LFC is guaranteed to enhance the power conversion efficiency, while only a balanced dc link voltage is considered. Besides, the flexible power flow control between the dc ports is not available in these methods.

In contrast, the proposed dual-layer SVM-based power flow control scheme provides flexible power flow between the dc ports in an ANPC-type multiport inverter with the fundamental frequency operation of LFC under unbalanced dc-port voltage. It enhances system efficiency through single-stage power conversion and fewer switching times. In addition, the proposed scheme simplifies modulation with direct power flow modeling and decoupled modulation processes, while ensuring the motor drive control.

V. CONCLUSION

This article proposed dual-layer SVM-based power flow control of ANPC-type multiport inverters to simultaneously realize power flow control between the dc sources and motor drive control under the unbalanced dc port voltage. In the proposed scheme, the asymmetrical three-level SVM is decomposed into symmetrical upper-layer and lower-layer SVMs according to the switching state of the low-frequency cell to avoid the dwell time calculation under unbalanced dc-link voltages. Subsequently, direct power control in the upper layer SVM is put forward to achieve the desired power flow control between the dc sources. Besides, the fundamental-frequency operation of the LFC is also guaranteed with the proposed dual-layer SVM, even under unbalanced dc-link voltages. Experimental results on a PMSM-based laboratory prototype verify that the proposed scheme can simultaneously realize power distribution and motor drive control under the unbalanced dc port voltage. In light of these results, the proposed dual-layer SVM-based power flow control scheme can be seen as a promising solution to exploit the full potential of ANPC-type multiport inverters in MEV.

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