Direct Mitigation of Common Mode Current in Transformerless Flexible Interconnection Devices

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***Abstract*—The use of flexible interconnection device (FID) in low-voltage distribution networks results in significant common-mode current (CMC). To overcome these drawbacks, a CMC direct mitigation strategy based on specific average common mode voltage space vector modulation (specific average-CMV SVM) for low-voltage distribution networks in transformerless FID is proposed. First, a common-mode equivalent circuit is established to derive the relationship between the CMC and CMV. Second, a closed-loop CMC mitigation method is proposed. Third, based on the average-CMV during switching cycles, an improved SVM strategy with direct regulation of the average-CMV is proposed by adjusting the duration of zero vector. Furthermore, to overcome the limitations of the average-CMV regulation capability of single converter, a coordinated control method of the average-CMV for both the rectifier and inverter is proposed, which expands the CMC mitigation capability for the FID system. Finally, simulations and experimental results demonstrate the effectiveness of the proposed method.**

***Index Terms*—Common mode current (CMC), space vector modulation (SVM), transformerless flexible interconnection device (FID).**

I. Introduction

THE incorporation of flexible interconnection devices (FIDs) into distribution networks presents an effective technical approach for improving system reliability, scalability, flexibility, and redundancy, while also facilitating renewable energy integration and optimal utilization of distributed generation resources [1]. Transformerless FIDs, distinguished by their compact dimensions and lightweight construction, offer a viable solution for this application. Nevertheless, transformerless FIDs encounter the challenge of common mode current (CMC), which has the potential to induce significant common mode electromagnetic interference, thereby disrupting the proper functioning of adjacent control systems and electronic equipment [2], [3]. Furthermore, excessive CMC amplitudes may trigger protective circuit malfunctions, inadvertent relay trips, and system outages, thereby compromising the safety and operational reliability of power distribution systems. The adverse effects of CMC have prompted substantial research efforts across academia and industry to develop effective mitigation and elimination strategies.

Significant research efforts have been devoted to CMC mitigation in FID systems, primarily through two approaches: hardware-based solutions [4] and improved software control strategies [5].

Passive common-mode filters, utilizing components such as common-mode chokes [6], [7], [8], [9] and LCR filter [10], [11], [12], demonstrate effective CMC suppression across wide frequency ranges. Alternative approaches integrating additional hardware circuits with energy storage systems [13] have also been explored, where the common mode voltage (CMV) is harnessed to charge the energy storage units. However, as a passive mitigation method, conventional filter-based solutions exhibit limited effectiveness. To address these constraints, active CMC suppression strategies have been proposed, including active CMV reduction filters [8], [14], [15] and fourth-leg compensation techniques [16], [17]. Active CMV reduction filters operate by injecting phase-opposed CMVs to neutralize original CMVs, thereby reducing CMC impacts. These active methods demonstrate superior CMC mitigation capabilities compared to passive approaches. The fourth-leg compensation method introduces an additional bridge leg to conventional three-phase converters, combined with a four-phase *LC* filter, enabling zero neutral-to-ground voltage output and effectively eliminating inherent CMV issues in traditional modulation schemes. Nevertheless, active CMV suppression strategies generally require extra computational and control circuitry, which may compromise system efficiency. In summary, hardware-based CMC mitigation strategies inevitably demand supplementary circuits that increase system complexity, physical dimensions, and implementation costs.

Unlike hardware-based solutions, the software-based CMC mitigation strategy eliminates the requirement for auxiliary circuits, offering superior cost-efficiency and adaptability. This makes it a promising approach for reducing or eliminating CMV to achieve effective CMC mitigation. Various CMV suppression methods have been proposed, including RSPWM, AZSPWM1, NSPWM, and AZSPWM3 [18], [19], [20], [21]. The underlying principle involves replacing zero vectors with nonzero vectors, as zero vectors are associated with higher CMV compared to non-zero vectors. Consequently, this modulation technique can effectively reduce the amplitude of the output CMV. Applying this strategy to back-to-back converters can further mitigate the impact of CMC [22]. However, for FID, the CMC is determined

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by the difference of the CMVs between the rectifier and inverter. The aforementioned CMV reduction methods primarily focus on reducing CMV values in individual converters. As a consequence, these approaches exhibit limited CMC mitigation effectiveness. as fail to consider the CMV difference between rectifier and inverter.

To overcome these limitations, research has been conducted on CMV suppression in back-to-back "double bridge" or "rectifier/inverter" circuits within motor drive systems. In [23], a strategy is proposed to minimize CMV by coordinating the vector switching sequences of the rectifier and inverter. In [24], a method is introduced to reduce CMV and leakage current by aligning the active voltage vectors of the inverter with those of the rectifier. In [25], a technique is presented to lower CMV by selecting different zero-space vectors based on the voltage difference between the dc-link midpoint and the ground. Additionally, [26] proposes a space vector modulation (SVM) strategy that synchronizes the odd/even vectors or zero vectors of the rectifier and inverter to reduce system CMV. In [27], a method that reduces the CMV of a rectifier/inverter system by modifying the distribution of the zero-voltage vector is proposed. However, this method only reduces the peak value of the CMV difference between the rectifier and inverter. In [28] and [29], an edge-aligned modulation technique to suppress leakage current in the back-to-back converter has been proposed. However, this method can only achieve effective leakage current suppression under certain constraint conditions and requires strict alignment of the pulse signals within the switching period. Moreover, the shifting of PWM pulses introduces asymmetry within each carrier period, resulting in increased system harmonics and a degradation of current quality.

Additionally, research has extended traditional SVM by introducing a zero-sequence axis, forming a three-dimensional SVM (3D-SVM), and applied it to CMC mitigation. In [29], a 3D-SVM method was proposed for a three-wire four-phase active power filter, addressing the limitation of traditional SVM method in handling neutral line current (zero-sequence component). In [30], a 3D-SVM technique was introduced, which flexibly adjusts the zero-voltage vector duration based on the active vector duration time, ensuring zero-sequence voltage balance over a switching cycle and thereby reducing CMV impact. In [31], a zero-sequence current mitigation strategy was proposed for an open-end winding permanent magnet synchronous generator system. This strategy integrates 3D-SVM to mitigate zero-sequence current issues caused by single dc bus supply. However, 3D-SVM typically involves complex procedures such as three-dimensional sector division, tetrahedron identification, and synthesis vector selection, making its implementation more intricate compared to traditional SVM modulation strategies.

Existing methods primarily passively mitigate the CMC by reducing the CMV in rectifier/inverter system. To solve the problem, this article proposed a novel closed-loop active method for CMC mitigation. First, the common-mode equivalent current is established, and based on the mechanism of CMC generation, the relationship between the CMC and CMV is derived. Then, a closed-loop CMC mitigation method based on average-CMV direct regulation is proposed, which enables unified control and modulation of differential mode and common mode signals. In addition, considering the different voltages of the distribution networks, to overcome the limitations of single converter control, a coordinated control method for the average-CMV of both the rectifier and inverter is proposed, which expands the regulation range of average-CMV for the FID system.

II. Mechanism of CMC Generation in Transformerless FID

Transformerless FID implementation in low-voltage distribution networks has gained significant research interest. As illustrated in Fig. 1, FIDs serve as critical interfaces between distribution networks with high renewable energy penetration and concentrated intensive loads. The FID comprises a co-located rectifier and inverter, with R denoting the equivalent impedance between grounding points GND_1 and GND_2 [32]. The dc-link is characterized by capacitance C_{dc} and V_{dc}, while C, L_1, and L_2 represent the filter capacitance, converter-side inductance, and grid-side inductance, respectively. The current references in the dq rotating frame for the rectifier are denoted as i_d^{ref} and i_q^{ref}. The rectifier and inverter output currents are expressed as $i_{r,abc}$ and $i_{i,abc}$, respectively, while $v_{g1,abc}$ and $v_{g2,abc}$ represent the three-phase voltages of distribution networks 1 and 2, with corresponding phase angles θ_1 and θ_2. The active and reactive power references are designated as P_{ref} and Q_{ref}. The switching states of the six power devices in three-phases are represented by S_{x1}, S_{x3}, and S_{x5}, where x indicates r (rectifier) or i (inverter). The proposed control scheme includes the traditional differential mode current controller for the rectifier and inverter [2], [33], as well as direct mitigation control of CMC. Given the operational symmetry between the rectifier and inverter in the back-to-back FID configuration, this article primarily focuses on the rectifier analysis, with the derived principles being equally applicable to the inverter side, thereby establishing a comprehensive understanding of the FID system.

The three-phase output voltage of the rectifier can be expressed as

$$\begin{cases} v_{ao} = S_{r1}V_{\mathrm{dc}} - 0.5V_{\mathrm{dc}} \\ v_{bo} = S_{r3}V_{\mathrm{dc}} - 0.5V_{\mathrm{dc}} \\ v_{co} = S_{r5}V_{\mathrm{dc}} - 0.5V_{\mathrm{dc}} \end{cases} \tag{1}$$

where v_{ao}, v_{bo}, and v_{co} represent the three-phase output voltages of the rectifier. The switching states S_{r1}, S_{r3}, and S_{r5} determine the conduction status of the power devices: when set to 1, the corresponding upper switches are in the conducting state while the lower switches remain OFF; conversely, when set to 0, the upper switches are non-conducting and the lower switches are activated.

The CMV of the FID is mathematically defined as the difference between the rectifier and inverter terminals

$$\begin{aligned} v_{\mathrm{cm}} &= v_{\mathrm{cm}r} - v_{\mathrm{cm}i} \\ &= \left(v_{ao} + v_{bo} + v_{co} - v_{uo} - v_{vo} - v_{wo}\right)/3 \end{aligned} \tag{2}$$

where v_{uo}, v_{vo}, and v_{wo} denote the three-phase output voltages of the inverter, and v_{cm} represents the CMV of the FID. The

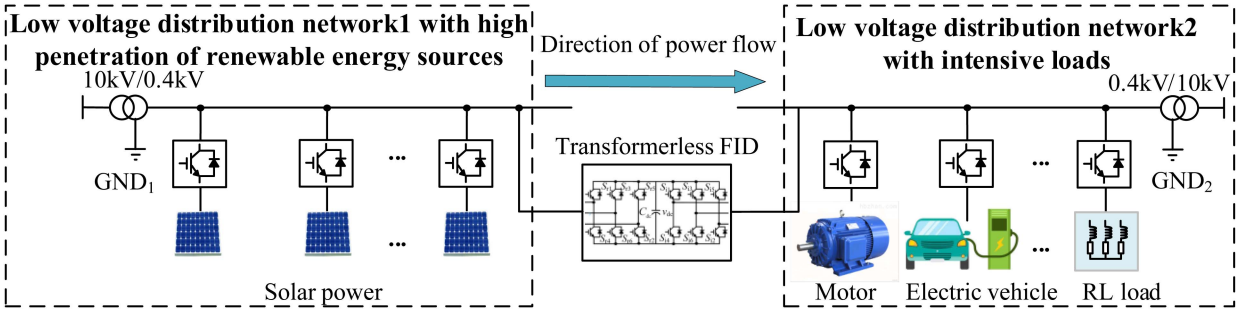

Fig. 1. Schematic of FID installation and operation in distribution networks.

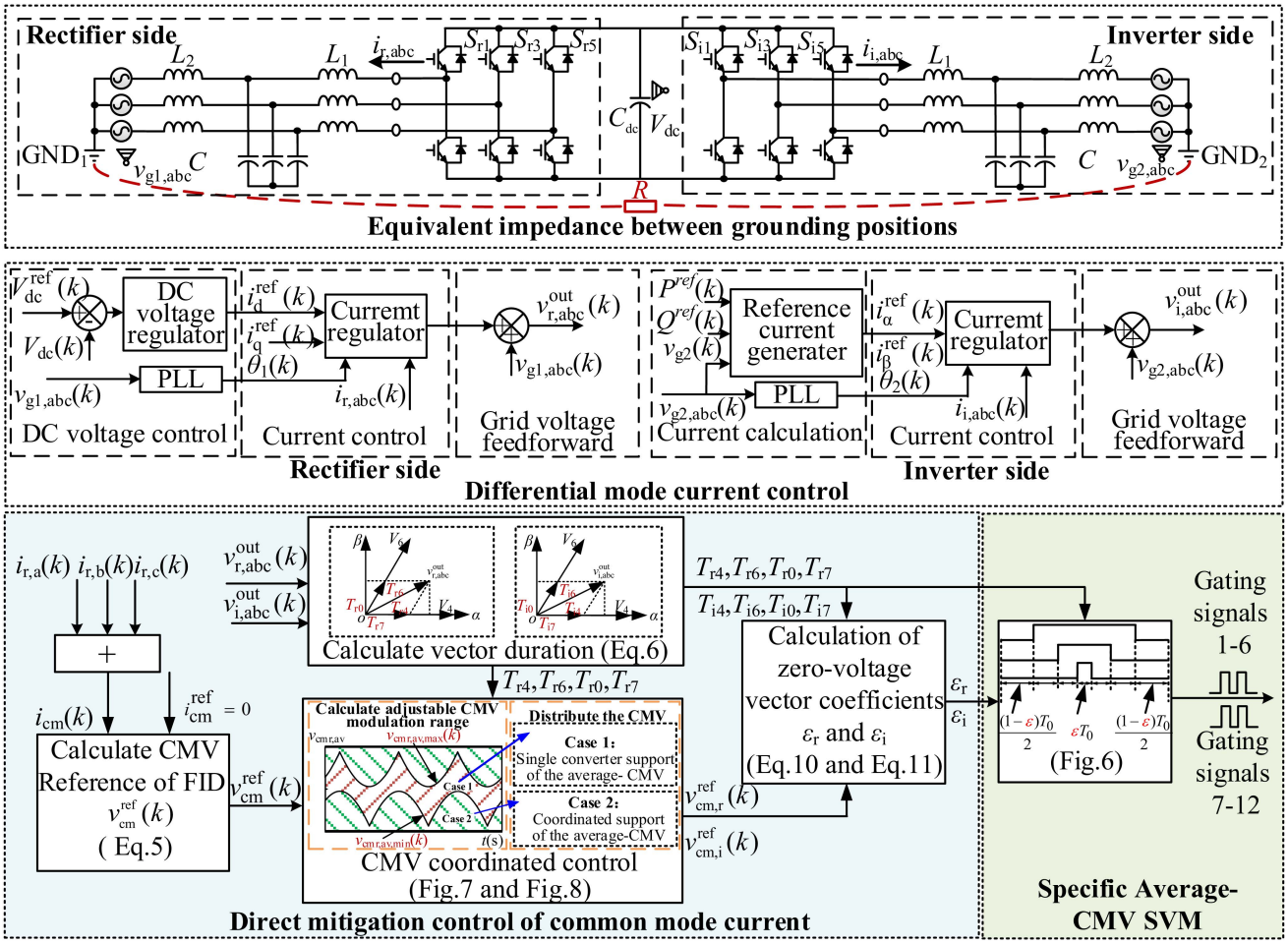

Fig. 2. Structure and control block diagram of the proposed method for transformerless FID.

variables $v_{\mathrm{cm}r}$ and $v_{\mathrm{cm}i}$ represent the CMV of the rectifier and inverter, respectively.

The CMV of the FID is primarily generated by the distinct switching patterns of the rectifier and inverter. Consequently, the CMC is determined by the CMV excitation characteristics and the impedance of the common-mode loop.

The converters in the FID system are modeled as equivalent pulse voltage sources, as illustrated in Fig. 3(a), where $v_{r,abc}$ and $v_{i,abc}$ denote the three-phase output voltages of the rectifier and inverter, respectively. To facilitate theoretical analysis, the simplified circuit is subsequently transformed into differential-mode ($\alpha\beta$-axis) and common-mode (γ-axis) equivalent circuits, depicted in Fig. 3(b) and (c), respectively. The relationship between CMC and CMV is passively determined by the circuit characteristics, independent of control and modulation strategies. The Bode plots of the common-mode loop impedance is shown in Fig. 4. It can be observed that the system exhibits high impedance characteristics in the high-frequency range and low impedance in the low-frequency range. Therefore, particular attention should be given to the low-frequency characteristics of the CMV.

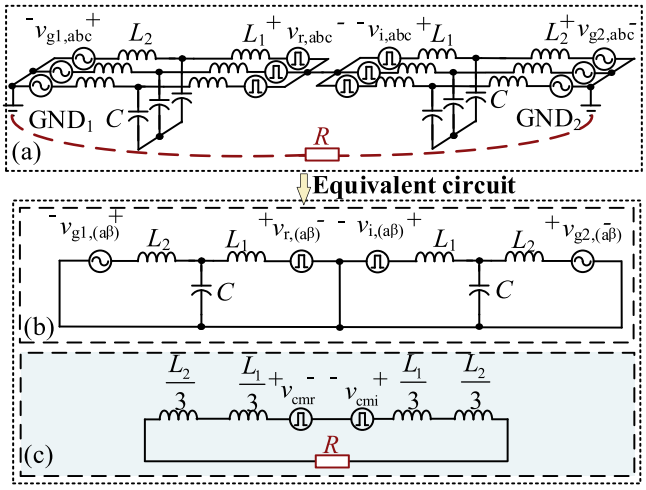

Fig. 3. Equivalent circuit of the transformerless FID. (a) Equivalent circuit under the abc axis. (b) equivalent circuit under the $\alpha\beta$-axis. (c) The Equivalent circuit under the γ-axis.

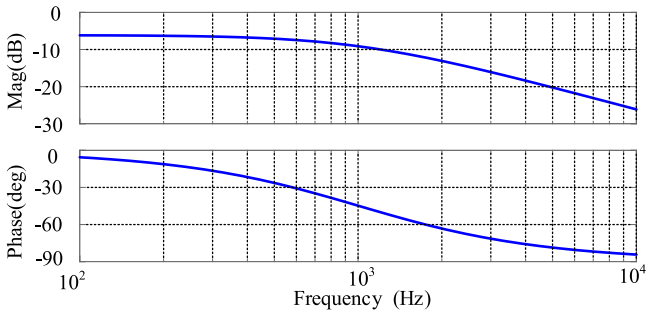

Fig. 4. Bode plot of the common-mode loop impedance of the transformerless FID.

III. Proposed Direct Mitigation of CMC in Transformerless FID

A. System Operation Controller

As shown in Fig. 2, the differential-mode circuit is analyzed separately for both the rectifier and the inverter. For the rectifier, the control architecture employs a dual-loop structure: an outer dc voltage loop utilizing a proportional-integral controller, and an inner current loop based on a proportional-resonant (PR) controller. Similarly, the inverter controller features a reference current generation module and a PR-based current control loop.

The direct CMC mitigation strategy comprises three key components: closed-loop control of CMC for CMV reference generation; the proposed Specific Average-CMV SVM technique; and coordinated average-CMV control of rectifier and inverter. The proposed control and modulation strategy enables unified control and modulation of both differential-mode and common-mode components. The comprehensive implementation details of the system operation controller will be elaborated in subsequent subsections.

B. Proposed Direct Mitigation of CMC Controller

Considering the superior dynamic response characteristics of deadbeat control, this article implements a deadbeat controller for CMV reference calculation within the closed-loop CMC control scheme.

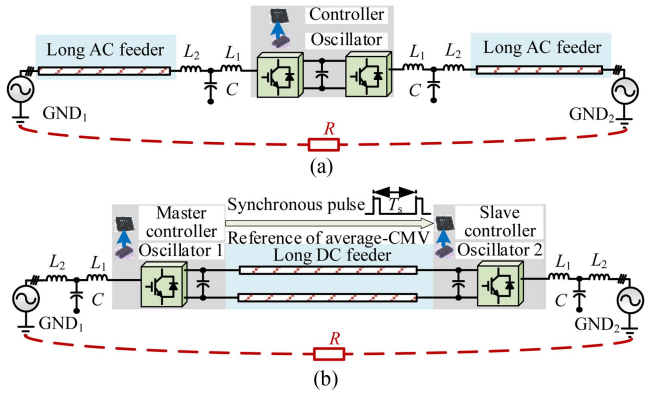

Fig. 5. Structure of synchronization implementation for two types of FID controllers. (a) Structure with long AC feeders, (b) structure with long DC feeders.

The common-mode equivalent circuit illustrated in Fig. 3(c) can be mathematically modeled and theoretically analyzed through

$$\begin{cases} i_{\rm cm} = i_{r,a} + i_{r,b} + i_{r,c} \\ v_{\rm cmr} - v_{\rm cmi} = \frac{2(L_1+L_2)}{3}\frac{di_{\rm cm}}{dt} + i_{\rm cm}R \end{cases}. \tag{3}$$

Based on the first-order forward Euler discretization method, the discrete-time representation of CMC in the FID system is expressed as:

$$v_{\rm cmr}(k) - v_{\rm cmi}(k) = \frac{2(L_1+L_2)}{3}\frac{i_{\rm cm}(k+1) - i_{\rm cm}(k)}{T_s} + i_{\rm cm}(k)R \tag{4}$$

where T_s is the sampling period.

From (4), the method proposed in this article requires a synchronized operation and a coordinated controller. In the control system, the oscillator frequency of each controller determines the timing sequence of individual converters. Given the intrinsic limitations of oscillator accuracy, multicontroller systems require synchronized operation and coordinated control to achieve phase alignment of digital carrier signals. The FID system accommodates two distinct interconnection schemes. When the structure shown in Fig. 5(a) is used, the FID achieves flexible interconnection between two distribution networks via a long ac feeder. In this case, since the rectifier and inverter are located close to each other, a single controller can be used to manage control, facilitating synchronized operation and coordinated control between the rectifier and inverter. On the other hand, when the structure shown in Fig. 5(b) is employed, the FID is interconnected through long dc feeders between the rectifier and inverter. In this scenario, the rectifier and inverter are located farther apart, and two controllers are typically used to separately control the rectifier and inverter. In such cases, it is necessary for the master controller to send synchronization signals to the slave controller to achieve synchronized operation and coordinated control of the rectifier and inverter.

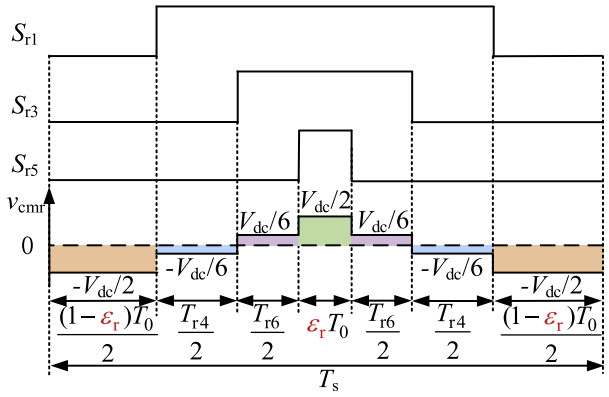

Fig. 6. Switching sequence pattern and corresponding CMV.

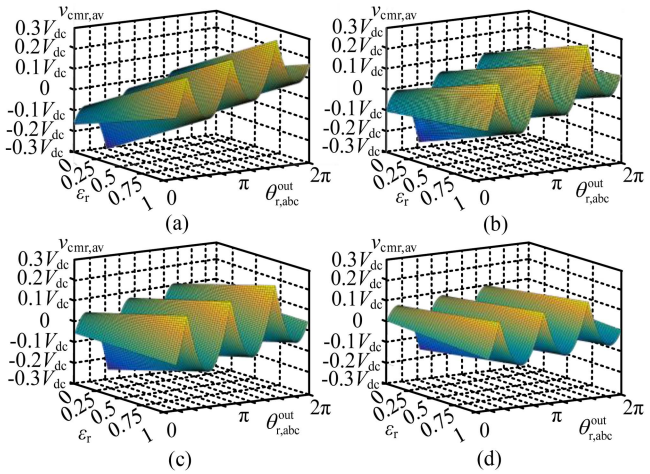

Fig. 7. Average-CMV under different zero vector distribution coefficients ε_r. (a) $m_a = 0.7$. (b) $m_a = 0.8$. (c) $m_a = 0.9$. (d) $m_a = 1.0$.

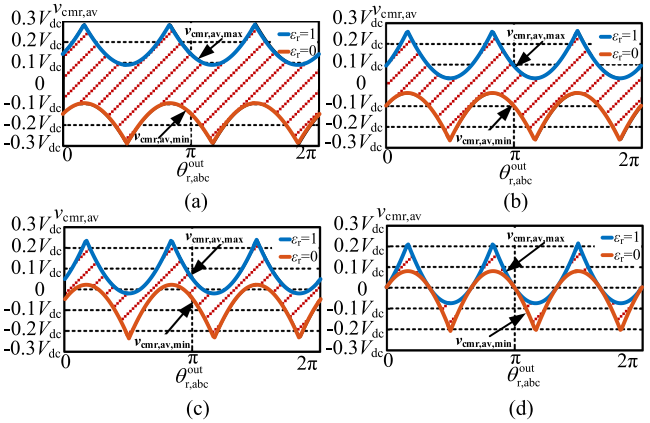

Fig. 8. Modulation range of the average-CMV. (a) $m_a = 0.7$. (b) $m_a = 0.8$. (c) $m_a = 0.9$. (d) $m_a = 1.0$.

The primary objective of CMC mitigation is to achieve zero CMC at the (k+1)th sampling instant. The required CMV reference for the FID at the kth time step is given by

$$v_{\mathrm{cm}}^{\mathrm{ref}}(k) = v_{\mathrm{cm}r}(k) - v_{\mathrm{cm}i}(k) = \left(R - \frac{2(L_1+L_2)}{3T_s}\right) i_{\mathrm{cm}}(k). \quad (5)$$

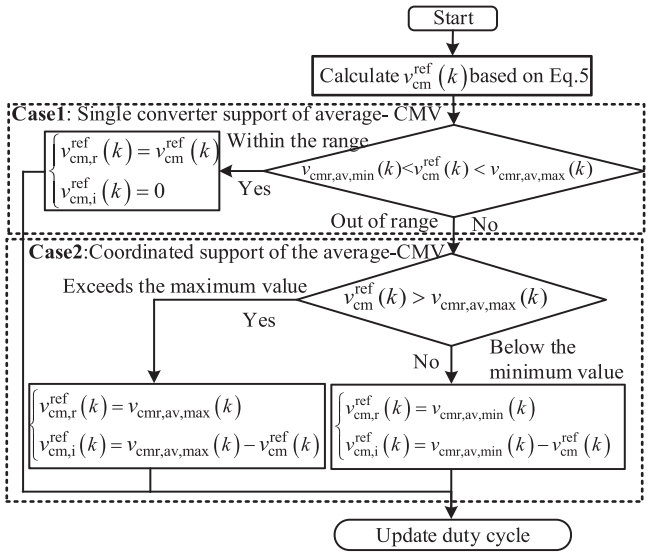

Fig. 9. Flowchart of coordinated control of average-CMV for FID both-side converters.

C. Proposed Specific Average-CMV SVM

A novel specific average-CMV SVM is proposed that enables direct regulation of the average-CMV. The improved seven-segment SVM simultaneously satisfies the area balance principle for both common-mode and differential-mode components.

The conventional seven-segment SVM technique synthesizes the reference voltage vector through optimal combination of two active vectors and two zero vectors. Considering the rectifier-side reference voltage vector in sector I as a representative case, the duration for each basic vector is given as

$$\begin{cases} T_{r4} = \sqrt{3}\left(\sqrt{3}v_{r\alpha} - v_{r\beta}\right) T_s/2/V_{\mathrm{dc}} \\ T_{r6} = \sqrt{3}v_{r\beta}T_s/2/V_{\mathrm{dc}} \\ T_0 = T_s - T_{r4} - T_{r6} \\ T_{r0} = T_{r7} = 0.5T_0 \end{cases} \quad (6)$$

where T_{r4}, T_{r6}, T_{r0}, and T_{r7} denote the durations of voltage vectors V_{r4}, V_{r6}, V_{r0}, and V_{r7}, respectively. The T_0 represents the total duration of zero vectors within one switching period T_s. The variables $v_{r\alpha}$ and $v_{r\beta}$ correspond to the $\alpha\beta$-axis components of the rectifier output voltage $v^{\mathrm{out}}_{r,abc}$.

Table I summarizes the output voltage characteristics and their corresponding α, β, and common mode components for all eight switching states. Based on the equal area principle, the concept of average-CMV is introduced. The average-CMV for one switching period T_s can be derived as shown in

$$v_{\mathrm{cm}r,\mathrm{av}} = V_{\mathrm{dc}}\left(\left(T_{r6} - T_{r4}\right) + 3\left(T_{r7} - T_{r0}\right)\right)/6/T_s. \quad (7)$$

Zero voltage vectors V_{r0} and V_{r7} exhibit identical differential-mode characteristics while demonstrating distinct common-mode behaviors. As evidenced by (7), the utilization of redundant zero vectors introduces an additional degree of freedom for CMV control.

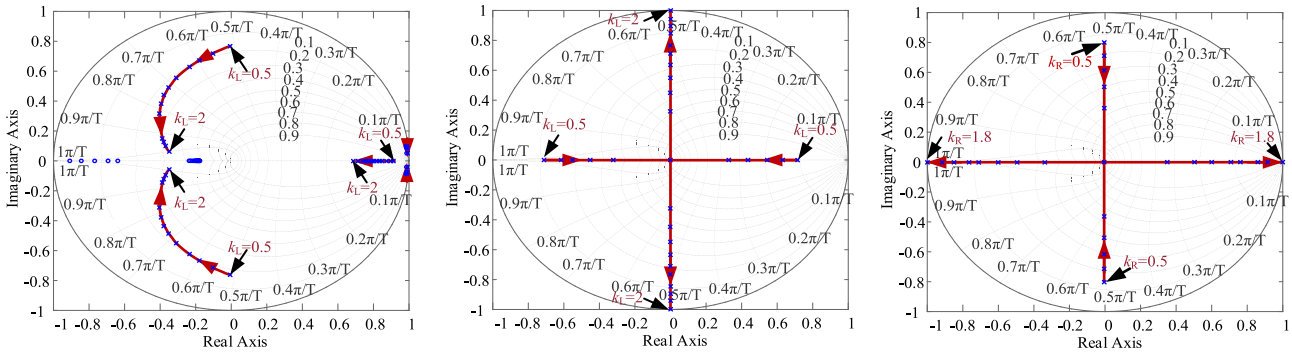

Fig. 10. Root loci of the system when the physical inductances and resistance of the transformerless FID system change of the nominal value. (a) DMC loop based on the PR controller when the physical inductances L_1 and L_2 change. (b) CMC loop based on the proposed deadbeat controller when the physical inductances L_1 and L_2 change. (c) CMC loop based on the proposed deadbeat controller when the physical resistance R changes.

TABLE I
VOLTAGE COMPONENTS FOR DIFFERENT SWITCHING STATES

S_{r1}	S_{r3}	S_{r5}	Vector	$v_{r\alpha}$	$v_{r\beta}$	v_{cmr}
0	0	0	Vr_0	0	0	$-1/2V_{dc}$
1	0	0	Vr_4	$2/3V_{dc}$	0	$-1/6V_{dc}$
1	1	0	Vr_6	$1/3V_{dc}$	$\sqrt{3}/3V_{dc}$	$1/6V_{dc}$
0	1	0	Vr_2	$-1/3V_{dc}$	$\sqrt{3}/3V_{dc}$	$-1/6V_{dc}$
0	1	1	Vr_3	$-2/3V_{dc}$	0	$1/6V_{dc}$
0	0	1	Vr_1	$-1/3V_{dc}$	$-\sqrt{3}/3V_{dc}$	$-1/6V_{dc}$
1	0	1	Vr_5	$1/3V_{dc}$	$-\sqrt{3}/3V_{dc}$	$1/6V_{dc}$
1	1	1	Vr_7	0	0	$1/2V_{dc}$

The zero vector distribution coefficient, denoted as ε_r, is defined as the ratio of the duration of zero vector V_{r7} to the total zero vector duration T_0 within one switching period T_s

$$\varepsilon_r = \frac{T_{r7}}{T_0}. \tag{8}$$

Consequently, the relationship between the average-CMV and ε_r can be established as

$$v_{cmr,av} = \left(\frac{(2\varepsilon_r - 1)T_0}{2} + \frac{T_{r6} - T_{r4}}{6}\right)\frac{V_{dc}}{T_s}. \tag{9}$$

Based on (9), zero vector distribution coefficient, ε_r, is expressed as

$$\varepsilon_r = \frac{1}{T_0}\left(\frac{v_{cmr,av}T_s}{V_{dc}} - \frac{T_{r6} - T_{r4}}{6}\right) - \frac{1}{2}. \tag{10}$$

The three-phase switching states and their corresponding output CMV are shown in Fig. 6.

Similarly, zero vector distribution coefficient for the inverter, ε_i, is defined by

$$\varepsilon_i = \frac{1}{T_0}\left(\frac{v_{cmi,av}T_s}{v_{dc}} - \frac{T_{i6} - T_{i4}}{6}\right) - \frac{1}{2}. \tag{11}$$

The relationship between the average-CMV $v_{cmr,av}$ and zero vector distribution coefficient ε_r for modulation index m_a of 0.7, 0.8, 0.9, and 1.0 is shown in Fig. 7. It can be clearly seen that the average-CMV of the converter within a cycle under the proposed specified average-CMV SVM modulation strategy can be effectively adjusted by varying the zero vector distribution coefficients ε_r. For the same modulation index m_a and fundamental frequency phase angle $\theta^{out}_{r,abc}$, the average CMV increases with the increase of the zero vector distribution coefficients ε_r.

For $\varepsilon_r = 0$, the average-CMV $v_{cmr,av}$ attains the minimum value $v_{cmr,av,min}$, while for $\varepsilon_r = 1$, $v_{cmr,av}$ achieves the maximum value $v_{cmr,av,max}$, as expressed in

$$\begin{cases} v_{cmr,av,min} = \left(\frac{T_{r6}-T_{r4}}{6} - \frac{T_0}{2}\right)\frac{V_{dc}}{T_s} \\ v_{cmr,av,max} = \left(\frac{T_{r6}-T_{r4}}{6} + \frac{T_0}{2}\right)\frac{V_{dc}}{T_s} \end{cases}. \tag{12}$$

Based on (12), The minimum and maximum average-CMV for a modulation index $m_a = 0.7, 0.8, 0.9$, and 1.0 at $\varepsilon_r = 0$ and $\varepsilon_r = 1$ is shown in Fig. 8. The range between $v_{cm,av,max}$ and $v_{cm,av,min}$ defines the adjustable regulation range of average-CMV, indicating that the adjustable range of average-CMV gradually decreases as the modulation index m_a increases.

D. Coordinated Control of Average-CMV

Considering the regulation limit of the average-CMV for a single converter, using only a single converter to support the average-CMV reference of FID may cause the regulation to enter an overmodulation region. To overcome these limitations, a coordinated control method for the average-CMV of both the rectifier and inverter is proposed, where the average-CMV of both the rectifier and inverter are used together to fully utilize the freedoms of the average-CMV regulation capability.

The proposed coordinated average-CMV controller prioritizes rectifier-side adjustment based on the relationship between the average-CMV reference v^{ref}_{cm} and the rectifier average-CMV boundaries ($v_{cmr,av,min}$ and $v_{cmr,av,max}$), and is implemented through two distinct operational cases, with the control flowchart shown in Fig. 9.

1) Case 1. Single Converter Average-CMV Support Mode: When the FID average-CMV reference v^{ref}_{cm} falls within the

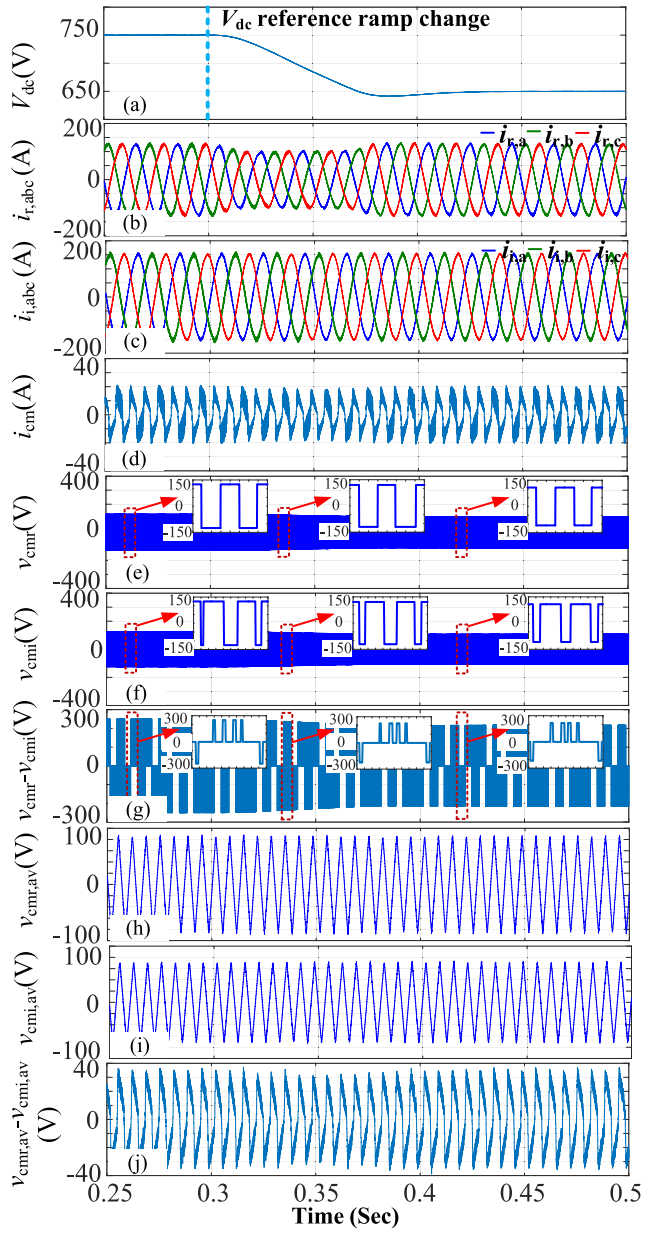

Fig. 11. Performance of the system using AZSPWM. (a) DC voltage. (b) Grid-side current of the rectifier. (c) Grid-side current of the inverter. (d) CMC of the FID. (e) CMV of the rectifier. (f) CMV of the inverter. (g) CMV difference between rectifier and inverter. (h) average-CMV of the rectifier. (i) Average-CMV of the inverter. (j) Average-CMV of the FID.

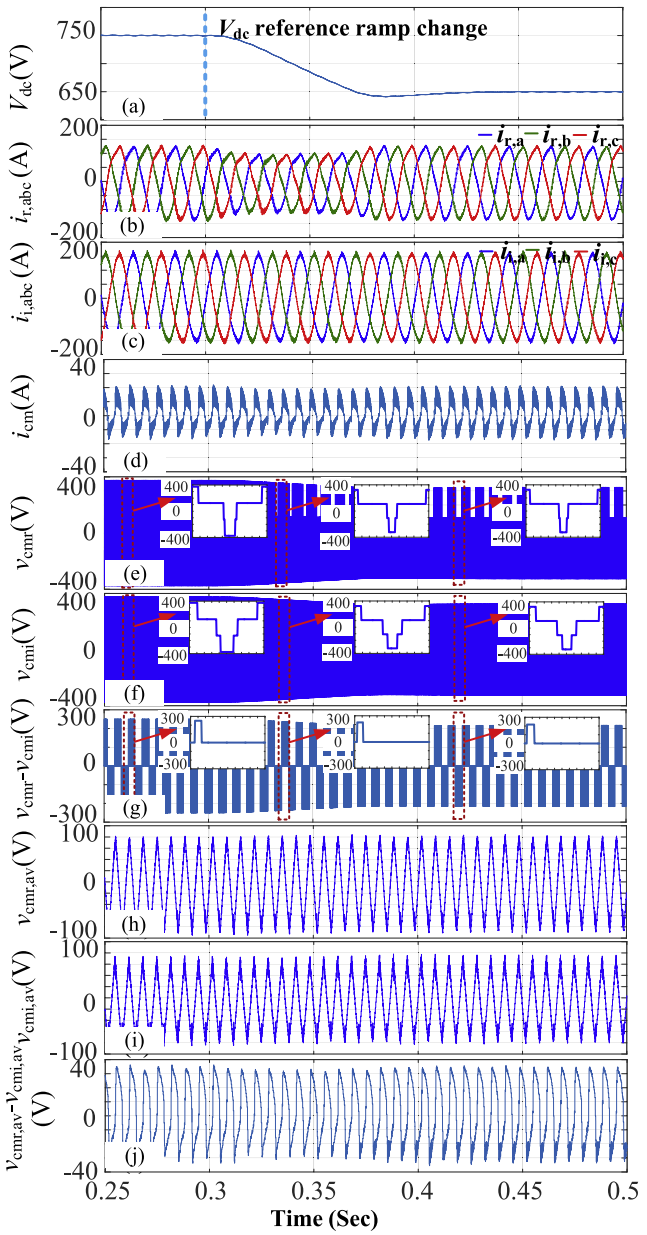

Fig. 12. Performance of the system using the method in [28] and [29]. (a) DC voltage. (b) Grid-side current of the rectifier. (c) Grid-side current of the inverter. (d) CMC of the FID. (e) CMV of the rectifier. (f) CMV of the inverter. (g) CMV difference between rectifier and inverter. (h) Average-CMV of the rectifier. (i) average-CMV of the inverter. (j) Average-CMV of the FID.

adjustable range of average-CMV for the rectifier, satisfying $v_{\mathrm{cm}r,\mathrm{av},\min} \le v_{\mathrm{cm}}^{\mathrm{ref}} \le v_{\mathrm{cm}r,\mathrm{av},\max}$, the FID average-CMV is supported by the rectifier. In this case, the rectifier average-CMV reference is set as $v_{\mathrm{cm},r}^{\mathrm{ref}} = v_{\mathrm{cm}}^{\mathrm{ref}}$, while the inverter average-CMV reference is maintained at $v_{\mathrm{cm},i}^{\mathrm{ref}} = 0$. In this case, synchronized operation between the rectifier and inverter is required, without the need for coordinated control of the average-CMV reference.

2) Case 2. Coordinated Support of the Average-CMV Mode: When the FID average-CMV reference $v_{\mathrm{cm}}^{\mathrm{ref}}$ exceeds the adjustable range of rectifier, requiring synchronized operation and coordinated control between the rectifier and inverter, the following control strategy is implemented as follows: for the condition $v_{\mathrm{cm}}^{\mathrm{ref}} > v_{\mathrm{cm}r,\mathrm{av},\max}$, the average-CMV reference for rectifier is set to $v_{\mathrm{cm},r}^{\mathrm{ref}} = v_{\mathrm{cm}r,\mathrm{av},\max}$, with the CMV reference for inverter calculated as $v_{\mathrm{cm},i}^{\mathrm{ref}} = v_{\mathrm{cm}r,\mathrm{av},\max} - v_{\mathrm{cm}}^{\mathrm{ref}}$; for the case where $v_{\mathrm{cm}}^{\mathrm{ref}} \le v_{\mathrm{cm}r,\mathrm{av},\min}$, the average-CMV reference for rectifier is configured as $v_{\mathrm{cm},r}^{\mathrm{ref}} = v_{\mathrm{cm}r,\mathrm{av},\min}$ while the average-CMV reference for inverter is determined by $v_{\mathrm{cm},i}^{\mathrm{ref}} = v_{\mathrm{cm}r,\mathrm{av},\min} - v_{\mathrm{cm}}^{\mathrm{ref}}$.

Then, the zero vector distribution coefficients ε_r and ε_i are updated according to the CMV references of both rectifier and inverter in the FID system. The proposed coordinated controller extends the average-CMV regulation range.

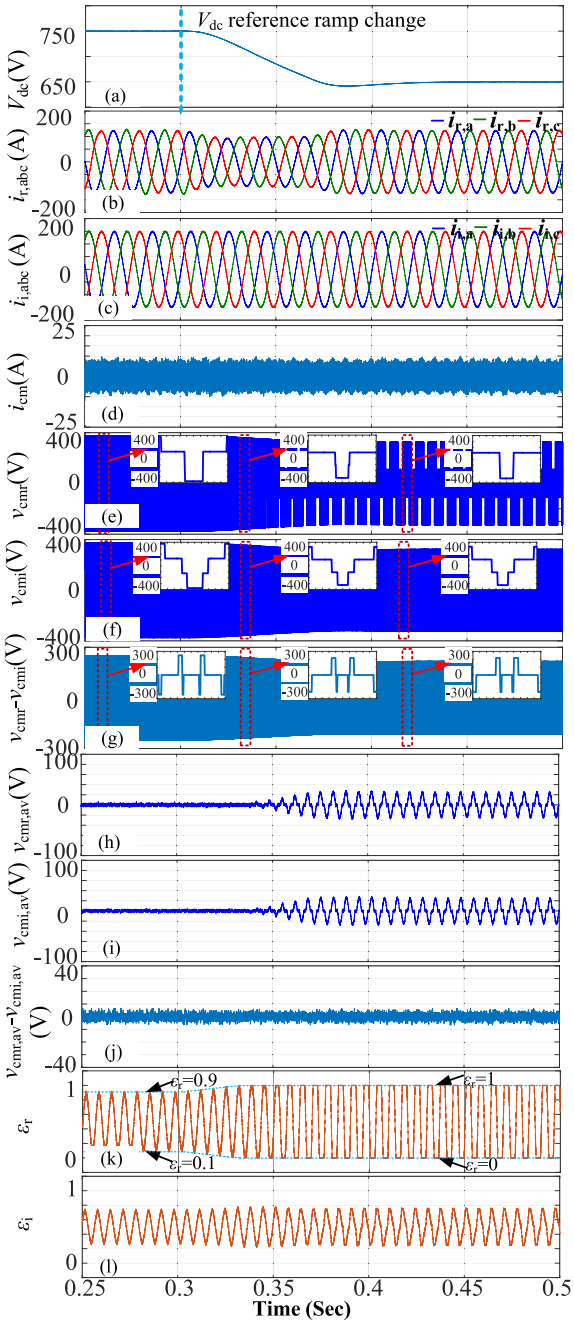

Fig. 13. Performance of the system using the proposed method. (a) DC voltage. (b) Grid-side current of the rectifier. (c) Grid-side current of the inverter. (d) CMC of the FID. (e) CMV of the rectifier. (f) CMV of the inverter. (g) CMV difference between rectifier and inverter. (h) average-CMV of the rectifier. (i) Average-CMV of the inverter. (j) Average-CMV of the FID. (k) Zero vector distribution coefficient ε_r of the rectifier. (l) Zero vector distribution coefficient ε_i of the inverter.

E. Stability Analysis of the Proposed Control Method

Considering the potential parameter mismatch in filter inductances (L_1 and L_2) and equivalent resistance R, the stability analysis of the proposed control method is investigated for both differential-mode current (DMC) and CMC controllers. The physical inductance and resistance are chosen to be the same as these in the simulation and experiment, as given in Table II.

TABLE II
PARAMETERS OF THE SIMULATED AND EXPERIMENTAL SYSTEM

Parameter	Signal	Simulated value	Experimental value
DC-bus voltage	V_{dc}	750 V	250 V
Voltage of grid1	$v_{g1,abc}$	430 V	145 V
Voltage of grid2	$v_{g2,abc}$	350 V	115 V
Grid frequency	f	50 Hz	
Switching frequency	f_{sw}	5 kHz	
converter side Inductance	L_1	0.4 mH	
grid side Inductance	L_2	0.08 mH	
filter capacitor	C	120 uF	
Dc-bus capacitance	C_{dc}	12 000 uF	
Grounding equivalent resistance	R	2 Ω	

In this article, k_L and k_R are defined as the ratios of the inductance and resistance to their actual values in the controller, respectively. For the DMC control utilizing the PR controller, Fig. 10(a) illustrates the zero-pole distribution of the DMC control system under varying k_L. The system maintains stability within the range $0.5 < k_L < 5$, as evidenced by all poles remaining inside the unit circle, demonstrating strong robustness against parameter variations. Regarding the CMC control employing the deadbeat controller, Fig. 10(b) and (c) illustrate the zero-pole distributions under varying k_L and k_R, respectively. The CMC control system exhibits stability within the ranges $0.5 < k_L < 2$ and $0.5 < k_R < 1.8$, with all poles located inside the unit circle. However, the proposed deadbeat control-based CMC mitigation method requires careful consideration to prevent substantial reductions in inductance and resistance values.

IV. Performance Evaluation

To verify the effectiveness of the proposed direct mitigation method of CMC in transformerless FID, simulated and experimental results are obtained in this section.

A. Simulated Results

Simulations have been conducted in the MATLAB/Simulink environment. The control architecture and circuitry parameters can be found in Fig. 2 and Table II.

First, the reference current magnitude for the inverter in the FID is set to 150 A. At 0.3 s, the dc voltage reference is ramped down from 750 to 650 V. The system performance is evaluated through three approaches: the AZSPWM method based on the CMV peak value reduction method; the method by decreasing the CMV difference between rectifier and inverter in [28], [29]; and the proposed direct CMC mitigation method, as illustrated in Figs. 11, 12, and 13, respectively. It can be observed that all control approaches ensure similar performance in terms of the accuracy of DMC control in the FID system, as shown in Fig. 11(a), (b), and (c), 12(a), (b), and (c), and 13(a), (b), and (c). However, the CMC control characteristics are significantly different.

When AZSPWM is used, the waveform is shown in Fig. 11. The peak value of CMC is 22 A, as demonstrated in Fig. 11(d). In detail, the peak value of CMV of the rectifier and inverter is $V_{dc}/6$, as shown in Fig. 11(e) and (f), which is significantly lower than $V_{dc}/2$. The peak value of CMV difference of rectifier

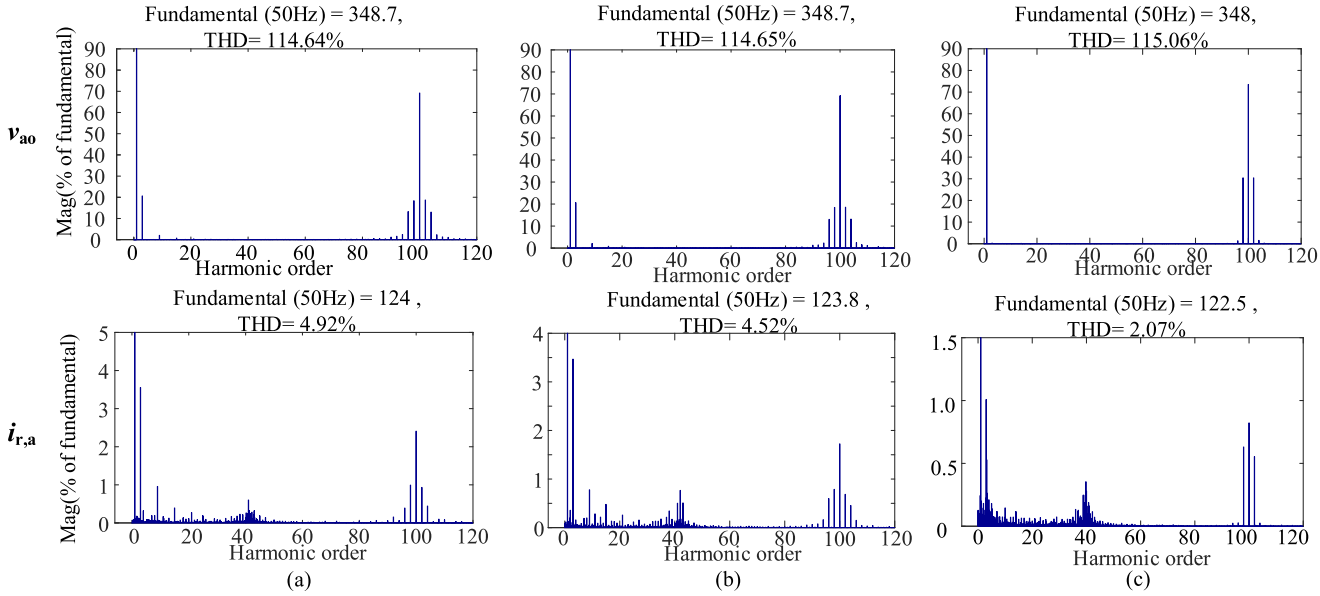

Fig. 14. Harmonic spectrum of the rectifier under different methods. (a) AZSPWM method. (b) Method in [28], [29]. (c) Proposed method (From top to bottom: A-phase voltage of the rectifier; A-phase grid current of the rectifier-side).

and inverter is $V_{\rm dc}/3$, as shown in Fig. 11(g). Additionally, the peak value of the average-CMV for the rectifier, inverter and FID system is 95, 85, and 36 V, respectively, as shown in Fig. 11(h) and (j).

When the method by decreasing the CMV difference between the rectifier and inverter in [28] and [29] is used, the waveform is shown in Fig. 12. The peak value of CMC is 20 A, as demonstrated in Fig. 12(d). Specifically, the peak value of CMV of the rectifier and inverter is $V_{\rm dc}/2$, as shown in Fig. 12(e) and (f), which is significantly higher than $V_{\rm dc}/6$ when using the AZSPWM method. The peak value of CMV difference of rectifier and inverter is $V_{\rm dc}/3$, as shown in Fig. 12(g). Additionally, the peak value of the average CMV for the rectifier, inverter and FID system is 92, 87, and 35 V, respectively, as shown in Fig. 12(h) and (j).

It can be observed that under the AZSPWM method and the method in [28] and [29], the average-CMV remains relatively high, resulting in a relatively high CMC.

The waveform obtained using the proposed CMC direct mitigation method is illustrated in Fig. 13. As illustrated in Fig. 13(d), the peak value of the CMC is 7 A. Additionally, the peak value of CMV of the rectifier and inverter is $V_{\rm dc}/2$, as shown in Fig. 13(e) and (f), which is consistent with the method in [28] and [29], but significantly higher than $V_{\rm dc}/6$ when using the AZSPWM method. The peak value of CMV difference of rectifier and inverter is $V_{\rm dc}/3$, as shown in Fig. 13(g). The average-CMVs of the rectifier, average-CMV of the inverter, average-CMV of the FID system, zero vector distribution coefficient of the rectifier (ε_r), and zero vector distribution coefficient of the inverter (ε_i) are presented in Fig. 13(h) and (l), respectively. When the dc voltage reference is 750 V, the maximum zero vector distribution coefficient ε_r is 0.9. At this point, the average-CMV reference of the FID system is supported by the rectifier, while the average-CMV of the inverter is zero, corresponding to Case 1 in Section III-D. As the dc-bus voltage gradually decreases to 650 V, the average-CMV adjustable range of the rectifier decreases. The maximum zero vector duration distribution coefficient of the rectifier, $\varepsilon_{\rm r,}$ gradually increases to 1, reaching the limit of the average-CMV adjustable range, as shown in Fig. 13(k). At this point, the average-CMV reference of the FID system is coordinated supported by both the rectifier and inverter, corresponding to case 2 in Section III-D. Specifically, the peak value of average-CMV for both the rectifier and the inverter increases from 3 to 26 V, as shown in Fig. 13(h) and (i). As a consequence, the peak value of average-CMV for FID system maintains at 3, as shown in Fig. 13(j). Meanwhile, the peak value of CMC remains at 7 A, as shown in Fig. 13(d).

To gain a better understanding of the harmonic characteristics of the proposed approach, the harmonic spectra of the converter output voltage and grid current are presented, as shown in Fig. 14 (using the A-phase of the rectifier as an example when the dc voltage is 750 V). By observing the output voltage spectrum, the spectral distribution under the different schemes is generally consistent. However, the proposed method achieves lower levels in the low-frequency bands, such as the third and ninth harmonics. Similarly, by observing the grid current spectrum, the spectral distribution is also consistent across the different schemes, but the proposed method results in a lower THD. This demonstrates that the proposed method performs similarly to the other methods in terms of harmonics and does not negatively affect harmonic levels. Furthermore, as shown in Fig. 14(c), the supraharmonics of the converter output current are significantly suppressed after being filtered by the *LCL* filter, with minimal impact on grid stability and filter design.

Then, the performance of the proposed direct mitigation of CMC is tested under step changes in current reference. As shown in Fig. 15, the peak value of CMC remains at 7 A, even when the magnitude of the current reference for the inverter in the

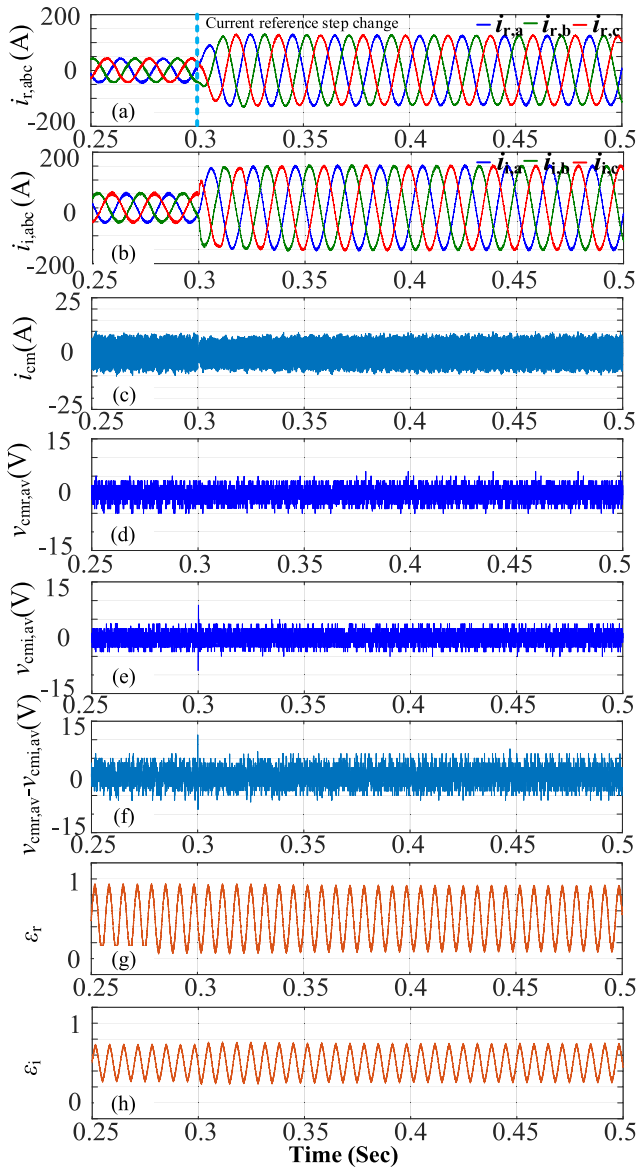

Fig. 15. Performance of the transformerless FID system using the proposed method when the current reference step change. (a) Grid-side current of the rectifier. (b) Grid-side current of the inverter. (c) CMC of the FID. (d) Average-CMV of the rectifier. (e) average-CMV of the inverter. (f) Average-CMV of the FID system. (g) Zero vector distribution coefficient ε_r of the rectifier. (h) Zero vector distribution coefficient ε_i of the inverter.

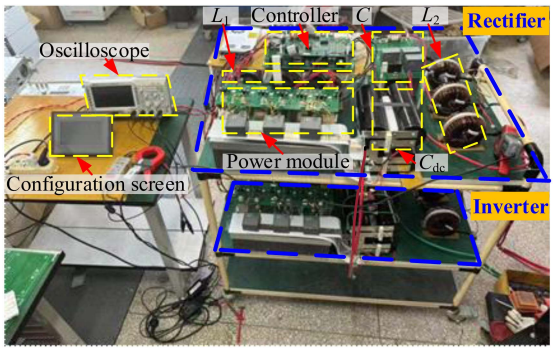

Fig. 16. Experimental platform of the transformerless FID prototype.

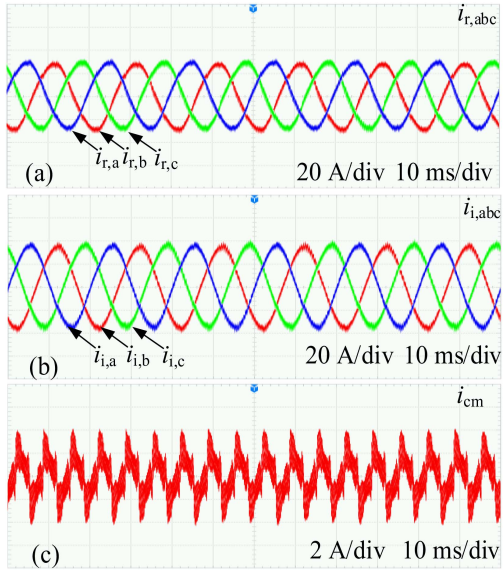

Fig. 17. Experimental waveforms of the system under AZSPWM method. (a) Grid-side current of the rectifier. (b) Grid-side current of the inverter. (c) CMC of the FID.

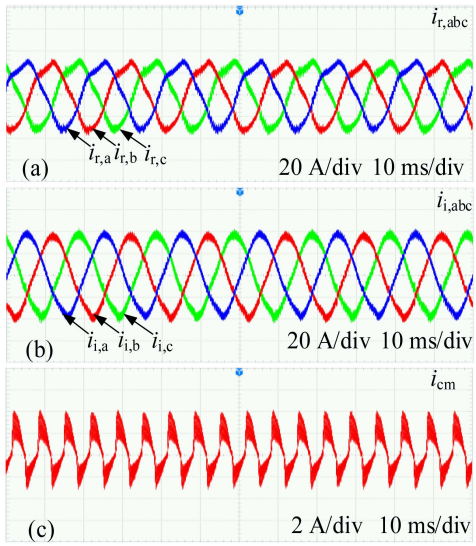

Fig. 18. Experimental waveforms of the system under the method in [28] and [29]. (a) Grid-side current of the rectifier. (b) Grid-side current of the inverter. (c) CMC of the FID.

FID has a step change from 50 to 150 A at 0.3 s. Meanwhile, the grid-connected current control maintains excellent regulation performance.

According to the previous analysis, the simulation results demonstrate that the proposed direct mitigation of CMC is more effective than that of reducing instantaneous CMV or the CMV difference between rectifier and inverter.

B. Experimental Results

Experiments are also conducted on an experimental laboratory test-rig, as shown in Fig. 16. In this experimental system, the detailed system parameters are listed in Table II.

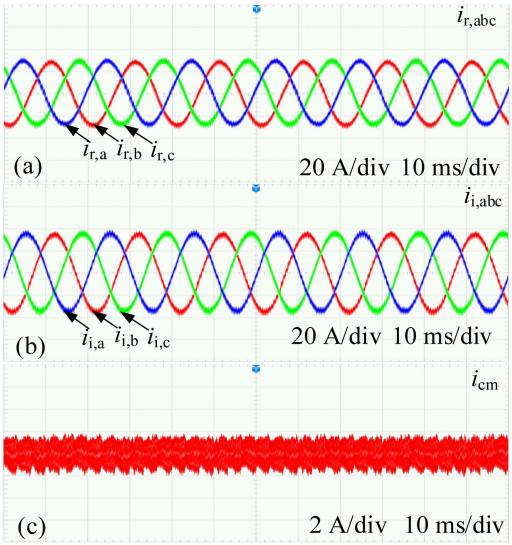

Fig. 19. Experimental waveforms of the system under the proposed method of CMC. (a) Grid-side current of the rectifier. (b) Grid-side current of the inverter. (c) CMC of the FID.

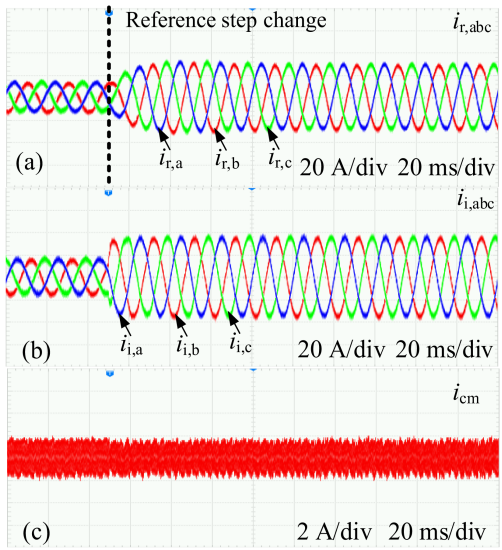

Fig. 20. Experimental waveforms of the system under the proposed method during current reference sudden changes. (a) Grid-side current of the rectifier. (b) Grid-side current of the inverter. (c) CMC of the FID.

First, the waveforms of using AZSPWM method, the method by decreasing the CMV difference between rectifier and inverter in [28], [29], and the proposed method to mitigate the CMC in transformerless FID are shown in Figs. 17, 18, and 19, respectively. In the experiment, the reference current amplitude of the inverter in the FID is set to 35 A. As shown in Fig. 17(a) and (b), Fig. 18(a) and (b), and Fig. 19(a) and (b), the three different methods can achieve similar accurate control of the DMC. However, the method by decreasing the CMV difference between rectifier and inverter in [28] and [29] will lead to an increase in the harmonic of the differential current. Additionally, as illustrated in Figs. 17(c), 18(c), and 19(c), the peak values of the CMC under the AZSPWM method, the method in [28] and [29], and the proposed direct CMC mitigation method are 4, 3.8, and 2 A, respectively. The experimental results demonstrate the superior CMC mitigation performance of the proposed method in this article.

TABLE III
COMPARISON OF CMC MITIGATION METHODS

Functionality / Method	Design Complexity	CMV Regulation Range	Active/Passive Mitigation
Conventional SVM Method	Low	N/A	N/A
AZSPWM Method	Moderate	Limited	Passive
Method in [28],[29]	High	Moderate	Passive
3D SVM Method	High	Moderate	Active
Proposed Method	Moderate	Extensive	Active

Then, to verify the dynamic performance of the proposed method, the magnitude of reference current for the FID inverter is first set to 15 A and then stepped up to 35 A. As shown in Fig. 20(c), the peak value of CMC maintains at 2 A even when the current reference has a step change. It can be clearly observed that the proposed method maintains effective mitigation of the CMC even during sudden increases in the FID reference current, while also maintaining precise control of the DMC, as shown in Fig. 20(a) and (b).

V. CONCLUSION

This article proposes a direct CMC mitigation method based on the direct regulate of average-CMV in CMC closed-loop control for transformerless FID. First, the differential mode and common mode equivalent circuits were derived, enabling analysis of the relationship between CMC and CMV based on the common mode equivalent circuit. Then, a closed-loop mitigation of CMC is proposed. Furthermore, by adjusting the duration of zero vector in the classic 7-segment SVM, an improved SVM with average-CMV direct regulation is proposed, which allows unified decoupled modulation of both DMV and CMV. As a result, the CMC can be effectively mitigated while the DMC can be accurately controlled by this method. In addition, considering the limitations of the average-CMV regulation capability of a single converter, using only a single side converter of the FID to provide the average-CMV may lead the system runs into an over modulation region. A coordinated controller for the average-CMV of both the rectifier and inverter is proposed to expand the average-CMV regulation range, thereby improving CMC mitigation capability.

Finally, the performance and characterstics of a few typical mitigation of CMC approaches are given in Table III. As indicated, compared with other CMC mitigation strategies, the proposed method achieves closed-loop active CMC mitigation and provides a simplified computational solution with an extended CMV regulation range.

REFERENCES

[1] H. Ji, C. Wang, P. Li, F. Ding, and J. Wu, "Robust operation of soft open points in active distribution nestworks with high penetration of photovoltaic integration," *IEEE Trans. Sustain. Energy*, vol. 10, no. 1, pp. 280–289, Jan. 2019, doi: 10.1109/TSTE.2018.2833545.

[2] M. Wu, L. Ding, X. Xu, K. Wang, Q. Lu, and Y. W. Li, "A common-mode voltage elimination scheme by reference voltage decomposition for back-to-back two-level converters," *IEEE Trans. Ind. Electron.*, vol. 71, no. 5, pp. 4463–4473, May 2024, doi: 10.1109/TIE.2023.3285969.

[3] M. Wu, C. Xue, Y. W. Li, and K. Yang, "A generalized selective harmonic elimination PWM formulation with common-mode voltage reduction ability for multilevel converters," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10753–10765, Sep. 2021, doi: 10.1109/TPEL.2021.3063299.
[4] A. Wang, Y. Zhou, Z. Li, G. Peng, F. Zheng, and X. Li, "Design of integrated CM inductors on both DC and AC sides for DC-fed motor drive systems: Structure, modeling, and optimization method," *IEEE Trans. Power Electron.*, vol. 39, no. 9, pp. 11110–11123, Sep. 2024, doi: 10.1109/TPEL.2024.3403572.
[5] X. Guo, D. Xu, and B. Wu, "Common-mode voltage mitigation for back-to-back current-source converter with optimal space-vector modulation," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 688–697, Jan. 2016, doi: 10.1109/TPEL.2015.2399016.
[6] J. Biela, A. Wirthmueller, R. Waespe, M. L. Heldwein, K. Raggl, and J. W. Kolar, "Passive and active hybrid integrated EMI filters," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1340–1349, May 2009, doi: 10.1109/TPEL.2009.2012404.
[7] D. Xu, C. K. Lee, S. Kiratipongvoot, and W. M. Ng, "An active EMI choke for both common- and differential-mode noise suppression," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 4640–4649, Jun. 2018, doi: 10.1109/TIE.2017.2764859.
[8] J.-H. Jung, S.-I. Hwang, and J.-M. Kim, "A common-mode voltage reduction method using an active power filter for a three-phase three-level NPC PWM converter," *IEEE Trans. Ind. Appl.*, vol. 57, no. 4, pp. 3787–3800, Jul./Aug. 2021, doi: 10.1109/TIA.2021.3053216.
[9] J.-H. Jung, J.-M. Kim, and M. Liserre, "Conducted EMI reduction by active power filter embedded in neutral-point-clamped converters," *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 15551–15565, Dec. 2023, doi: 10.1109/TPEL.2023.3312571.
[10] M. Li, Y. Yang, Z. Hao, and J. Xu, "Common-mode voltage reduction scheme for back-to-back three-level converters based on passive filters," in *Proc. IEEE 10th Int. Power Electron. Motion Control Conf.*, 2024, pp. 2004–2009, doi: 10.1109/IPEMC-ECCEAsia60879.2024.10567126.
[11] Y. Murai, T. Kubota, and Y. Kawase, "Leakage current reduction for a high-frequency carrier inverter feeding an induction motor," *IEEE Trans. Ind. Appl.*, vol. 28, no. 4, pp. 858–863, Jul./Aug. 1992, doi: 10.1109/28.148452.
[12] D. A. Rendusara and P. N. Enjeti, "An improved inverter output filter configuration reduces common and differential modes dv/dt at the motor terminals in PWM drive systems," *IEEE Trans. Power Electron.*, vol. 13, no. 6, pp. 1135–1143, Nov. 1998, doi: 10.1109/63.728340.
[13] Y. -S. Kim and S.-K. Sul, "A novel ride-through system for adjustable-speed drives using common-mode voltage," *IEEE Trans. Ind. Appl.*, vol. 37, no. 5, pp. 1373–1382, Sep./Oct. 2001, doi: 10.1109/28.952513.
[14] P. Ide, F. Schafmeister, and N. Froehleke, "Active common-mode voltage cancellation for three-phase PWM rectifier/inverter systems based on a new topology," in *Proc. 16th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2001, pp. 201–207, doi: 10.1109/APEC.2001.911648.
[15] S. Takahashi, S. Ogasawara, M. Takemoto, K. Orikawa, and M. Tamate, "Common-mode voltage attenuation of an active Common-mode filter in a motor drive system fed by a PWM inverter," *IEEE Trans. Ind. Appl.*, vol. 55, no. 3, pp. 2721–2730, May–Jun. 2019, doi: 10.1109/TIA.2019.2892364.
[16] L. Julian, G. Oriti, and T. A. Lipo, "Elimination of common-mode voltage in three-phase sinusoidal power converters," *IEEE Trans. Power Electron.*, vol. 14, no. 5, pp. 982–989, Sep. 1999, doi: 10.1109/63.788504.
[17] X. Guo, R. He, J. Jian, Z. Lu, X. Sun, and J. M. Guerrero, "Leakage current elimination of four-leg inverter for transformerless three-phase PV systems," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1841–1846, Mar. 2016, doi: 10.1109/TPEL.2015.2477539.
[18] A. Hota and V. Agarwal, "Novel three-phase H10 inverter topology with zero or constant common-mode voltage for three-phase induction motor drive applications," *IEEE Trans. Ind. Electron.*, vol. 69, no. 7, pp. 7522–7525, Jul. 2022, doi: 10.1109/TIE.2021.3097656.
[19] A. M. Hava and E. Ün, "A high-performance PWM algorithm for common-mode voltage reduction in three-phase voltage source inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1998–2008, Jul. 2011, doi: 10.1109/TPEL.2010.2100100.
[20] Y. Zhang, C. Li, M. Schutten, C. F. De Leon, and S. Prabhakaran, "Common-mode EMI comparison of NSPWM, DPWM1, and SVPWM modulation approaches," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2019, pp. 6430–6437, doi: 10.1109/ECCE.2019.8912686.
[21] X. Wu, G. Tan, Z. Ye, Y. Liu, and S. Xu, "Optimized common-mode voltage reduction PWM for three-phase voltage-source inverters," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2959–2969, Apr. 2016, doi: 10.1109/TPEL.2015.2451673.
[22] Q. Yin, R. J. Kerkman, T. A. Nondahl, and H. Lu, "Analytical investigation of the switching frequency harmonic characteristic for common mode reduction modulator," in *Proc. 40th IAS Annu. Meeting. Conf. Rec. Ind. Appl. Conf.*, 2005, pp. 1398–1405, doi: 10.1109/IAS.2005.1518542.
[23] A. M. De Broe, A. L. Julian, and T. A. Lipo, "Neutral-to-ground voltage minimization in a PWM-rectifier/inverter configuration," in *Proc. 6th Int. Conf. Power Electron. Variable Speed Drives*, 1996, pp. 564–568, doi: 10.1049/cp:19960975.
[24] H. -D. Lee and S.-K. Sul, "A common mode voltage reduction in boost rectifier/inverter system by shifting active voltage vector in a control period," *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 1094–1101, Nov. 2000, doi: 10.1109/63.892824.
[25] H. -D. Lee, Y.-C. Son, and S.-K. Sul, "A new space vector pulsewidth modulation strategy for reducing ground to stator-neutral voltage in inverter-fed AC motor drives," in *Proc. 15th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2000, pp. 918–923, doi: 10.1109/APEC.2000.822614.
[26] M. Garcia, D. G. Holmes, and T. A. Lipo, "Reduction of bearing currents in doubly Fed induction generators," in *Proc. Conf. Rec. IEEE Ind. Appl. Conf. Forty-1st IAS Annu. Meeting*, 2006, pp. 84–89, doi: 10.1109/IAS.2006.256488.
[27] H. -D. Lee and S.-K. Sul, "Common-mode voltage reduction method modifying the distribution of zero-voltage vector in PWM converter/inverter system," in *IEEE Trans. Ind. Appl.*, vol. 37, no. 6, pp. 1732–1738, Nov./Dec. 2001, doi: 10.1109/28.968185.
[28] M.-J. Tsai, Y.-Y. Shen, M.-J. Chao, and P.-T. Cheng, "An edge-aligned modulation technique to suppress leakage current in the back-to-back neutral-point clamped converter," *IEEE Trans. Ind. Appl.*, vol. 57, no. 3, pp. 3179–3187, May–Jun. 2021, doi: 10.1109/TIA.2020.3020934.
[29] A. Videt, M. Messaoudi, N. Idir, H. Boulharts, and H. Vang, "PWM strategy for the cancellation of common-mode voltage generated by three-phase back-to-back inverters," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2675–2686, Apr. 2017, doi: 10.1109/TPEL.2016.2573831.
[30] R. Zhao, X. Jiang, C. Wang, Y. Wang, H. Xu, and Q. Yan, "A novel zero-sequence-voltage-balanced SVPWM with the analyses of common-mode voltage and differential-mode current," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 2, pp. 2483–2496, Apr. 2022, doi: 10.1109/JESTPE.2021.3120624.
[31] H. Nian, Y. Zhou, and H. Zeng, "Zero-sequence current suppression strategy for open winding PMSG fed by semicontrolled converter," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 711–720, Jan. 2016, doi: 10.1109/TPEL.2015.2400438.
[32] Y. Zou et al., "An optimized DPWM with reduced leakage current for three-phase three-level inverters with unbalanced neutral-point voltage," *IEEE Trans. Power Electron.*, vol. 39, no. 12, pp. 16346–16360, Dec. 2024, doi: 10.1109/TPEL.2024.3450409.
[33] X. Lang, T. Yang, C. Li, H. B. Enalou, S. Bozhko, and P. Wheeler, "A dual-channel-enhanced power generation architecture with back-to-back converter for MEA application," *IEEE Trans. Ind. Appl.*, vol. 56, no. 3, pp. 3006–3019, May/Jun. 2020, doi: 10.1109/TIA.2020.2974145.

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