A Monolithic GaN-Based LLC-SRC With Sub-1 mA Quiescent Current and 98.6% Peak Efficiency for Energy Star Standard and 80 Plus Titanium Standard

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***Abstract*—The proposed GaN-based hybrid gate driver consists of two types of inverters and achieves a low quiescent current (I_Q) of 23.2 μA with a fast-operating frequency of 25 MHz. At the same time, the automatic precharge technique senses the voltage of the bootstrapped capacitor and reduces the standby mode leakage current (I_{LKG}) from a few milliamps to 62 μA. Therefore, the efficiency is greater than 92% at the entire output load. Finally, the soft startup clamping technique limits the peak voltage from 2.51 kV to 620 V, reducing power consumption during soft-start and preventing 650 V GaN devices from being damaged by high-voltage stress. As a result, the *LLC* converter achieves a peak efficiency of 98.6% and complies with the 80 Plus Titanium and Energy Star standards for power supply units.**

***Index Terms*—Automatic precharge technique, *LLC* series resonant converter, low-I_Q gate driver, overvoltage protection (OVP), power supply unit, self-bootstrapped low-I_Q inverter, soft start.**

I. Introduction

With the increasing awareness of environmental protection and the development of the green energy industry, it is essential to improve the efficiency of electrical equipment such as data centers, servers, and telecommunications. High-power *LLC* series resonant converters (*LLC*-SRCs) are widely used as front-end converters or power supply units in these devices due to their soft switching characteristics over a wide output load, including zero-voltage switching (ZVS) on the primary side and zero-current switching on the secondary side [1], [2], [3], [4], [5]. However, the large output parasitic capacitance (C_{OSS}) of silicon-based power MOSFET results in a long dead time and limits the switching frequency [6]. Therefore, the size of passive components, such as resonant capacitors and resonant inductors, must be large enough to provide a stable output voltage, sacrificing power density and increasing cost.

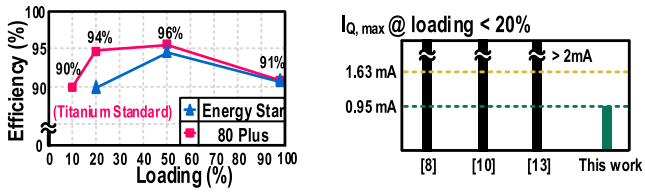

Fig. 1. (a) Two commercial standards of efficiency criteria. (b) Computational I_Q based on two standards.

Compared with silicon-based power MOSFETS, gallium nitride (GaN) high electron mobility transistors have become a popular choice for switching converters due to their small C_{OSS}, small ON-resistance (R_{ON}), and no reverse recovery charge loss. At the same time, high switching frequency and high-power density are pursued [7]. Previous works [8], [9], [10], [11] implement the *LLC* converter using discrete components. However, Yan and Ma [12] highlighted that monolithic GaN-based solutions can effectively minimize parasitic components, such as inductors and resistors, in both the printed circuit board (PCB) and the package, thereby mitigating electromagnetic interference. Additionally, these solutions help reduce gate-driving propagation delays. As a result, GaN-based solutions are highly suitable for monolithic GaN-based drivers. Unfortunately, the lack of a p-type transistor in the GaN process presents a design challenge. Although the state-of-the-art [12], [13], [14], [15] uses resistors to replace the pull-up function of PMOS, the quiescent current (I_Q) is inevitably large. As a result, the efficiency of the *LLC* converter decreases, and it cannot meet Energy Star and 80 plus titanium standards at light loads, as shown in Fig. 1(a).

According to the efficiency requirements of these two standards, the I_Q on the primary side under light load needs to be less

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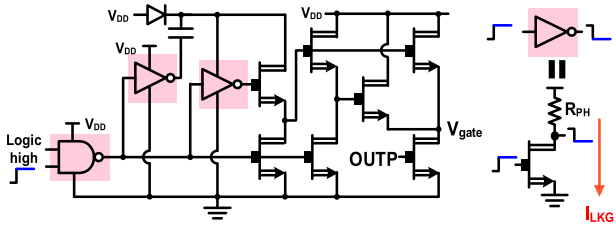


Fig. 2. Multiple leakage paths in [14] and [15].

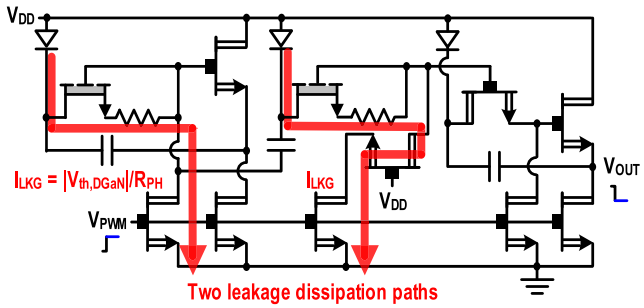


Fig. 3. Multiple leakage paths in [16], [17], and [18].

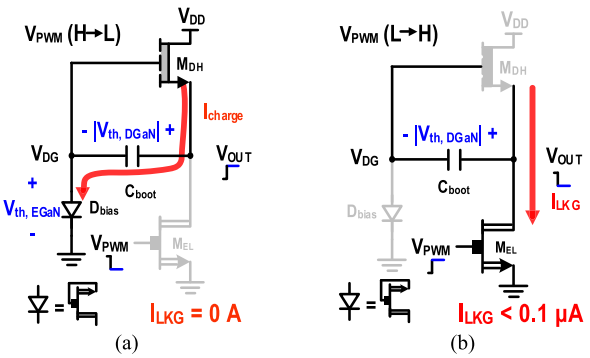


Fig. 4. (a) Charging phase of the SLI. (b) Discharging phase of the SLI.

than 1.63 mA, as shown in Fig. 1(b). However, the traditional GaN-based circuit designs [14], [15] and [16], [17], [18] in Figs. 2 and 3, respectively, do not meet the requirements. The reason is that once the input signal changes from low level to high level, the pull-up resistor (R_{PH}) in Fig. 2 will generate a leakage current (I_{LKG}), which equals to V_{DD}/R_{PH} and increases I_Q. Furthermore, other logic cells, such as NAND gates, also use similar designs, so there are multiple leakage paths in different logic cells, making the I_{LKG} larger. The driver design in Fig. 3 uses depletion-mode GaN (DGaN) in series with a resistor to reduce the I_{LKG} from V_{DD}/R_{PH} to $|V_{th,DGaN}|/R_{PH}$, but the issue of multiple leakage paths remains unresolved. Although increasing the resistance of R_{PH} can reduce I_{LKG}, it also increases the die area size and reduces the power density. Furthermore, increasing the resistance extends the delay of the driver during the pull-high process. Therefore, the tradeoff between power consumption and propagation delay is a challenge for the design of GaN-based drivers.

To address the above issues, the self-bootstrapped low-I_Q inverter (SLI) in Fig. 4 replaces the resistor with a capacitor

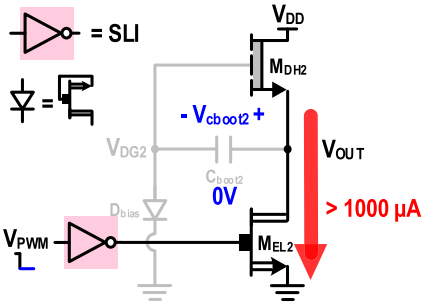


Fig. 5. Issues in low-I_Q gate driver cascaded by the SLI.

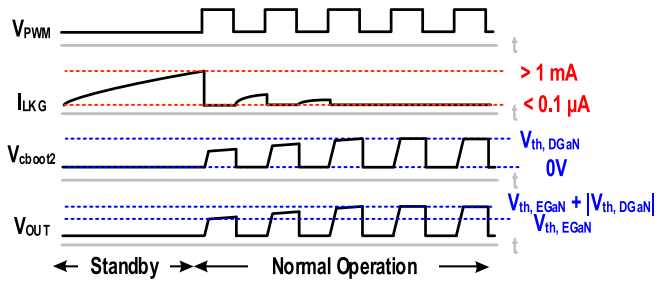


Fig. 6. Timing diagram of the low-I_Q gate driver under different modes.

to reduce I_{LKG}. The well-charged bootstrapped capacitor C_{boot} keeps M_{DH} in the subthreshold region, so M_{DH} consumes a small amount of I_{LKG}. The V_{PWM} changes from high level to low level to initiate the charging phase. Therefore, M_{DH} starts to charge C_{boot} until the voltage across C_{boot} is equal to $|V_{th,\,DGaN}|$, and then M_{DH} is in the subthreshold region, as shown in Fig. 4(a). In the other phase, V_{OUT} is pulled to zero by M_{EL} when V_{PWM} changes from low level to high level, so C_{boot} generates a negative voltage to turn OFF M_{DH}, as shown in Fig. 4(b). In both cases, I_{LKG} is almost zero since M_{DH} is almost always turned OFF. The output voltage level can rise to $|V_{th,\,DGaN}| + V_{th,\,EGaN}$ when the input signal V_{PWM} is low, through the diode D_{bias}, and drop to zero when the V_{PWM} changes in the opposite direction. This constitutes the basic functionality of an inverter with low-I_Q characteristics.

Two SLIs are cascaded to implement a low I_Q gate driver, as shown in Fig. 5, which can meet the efficiency requirements of normal operating mode. However, when the *LLC* converter switches to standby mode at light loads, the V_{PWM} operates at a lower frequency [19]. The low-level V_{PWM} lasts for a long time, causing the bootstrapped capacitor C_{boot2} of the second-level SLI to not charge for a long time. In addition, I_{LKG} of the M_{DH2} gate $I_{LKG,\,gate}$ will also discharge C_{boot2}, reducing V_{cboot2}. Therefore, the pull-up switch M_{DH2} gradually turns ON, and the shoot-through current is then dissipated from M_{DH2} to M_{EL2} until the standby mode ends. I_{LKG} is greater than 1 mA, which is not able to meet both standards.

Once normal operating mode is initiated, it takes multiple cycles to restore V_{cboot2} to $|V_{th,\,DGaN}|$, as shown in Fig. 6. In addition, although the charged C_{boot2} ensures that M_{DH2} is turned OFF to avoid I_{LKG}, it also means that the low I_Q gate driver cannot provide a strong driving current to quickly turn

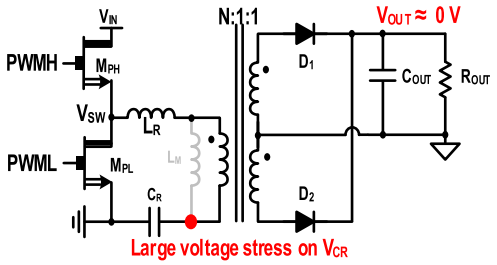


Fig. 7. Issue of *LLC* converter during startup.

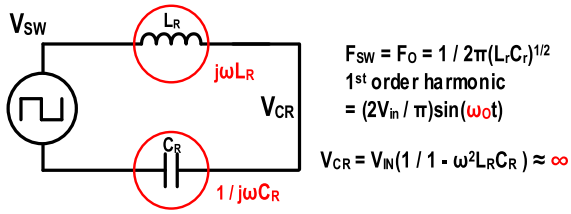


Fig. 8. Equivalent circuits during startup.

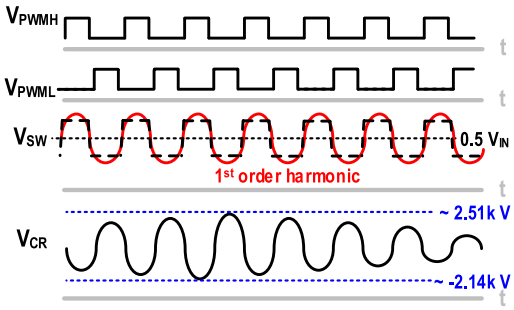


Fig. 9. Timing diagram of the *LLC*-SRC during startup.

ON the GaN power switches, thus limiting the operating range of the switching frequency. In addition to the small driving current, the maximum voltage level is equal only to $|V_{th,\,DGaN}| + V_{th,\,EGaN}$, which is not able to fully turn ON GaN power switches, inducing additional conduction loss. A new topology for GaN-based gate drivers is needed that can properly turn ON GaN power switches and consume less I_Q compared to existing technologies. Therefore, the *LLC* converter can operate efficiently in different modes.

In addition to poor efficiency in standby mode, *LLC* converters also face high-voltage stress issues during startup. In Fig. 7, since the output voltage V_{OUT} of the *LLC* converter has not yet been established, the voltage across the transformer and the magnetizing inductor L_M is zero [20]. Therefore, the equivalent circuit consists only of the resonant inductor L_R and the resonant capacitor C_R connected in series. Once the *LLC* converter operates at the oscillation frequency F_O, it experiences high voltage stress on C_R, as shown in Fig. 8. In Fig. 9, the maximum and minimum voltages 2.51 kV and -2.14 kV damage the 650 V GaN power switches and primary-side passive components due to the oscillation between C_R and L_R. In addition, a large amount of current is dissipated and converted into heat, which wastes a lot of power and reduces the reliability of the *LLC* converter.

This article proposes a monolithic GaN solution that reduces the overall system leakage current I_{LKG} while also providing overvoltage protection to safely turn ON the *LLC* converter during startup. The design objective is to meet the requirements of both commercial standards under a similar output level in [8], [9], [10], and [11], especially at light loads. The rest of this article is organized as follows. Section II presents the architecture of the proposed monolithic GaN solution. Section III shows the detailed circuit implementation, including the proposed GaN-based gate driver and the proposed three-phase soft startup clamping technique. Section IV presents measurement results and comparison tables demonstrating that the efficiency improvements of the proposed circuits are achieved by minimizing power losses rather than increasing the output power rating. Additionally, recent work from top-tier solid-state conferences [21], [22], [23] and commercial product [24] is included to strengthen the credibility of the comparison. Finally, Section V concludes this article.

II. *LLC* Series Resonant Converter

A. LLC-*SRC Topology*

Fig. 10 shows the architecture of the proposed *LLC* converter. The high-efficiency GaN-based *LLC* converter consists of the proposed hybrid gate driver (HGD) to rapidly turn ON the 650 V GaN power switches, M_{PH} and M_{PL}, respectively, while keeping the I_Q lower than 1.63 mA to meet the efficiency requirements [25]. In addition, the proposed automatic precharge technique (APC) keeps the bootstrapped capacitor well charged to avoid a large I_{LKG}, improving efficiency under standby mode. Furthermore, the proposed three-phase soft startup clamping technique (SSC) prevents the *LLC* converter from being damaged by high voltage stress during the startup period, improving the reliability of the *LLC* converter. The monolithic GaN-based solution with the proposed circuits on the primary side is used to minimize the parasitic effect, whereas silicon-based control with synchronous half-bridge rectifiers is used on the secondary side to replace the diodes. Therefore, the efficiency will not be degraded by the forward bias voltage [26], [27], [28]. Finally, the optical coupler is used to send accurate feedback signals back to the primary side to modulate the switching frequency of the *LLC* converter.

B. *Hybrid Gate Driver With Automatic Precharge Technique*

In Fig. 11, the HGD consists of two cascaded inverters with different characteristics, where the first stage is a modified SLI and the second stage is a fast inverter (FI). Compared to SLI, the modified SLI can maintain low I_Q operation for a long time, while FI achieves rail-to-rail output voltage swing and has strong current drive capability to fully turn ON the GaN power switch. The APC technique automatically charges the bootstrapped capacitor of the FI by sensing the voltage of the bottom plate of the capacitor, V_{DET2}. Since the FI directly drives the GaN power switch, the bootstrapped capacitor needs to be fully charged to avoid generating a large I_{LKG} in the FI, causing the GaN power switch to turn ON abnormally.

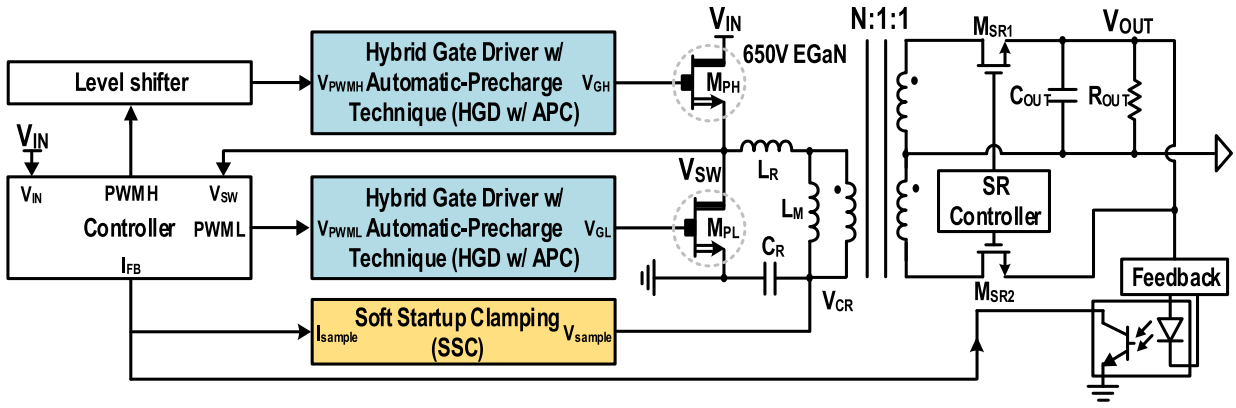


Fig. 10. Architecture of the proposed low-I_Q *LLC* series resonant converter.

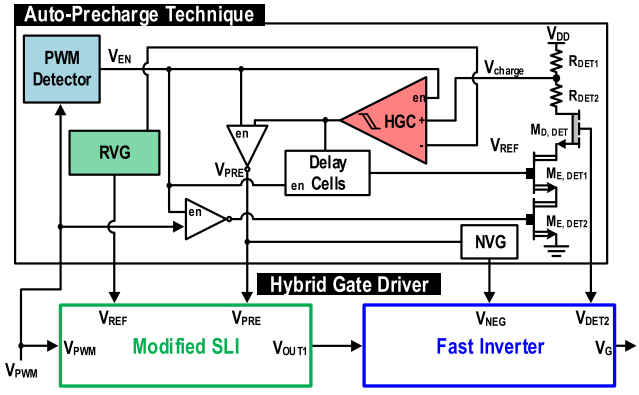


Fig. 11. Topology of the proposed HGD and APC technique.

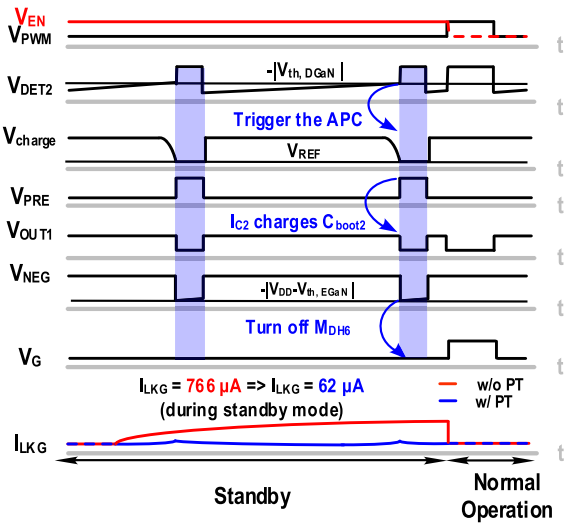


Fig. 12. Timing diagram of precharging process under standby mode.

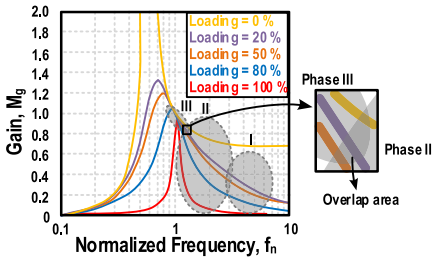


Fig. 13. Operating point of the *LLC* converter in Phase I, Phase II, and Phase III.

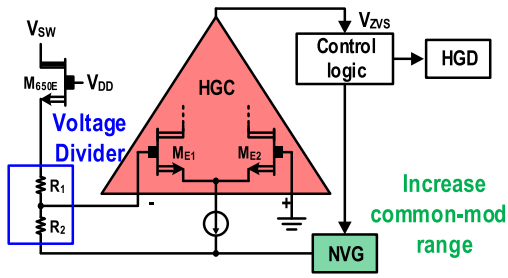


Fig. 14. Low-side sensing circuit.

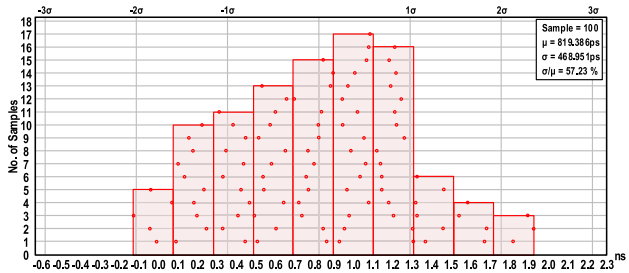


Fig. 15. Simulation result of the Monte Carlo.

The entire precharging process in standby mode is shown in Fig. 12. Since V_{PWM} remains low level for a long period, the bootstrapped capacitor of the FI is discharged due to the $I_{LKG,\ gate}$. Therefore, V_{DET2} gradually increases from negative to zero voltage. Once V_{DET2} exceeds the threshold voltage $V_{th,\ DGaN}$, $V_{charged}$ will be pulled low and compared with the reference voltage V_{REF}. The proposed high-gain comparator (HGC) quickly responds to changes in V_{charge}, triggering the one-shot signal V_{PRE}. Consequently, the output V_{OUT1} of the modified SLI temporarily drops low, allowing the bootstrapped capacitor in the FI to be charged by the constant current source I_{C2}, as illustrated in Fig. 16. At the same time, the negative

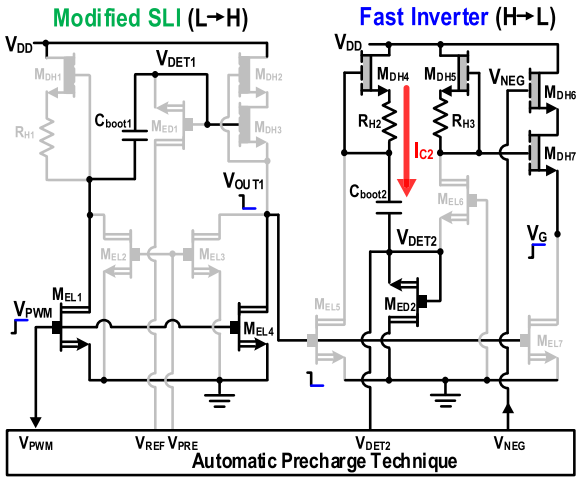


Fig. 16. Operation of the HGD when V_{PWM} is high.

voltage generator (NVG) turns OFF the pull-up switch of the FI to prevent the V_G from becoming a high voltage level. When V_{PRE} goes low again, the precharge process ends. At the end of the standby mode, the APC is no longer needed. Therefore, the output signal V_{EN} of the PWM detector changes from high level to low level, and most of the circuits in the APC are turned OFF to further reduce I_Q.

C. Three-Phase Soft Startup

According to the operation of the *LLC* converter [29] and the voltage gain of the *LLC* converter (1)–(3), the switching frequency must be modulated to avoid high voltage stress

$$M_G = \frac{f_n^2\left(L_n-1\right)}{\left(f_n^2-1\right)^2+f_n^2 x\left(f_n^2-1\right)\left(L_n-1\right)^2 Q^2} \tag{1}$$

$$f_n = \frac{f_{sw}}{f_r} \quad f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2}$$

$$Q = \frac{\sqrt{L_r/C_r}}{R_{ac}} \quad R_{ac} = \frac{8xn^2}{\pi} \quad L_n = \frac{L_M}{L_R}. \tag{3}$$

In Fig. 13, since the gain of the *LLC* converter M_G is inversely proportional to the second power of the normalize frequency, f_n, f_n increases much higher than 1 rapidly to lower M_G in phase I. Phase I is defined as the period during which the *LLC* converter transitions from zero power to when the voltage V_{CR} across the resonant capacitor reaches its peak value. During this phase, the proposed SSC technique rapidly increases the switching frequency to reduce the gain (M_G) of the *LLC* converter.

Therefore, the voltage stress is reduced to less than 650 V, and the V_{OUT} of the *LLC* converter can gradually build up. When the startup process changes to phase II, f_n slowly returns to 1. Phase II is defined as the period during which the *LLC* converter continues the soft-start process until the SSC ceases modulating the switching frequency. Since V_{OUT} is larger than 0 V, the equivalent circuits in Fig. 8 no longer exist. The components on the primary side can operate safely without being damaged by high-voltage stress. At the end of Phase II, the *LLC* converter is almost in a steady state.

Phase III is defined as the stage where the *LLC* converter starts regulating the output voltage by modulating the switching frequency, with the SSC technique no longer influencing the switching frequency. In the last phase, the *LLC* converter operates in a steady state, and the proposed SSC technique will automatically turn OFF. Therefore, I_Q can be further reduced without affecting steady-state operation.

D. Zero-Voltage Switching

To enhance the efficiency of the *LLC* converter, achieving ZVS is essential to minimize additional switching losses. A GaN-based sensing circuit plays a critical role in this process by providing rapid voltage sensing at V_{SW}. For ZVS to be achieved for the high-side switch (M_{PH}), the V_{IN} and V_{SW} voltages are scaled down and compared by the HGC. When V_{SW} exceeds V_{IN}, the HGC output changes, prompting the HGD to turn ON M_{PH} immediately. However, detecting 0 V for n-type GaN transistors is more challenging than detecting a positive voltage level. To address this, the NVG is incorporated into the low-side sensing circuit, as shown in Fig. 14. The HGC ensures that the comparison result (V_{ZVS}) responds quickly to input changes, while the NVG extends the common-mode range of the input differential pairs, enabling accurate detection of 0 V. Additionally, a voltage divider is used to introduce an offset, allowing V_{ZVS} to switch high earlier, compensating for delays introduced by the controller and the HGD. In Fig. 15, the simulation result of the Monte Carlo shows that the average delay is less than 1 ns. As a result, M_{PH} and M_{PL} can be turned ON when V_{DS} is close to 0 V, ensuring efficient ZVS operation.

III. Circuit Implementation

A. Modified SLI and the FI

This section presents the detailed implementation and operation of the proposed HGD with the characteristics of low I_Q and strong driving capability during the normal operation. In Fig. 16, when the V_{PWM} changes from low to high, M_{EL1} pulls the top terminal of C_{boot1} to zero. Consequently, the V_{DET1} becomes a negative voltage. Thus, V_{OUT1} is pulled low by turning OFF M_{DH3} and turning ON M_{EL4}. I_{C2}, which is generated by the constant current source, composed of M_{DH4} and R_{H2}, charges C_{boot2} to V_{DD}-$V_{th,\,EGaN}$ when M_{EL5} and M_{EL7} are turned OFF by V_{OUT1}. Since V_{DET2} is equal to $V_{th,\,EGaN}$, M_{EL6} is also turned OFF due to zero gate voltage. Finally, the gate of M_{DH7} can be rapidly pulled high by another constant current source, composed of M_{DH5} and R_{H3}. Therefore, M_{DH7} is able to provide a strong driving current to turn ON the GaN power switch immediately.

The other case is shown in Fig. 17. When the V_{PWM} changes from high to low level, C_{boot1} is charged by another constant current source I_{C1}, composed of M_{DH1} and R_{H1}. Therefore, M_{DH3} is turned ON and then pulls high V_{OUT1}, while V_G quickly drops to zero by M_{EL7}. Meanwhile, since a large amount of charges have been stored in C_{boot2} in the last phase, M_{DH7} dissipates zero current by a large negative voltage (-V_{DD}+$V_{th,\,EGaN}$) applied to its gate through M_{EL6}. Although the gate of M_{DH7}

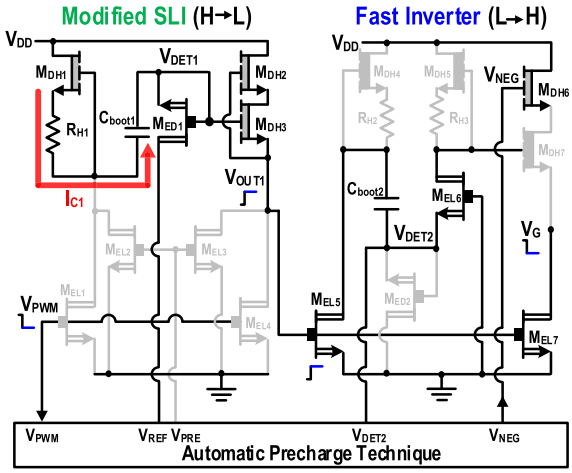


Fig. 17. Operation of the HGD when V_{PWM} is low.

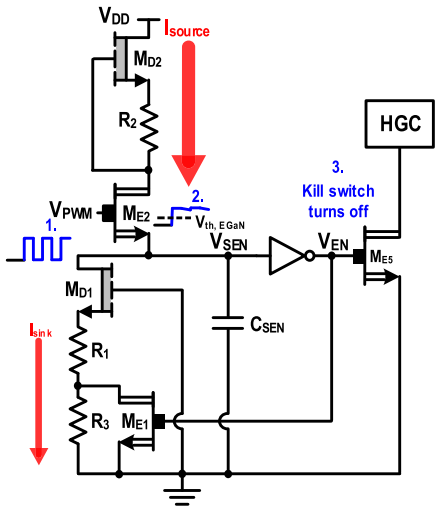


Fig. 18. Implementation of proposed PWM detector.

TABLE I
COMPARISON OF DIFFERENT GATE DRIVERS

Design	[13] ISSCC'23	[14] ISSCC'20	[17] ISSCC'22	This work
Topology	GaN Driver + GaN Switch	GaN Driver + GaN Switch	GaN Driver + GaN Switch	GaN Driver + GaN Switch
Pull-up Switch	EGaN	EGaN	EGaN	DGaN
Operating Frequency	500 kHz	262 kHz	12.5 MHz*	25 MHz
Power Consumption	1.036 mW**	1.72 mW**	0.618 mW**	0.14 mW**

*V_{IN}=400 V ** measuring test key

dissipates $I_{LKG,\ gate}$ and discharges C_{boot2}, M_{DH7} remains OFF due to the well-charged C_{boot2}. Furthermore, except for $I_{C1,\ 2}$, there is only one leakage path formed by M_{DH1} and R_{H1} when V_{PWM} is high, while M_{DH4} and R_{H2} form another leakage path when V_{PWM} is low in the proposed HGD at the same time, so the multiple leakage path in the traditional GaN-based driver design is well solved by reducing the number of leakage paths to one regardless of the state of V_{PWM}.

When the *LLC* converter switches to standby mode, the APC wakes up and starts to detect V_{DET2}. Once V_{PRE} is activated, M_{EL2} and M_{EL3} are immediately turned ON, forcing V_{OUT1} to temporarily be low level. In addition, V_{NEG} becomes a negative voltage to turn OFF M_{DH6}, so V_G remains a low voltage without triggering the GaN power switch. Since M_{EL5} and M_{EL7} are also turned OFF, C_{boot2} can be charged by I_{C2} until V_{PRE} becomes low again. In both operation modes, C_{boot1} and C_{boot2} are always charged to avoid the malfunction of the HGD.

The I_Q, which includes I_{LKG} and $I_{C1,\ 2}$ of the HGD is reduced to 23.2 μA thanks to the modified SLI, while it can also operate at 25 MHz due to the FI. Table I shows a detailed comparison by measuring test keys of different topologies. Compared to other topologies, the proposed HGD achieves the lowest power consumption while reaching the fastest switching frequency, which is able to meet the requirements of both standards and is suitable for the application of *LLC* converter.

B. PWM Detector and High Gain Comparator

The comparator in the APC technique needs to respond rapidly to restore charge to C_{boot2} immediately, or I_{LKG} starts to increase and abnormally turn ON the GaN power switch, reducing the efficiency of the *LLC* converter under light load. Furthermore, since C_{boot1} and C_{boot2} are periodically charged in normal operation mode, the circuits of the APC technique are idle while still consuming extra power. Therefore, the proposed PWM detector can decide whether to turn ON or OFF the entire APC technique according to the mode of the *LLC* converter. The topology of the proposed PWM detector is shown in Fig. 18. Since I_{source} is larger than I_{sink}, the top plate voltage V_{SEN} of C_{SEN} increases rapidly as M_{E2} is activated by fast-switching frequency V_{PWM}. When V_{SEN} exceeds the threshold voltage $V_{th,EGAN}$, the enable signal V_{EN} becomes low to disable the HGC. Instead, once V_{PWM} remains low for a period of time in standby mode, C_{SEN} is discharged by I_{SINK} and V_{SEN} decreases gradually. Once V_{SEN} becomes lower than $V_{th,\ EGaN}$, V_{EN} goes high to turn ON M_{E1}. Therefore, the C_{SEN} is discharged rapidly to initiate the HGC. Furthermore, M_{E1} forms the hysteresis control to prevent the HGC from being accidentally turned OFF in standby mode, or the APC fails and the I_{LKG} increases.

In addition to the HGC, other control logic cells in the APC technique, such as delay cells and inverters, are also controlled by the V_{EN}, which changes according to the operation of the *LLC* converter. Furthermore, although the architecture of the NVG is the same as the FI while excluding the output stages M_{DH6}, M_{DH7}, and M_{EL7}, as shown in Fig. 19, the power consumption of the NVG is negligible since it only operates when V_{PRE} is triggered. Therefore, most parts of the APC technique are turned OFF except for the PWM detector and the proposed process-independent reference voltage generator (RVG), which reduces the extra power consumption by the idle circuits in the APC technique during the normal operation mode of the *LLC* converter.

Fig. 20 shows the implementation of the proposed HGC. Designing a GaN-based single-ended amplifier without a P-type semiconductor is also a challenge. Therefore, the HGC adopts a DGaN with a cascaded EGaN to form a PMOS-emulated current mirror to ensure that the gain of the HGC can reach 42 dB.

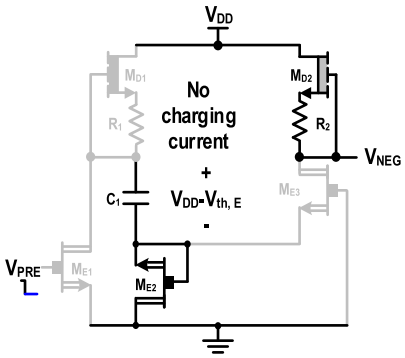


Fig. 19. Implementation of NVG.

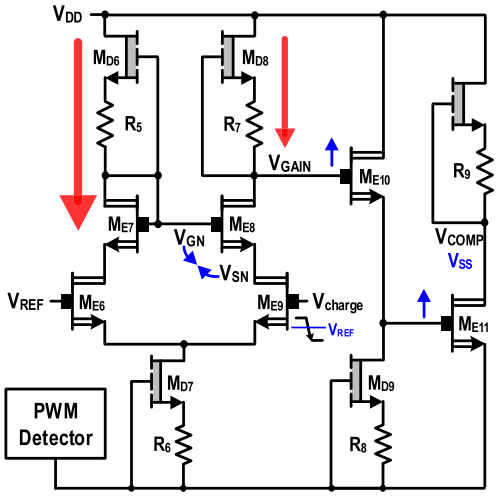


Fig. 20. Implementation of proposed HGC.

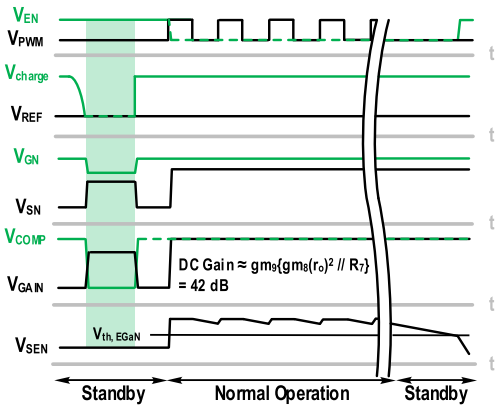


Fig. 21. Timing diagram of the HGC under different modes.

Since the voltage swing of V_{GAIN} is large, the HGC can operate instantly according to the change in V_{charge}.

Fig. 21 shows the entire comparison process of the HGC. When V_{charge} is lower than the reference signal V_{REF}, the bias current at the left-hand side of the PMOS emulated current mirror becomes larger than the bias current at the right-hand side. Therefore, the gate node V_{GN} of M_{E8} is pulled low due to the larger bias current. On the contrary, the source node V_{SN} of

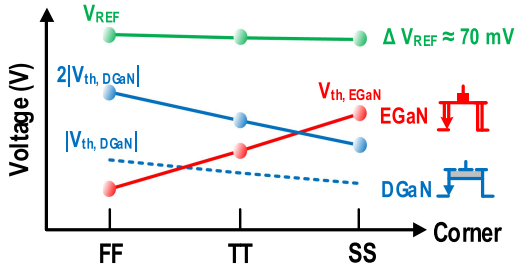


Fig. 22. Variation of the threshold voltage under different corner.

M_{E8} changes in opposite directions due to the smaller bias current. As a result, the drain node V_{GAIN} can change rapidly due to the PMOS-emulated current mirror. The HGC guarantees fast operation of the APC technique to keep C_{boot2} charged, allowing I_Q to remain lower than 62 μA under standby mode while maintaining the strong driving capability of the HGD under normal operation mode.

C. Process-Independent Reference Voltage Generator

To ensure that the APC technique is triggered correctly across different process corners, it is essential to keep the variation of V_{REF} small. If V_{REF} drops too low in one corner, the APC may not activate, preventing C_{boot2} from charging immediately, which can cause the DGaN transistor in the FI to conduct the current prematurely. On the other hand, if V_{REF} is too high in other corners, the APC may stay constantly ON, resulting in C_{boot1} in the modified SLI remaining uncharged until the system exits standby mode. In both cases, once the bootstrapped capacitors have no charge, the high I_{LKG} will reduce the efficiency of the *LLC* converter.

The GaN process is known for its significant corner variations, making it challenging to design an ON-chip RVG. However, as referenced in [30], the variation of threshold voltage $V_{th,\ EGaN}$ of EGaN transistors exhibits an opposite trend to that of DGaN transistors across different process corners, as illustrated in Fig. 22. Additionally, the variation in $V_{th,\ EGaN}$ is approximately twice that of $|V_{th,\ DGaN}|$, as shown in

$$\Delta V_{th,\ EGaN} \simeq -2\Delta V_{th,\ DGaN}\ . \tag{4}$$

To address this, the proposed process-independent RVG, as depicted in Fig. 23, utilizes a cascade of two DGaN transistors and one EGaN transistor to generate the reference voltage V_{REF}, as described in

$$V_{REF} = V_{th,\ EGaN} + 2\,|V_{th,\ DGaN}|\ . \tag{5}$$

Finally, this configuration effectively reduces the variation of V_{REF} to 70 mV across different process corners, ensuring the reliable operation of the APC technique.

D. Soft Startup Clamping Technique

Optimal trajectory control (OTC) is a widely used method in the industry to address start-up challenges. OTC leverages

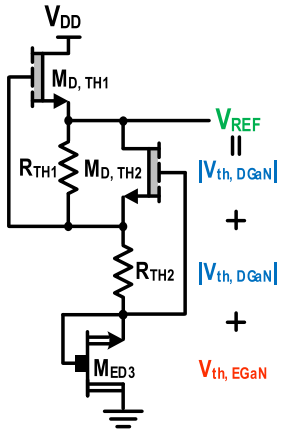


Fig. 23. Proposed process-independent RVG.

the mathematical model of the *LLC* converter to design an optimal trajectory for voltage and current, enabling a smooth and controlled transition by dynamically adjusting the switching frequency. However, implementing OTC requires a microcontroller unit (MCU) [31] to manage the transition from zero power to steady-state operation, which increases I_Q and occupies additional PCB space. Furthermore, OTC also relies on both voltage and current sensing, adding to the overall design complexity.

Another method involves using PWM control [32]. This approach sets a switching frequency equal to the resonant frequency at the beginning of the startup process. Then, the duty will gradually increase from the minimum value to the duty cycle of 0.5 to achieve a soft start. Finally, the PWM control will switch back to the PFM control for the rest of the start-up and steady-state operation. PWM control involves the use of two control strategies, increasing the design complexity and becoming difficult to integrate on the chip. In addition, the PWM control circuit becomes idle once the start-up process ends, which may increase the I_Q. This method can also be implemented by the MCU, but the issues are the same as using OTC. In contrast, the proposed SSC technique offers significant advantages. It operates only during the start-up period and automatically turns OFF in steady-state operation, reducing I_Q. Additionally, the SSC technique requires only the voltage of the resonant capacitor for sensing, greatly simplifying circuit implementation. Finally, the SSC technique is fully integrated into the chip, eliminating the need for additional PCB area.

In Fig. 24, the proposed three-phase SSC technique samples the voltage V_{CR} of the resonant capacitor during the soft startup period of the *LLC* converter. Since the rated voltage of the GaN process is 12 V, the high-rated voltage component DGaN M_{clamp} is used to block the high voltage from the V_{CR}. The V_{CR} is scaled by the resistors $R_{scale1,\ 2}$ and sampled by the capacitor C_{sample}. The sample voltage V_{sample} is then compared with the high-threshold $V_{th,\ H}$, and low-threshold $V_{th,\ L}$, to determine the end of the first and second startup phases. In addition, V_{sample} is converted to I_{sample} by the GaN-based operational transconductance amplifier, and I_{sample} is added to the feedback current to modulate the switching frequency. Therefore, M_G can be temporarily reduced to prevent V_{CR} from being greater than

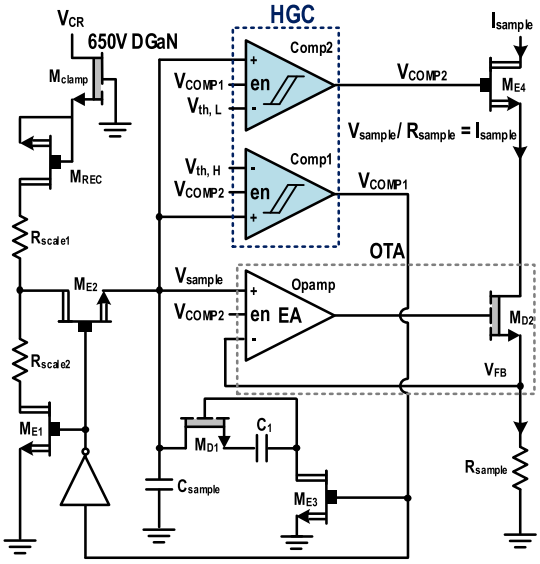


Fig. 24. Topology of the proposed SSC technique.

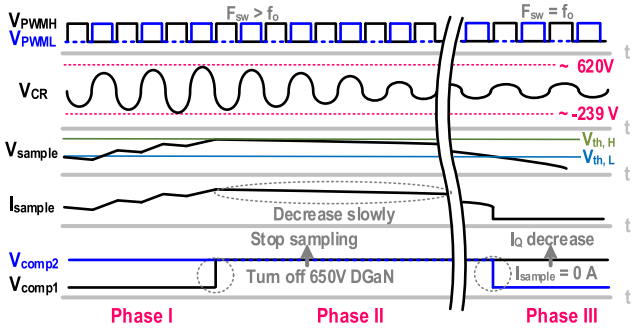


Fig. 25. Timing diagram of the three-phase SSC technique.

2 kV or lower than -2 kV. In phase I, the V_{smaple} increases rapidly until the V_{CR} reaches its maximum, which is around 600 V, and the V_{sample} becomes higher than $V_{th,\ H}$ simultaneously. As a result, the output signal V_{COMP1} of the comparator Comp1 increases, activating both M_{E3} and Comp2. Next, phase II begins, and the SSC technique stops sampling V_{CR} by turning OFF M_{E1} and M_{E2}. Furthermore, the small discharging current, which is generated by M_{D1} and C_1, slowly pulls the V_{sample} low, and so does the I_{sample}. Therefore, the *LLC* converter can gradually startup without being damaged by high-voltage stress. Once the V_{sample} becomes lower than the $V_{th,\ L}$, which also means that the *LLC* converter almost turns to the steady state, V_{COMP2} becomes low level to turn OFF M_{E4}. As a result, the feedback current is not affected by I_{sample} and is capable of regulating the output voltage. In addition, the low-level V_{COMP2} also disables the error amplifier (EA) and Comp1, so the entire SSC technique is turned OFF to reduce I_Q.

Due to the proposed SSC technique, the maximum and minimum values are 620 V and -239 V, respectively, as shown in Fig. 25. The entire SSC technique is turned OFF once V_{COMP1} becomes high and V_{COMP2} becomes low. Table II shows the summary of the I_Q under different modes to show the low power consumption of the proposed HGD, APC, and SSC.

TABLE II
SUMMARY OF IQ UNDER DIFFERENT MODES

	Standby	Normal Operation
Hybrid Gate Driver	23.2 μA	
Automatic-Precharge Technique	38.8 μA (62-23.2)	4.4 μA (PWM detector & RVG)
Soft Startup Clamping	<10 μA	

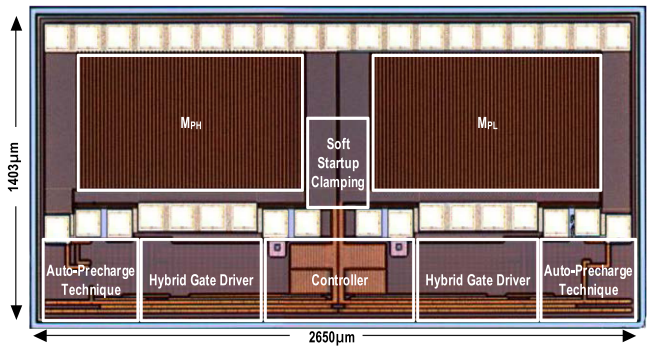
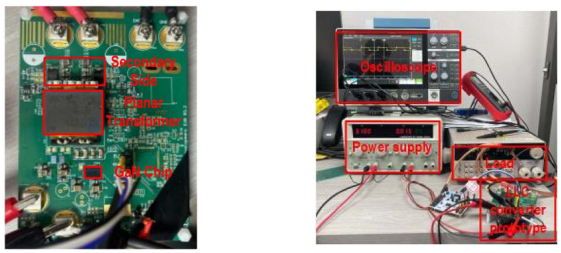


Fig. 26. Chip micrograph of the primary-side GaN-based chip.



(a) (b)

Fig. 27. (a) Prototype. (b) Measurement setup.

TABLE III
DEVICE PARAMETERS AND SPECIFICATIONS

Device Parameters and Specifications	Value
Magnetizing Inductor (L_M)	58 μH
Resonant Inductor (L_R)	16.5 μH
Resonant Capacitor (C_R)	1.45 nF
High-side bootstrapped capacitor	2 μF
Output Capacitor (C_{OUT})	4×4.7 μH
Transformer Ratio	15:2:2
Input Voltage (V_{IN})	380 V
Output Voltage (V_{OUT})	24 V
Max. output current	5 A
Switching Frequency	1 MHz
$I_{Q,max}$ @ loading < 20% (primary side)	1.63 mA

IV. MEASUREMENT RESULTS

The low-I_Q *LLC* series resonant converter of the primary side is fabricated in 0.5 μm GaN process with 2650 × 1403 μm^2, as shown in Fig. 26. In Fig. 27, the prototype and the measurement setup are shown with the device parameters and specifications shown in Table III . To show the low quiescent current of the proposed HGD, the measurement results of the test key with 23.2 μA is shown in Fig. 28. Fig. 29 shows the double pulse testing to verify the driving ability of the proposed HGD. Due to the FI, the maximum operating frequency is up to 25 MHz. During soft startup, the measurement results of the maximum and minimum values of V_{CR} without clamping technique are 2.51 kV and -2.14 kV, as shown in Fig. 30. In contrast, the proposed SSC technique limits the peak value in both positive and negative voltages, 620 V and -239 V, respectively, so the large power dissipation during startup is reduced. The *LLC* converter functions efficiently with the proposed HGD under heavy load (I_{load} = 5 A), with an input voltage of 380 V and an output voltage of 24 V, as shown in Fig. 31.

Fig. 32 shows the root-mean-square (rms) I_Q of the proposed *LLC* converter, including the primary side and the secondary side. The measured rms I_Q is reduced to 3.26 mA under 10% I_{load}; therefore, the efficiency can reach 92.3%, which is higher than the standard of Energy Star. Table IV presents a comparison of the I_Q with commercial *LLC* converters. The I_Q of the

TABLE IV
COMPARISON OF I_Q WITH THE COMMERCIAL LLC CONVERTERS

Design	TEA2017AAT/2	SSC3S927	This work
Cooperation	NXP Semiconductors	Sanken Electric	N/A
Quiescent Current*	8 mA	10 mA	4.8 mA

*In operation

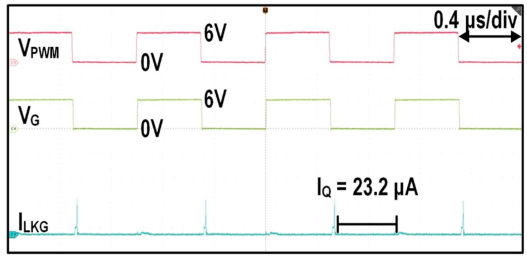


Fig. 28. Measured I_Q of the proposed HGD.

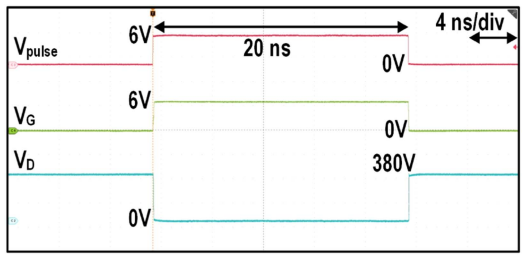


Fig. 29. Double pulse testing of the proposed HGD.

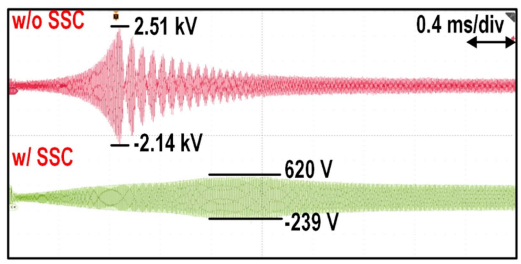


Fig. 30. Measured V_{CR} with the proposed SSC technique during startup.

TABLE V
COMPARISON TABLE WITH STATE-OF-THE-ARTS

Design	[8] TCASII'23	[9] TPE'23	[10] TPE'23	[11] TPE'21	[21] APEC'23	[22] APEC'25	[23] CICC'24	[24] DCW150-110-24FT	This work
Process*	Discrete Power switch: Si	Discrete Power switch: GaN**	Discrete Power switch: GaN	Discrete Power switch: SiC	Discrete Power switch: Si	Discrete Power switch: Si	0.35μm CMOS	N/A	GaN
V_{IN} Range	450 V	50 V–90 V	72 V	280 V–360 V	400 V	380 V	365 V–410 V	110 V	380 V
V_{OUT} Range	12 V / 24 V	20 V	24 V	48 V	48 V	12 V	24 V	24 V	24 V
Switching Frequency	77 kHZ-100 kHz	400 kHz	200 kHZ	70 kHZ	300 kHz	140 kHz	100 kHz	N/A	1 MHZ
L_m	1224 μH	12.5 μH	17 μH	336 μH	116 μH	2.75 mH	480 μH	N/A	58 μH
L_r	276 μH	2.5 μH	0.8 μH	71 μH	6 μH	25 μH	80 μH	N/A	16.5 μH
C_r	10 nF	62 nF	660 nF	33 nF + 2.2 nF	47 nF	50 nF	30 nF	33 nF + 2.2 nF	1.45 nF
Max. efficiency	88.7 %	96 %**	< 96 %**	95.79%	94.8 %	93.695 %	95.04 %	83 %***	98.6 %
80 plus	No	No	No	No	No	No	No	No	Yes
Energy Star	No	No	Yes	Yes	No	Yes	Yes	No	Yes
Rated output power	60 W	150 W	180 W	192 W	500 W	500 W	240 W	144 W	120 W
Soft startup OVP	No	No	No	No	No	No	No	No	Yes
Power density	5.93 W/in³****	14.08 W/in³****	5.28 W/in³****	N/A	31.92 W/in³****	36.97 W/in³****	N/A	4.19 W/in³****	13.16 W/in³

*primary side; **Only LLC stage; *** typically value; **** by estimation; ***** calculated by the size of the whole package;

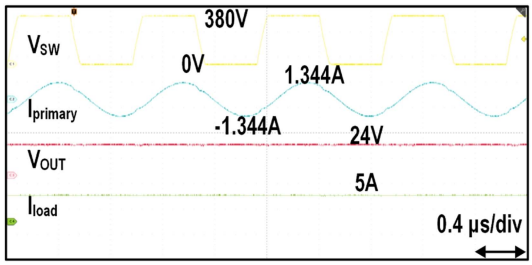


Fig. 31. Measured waveform under heavy load.

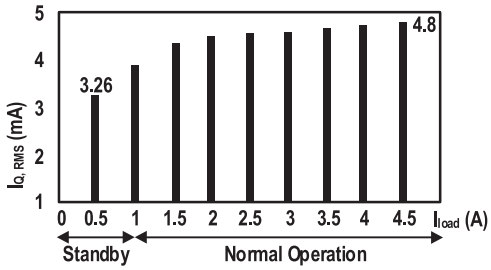


Fig. 32. Measured I_Q under different output loadings when $V_{IN} = 380$ V and $V_O = 24$ V.

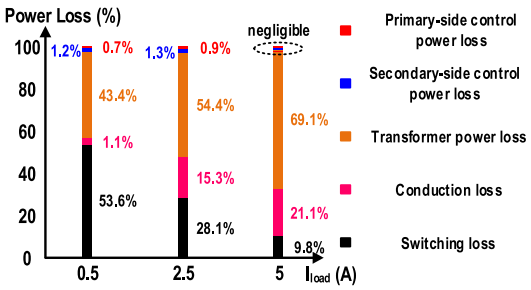


Fig. 33. Power loss of the proposed *LLC* converter.

TEA2017AAT/2 and SSC3S927 are 8 mA and 10 mA, respectively, while the proposed *LLC* converter achieves a significantly lower maximum I_Q of 4.8 mA.

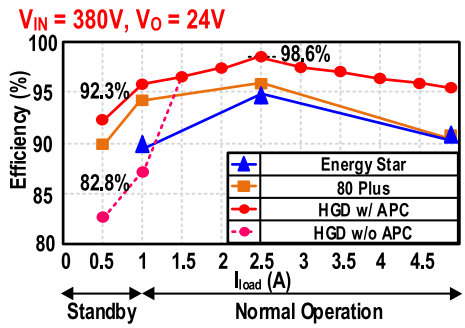


Fig. 34. Efficiency under different output loadings.

The analysis of various power losses is illustrated in Fig. 33. Thanks to the low-I_Q characteristic of the proposed *LLC* converter, the quiescent power loss becomes negligible across the entire output load range. Fig. 34 shows the efficiency of the proposed *LLC* converter, when $V_{IN} = 380$ V and $V_{OUT} = 24$ V, the proposed APC technique improves the efficiency by 9.5% in standby mode. Therefore, the efficiency is higher than 92% under the whole output load, which can meet the efficiency requirement of both commercial standards.

Table V shows a detailed comparison of the proposed and prior art. This work proposes a 380 V to 24 V *LLC*-SRC using the proposed HGD with APC. Thanks to the HGD and the APC, the efficiency is able to reach 98.6% ($I_{load} = 2.5$ A), which is the highest compared to the prior art. The proposed design is the only work that also focuses on the startup process. Therefore, the reliability of the *LLC* converter is improved by the GaN-based SSC technique. Due to the monolithic GaN on the primary side, the switching frequency of the *LLC* converter is 1 MHz, which reduces the size of the passive components. The sizes of the L_M, L_R, and C_R are 58 μH, 16.5 μH, and 1.45 nF, respectively.

V. CONCLUSION

This article presents a resonant *LLC* converter that steps down 380 V to 24 V, achieving a peak efficiency of 98.6%, compliant with both Energy Star and 80 Plus Titanium standards. The proposed HGD delivers strong drive capability while maintaining

a low quiescent current I_Q of just 23.2 μA, making it ideal for monolithic GaN-based *LLC* converters that require high efficiency. To prevent shoot-through, an APC circuit rapidly charges the HGD's bootstrap capacitor. A process-independent RVG ensures only 70 mV variation across corners and temperatures, enabling precise APC activation in standby mode. Additionally, the PWM detector activates the APC only when needed, further lowering I_Q and boosting standby efficiency by 9.5%. For reliable startup, the proposed SSC circuit limits the voltage swing of the V_{CR} to suppress oscillation-induced power loss. The SSC is automatically disabled after startup to avoid unnecessary power consumption and maintain low I_Q.

REFERENCES

[1] W. Feng, F. C. Lee, P. Mattavelli, and D. Huang, "A universal adaptive driving scheme for synchronous rectification in LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3775–3781, Aug. 2012.

[2] C. Fei, Q. Li, and F. C. Lee, "Digital implementation of adaptive synchronous rectifier (SR) driving scheme for high-frequency LLC converters with microcontroller," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5351–5361, Jun. 2018.

[3] M. Li, Z. Ouyang, M. A. E. Andersen, and B. Zhao, "Self-driven gate driver for LLC synchronous rectification," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 56–60, Jan. 2021.

[4] K.-W. Kim, H.-S. Youn, J.-I. Baek, Y. Jeong, and G.-W. Moon, "Analysis on synchronous rectifier control to improve regulation capability of high-frequency LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 7252–7259, Aug. 2018.

[5] K.-B. Park, B.-H. Lee, G.-W. Moon, and M.-J. Youn, "Analysis on center-tap rectifier voltage oscillation of LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2684–2689, Jun. 2012.

[6] R. Beiranvand, B. Rashidian, M. R. Zolghadri, and S. M. H. Alavi, "Optimizing the normalized dead-time and maximum switching frequency of a wide-adjustable-range LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 462–472, Feb. 2011.

[7] A. Pal and G. Narayanan, "Comparative study of enhancement-mode gallium nitride FETs and silicon MOSFETs for power electronic applications," in *Proc. IEEE 6th India Int. Conf. Power Electron.*, 2014, pp. 1–6.

[8] C.-H. Chou, C.-Y. Hsiao, and Y.-H. Liu, "Half-bridge LLC series-resonant converter with hybrid rectifier for LED signage backlighting systems," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 2, pp. 566–570, Feb. 2023.

[9] W. Wang, Y. Liu, J. Zhao, P. Zhang, and P. C. Loh, "A dynamic control method for buck + LLC cascaded converter with a wide input voltage range," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 1522–1534, Feb. 2023.

[10] W. Wang, Y. Liu, P. Zhang, Y. Yuan, J. Zhao, and P. C. Loh, "A fault-tolerant LLC converter with high reliability and low cost for two-stage converters," *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 9647–9659, Aug. 2023.

[11] Y. Wei, Q. Luo, Z. Wang, and H. A. Mantooth, "A complete step-by-step optimal design for LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3674–3691, Apr. 2021.

[12] D. Yan and D. B. Ma, "A monolithic GaN power IC with on-chip gate driving, level shifting, and temperature sensing, achieving direct 48-V/1-V DC–DC conversion," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3865–3876, Dec. 2022.

[13] D. Yan and D. B. Ma, "A monolithic GaN direct 48V/1V AHB switching power IC with auto-lock auto-break level shifting, self-bootstrapped hybrid gate driving, and on-die temperature sensing," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2022, pp. 1–3.

[14] M. Kaufmann, M. Lueders, C. Kaya, and B. Witch, "18.2 A monolithic E-mode GaN 15W 400V offline self-supplied hysteretic buck converter with 95.6% efficiency," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2020, pp. 288–290.

[15] M. Kaufmann and B. Wicht, "A monolithic GaN-IC with integrated control loop for 400-V offline buck operation achieving 95.6% peak efficiency," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3169–3178, Dec. 2020.

[16] H.-Y. Chen et al., "33.1 A fully integrated GaN-on-silicon gate driver and GaN switch with temperature-compensated fast turn-on technique for improving reliability," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2021, pp. 460–462.

[17] Y.-Y. Kao et al., "A monolithic GaN-based driver and GaN power HEMT with diode-emulated GaN technique for 50MHz operation and sub-0.2ns deadtime control," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2022, pp. 228–230.

[18] T.-W. Wang et al., "Monolithic GaN-based driver and GaN switch with diode-emulated GaN technique for 50-MHz operation and Sub-0.2-ns deadtime control," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3877–3888, Dec. 2022.

[19] Y. Fang, D. Xu, Y. Zhang, F. Gao, L. Zhu, and Y. Chen, "Standby mode control circuit design of LLC resonant converter," in *Proc. IEEE Power Electron. Specialists Conf.*, 2007, pp. 726–730.

[20] H. Xie, Q. Liu, J. Niu, and L. Jing, "Research on soft-start method and light load intermittent control of LLC resonant converter," in *Proc. 4th Int. Conf. Smart Power Internet Energy Syst.*, 2022, pp. 244–249.

[21] K.-W. Heo, H.-P. Park, and J.-H. Jung, "EM noise mitigation using partial power regulated LLC resonant converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2023, pp. 1737–1740.

[22] Y.-C. Liu and S.-S. Wu, "LLC converter main transformer losses: Eliminating air gaps and integrating parallel external inductors," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2025, pp. 2179–2186.

[23] H. Shi et al., "A 2.4-to-240W, 95.04% peak efficiency LLC isolate converter controller with symmetric pulse-width balancing and fixed-period hysteresis burst control," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2024, pp. 1–2.

[24] "DCW 100 $\sim$ 200 series," Helios Power Solutions, Auckland, New Zealand, [Online]. Available: https://heliosps.com/product/hps-dc-dc-converters-industrial-dcw100-200/

[25] C.-Y. Chen et al., "A monolithic GaN-based gate driver for LLC-SRC with three-phase startup clamping achieving 23.2μA IQ and 98.6% peak efficiency," in *Proc. IEEE Symp. VLSI Technol. Circuits*, 2024, pp. 1–2.

[26] X. Zhu et al., "A sensorless model-based digital driving scheme for synchronous rectification in 1-kV input 1-MHz GaN LLC converters," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 8359–8369, Jul. 2021.

[27] P. Amiri, C. Botting, M. Craciun, W. Eberle, and L. Wang, "Analytic–adaptive LLC resonant converter synchronous rectifier control," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5941–5953, May 2021.

[28] J. Zhang, J. Wang, G. Zhang, and Z. Qian, "A hybrid driving scheme for full-bridge synchronous rectifier in LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4549–4561, Nov. 2012.

[29] W. Feng and F. C. Lee, "Optimal trajectory control of LLC resonant converters for soft start-up," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2013, pp. 1445–1451.

[30] P.-J. Chiu et al., "A 15.4ppm/°C GaN-based voltage reference with process-variation-immunity and high PSR for EV power systems," in *Proc. IEEE Symp. VLSI Circuits*, 2024, pp. 1–2.

[31] C. Fei, F. C. Lee, and Q. Li, "Soft start-up for high frequency LLC resonant converter with optimal trajectory control," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2015, pp. 609–615.

[32] Y. Cheng, Z. Ge, Y. Liu, F. Yang, and H. Wu, "Fundamental harmonic amplitude-frequency hybrid modulation strategy for half-bridge LLC resonant converters," *CPSS Trans. Power Electron. Appl.*, vol. 8, no. 2, pp. 161–169, Jun. 2023.

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