Virtual Admittance Reshaping Based Ripple Current Suppression Strategy of DC-Link Capacitors for PMSM Drives

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***Abstract*—In single-phase input permanent magnet synchronous motor (PMSM) drives, the dc-link electrolytic capacitors exhibit low tolerance to second-harmonic ripple current (SHRC). This limitation hinders further enhancements in system reliability and power density. Therefore, a ripple current suppression strategy of dc-link capacitors based on virtual admittance reshaping is proposed. The second-harmonic ripple characteristics of dc-link capacitors are characterized through admittance analysis. Based on system admittance modeling, a virtual path for the SHRC is established by paralleling admittance. In this way, the suppression degradation caused by the bandwidth limitation of traditional strategies can be mitigated. Moreover, the SHRC suppression rate is derived from the constant thermal power. On this basis, the virtual admittance parameters are designed, and the sensitivity is analyzed. The proposed strategy requires no additional hardware and exhibits low parameter sensitivity. Finally, the effectiveness of the proposed strategy is verified on the experimental platform with dc-link capacitance reduced by 70%.**

***Index Terms*—Admittance reshaping, electrolytic capacitor, permanent magnet synchronous motor (PMSM), second-harmonic ripple current (SHRC).**

I. Introduction

PERMANENT magnet synchronous motor (PMSM) has been extensively utilized in various fields, such as industry and transportation, due to its advantages of high power density, high efficiency, and good dynamic performance [1], [2], [3], [4], [5]. Aluminum electrolytic capacitors are usually used to balance power, absorb ripple current, and stabilize dc-link voltage [6], [7], [8], [9]. However, aluminum electrolytic capacitors exhibit low tolerance to ripple current, so they have become one of the weakest components in drive systems. Moreover, the smaller the capacitance, the poorer the tolerance. According to the statistics, about 60% of drive failures and 30% of converter failures are caused by the aging of electrolytic capacitors [10], [11], [12], [13]. Therefore, to improve system reliability and power density, it is necessary to suppress the ripple current of dc-link capacitors in PMSM drives.

In recent years, lots of research has been conducted to achieve the ripple current suppression of electrolytic capacitors. Based on the frequency range, the capacitor ripple current can be divided into the high-frequency ripple current and the low-frequency ripple current. Among them, the high-frequency ripple current is related to the switching action and can be suppressed by adjusting the switching mode of power devices [14], [15], [16], [17]. In [14], a direct pulse control strategy based on the finite-control-set model predictive control was proposed, which could achieve the high-frequency current pulse cancellation. In [15], To suppress the ripple current, the fluctuation of the inverter input current near its average value was minimized by avoiding the use of zero vectors. In [16], a hybrid-frequency phase-shift pulse width modulation strategy was proposed, which could simultaneously mitigate the ripple current on both sides of ac and dc. In [17], a carrier selection strategy for generalized discontinuous pulse width modulation was proposed, which could suppress the ripple current and maintain minimum switching losses. In summary, the high-frequency ripple current can be effectively suppressed by optimizing the switching strategy of power devices.

Due to the increase in equivalent series resistance (ESR) with decreasing frequency, electrolytic capacitors exhibit relatively poorer tolerance to low-frequency ripple currents [18]. In single-phase input PMSM drives, the second-harmonic ripple current (SHRC) is the main component of low-frequency ripple currents. Usually, the suppression strategies for the SHRC can be divided into hardware and software methods. The hardware methods suppress the ripple current by changing the hardware structure [19], [20], [21], [22], [23], [24], [25]. In [19], the dc-link voltage fluctuation was compensated by connecting a voltage source in series with the dc-link. The dc-link shunt compensator was used to suppress the capacitor ripple current in single-phase input

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[20] and three-phase input [21] motor drives, respectively. In [22], using a similar compensator, a hybrid one-cycle control strategy was proposed to ensure the stable operation of the system. To reduce the efficiency reduction caused by compensators, the flying-capacitor-clamped boost three-level converter was adopted as the dc converter in photovoltaic systems [23], [24]. The ripple current suppression strategies were studied in the maximum power point tracking mode [23] and the dc-link voltage regulation mode [24], respectively. In [25], a boost-based active power decoupling circuit with voltage compensation was proposed, and the dc-link voltage ripple was suppressed by connecting the decoupling capacitor in series with the boost capacitor. However, the additional hardware in the above strategies reduces both power density and cost-effectiveness.

To overcome the limitations of hardware methods, many scholars conduct research from the perspective of software algorithms [26], [27], [28], [29], [30], [31]. For LED drive systems, the SHRC suppression is achieved by a modest reduction in grid-side performance [26], [27], [28]. In [26], by injecting the third harmonic current on the grid side of the power factor correction (PFC) converter, the root mean square value of the capacitor ripple current was reduced. On this basis, the third and fifth harmonic currents were injected together to reduce the peak-to-average ratio of the output current [27]. In [28], to expand the application range, an adaptive harmonic injection strategy was proposed, which could reduce the capacitor ripple current under different power levels. For motor drive systems, the SHRC suppression is achieved by introducing power fluctuations on the motor side [29], [30], [31]. In [29] and [30], the second-harmonic current was injected to suppress the capacitor ripple current, which resulted in the torque fluctuation. On this basis, a harmonic injection strategy based on reactive power fluctuation was proposed [31], which suppresses the SHRC and reduces the torque fluctuation. However, for the above strategies based on harmonic injection, their suppression effect is often limited by the controller bandwidth.

The virtual impedance technology has been extensively utilized to improve system stability and enhance power quality, due to its flexibility, ease of implementation, and clear physical meaning [32], [33], [34], [35], [36], [37], [38]. In [32], an active damping method based on the virtual damping resistor was applied to suppress the *LC* resonance and improve the drive system stability. In [33], the harmonics at the inherent frequency were selectively suppressed by designing the impedance around the *LC* resonance frequency. On this basis, an adaptive virtual admittance reshaping-based resonance suppression strategy was proposed to achieve the optimal performance under different operating states [34]. In [35], a dc-link voltage feedback active damping control method was proposed to improve system stability, and the oversampling method was used to reduce the digital control delay. In [36], an active damping method was used to suppress harmonics in the grid current. In [37], based on a flexible active damping method, the damping ratio of the LCL resonance was freely designed by the proposed high-order partial-state feedback. In [38], the system stability was improved without the additional sensor based on the super-twisting sliding mode-based disturbance observer. However, the existing studies have not mentioned the suppression of capacitor ripple current by virtual impedance technology in PMSM drives fed by a PFC converter.

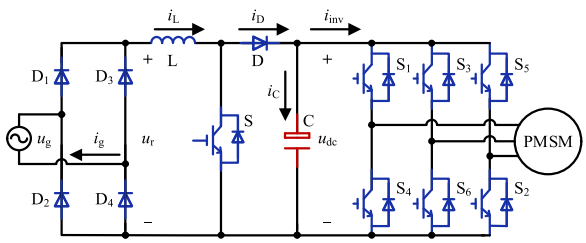

Fig. 1. Topology of PMSM drive fed by single-phase boost PFC converter.

In this article, a ripple current suppression strategy of dc-link capacitors based on virtual admittance reshaping for PMSM drives is proposed. The main contributions of the article are summarized as follows:

1) The second-harmonic ripple characteristics under different dc-link capacitors are analyzed using the system equivalent admittance model. Based on the admittance reshaping principle, a high-admittance path is established to suppress the capacitor ripple current by paralleling the virtual admittance. Equivalent admittance power required for admittance reshaping is generated by adding the admittance voltage commands to the original voltage commands, thereby reducing the algorithm complexity and the burden of current regulators.
2) The virtual admittance parameters are intentionally designed to be nonzero exclusively at twice the grid frequency, thereby selectively suppressing the SHRC of dc-link capacitors. The target suppression rate of SHRC is determined based on the constant thermal power principle. The optimal parameters minimizing the virtual admittance amplitude are calculated according to the suppression rate, thereby reducing the impact of equivalent admittance power on motor performance. Besides, the parameter sensitivity analysis demonstrates that the proposed strategy exhibits high robustness.

II. Analysis of the Second-Harmonic Ripple Characteristics of DC-Link Capacitors

The topology of PMSM drive fed by single-phase boost PFC converter is shown in Fig. 1. Under the action of the PFC converter, the capacitor current and dc-link voltage fluctuate at twice the grid frequency, which is referred to as the second-harmonic ripple characteristics of dc-link capacitors in this article.

To further analyze the second-harmonic ripple characteristics of dc-link capacitors, it is necessary to establish the system admittance model. By equating the PFC converter side and the dc-link capacitors as the input and output of the system, respectively, the admittance equivalent model of the PMSM drive can be obtained, as shown in Fig. 2. The admittance of dc-link capacitors can be expressed as

$$Y_C(s) = \frac{sC}{1 + sCR_C} \tag{1}$$

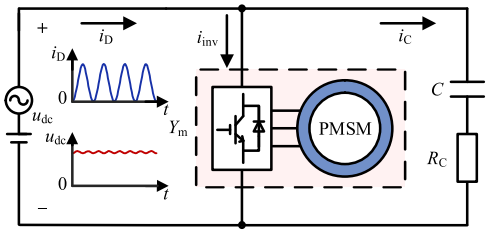

Fig. 2. Admittance equivalent model of PMSM drive.

where s represents the complex frequency, and C and R_C represent the capacitance and the ESR of dc-link capacitors, respectively.

Neglecting the inverter losses, according to (1), the transfer function from the diode current to the dc-link capacitor current can be expressed as

$$G(s) = \frac{Y_C(s)}{Y_C(s) + Y_m(s)} = \frac{sC}{sC + (1 + sCR_C)Y_m(s)} \tag{2}$$

where Y_m represents the motor admittance, as shown in (3), shown at the bottom of this page, and the detailed derivation process of (3) is provided in [32]. In (3), I_{inv}, U_{dc}, U_{dc_e}, U_{dref}, and U_{qref} represent the dc components of the inverter current, the dc-link voltage, the equivalent sampled dc-link voltage (delay of $1.5T_s$), the d-axis reference voltage, and the q-axis reference voltage, respectively. R_s, ω_e, T_s, and $L_{d,q}$ represent the stator resistance, the electrical angular velocity, the switching period, and the dq-axis inductances, respectively. $U_{d,q}$ and $I_{d,q}$ represent the dc components of dq-axis voltages and currents, respectively. G_d and G_q represent the transfer functions of dq-axis current controllers, respectively, and they can be expressed as

$$\begin{cases} G_d(s) = \omega_{cc} L_d + \frac{\omega_{cc} R_s}{s} \\ G_q(s) = \omega_{cc} L_q + \frac{\omega_{cc} R_s}{s} \end{cases} \tag{4}$$

where ω_{cc} represents the bandwidth of current controllers.

According to (2), the SHRC amplitude of dc-link capacitors can be calculated as

$$I_{C2} = I_{D2}\,|G(j\omega_2)| = \frac{P_m}{U_{dc}} \left| \frac{j\omega_2 C}{j\omega_2 C + (1 + j\omega_2 C R_C) Y_m(j\omega_2)} \right| \tag{5}$$

where j, ω_2, I_{D2}, and P_m represent the imaginary unit, twice the grid angular frequency, the SHRC amplitude of the diode, and the motor power. The motor power can be expressed as

$$P_m = \frac{3}{2}(U_d I_d + U_q I_q). \tag{6}$$

TABLE I
PARAMETERS OF EXPERIMENTAL PLATFORM

Parameter	Value	Parameter	Value
Grid voltage	220 Vrms	Grid frequency	50 Hz
DC-link voltage	350 V	Switching frequency	10 kHz
Stator resistance	0.78 Ω	D-axis inductance	5.4 mH
Flux linkage	0.11 Wb	Q-axis inductance	8.4 mH
Rotational inertia	0.3 g·m²	Number of pole pairs	3
Rated power	1200 W	Controller bandwidth	500 Hz
Original capacitance	1259.42 μF	Original ESR	56.31 mΩ
Capacitance of C_{e4}	379.32 μF	ESR of C_{e4}	303.51 mΩ

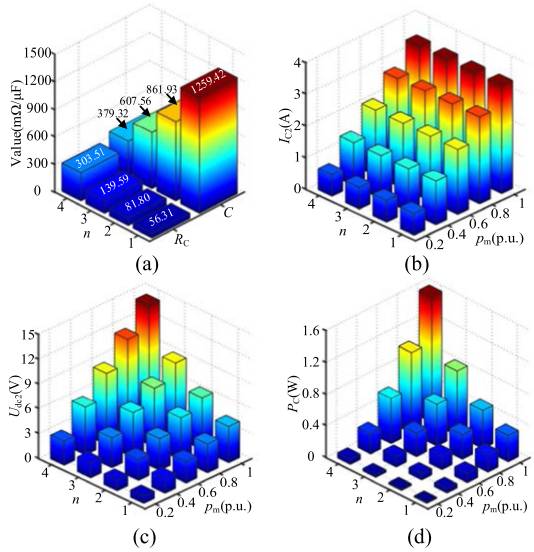

Fig. 3. Analysis of second-harmonic ripple characteristics under different DC-link capacitors. (a) Electrolytic capacitor parameters. (b) Second-harmonic ripple current. (c) Second-harmonic ripple voltage. (d) Power generated by the SHRC.

According to (5), the amplitude of the second-harmonic ripple voltage can be derived as

$$U_{dc2} = \frac{I_{C2}}{|Y_C(j\omega_2)|} = \frac{P_m}{U_{dc}} \left| \frac{1 + j\omega_2 C R_C}{j\omega_2 C + (1 + j\omega_2 C R_C) Y_m(j\omega_2)} \right|. \tag{7}$$

According to (5), the power generated by the SHRC can be derived as

$$P_C = \frac{I_{C2}^2 R_C}{2} = \frac{P_m^2 R_C}{2U_{dc}^2} \left| \frac{j\omega_2 C}{j\omega_2 C + (1 + j\omega_2 C R_C) Y_m(j\omega_2)} \right|^2. \tag{8}$$

The drive parameters are shown in Table I. The per-unit value of motor power is denoted as p_m, and the base value is set to the rated power of 1200 W. The parameters of different electrolytic capacitors C_{en} ($n = 1, 2, 3,$ and 4) are shown in Fig. 3(a), and the ESR increases as capacitance decreases. Under different n and p_m, I_{C2}, U_{dc2}, and P_C can be derived from (5), (7), and (8), as shown in Fig. 3(b)–(d), respectively. Combining Fig. 3(b) with

$$Y_m(s) = -\frac{I_{inv}}{U_{dc}} + \frac{3(1 - e^{-1.5T_s s})}{2U_{dc}U_{dc\_e}} \left\{ \begin{array}{l} \left[\frac{(R_s + L_d s)U_{dref}}{R_s + L_d s + G_d(s)} - \frac{\omega_e L_q U_{qref}}{R_s + L_q s + G_q(s)} \right] I_d + \frac{U_{dref} U_d}{R_s + L_d s + G_d(s)} \\ + \left[\frac{\omega_e L_d U_{dref}}{R_s + L_d s + G_d(s)} + \frac{(R_s + L_q s)U_{qref}}{R_s + L_q s + G_q(s)} \right] I_q + \frac{U_{qref} U_q}{R_s + L_q s + G_q(s)} \end{array} \right\}. \tag{3}$$

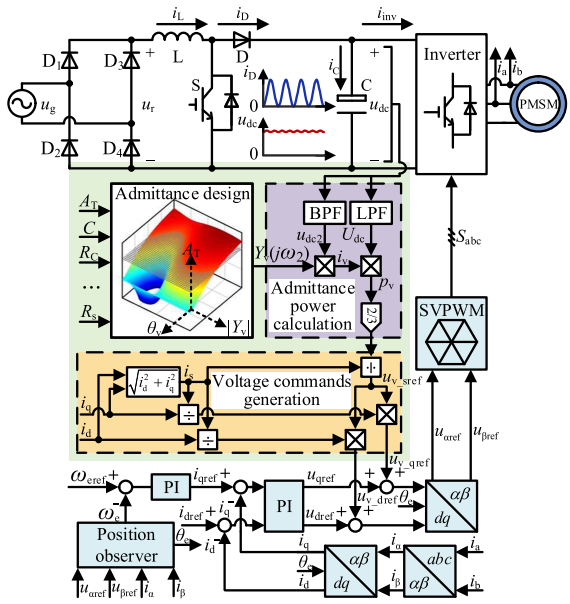

Fig. 4. Block diagram of the proposed SHRC suppression strategy based on virtual admittance parallel reshaping.

(d), when n remains unchanged, I_{C2} and P_C increase with p_m. When p_m remains unchanged, I_{C2} is not significantly affected by n. However, since the ESR of small-capacitance capacitors is larger, P_C increases with n. As shown in Fig. 3(c), when n remains unchanged, U_{dc2} increases with p_m. When p_m remains unchanged, U_{dc2} increases with n.

III. Ripple Current Suppression Strategy Based on Virtual Admittance Reshaping

A. Admittance Reshaping of Drive System

The proposed SHRC suppression strategy based on virtual admittance parallel reshaping is shown in Fig. 4. The strategy can be mainly divided into three parts: the admittance parameters design, the admittance power calculation, and the voltage commands generation. Firstly, the SHRC suppression rate is determined by maintaining constant SHRC-generated power. Next, the admittance parameters are designed based on the SHRC suppression rate and the system admittance equivalent model. Then, the admittance power is calculated based on the designed virtual admittance and the sampled dc-link voltage. On this basis, combining the dq-axis currents with admittance power, the voltage commands are obtained by aligning the admittance voltage vector with the stator current vector. Finally, the admittance voltage commands are added to the original voltage commands to establish a virtual path for SHRC, thereby achieving the SHRC suppression of dc-link capacitors.

The drive admittance equivalent model after paralleling virtual admittance is shown in Fig. 5. To suppress the SHRC of dc-link capacitors, the virtual admittance is paralleled to establish a high-admittance path, which promotes the diode SHRC to flow towards the motor side. The paralleled virtual admittance is zero except for the second-harmonic component, and the virtual

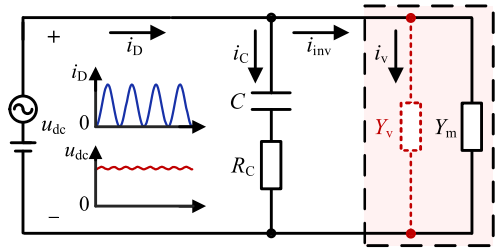

Fig. 5. Drive admittance equivalent model after paralleling virtual admittance.

admittance at twice the grid frequency can be expressed as

$$Y_v(j\omega_2) = |Y_v|\cos\theta_v + j|Y_v|\sin\theta_v \tag{9}$$

where $|Y_v|$ and θ_v represent the amplitude and the phase of virtual admittance at twice the grid frequency, respectively.

According to (9) and Ohm's law, the phasor form of virtual admittance second-harmonic current can be expressed as

$$\boldsymbol{I}_{v2} = Y_v(j\omega_2)\boldsymbol{U}_{dc2} = |Y_v|\,U_{dc2}\angle(\theta_v + \theta_{udc2}) \tag{10}$$

where $\boldsymbol{U}_{dc2}$ and θ_{udc2} represent the phasor form of dc-link second-harmonic voltage and the phase of $\boldsymbol{U}_{dc2}$, respectively.

Since the virtual admittance is designed to be zero except for the second-harmonic component, the admittance current is only the second-harmonic component. According to (10), the admittance current can be expressed as

$$i_v = i_{v2} = |Y_v|\,U_{dc2}\cos(\omega_2 t + \theta_v + \theta_{udc2}) \tag{11}$$

where i_{v2} and t represent the virtual admittance second-harmonic current and time, respectively. Because the phase of i_v leads that of u_{dc2}, the future value of u_{dc2} is replaced with the historical value from the previous cycle for i_v calculation.

Neglecting the high-frequency components of dc-link voltage, according to (11), the admittance power can be expressed as

$$p_v = i_v u_{dc} = |Y_v|\,U_{dc2}U_{dc}\cos(\omega_2 t + \theta_v + \theta_{udc2}) \tag{12}$$

where u_{dc} represents the dc-link voltage.

According to (12), it is necessary to generate the corresponding admittance power for admittance reshaping. To relieve the burden of dq-axis current controllers, the admittance power is generated by adding the admittance voltage commands to the original voltage commands. Moreover, the admittance voltage vector is aligned with the stator current vector, which can be expressed as

$$u_{v\_sref} = \frac{2p_v}{3i_s} = \frac{2\,|Y_v|\,U_{dc2}U_{dc}}{3\sqrt{i_d^2+i_q^2}}\cos(\omega_2 t + \theta_v + \theta_{udc2}) \tag{13}$$

where i_s represents the stator current.

Therefore, according to (13), the dq-axis admittance voltage commands are expressed as

$$\begin{cases} u_{v\_dref} = u_{v\_sref}\dfrac{i_d}{i_s} = \dfrac{2|Y_v|U_{dc2}U_{dc}i_d}{3(i_d^2+i_q^2)}\cos(\omega_2 t + \theta_v + \theta_{udc2}) \\ u_{v\_qref} = u_{v\_sref}\dfrac{i_q}{i_s} = \dfrac{2|Y_v|U_{dc2}U_{dc}i_q}{3(i_d^2+i_q^2)}\cos(\omega_2 t + \theta_v + \theta_{udc2}) \end{cases} \tag{14}$$

where i_d and i_q represent the dq-axis currents, respectively.

The dc component and the second-harmonic component of dc-link voltage can be obtained by the low-pass filter and the bandpass filter (BPF), respectively. The transfer function of the BPF can be expressed as

$$H(s) = \frac{2\xi\omega_{\mathrm{n}} s}{s^2 + 2\xi\omega_{\mathrm{n}} s + \omega_{\mathrm{n}}^2} \tag{15}$$

where ω_{n} represents the center angular frequency set to 200π rad/s, and ξ represents the damping ratio set to 0.05, corresponding to a bandwidth of 10 Hz. The BPF is digitally implemented via the bilinear transform with a 10 kHz sampling frequency.

B. Admittance Parameters Design

After the admittance reshaping, at twice the grid frequency, the transfer function from the diode current to the dc-link capacitor current can be expressed as

$$\begin{aligned} G_{\mathrm{v}}(j\omega_2) &= \frac{Y_{\mathrm{C}}(j\omega_2)}{Y_{\mathrm{C}}(j\omega_2) + Y_{\mathrm{m}}(j\omega_2) + Y_{\mathrm{v}}(j\omega_2)} \\ &= \frac{j\omega_2 C}{\begin{array}{l} j\omega_2 C + (1 + j\omega_2 C R_{\mathrm{C}})[Y_{\mathrm{m}}(j\omega_2) \\ +|Y_{\mathrm{v}}|\cos\theta_{\mathrm{v}} + j|Y_{\mathrm{v}}|\sin\theta_{\mathrm{v}}] \end{array}}. \end{aligned} \tag{16}$$

Combining (5) with (16), the SHRC amplitude of dc-link capacitors after admittance reshaping can be derived as

$$\begin{aligned} I_{\mathrm{C2\_v}} &= \frac{P_{\mathrm{m}}}{U_{\mathrm{dc}}} |G_{\mathrm{v}}(j\omega_2)| \\ &= \frac{P_{\mathrm{m}}}{U_{\mathrm{dc}}} \left| \frac{j\omega_2 C}{\begin{array}{l} j\omega_2 C + (1 + j\omega_2 C R_{\mathrm{C}})[Y_{\mathrm{m}}(j\omega_2) \\ +|Y_{\mathrm{v}}|\cos\theta_{\mathrm{v}} + j|Y_{\mathrm{v}}|\sin\theta_{\mathrm{v}}] \end{array}} \right|. \end{aligned} \tag{17}$$

Similarly, after admittance reshaping, the amplitude of the second-harmonic ripple voltage can be derived as

$$\begin{aligned} U_{\mathrm{dc2\_v}} &= \frac{P_{\mathrm{m}} |G_{\mathrm{v}}(j\omega_2)|}{U_{\mathrm{dc}} |Y_{\mathrm{C}}(j\omega_2)|} \\ &= \frac{P_{\mathrm{m}}}{U_{\mathrm{dc}}} \left| \frac{1 + j\omega_2 C R_{\mathrm{C}}}{\begin{array}{l} j\omega_2 C + (1 + j\omega_2 C R_{\mathrm{C}})[Y_{\mathrm{m}}(j\omega_2) \\ +|Y_{\mathrm{v}}|\cos\theta_{\mathrm{v}} + j|Y_{\mathrm{v}}|\sin\theta_{\mathrm{v}}] \end{array}} \right|. \end{aligned} \tag{18}$$

When the system operates stably at a certain power, $|Y_{\mathrm{C}}(j\omega_2)|$, P_{m}, and U_{dc} are approximately constant. According to (17) and (18), $I_{\mathrm{C2\_v}}$ and $U_{\mathrm{dc2\_v}}$ decrease with $|G_{\mathrm{v}}(j\omega_2)|$. The expression for SHRC suppression rate is defined as follows:

$$\begin{aligned} A &= 1 - \frac{|G_{\mathrm{v}}(j\omega_2)|}{|G(j\omega_2)|} \\ &= 1 - \left| \frac{j\omega_2 C + (1 + j\omega_2 C R_{\mathrm{C}}) Y_{\mathrm{m}}(j\omega_2)}{\begin{array}{l} j\omega_2 C + (1 + j\omega_2 C R_{\mathrm{C}})[Y_{\mathrm{m}}(j\omega_2) \\ +|Y_{\mathrm{v}}|\cos\theta_{\mathrm{v}} + j|Y_{\mathrm{v}}|\sin\theta_{\mathrm{v}}] \end{array}} \right|. \end{aligned} \tag{19}$$

According to (19), the SHRC suppression ability decreases with A. When A is less than zero, the SHRC increases in the reverse direction after admittance reshaping. To improve the power density, the smaller electrolytic capacitors C_{e4} (379.32 μF, 303.51 mΩ) are used to replace the original dc-link capacitors C_{e1} (1259.42 μF, 56.31 mΩ). The capacitance decreases to 30.1% of the original value, and the ESR increases to 5.39 times the original value. Therefore, to keep the thermal power caused by SHRC unchanged, the target suppression rate of SHRC A_{T} can be calculated to be 0.569.

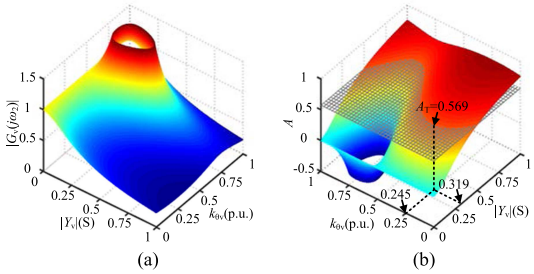

Fig. 6. Effect of admittance parameters on the SHRC suppression. (a) SHRC transfer function $|G_{\mathrm{v}}(j\omega_2)|$. (b) SHRC suppression rate A.

The drive parameters are shown in Table I. The per-unit value of virtual admittance phase is denoted as $k_{\theta\mathrm{v}}$, and the base value is 2π. According to (16) and (19), when the system operates at the rated power, the SHRC transfer function $|G_{\mathrm{v}}(j\omega_2)|$ and the SHRC suppression rate A can be obtained under different $|Y_{\mathrm{v}}|$ and $k_{\theta\mathrm{v}}$, as shown in Fig. 6. As shown in Fig. 6(a), when $|Y_{\mathrm{v}}|$ remains unchanged, with $k_{\theta\mathrm{v}}$ increasing, $|G_{\mathrm{v}}(j\omega_2)|$ first decreases, then increases, and then decreases again. When $k_{\theta\mathrm{v}}$ remains unchanged, $|G_{\mathrm{v}}(j\omega_2)|$ decreases as $|Y_{\mathrm{v}}|$ increases. As shown in Fig. 6(b), when $|Y_{\mathrm{v}}|$ remains unchanged, with $k_{\theta\mathrm{v}}$ increasing, A first increases, then decreases, and then increases again. When $k_{\theta\mathrm{v}}$ remains unchanged, A increases with $|Y_{\mathrm{v}}|$. Therefore, it is necessary to select the appropriate admittance parameters for the SHRC suppression. The inappropriate admittance parameters make A less than zero, which not only fails to suppress the SHRC but even results in an increase in the SHRC. In addition, the smaller the admittance amplitude, the smaller the impact on the motor side [33]. Finally, the amplitude and phase of virtual admittance are selected as 0.319 S and 0.245 p.u., respectively.

The drive parameters are shown in Table I. According to (5), (7), (17), and (18), under different power levels p_{m}, the second-harmonic ripple components of dc-link voltage (U_{dc2}, $U_{\mathrm{dc2\_v}}$) and the capacitor current (I_{C2}, $I_{\mathrm{C2\_v}}$) can be obtained before and after admittance reshaping, as shown in Fig. 7. In Fig. 7, after admittance reshaping, the second-harmonic ripple components of dc-link voltage and capacitor current are effectively suppressed.

C. Parameter Sensitivity Analysis

In practical systems, considering nonideal factors such as the controller bandwidth and parametric nonlinearity, the performance of the proposed strategy may deviate from the theoretical design. Therefore, it is necessary to analyze the parameter sensitivity.

To analyze the effect of above factors on the SHRC suppression, the expression of related system parameter is defined as

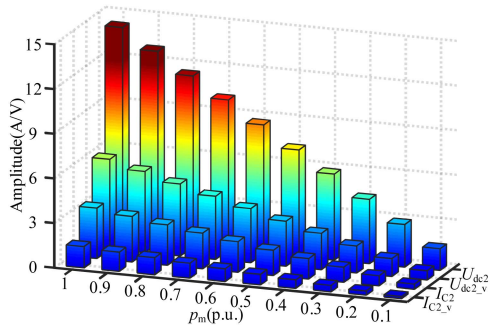

Fig. 7. Comparison of the second-harmonic ripple components of dc-link voltage and capacitor current before and after admittance reshaping.

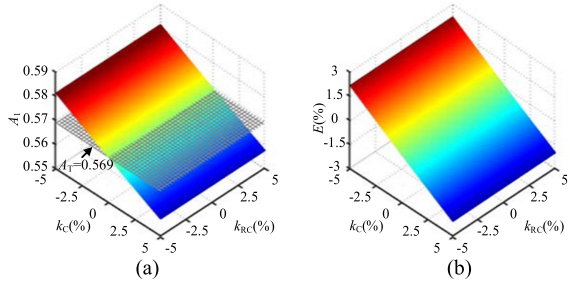

Fig. 8. Effect of C and R_C on the SHRC suppression. (a) SHRC suppression rate A_1. (b) Percentage error E.

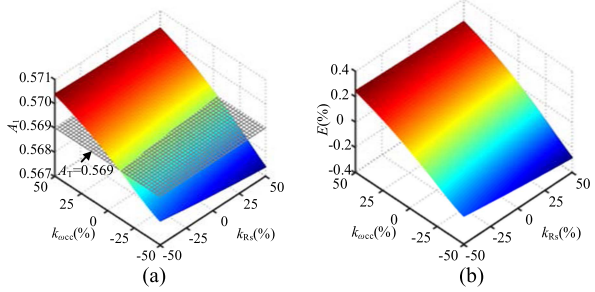

Fig. 9. Effect of ω_{cc} and R_s on the SHRC suppression. (a) SHRC suppression rate A_1. (b) Percentage error E.

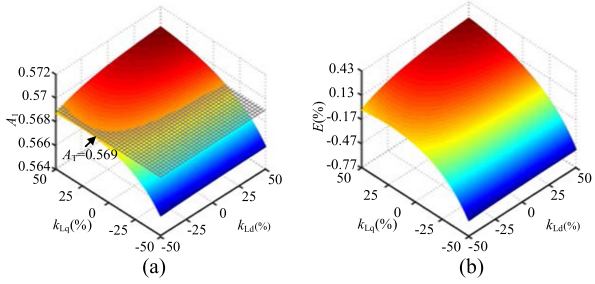

Fig. 10. Effect of L_d and L_q on the SHRC suppression. (a) SHRC suppression rate A_1. (b) Percentage error E.

follows:

$$X_1 = X(1 + k_X) \tag{20}$$

where k_X represents the change rate of X considering nonideal factors, X represents one of ω_{cc}, C, R_C, R_s, L_d, and L_q.

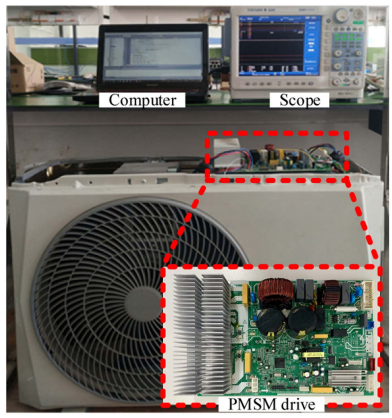

Fig. 11. Experimental platform of permanent magnet compressor system driven by boost PFC converter.

Substituting (20) into (3), the input admittance of the motor considering nonideal factors Y_{m1} can be obtained. Combining with (19), the SHRC suppression rate considering nonideal factors can be expressed as

$$A_1 = 1 - \left| \frac{j\omega_2 C_1 + (1 + j\omega_2 C_1 R_{C1}) Y_{m1}(j\omega_2)}{j\omega_2 C_1 + (1 + j\omega_2 C_1 R_{C1})[Y_{m1}(j\omega_2) + |Y_v| \cos\theta_v + j|Y_v| \sin\theta_v]} \right|. \tag{21}$$

According to (19) and (21), the percentage error caused by nonideal factors can be derived as

$$E = \left(\frac{A_1}{A_T} - 1 \right) \times 100\%. \tag{22}$$

The drive parameters are shown in Table I. Under different k_C, k_{RC}, $k_{\omega cc}$, k_{Rs}, k_{Ld}, and k_{Lq}, according to (21) and (22), the SHRC suppression rate A_1 and the percentage error E can be obtained, as shown in Figs. 8–10, respectively. As shown in Fig. 8(a), when k_C remains unchanged, A_1 is not significantly affected by k_{RC}. When k_{RC} remains unchanged, A_1 decreases as k_C increases. From Fig. 8(b), when C and R_C change within $\pm 5\%$, the percentage error E is less than 3%. In Fig. 9(a), when ω_{cc} remains unchanged, A_1 is not significantly affected by k_{Rs}. When k_{Rs} remains unchanged, A_1 increases with ω_{cc}. As presented in Fig. 9(b), when ω_{cc} and R_s change within $\pm 50\%$, the percentage error E is less than 0.4%. From Fig. 10(a), when k_{Ld} remains unchanged, A_1 increases with k_{Lq}. When k_{Lq} remains unchanged, A_1 increases with k_{Ld}. As shown in Fig. 10(b), when L_d and L_q change within $\pm 50\%$, the percentage error E is less than 0.8%. Therefore, the nonideal factors such as the controller bandwidth and parametric nonlinearity have little influence on the SHRC suppression. The used parameters in the strategy can be directly selected as constant nameplate values.

IV. Experimental Results

The proposed strategy was verified on the experimental platform of a permanent magnet compressor system driven by a boost PFC converter, as shown in Fig. 11. The parameters of the experimental platform are shown in Table I. The smaller electrolytic capacitors C_{e4} (379.32 μF, 303.51 mΩ) are used

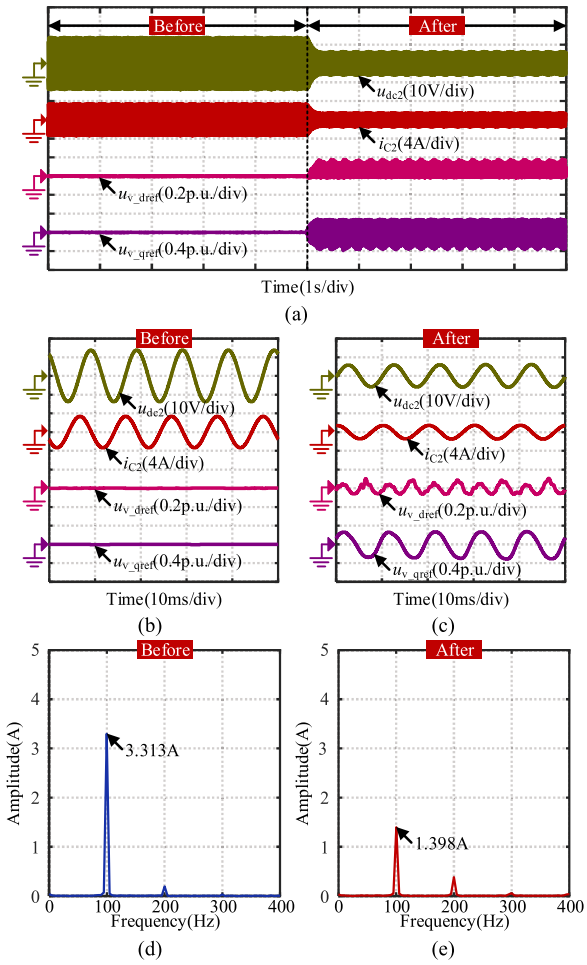

Fig. 12. Experimental results at the rated power (1200 W). (a) Overall waveforms. (b) Zoomed waveforms (before). (c) Zoomed waveforms (after). (d) FFT analysis of capacitor current (before). (e) FFT analysis of capacitor current (after).

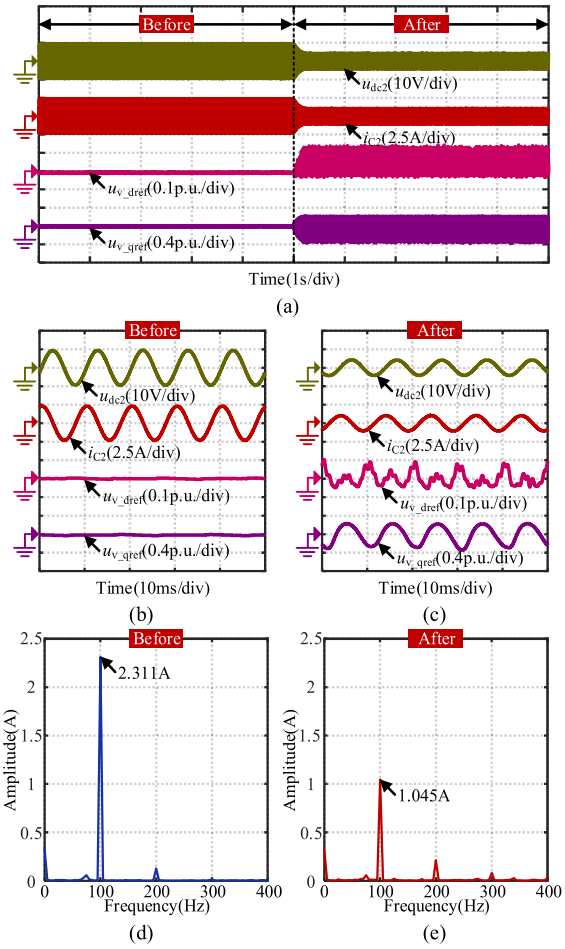

Fig. 13. Experimental results at 70% rated power (840 W). (a) Overall waveforms. (b) Zoomed waveforms (before). (c) Zoomed waveforms (after). (d) FFT analysis of capacitor current (before). (e) FFT analysis of capacitor current (after).

to replace the original dc-link capacitors C_{e1} (1259.42 μF, 56.31 mΩ). The proposed strategy utilizes the existing resources in the boost PFC converter to suppress the SHRC, and the control algorithm is executed by the R5F562T7DDF microcontroller of Renesas RX62T series with the switching frequency of 10 kHz. The sampling delay is compensated to reduce the impact on the virtual admittance phase.

To verify the effectiveness of the proposed strategy, the experimental results when the motor operates at the rated power are shown in Fig. 12. As shown in Fig. 12(a)–(c), the fluctuations of the capacitor current and dc-link voltage are significantly reduced. According to Fig. 12(d) and (e), before adopting the suppression strategy, the SHRC amplitude of dc-link capacitors is 3.313 A; after adopting the suppression strategy, the SHRC amplitude of dc-link capacitors is reduced to 1.398 A. The SHRC suppression rate is 0.578, which is slightly larger than the designed value of 0.569.

To verify the effectiveness of the proposed strategy under different load conditions, the experimental results when the motor operates at 70% rated power are shown in Fig. 13. As shown in Fig. 13(a)–(c), the fluctuations of the capacitor current and dc-link voltage can still be effectively reduced. According to Fig. 12(d) and (e), before adopting the suppression strategy, the SHRC amplitude of dc-link capacitors is 2.311 A; after adopting the suppression strategy, the SHRC amplitude of dc-link capacitors is reduced to 1.045 A. The SHRC suppression rate is 0.548, which is relatively close to the designed value of 0.569. Therefore, when the motor operates at 70% rated power, the proposed strategy can still effectively suppress the SHRC.

To verify the effectiveness of the proposed strategy under light load, the experimental results when the motor operates at 10% rated power are shown in Fig. 14. As shown in Fig. 14(a)–(c), the fluctuations of the capacitor current and dc-link voltage can still be effectively reduced. According to Fig. 14(d) and (e), before adopting the suppression strategy, the SHRC amplitude of dc-link capacitors is 0.421 A; after adopting the suppression strategy, the SHRC amplitude of dc-link capacitors is reduced to 0.207 A. The SHRC suppression rate is 0.508, which is slightly larger than the designed value of 0.569. The SHRC amplitude of dc-link capacitors is relatively small under light load. Therefore, a slight decrease in the SHRC suppression ability is also acceptable.

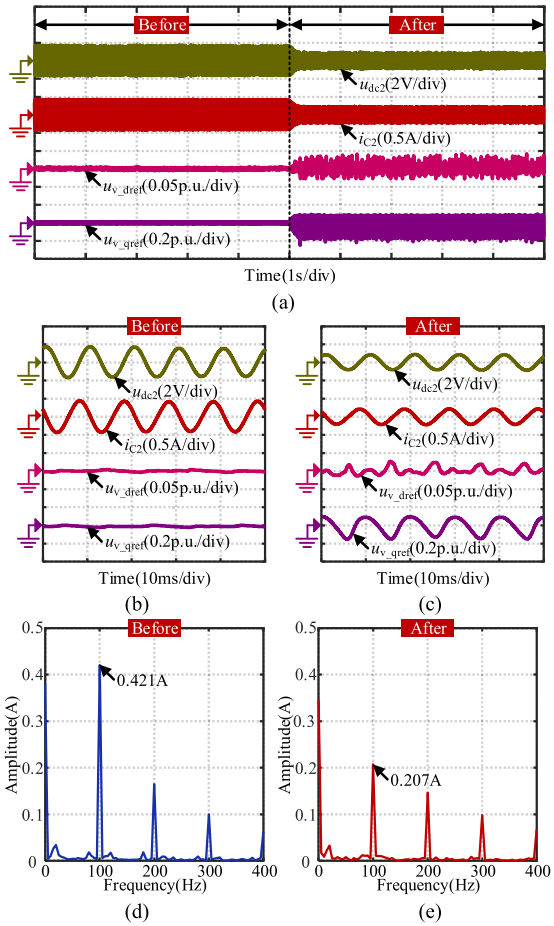

Fig. 14. Experimental results at 10% rated power (120 W). (a) Overall waveforms. (b) Zoomed waveforms (before). (c) Zoomed waveforms (after). (d) FFT analysis of capacitor current (before). (e) FFT analysis of capacitor current (after).

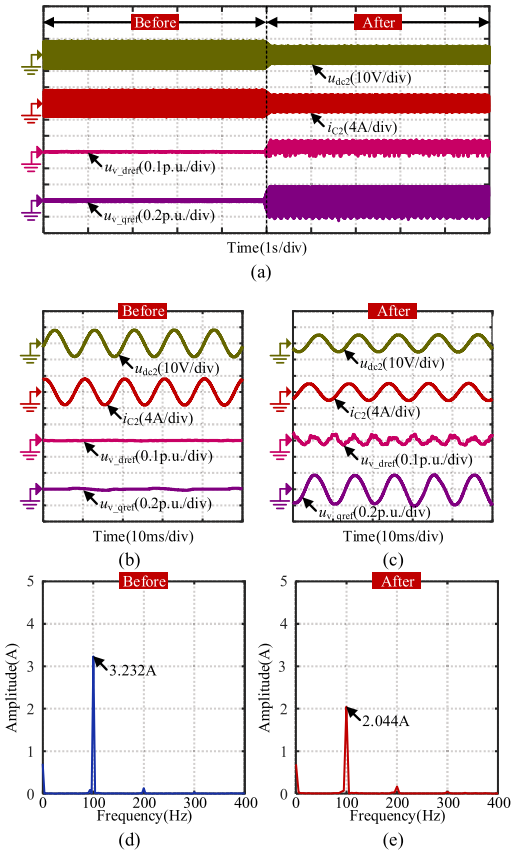

Fig. 15. Experimental results at the rated power (1200 W) using C_{e3} (607.56 μF, 139.59 mΩ). (a) Overall waveforms. (b) Zoomed waveforms (before). (c) Zoomed waveforms (after). (d) FFT analysis of capacitor current (before). (e) FFT analysis of capacitor current (after).

To verify the effectiveness of the proposed strategy under other capacitor conditions, the experimental results at the rated power (1200 W) using C_{e3} (607.56 μF, 139.59 mΩ) are shown in Fig. 15. When the electrolytic capacitors C_{e3} (607.56 μF, 139.59 mΩ) are used to replace the original dc-link capacitors C_{e1} (1259.42 μF, 56.31 mΩ), the target suppression rate is 0.365, and the amplitude and phase of virtual admittance are designed as 0.236 S and 0.244 p.u., respectively. As shown in Fig. 15(a)–(c), the fluctuations of the capacitor current and dc-link voltage are significantly reduced. According to Fig. 15(d) and (e), before adopting the strategy, the SHRC amplitude of dc-link capacitors is 3.232 A; after adopting the strategy, the SHRC amplitude of dc-link capacitors is reduced to 2.044 A. The SHRC suppression rate is 0.368, which is slightly larger than the designed value of 0.365.

To verify the practicality of the proposed strategy under grid conditions, the experimental results when the motor operates at the rated power are shown in Fig. 16. In Fig. 16(a), the grid voltage contains many harmonics, and the amplitude of the fundamental component is 320V, which is greater than the theoretical value (311 V). As shown in Fig. 16(b)–(d), the fluctuations of the capacitor current and dc-link voltage are significantly reduced. According to Fig. 16(e) and (f), before adopting the suppression strategy, the SHRC amplitude of dc-link capacitors is 3.214 A; after adopting the suppression strategy, the SHRC amplitude of dc-link capacitors is reduced to 1.375 A. Therefore, the proposed strategy can effectively suppress the SHRC under grid conditions, and the suppression rate is 0.572.

To verify the robustness of the proposed strategy to temperature, the thermal imaging device (UTi320E) is used to measure temperature. Due to the lack of constant temperature experimental conditions, the system continuously operates at the rated power with the cooling fan disabled to simulate the temperature variations. The experimental results after 6-minute continuous operation at the rated power (1200 W) are shown in Fig. 17. As shown in Fig. 17(a) and (b), the maximum temperature increases from 46.2°C to 76.1°C. According to Fig. 17(f) and (g), the SHRC amplitudes of dc-link capacitors before and after adopting the strategy are 3.421 A and 1.472 A, respectively, and the suppression rate is 0.570. Therefore, the proposed strategy exhibits good robustness under different temperature conditions.

The fluctuating admittance power as shown in (12) inevitably generates the dq-axis current harmonics, resulting in an increase in motor torque ripple. To analyze the impact of the proposed strategy on torque ripple, the experimental results on torque ripple at the rated power (1200 W) are shown in

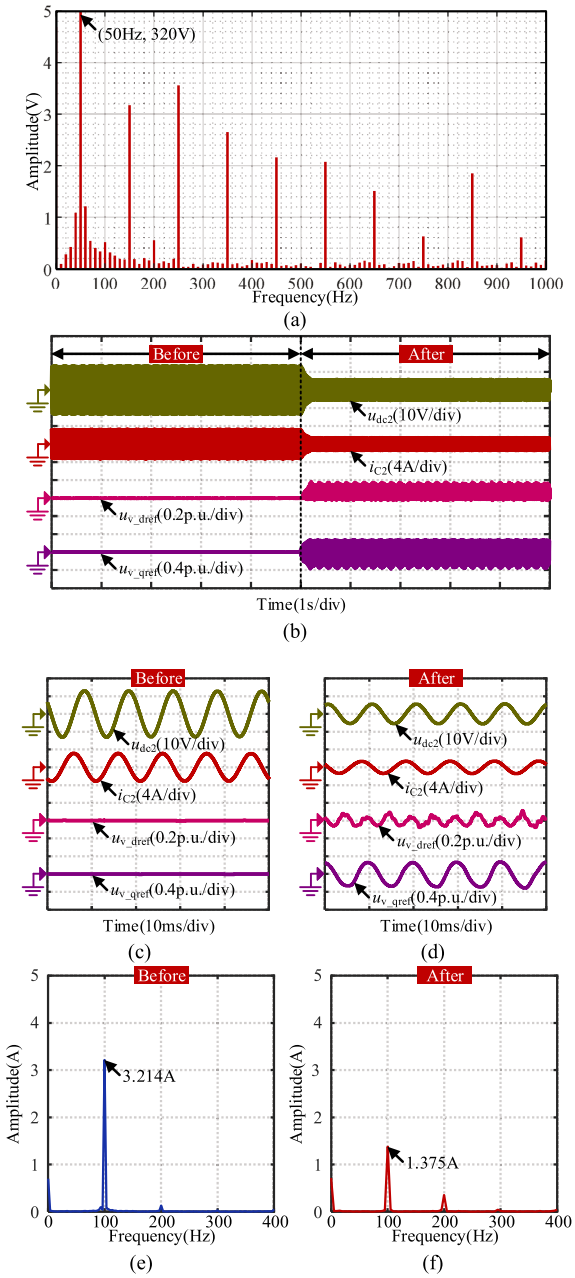

Fig. 16. Experimental results at the rated power (1200 W) under grid conditions. (a) FFT analysis of grid voltage. (b) Overall waveforms. (c) Zoomed waveforms (before). (d) Zoomed waveforms (after). (e) FFT analysis of capacitor current (before). (f) FFT analysis of capacitor current (after).

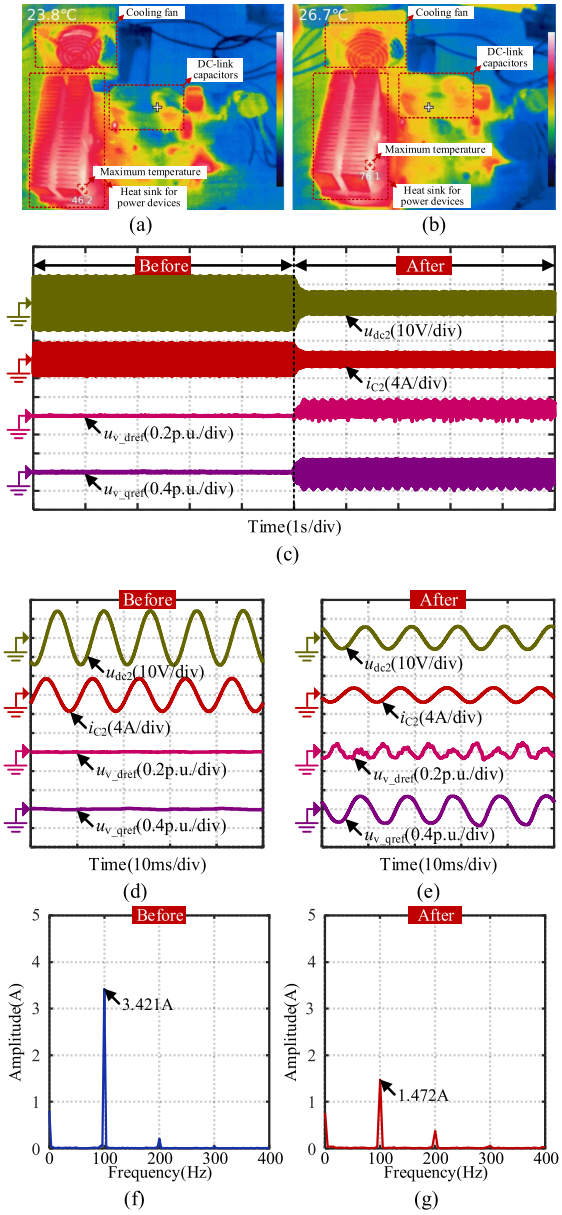

Fig. 17. Experimental results after 6-minute continuous operation at the rated power (1200 W). (a) Thermal imaging (initial). (b) Thermal imaging. (c) Overall waveforms. (d) Zoomed waveforms (before). (e) Zoomed waveforms (after). (f) FFT analysis of capacitor current (before). (g) FFT analysis of capacitor current (after).

Fig. 18. As shown in Fig. 18(a), the peak-to-peak torque ripple is 3.9 N·m and 6.6 N·m before and after adopting the proposed strategy, respectively. The peak-to-peak torque ripple increases to 1.69 times the initial value. As shown in Fig. 18(b) and (c), the second-harmonic components of dq-axis current increase after adopting the proposed strategy.

To verify the effectiveness of the proposed strategy during power changes, the experimental results when the motor operates between 360 and 600W are shown in Fig. 19. In Fig. 19, P_g represents the dc component of the grid power. In Fig. 19(a), before adopting the suppression strategy, the fluctuations of the capacitor current and dc-link voltage increase with the power increasing. According to Fig. 19(b), after adopting the suppression strategy, the fluctuations of the capacitor current and dc-link voltage are significantly reduced. Therefore, the proposed strategy shows good adaptability during power changes and can still suppress the SHRC effectively.

To further verify the effectiveness of the proposed strategy under sudden transient conditions, the experimental results when the motor operates between 360 and 840 W are shown in Fig. 20. The power variation increases to twice the original value (240–480 W), and the transition time decreases to approximately one-fifth the original value (10–2 s). In Fig. 20(a),

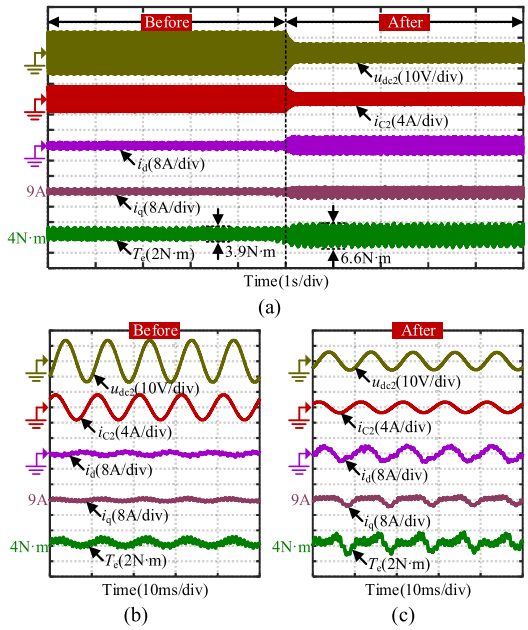

Fig. 18. Experimental results on torque ripple (1200W). (a) Overall waveforms. (b) Zoomed waveforms (before). (c) Zoomed waveforms (after).

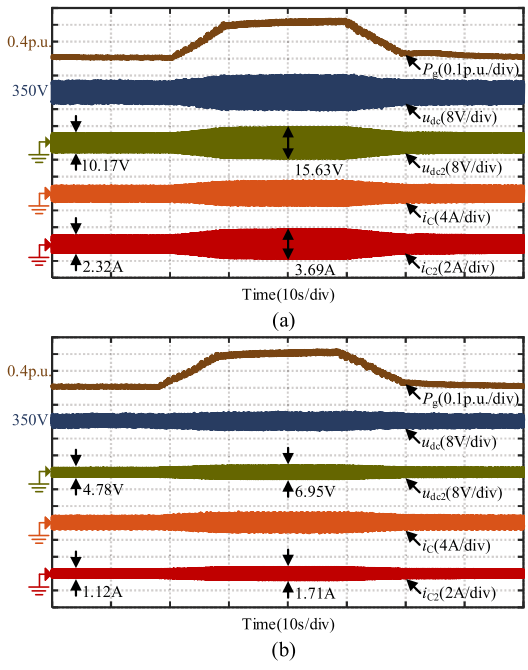

Fig. 19. Experimental results during power changes (360–600 W). (a) Disabled strategy. (b) Enabled strategy.

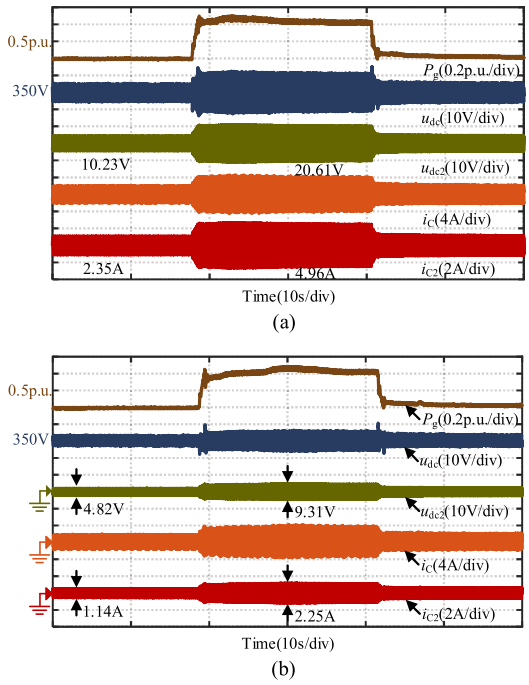

Fig. 20. Experimental results during power changes (360–840 W). (a) Disabled strategy. (b) Enabled strategy.

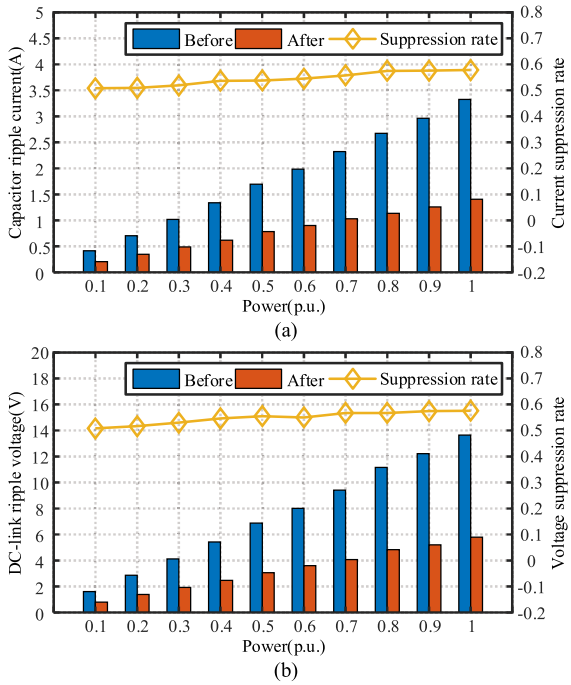

Fig. 21. Experimental results under different power levels. (a) Capacitor ripple current. (b) DC-link ripple voltage.

before adopting the suppression strategy, the fluctuations of the capacitor current and dc-link voltage increase with the power increasing. In Fig. 20(b), after adopting the suppression strategy, the fluctuations of the capacitor current and dc-link voltage are still significantly reduced.

To further verify the effectiveness of the proposed strategy under different power levels, when the grid power changes from 120 to 1200 W in steps of 120 W, the experimental results are shown in Fig. 21. To minimize the error, the experimental waveforms within 0.1 s are analyzed. As shown in Fig. 21, the proposed strategy has a good ripple suppression effect under different power levels, and the ripple suppression rate is larger than 0.5. In addition, since the second-harmonic current of the inverter increases with the power, the ripple suppression rates of the capacitor current and dc-link voltage increase with the power.

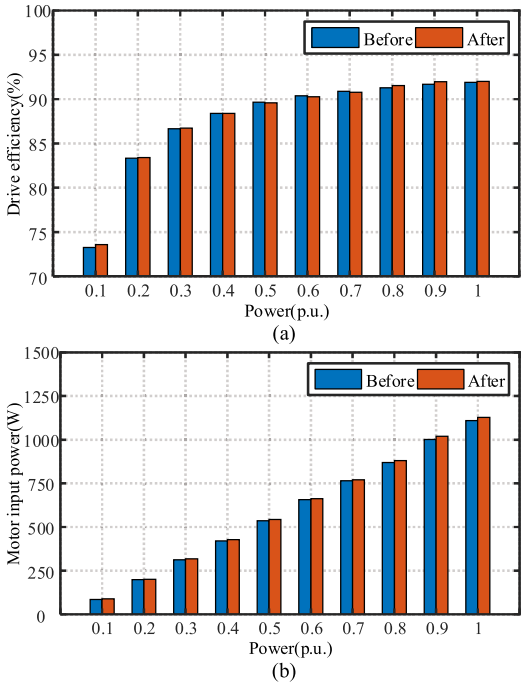

Fig. 22. Experimental results on additional losses. (a) Drive efficiency. (b) Motor input power.

TABLE II
TYPICAL RIPPLE CURRENT SUPPRESSION STRATEGIES

Reference	Algorithm (complexity)	Additional hardware
[23]	Virtual impedance technology and multi-loop control (medium)	Flying capacitor
[24]	Voltage control plus load-current feed-forward (low)	Flying capacitor
[25]	Instantaneous current control and voltage complementary control (low)	Boost-based active power decoupling circuit
[28]	Enhanced automatic power decoupling control. (medium)	N/A
[31]	Recursive algorithm (high)	N/A
Proposed	Virtual admittance reshaping (low)	N/A

To verify the impact of the proposed strategy on additional losses, the experimental results at different power levels are shown in Fig. 22. Assuming that the motor output power remains unchanged in a short time, the motor losses can be analyzed by the changes in the motor input power. In Fig. 22(a), the drive efficiency changes very little before and after adopting the strategy, indicating that the additional losses of the inverter are approximately equal to the reduced losses of the dc-link capacitors. In Fig. 22(b), although the motor input power slightly increases after adopting the strategy, which is still within an acceptable range.

To verify the novelty of the proposed strategy, it is necessary to compare it with existing strategies. The typical ripple current suppression strategies of dc-link capacitors are summarized in Table II. As shown in Table II, these existing strategies are usually confronted with challenges such as increased hardware costs or complex algorithm implementation. Compared with the existing strategies, the proposed strategy demonstrates the advantages of low cost and easy implementation.

V. CONCLUSION

In this article, a ripple current suppression strategy of dc-link capacitors based on virtual admittance reshaping for PMSM drives has been proposed. Based on the system admittance modeling, the variation patterns of the second-harmonic current, voltage, and power under different dc-link capacitors are revealed. By paralleling the virtual admittance, the transfer function from the diode current to the dc-link capacitor current is reshaped, thereby achieving the SHRC suppression of dc-link capacitors. According to the principle of constant thermal power, the SHRC suppression rate and virtual admittance parameters are determined. In addition, by analyzing the parameter sensitivity, it is concluded that the proposed strategy has stronger robustness. The experimental results show that when the dc-link capacitance decreases to 30%, the ripple suppression rate is larger than 0.5 across a wide power range. Compared with the existing strategies, the proposed strategy has the advantages of low cost and easy implementation, because it does not require additional hardware devices.

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