# Totem Pole Dual Output Bridgeless Rectifier for High-Performance Low Power SRM Drive

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***Abstract*—This article presents the analysis and design of totem pole bridgeless dual output (TPBLDO) power factor correction (PFC) converter to improve power quality of switched reluctance motor (SRM) system used in low-power applications. To provide efficient PFC with supply fluctuation and variable dc link voltage for SRM drive speed regulation, presented TPBLDO rectifier incorporates a nonisolated ac–dc converter. Here, the TPBLDO rectifier is designed to work in discontinuous mode, ensuring compliance with inherent grid power quality, reducing inductor size, and facilitating adaptability for low-power, low-cost applications by requiring only one sensor. In addition, DCM operation enables high-frequency diodes to be switched OFF and switches to be turned ON with zero current, based on the zero current switching operation principle for the designed bridgeless dual output PFC converter. TPBLDO converter-assisted SRM drive's working modes, component selection, and control are discussed in detail and its performance is initially verified with MATLAB simulation. Then, a proof-of-concept is validated through a hardware test bench at 400-W SRM drive. Finally, relevant results are outlined effectiveness in maintaining power quality as per IEC standard and wide-speed SRM control in low-power applications.**

***Index Terms*—Bridgeless (BL) rectifier, discontinuous current mode, dual output converter, low power applications, power quality standards, switched reluctance motor (SRM).**

## I. Introduction

OVER the past few decades, it has become evident that energy consumption for low-power applications in household or industrial equipment is a significant concern. Consequently, there is a growing necessity to enhance reliability, cost acceptability, and energy efficiency of low-power appliances. Considering current environmental impacts, energy-efficient appliances are getting attention from governments and researchers worldwide. In low-power domestic and industrial applications, motor-based equipment is prominent. So, market for motors in home and industrial appliances is experiencing fast evolution, driven by a strong focus on energy efficiency, technical developments, and adherence to regulations [1], [2]. Previously, induction motors (IMs) are often used in low-power appliances such as fans, water pumping, blowers, simple machine tools, etc. Major issues that diminish adaptability of IMs in energy-efficient low-power appliances include low power factor (PF), difficult variable speed operation, low power density, and poor efficiency [3], [4]. Advancements in power electronic switches and high-grade magnetic materials lead to an efficient replacement of IMs by permanent magnet (PM) motors in low-power applications [5], [6]. Despite high efficiency of PM motors, they are not cost-effective. The gradual loss of magnet performance is a major drawback of these systems. Hence, current research endeavors to provide a cost-effective solution that upholds performance benchmarks. In addition to PM motor's benefits, switched reluctance motor (SRM) motors, feature a simple structure with no winding and magnet-less rotor and are an excellent alternative to IMs and PM motors in low-power applications. Moreover, SRMs provide efficiency and high-power density close to PM motors [7], [8].

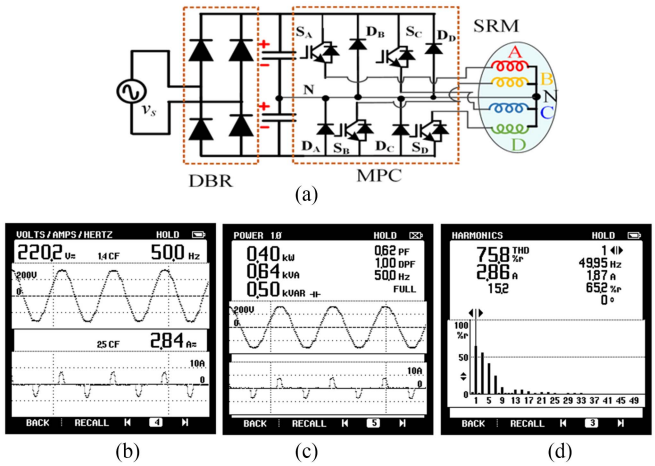


Fig. 1. Traditional DBR fed SRM drive. (a) Drive structure. (b) $v_s$ and $i_s$. (c) Power rating and PF. (d) Current THD with harmonics.

Conventionally, diode bridge rectifier (DBR) is connected to grid front end and provides dc link voltage for mid-point converter (MPC) assisted with switched reluctance motor (SRM) drive. DC link voltage achieved from DBR is constant and provides an uncontrolled SRM drive operation. An uncontrolled DBR-fed SRM drive configuration is illustrated in Fig. 1(a), as detailed in [9]. Supply current THD for DBR fed 6/4 SRM drive is 71.25% as discussed in [10]. In addition, in developed laboratory setup, significant distortion in grid current of DBR fed SRM drive system results in a high total harmonic distortion (THD) of grid current, reaching about 75% for a power rating of 400 W, as depicted in Fig. 1(b)–(d).

To mitigate power quality issues and for wide-range speed control of SRM drive, a front-end PFC converter is required,

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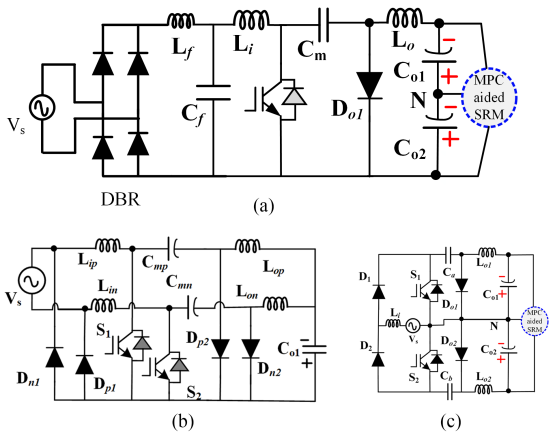


Fig. 2. Cuk derived BL topology. (a) Bridge rectifier Cuk fed SRM drive [16]. (b) BL Cuk modified in [17]. (c) TPBL SRM drive.

which varies dc link voltage. In general, two types of ac–dc PFC converters, single-stage, and double-stage, are used with their advantages and disadvantages. AC–DC and dc–dc converters are combined in a two-stage PFC converter. A large storage capacitor is required in between two stages. In addition, dc link voltage is controlled by second stage of a two-stage rectifier, while the current THD is controlled by first stage. Despite having excellent control of output voltage and high PF attained, control complexity, significant component requirements, low effectiveness, low power density, and high cost are several disadvantages, which restrict its implementation at low power levels [11], [12], [13].

Single-stage PFC converter is preferred for low-power applications as it requires low components, simple control, low cost, and efficiency. Depending on system structure, cost, complexity, and application, single-stage PFC converters are designed to operate in continuous conduction mode (CCM), or discontinuous conduction mode (DCM). CCM topologies are not preferred for low-cost applications as they require input voltage sensing for unit template-based complex control, bulky components, and high switching losses. However, DCM topologies are preferred for low-cost power applications as they require a single voltage sensor, simple control, and small-size magnetic components [14], [15]. Considerable conduction loss occurs in standard PFC converters due to bridge rectifiers on the supply side. To improve efficacy, bridgeless (BL) PFCs are designed. A BL PFC converter with a totem pole (TP) structure is further used to improve converter efficiency at cost of complex control. The development of a conventional Cuk converter with bridge rectifier fed SRM drive [16] and BL topology for PFC application [17] are shown in Fig. 2(a) and (b), respectively. After that, designed totem-pole BL PFC converter for MPC-aided SRM drive [as shown in Fig. 2(c)] with fewer components, simple control, and dual output is focused on this work.

For applications including electric vehicle (EV) battery chargers [18], [19], [20], [21], [22], wireless power transfer [23], switched mode power supply [24], LED lighting [25], [26], and motor drives [27], [28], [29], [30], [31], various front-end converters with BL topology are available in the literature. In addition, various PFC converters topology designed for wide applications in various fields with their design methodology are discussed in [32] and [33]. To increase power density and to consider cost and losses, a totem pole bridgeless (TPBL) PFC rectifier in CCM is proposed for wide band gap devices converter, capable of providing full soft switching over large variations in input supply and output load, operating in DCM for PFC at low power is presented in [19]. In [20], a TPBL-isolated modified single-ended primary inductor converter for power quality improvement in ac–dc converter-based LEV charger is discussed. Single-stage PFC converters for wireless charging and uninterruptable power supply are described in [23] and [24], respectively. Low power LED lighting system assisted with BL PFC front end converter, for unity PF at grid side, is elaborated in [25] and [26]. In [27] and [28], BL PFC converter to maintain grid current THD for BLDC motor and induction motor drives, respectively, are discussed. Hybrid-cell-based buck-type BL topologies, which combine two types of converter cell structures, for brushless dc motor drive over wide range voltage are described in [31]. This work is derived for MPC-aided SRM drive for wide speed control in low power applications, which is based on principle of voltage double PFC converter, operating in DCM as elaborated in [34].

The existing literature clearly shows that there has been substantial progress in development of high-tech, low-loss converters intended for use with a single output for EV charging and motor drives. However, there is barely any work on development of dual output converters that include a neutral point for applications using SRM drives. Hence, this work aims to address this deficiency by designing and executing dual output converters with a neutral point for SRM driving. Presented converters provide several benefits, including use of a low component count, zero current switching (ZCS) for turning on main switch, and ZCS for turning OFF diodes regardless of supply voltage and load fluctuations. In addition, they provide low THD in grid current without using an input filter, with a common midpoint between input and output, and a balanced dual output.

Proposed system is designed to address limitations of current PFC converter, resulting in suitable for use with MPC-assisted SRM drives. Here, a balanced dual-output front-end converter with neutral point availability is derived by integrating a conventional SEPIC converter with following key features.

1) A front-end ac–dc converter with balanced dual output voltage nature is developed, which is critically required for the MPC tailored SRM drive, providing a low power, cost-effective solution.
2) Proposed dual output PFC converter omits the requirement of input side filter, enhancing overall power quality and minimizing grid current THD due to availability of input side inductor.
3) Proposed dual output ac–dc converter has output side inductor, which provides continuous ripple-free current to motor, results in more uniform torque generation, reducing vibrations, hence improving overall system performance and durability. In addition, lower ripple in output minimizes size of dc link capacitor and extends their lifespan.
4) A totem-pole dual output BL PFC converter with hybrid converter topology along with ZCS operation is proposed for MPC aided SRM drive, which significantly reduces number of active switching devices operating simultaneously, lowering conduction and switching losses, minimizing thermal stress and enhancing system efficiency and reliability.
5) Proposed BL dual output PFC converter enhances grid power quality, complies with IEC guidelines for wide-range supply voltage fluctuations, and facilitates variable

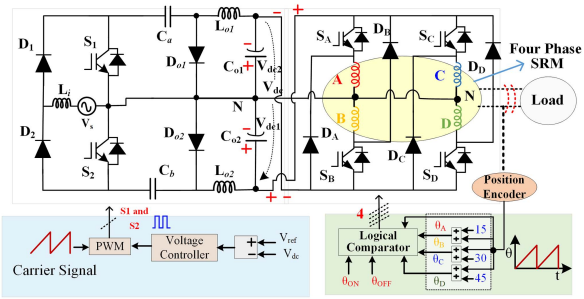


Fig. 3. TPBLDO rectifier fed high voltage low power SRM drive.

6) Voltage control approach for SRM speed control minimizes high-frequency switching, reduces power losses, improving system efficiency, reduces electromagnetic interference, enhancing system reliability and component lifespan as compared to PWM control SRM drive.

This work is showcased as follows. Introduction of low power totem pole bridgeless dual output (TPBLDO) PFC converter assisted SRM drive is outlined in Section II. Section III explores the working fundamentals of the presented PFC converter. Following that, Section IV provides detailed information on the design and selection procedure for power electronics components used in converters. Subsequently, Section V explains control for the power factor correction (PFC) converter used in SRM drive. In addition, Section VI includes validation findings that confirm the effectiveness, reliability, and performance of the presented PFC-fed SRM drive in different operating situations. Section VII provides a concise overview of test results.

## II. SRM Drive System Layout

PFC-assisted low-power SRM drive consists of a front-end PFC converter, SRM motor with MPC, and position sensor. Midpoint converter has a split dual output capacitor at input side. So, front end PFC converter at grid side is presented with balanced dual output using split dc link capacitors ($C_{o1}$ and $C_{o2}$). The structure of grid-fed low power SRM drive is presented in Fig. 3. Key parts PFC front-end converter, and MPC fed SRM with position sensor are discussed as follows.

### A. Midpoint Converter With SRM

An even-phase SR motor requires a less component MPC for its operation. Due to low cost, less component count, and less complex control, a four-phase SRM with MPC is considered for low-power low-cost household appliances. A 400-W SRM drive for domestic appliances is presented in this article. In SR motor, torque is generated due to a change in coenergy from one position to another position, which is derived from flux versus current characteristics for different positions, as depicted in Fig. 4. For performance analysis under different load conditions, a mathematical model is derived and given as

$$V_i = R_i i_i + \frac{\partial \lambda_i(\theta_i, i_i)}{\partial t} \tag{1}$$

$$V_i = R_i i_i + L_i(\theta_i, i_i).\frac{di_i}{dt} + E_i \tag{2}$$

$$Here\ L_i(\theta_i, i_i) = \frac{\partial \lambda_i(\theta_i, i_i)}{\partial i_i}\ and\ E_i = \omega.\frac{\partial \lambda_i(\theta_i, i_i)}{\partial \theta_i} \tag{3}$$

where $V_i$, $i_i$, and $R_i$ are $i$th phase phase-applied voltage, current,

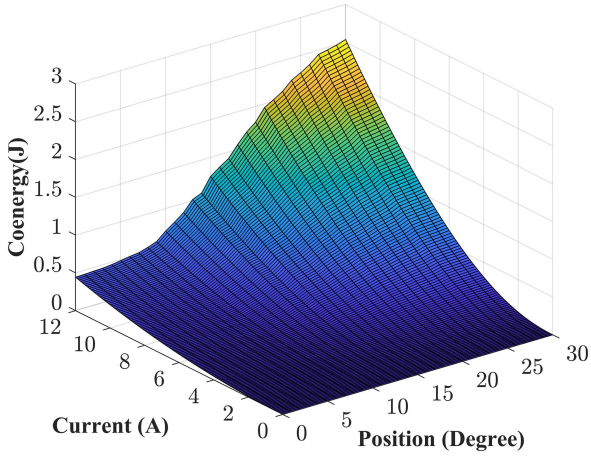


Fig. 4. Coenergy versus current characteristics for four-phase SRM.

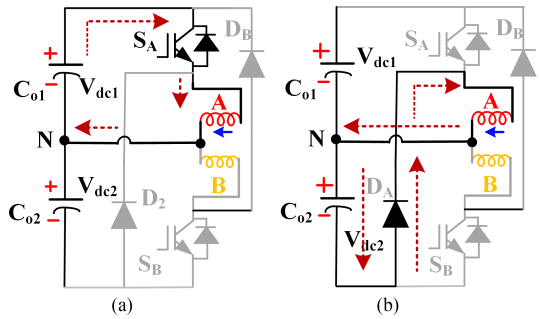


Fig. 5. MPC working. (a) Phase A magnetization. (b) Phase A de-energization.

($L_i$), speed ($\omega$), and $i$th phase back emf ($E_i$) are interrelated. Per phase torque ($T_i$) is developed from change in coenergy ($W_i$) from unaligned to aligned position when $i$th phase is excited. After that overall electromagnetic torque ($T_{em}$) is sum of all phase torque and given as

$$T_i = \frac{\partial W_i(\theta_i, i_i)}{\partial \theta_i} \tag{4}$$

$$T_{em} = \sum_i \frac{\partial}{\partial \theta_i}\left(\int_0^{i_i} \lambda_i(\theta_i, i_i) di_i\right). \tag{5}$$

Considering inertia ($J$), viscous coefficient ($B$), and load torque ($T_{ld}$), mechanical dynamic performance is generalized as

$$J\frac{d\omega}{dt} + B\omega = T_{em} - T_{ld}. \tag{6}$$

Phase excitation of four-phase SRM using an MPC is shown in Fig. 5. As switch $S_A$ is turned ON, phase A is energized through dc link capacitor $C_{o1}$. Demagnetization of phase A occurs through diode $D_A$ and capacitor $Co_2$. Similarly, phase B is energized and de-energized through switch $S_B$ and diode $D_B$. Excitation and demagnetization of phase A are illustrated in Fig. 5(a) and (b), respectively.

### B. PFC Converter Structure

Presented dual output balanced voltage with TPBL PFC converter is designed for MPC assisted SRM. PFC front-end converter is operated to maintain THD at input side along with

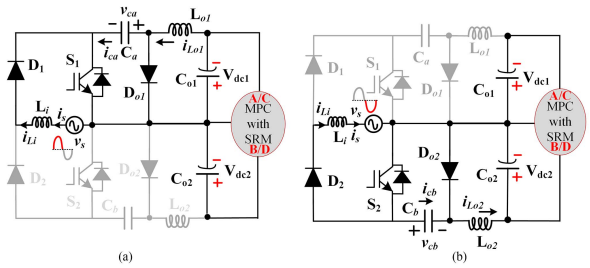


Fig. 6. TPBLDO rectifier's operation. (a) Positive grid cycle. (b) Negative grid cycle.

rectifier is depicted in Fig. 3. Converter's operation is dependent on nature of grid voltage, i.e., for positive grid supply upper half, and for negative supply lower half conduction occurs. Switch automatically comes into forward conduction mode according to polarity of supply voltage, i.e., supply voltage sensing is not required for functioning of BL converter. An input inductor $L_i$ operates in continuous current conduction mode (CICM) and intermediate capacitors ($C_a$ and $C_b$) are operating in continuous voltage conduction mode (CVCM). Output inductors ($L_{o1}$ and $L_{o2}$) are estimated considering discontinuous current conduction mode (DICM) operation.

The converter's analysis and functioning are considered under certain assumptions, which are as follows.

1) Power electronics switches and diodes are assumed as ideal switches.
2) Line frequency is significantly lower than switching frequency, i.e., line frequency variables, such as input current, and supply voltage are assumed to be constant for switching period.
3) Input inductor is enough to maintain CICM operation.
4) In analysis, voltage across capacitors C1, C2, Co1, and Co2 are constant during complete switch period.

## III. Functioning of Presented PFC Converter Fed SRM Drive

Front-end rectifier with dual output functioning is briefly explained and then after converter's analysis with component design is focused in this section. PFC converter operations are broadly sectioned under line frequency and switching frequency. Line frequency and switching frequencies are 50 Hz and 20 kHz, respectively, as per grid availability and rectifier's component design. Dual output rectifier's functioning with line frequency is depicted in Fig. 6. Here, Fig. 6(a) and (b) represents converter equivalent circuits under positive and negative grid availability, respectively. Under positive half cycle supply, upper half components $S_1$, $D_1$, $L_i$, $C_a$, $D_{o1}$, $L_{o1}$, $C_{o1}$ are in operation, and lower half components $S_2$, $D_2$, $L_i$, $C_b$, $D_{o2}$, $L_{o2}$, $C_{o2}$ are used with negative half cycle power supply. Converter's fed SRM drive operation under line and switching frequency are briefly explained as follows. Switching frequency-based operation of presented rectifier under positive and negative grid are illustrated in Fig. 7 and Fig. 8, respectively. The converter's passive components electrical parameters variations are exhibited in Fig. 9. In both positive and negative supply cycles, rectifier functions similarly. It is noteworthy that, supply voltage ($v_s$), grid current ($i_s$), energy transfer capacitor's voltage ($v_{Ca}$ and $v_{Cb}$), and output capacitor voltages ($V_{dc1}$ and $V_{dc2}$) are assumed to be fixed for converter's analysis. The rectifier's operation

TABLE I
Passive Component's Voltage/Current

| Components | State- $P_1/N_1$ | State- $P_2/N_2$ | State- $P_3/N_3$ |
|---|---|---|---|
| $L_i$ ($v_{Li}$) | $v_s$ | $v_s - V_{Ca}$ | $\approx 0$ |
| $L_{o1}$($V_{Lo1}$) / $L_{o2}$($V_{Lo2}$) | $-V_{Ca}$-$V_{dc1}$/-$V_{Cb}$-$V_{dc2}$ | $-V_{dc1}$/-$V_{dc2}$ | $\approx 0$ |
| $C_a$($i_{Ca}$) / $C_b$($i_{Cb}$) | $i_{Lo1}$ / $i_{Lo2}$ | $i_s$ | $i_s$ |

TABLE II
TPBLDO Converter Specifications

| Specification | Value |
|---|---|
| Rated Power ($P_{in}$) | 400 W |
| Grid single-phase voltage ($v_s$) | 160–260 V /50 Hz |
| Split DC lin voltage ($V_{dc1}$/$V_{dc2}$) | 50–150 V |
| $C_{o1}$ and $C_{o2}$ voltage ripple (α) | 5 % |
| $C_a$ and $C_b$ voltage ripple (β) | 25% |
| $L_i$ inductor's current ripple (g) | 20 % |
| Switching frequency ($f_{sw}$) | 20 kHz |
| Cutoff frequency ($f_c$) | 2000 Hz |

### A. Converter's Operation With Positive Supply

Under positive grid supply conditions, diode $D_1$ is forward-biased, and connects input inductor to the supply through switch $S_1$. Other passive components participating in the positive half are energy transferring capacitor ($C_a$), freewheel diode ($D_{o1}$), output inductor ($L_{o1}$), and output capacitor ($C_{o1}$). Circuit configuration under positive grid, shown in Fig. 6(a), is examined under three states, as discussed further.

*State-$P_1$ ($t_0$-$t_1$):* In this mode, diode $D_1$ is conducting, and switch $S_1$ is turned ON. Diode $D_2$ is in reversed bias in this mode. $L_i$ inductor stores energy from grid. The energy-transferring capacitor discharges its energy to $L_{o1}$. Input inductor current ($i_{Lo1}$) increases. SRM energy is fulfilled by intermediate capacitor $C_a$. Freewheeling diode $D_{o1}$ is revered biased mode in this state. Equivalent circuits and variation in electrical parameters of passive components are depicted in Figs. 7(a) and 9, respectively. At the end of this state, driving signal to $S_1$ is set to zero. Further, relevant expressions for $t_0$ to $t_1$ are summarized as given in Table I.

*State-$P_2$ ($t_1$-$t_2$):* As shown in Fig. 7(b), freewheeling diode $D_{o1}$ starts conduction, and switch is turned OFF in this mode. $L_i$ current starts decreasing and transfers energy to intermediate capacitor $C_a$ and $L_{o1}$ transfers its energy to load as depicted in Fig. 9. Table I summarizes current and voltage variation in this state.

*State-$P_3$ ($t_2$-$t_3$):* After full discharge of $L_{o1}$ energy, $S_1$ and $D_{o1}$ remain nonconducting. An equivalent circuit is outlined in Fig. 7(c). $v_{Li}$ and $v_{Lo1}$ become zero and a constant current is flowing through $C_a$ as shown in Fig. 9. Passive components currents and voltage expression are given in Table I.

### B. Converter's Operation With Negative Supply

With negative cycle grid supply, converter $D_1$ is reverse biased and $D_2$ is forward biased. $S_2$, $L_i$, $D_2$, $C_b$, $L_{o2}$, and $D_{o2}$ are involved in this mode. Fig. 8 interpretates electrical equivalent circuit under negative grid supply and stages are explained as follows.

*State-$N_1$ ($t_3$-$t_4$):* Output inductor is fully discharged at start of this stage. Input inductor starts storing energy from grid through $S_2$. Energy transferred by an intermediate capacitor, $C_b$, is taken

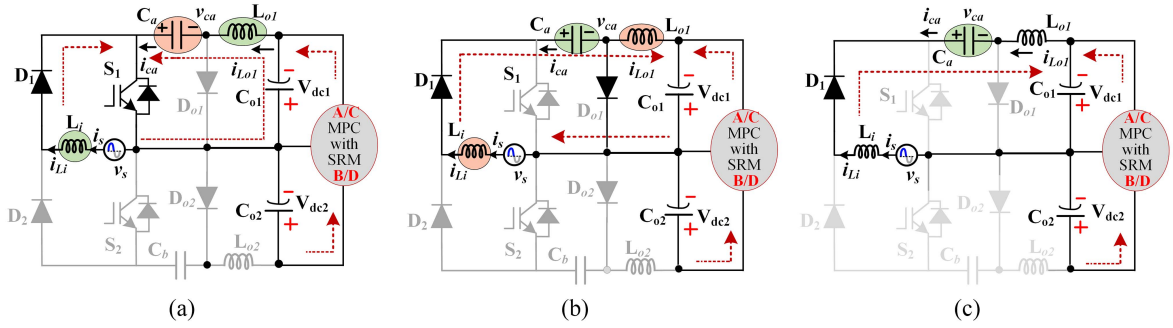


Fig. 7. Switching frequency operating states of TPBLDO converter with positive cycle. (a) P1-state. (b) P2- state. (c) P3-state.

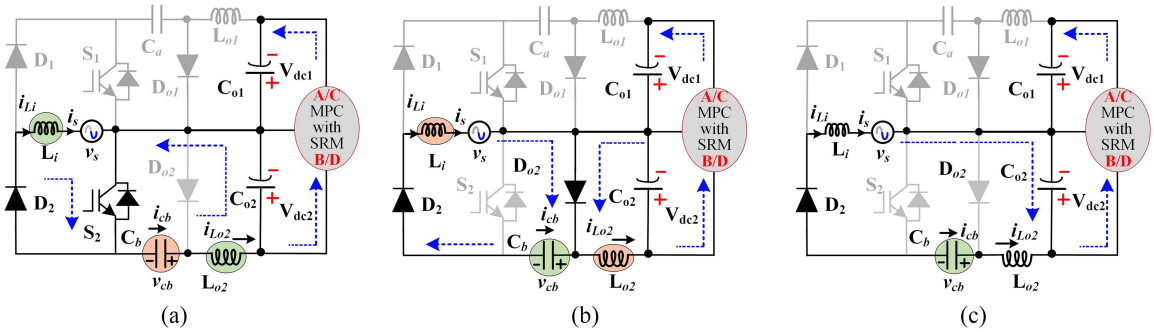


Fig. 8. Switching frequency operating states of TPBLDO converter with negative cycle. (a) N1-state. (b) N2- state. (c) N3-state.

TABLE III
PASSIVE COMPONENTS ESTIMATION AND SELECTION

| *Passive component* | *Design equation* | *Calculated value* | *Selected value* |
|---|---|---|---|
| $L_{o1}/L_{o2}$ | $\frac{V^2_{dc\min}\times V_{s\min}\sqrt{2}}{2\times f_s\times P_{in}\times(V_{dc\min}+V_{s\min}\sqrt{2})}=\frac{100^2\times160\sqrt{2}}{2\times20000\times400\times(100+160\sqrt{2})}$ | 410 $\mu$H | 110 $\mu$H |
| $L_i$ | $\frac{V_{s\_\min}}{\gamma}\sqrt{\frac{L_{o1/L_{o2}}\times\sqrt{2}\times V_{s\_\min}}{(V_{dc\min}+V_{s\_\min}\sqrt{2})\times P_{in}\times f_{sw}}}=\frac{160}{0.3}\sqrt{\frac{120\times10^{-6}\times\sqrt{2}\times160}{(100+160\sqrt{2})\times400\times20\times10^3}}$ | 1.71 mH | 2.0 mH |
| $C_a/C_b$ | $C_a/C_b=\frac{P_{in\_rated}}{f_{sw}\times\beta\times\left(\sqrt{2}\,v_{s\_\min}+V_{dc1/2\_\min}\right)^2}=\frac{400}{0.30\times20000\times\left(\sqrt{2}\times160+50\right)^2}$ | 873 nF | 1µF |
| $C_{o1}/C_{o2}$ | $C_{o1}/C_{o2}=\frac{I_{dc}}{2\times\omega_l\times\Delta v_{dc}}=\frac{P_{in}}{(8\times\pi\times f_l)\times\alpha\times V^2_{dc1/2\_\max}}=\frac{400}{2\times314\times0.03\times150^2}$ | 943.18 µF | 1100 µF |

TABLE IV
POSITION COMMUTATION LOGIC FOR SRM

| S.No. | Rotor position | Excited winding |
|---|---|---|
| 1 | $6^0\le\theta\le21^0$ | Phase A |
| 2 | $21^0\le\theta\le36^0$ | Phase B |
| 3 | $36^0\le\theta\le51^0$ | Phase C |
| 4 | $51^0\le\theta\le60^0$ && $0^0\le\theta\le6^0$ | Phase D |

equivalent circuit is shown in Fig. 8(a). Table I contains voltage and current in-state $N_1$.

*State-$N_2$ ($t_4$-$t_5$):* As depicted in Fig. 8(b), $S_2$ gate pulse is turned OFF and conduction of $D_{o1}$ starts in this state. $C_b$ capacitor voltage increases and $L_i$'s stored energy is transferred to the intermediate capacitor $C_b$. Load power requirement is compensated by $L_{o2}$ and $C_{o2}$. The voltage and current for this state are summarized in Table I.

*State-$N_3$ ($t_5$-$t_6$):* The output inductor ($L_{o2}$) energy becomes zero in this state. A small current flows through mid-capacitor ($C_b$), $L_i$, and $L_{o2}$. In this state, the equivalent circuit and passive component currents and voltages are shown in Figs. 8(c) and 9, respectively.

## IV. ANALYSIS, SPECIFICATIONS, AND DESIGN OF PRESENTED PFC FED SRM DRIVE

A TPBLDO rectifier is developed for a 400-W SRM drive, and passive components are selected according to voltage and current they can withstand. Allowable ripple and switching frequency determine passive component size for a given converter. Main features of BL PFC converter are shown in Table II. $L_i$ and $C_a$/$C_b$ are designed to operate in CCM whereas $L_{o1}$ and $L_{o2}$

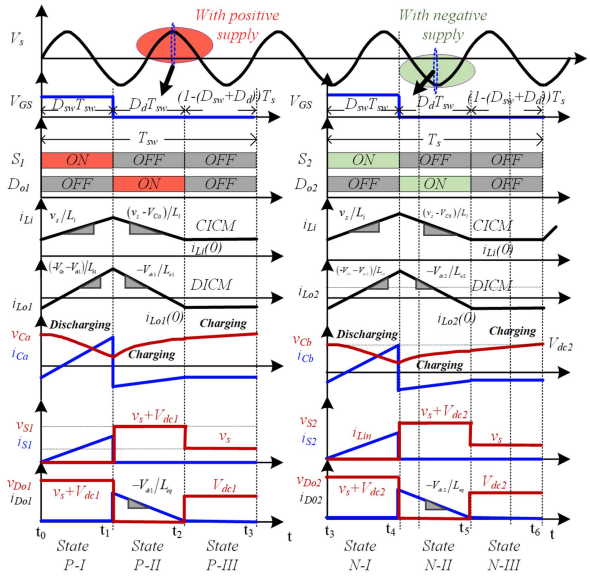


Fig. 9. Electrical parameters variation of passive components.

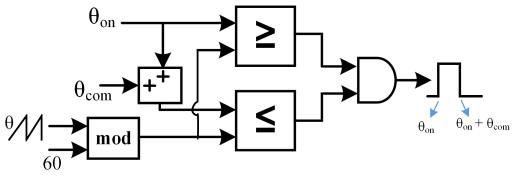


Fig. 10. Control block for SRM phase A gate pulse logic.

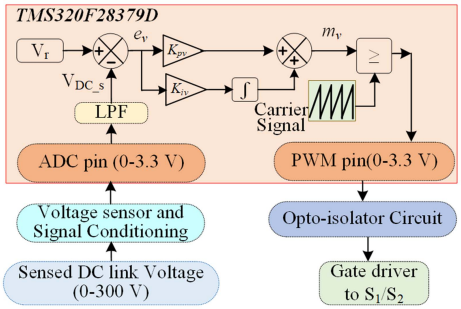


Fig. 11. Control block for presented TPBLDO converter.

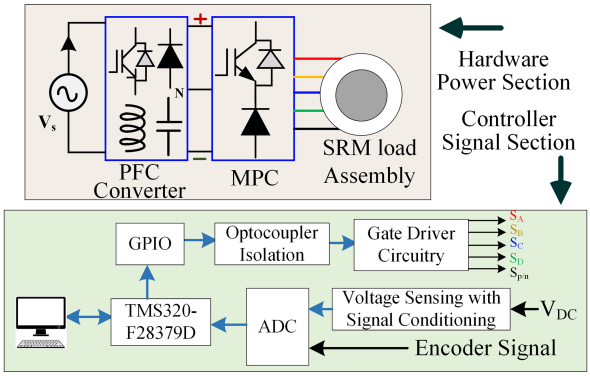


Fig. 12. Block diagram of PFC-assisted SRM drive.

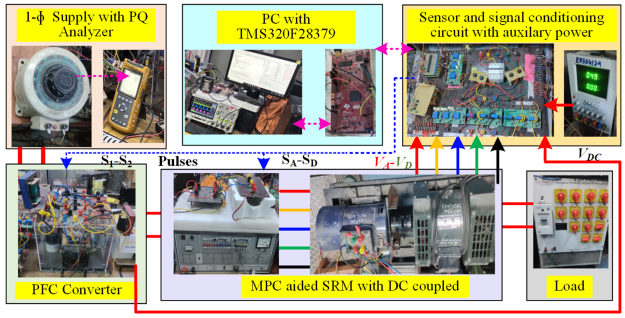


Fig. 13. Hardware prototype of presented converter-fed SRM drive.

TABLE V
HARDWARE COMPONENTS LIST

| Component Details | Manufacturer/ Ratings |
|---|---|
| Switches ($S_1/S_2$) | SKM100GAR IGBT diode module |
| Capacitors ($C_{dc1}/C_{dc2}$) | Nichicon's aluminum electrolytic capacitors, rated at 2200 µF/450 V |
| Capacitors ($C_a$ and $C_b$) | Polypropylene Capacitor (DEC MPB-SNB (L))1 $\mu$F/ 1000 V |
| Fast Diode ($D_{o1}$ and $D_{o2}$) | Fairchild's RHRG75120 (75 A, 1.2 kV) |
| Inductors ($L_i$, $L_{o1}$, and $L_{o2}$) | TDKs E 100/60/28 with solid round copper wire |
| Autotransformer | 0V RMS – 265V RMS/ 15 A RMS |
| Auxiliary Supply | Scientific's Multiple Power Supply (PSD3304) |
| Optocoupler Circuit | IC 6N136 |
| Voltage Sensors | LEMs LV-25 P |
| Controller | TI's TMS320F28379D Launchpad |
| Power Quality Analyzer | Fluke-43B |
| Digital Signal Oscilloscope | Keysight's four-channel MSO |

are designed in DICM. Both, positive grid operational mode circuit and negative grid operational circuit are symmetrical. Positive half-cycle analysis is sufficient for overall converter performance. Duties of switch ($S_1/S_2$) and diode's ($D_{o1}/D_{o2}$) are denoted as $D_{sw}$ and $D_d$, respectively, and are written as

$$D_{sw} + D_d < 1. \tag{7}$$

Using volt second balance with $L_i$, (for supply, $v_s = V_m \sin \omega t$)

$$D_d / D_{sw} = v_s / V_{dc1} = 2V_m \sin \omega t / V_{dc1} = 2 \sin \omega t / m_g \tag{8}$$

where

$$m_g = V_{dc1}/V_m \tag{9}$$

i.e., assuming wt = 90°

$$D_d / D_{sw} = 2/m_g = 2V_m / V_{DC}. \tag{10}$$

After that DICM condition using (7)

$$D_{sw} + 2\frac{D_{sw}}{m_g} < 1 \Rightarrow D_{sw} < \frac{m_g}{m_g + 2}. \tag{11}$$

For a switching period ($T_{sw}$), supply voltage ($v_s$) is assumed to be constant for accurate analysis. Average voltage across intermediate capacitor for switching period is $v_s$ -$V_{dc1}$. Input and output inductor's current increased and reach its peak at $D_{sw}T_{sw}$. Maximum current through switch $S_1$ over switching period is given as [35]

$$i \qquad i \qquad i \qquad \frac{V_m}{} D \quad T$$

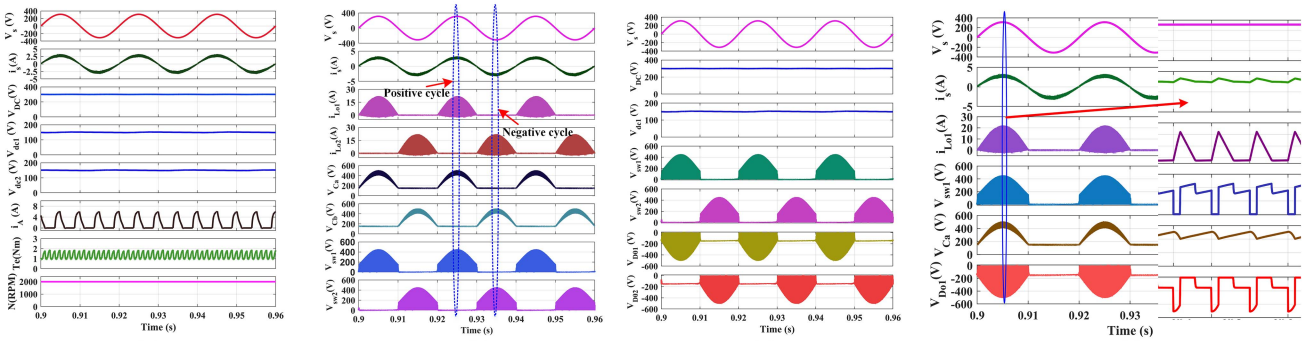


Fig. 14. Simulated performance of TPBLDO converter at $v_s = 220$ V, $V_{\rm DC} = 300$ V. (a) $v_s$, $i_s$, $V_{\rm DC}$, $V_{\rm dc1}$, $V_{\rm dc2}$, $i_A$, $T_e$, and speed, (b) $v_s$, $i_s$, $i_{Lo1}$, $i_{Lo2}$, $V_{Ca}$, $V_{Cb}$, $V_{\rm sw1}$, and $V_{\rm sw2}$. (c) $v_s$, $V_{\rm DC}$, $V_{\rm dc1}$, $V_{\rm sw1}$, $V_{\rm sw2}$, $V_{Do1}$, and $V_{Do2}$. (d) $v_s$, $i_s$, $i_{Lo1}$, $V_{\rm sw1}$, $V_{Ca}$, and $V_{Do1}$.

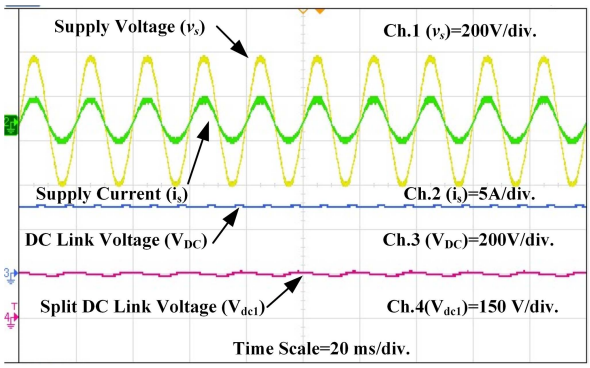


Fig. 15. Steady parameters with rated dc link voltage $v_s$, $i_s$, $V_{\rm DC}$, and $V_{\rm dc1}$.

$$+\frac{V_m}{L_{o1}}D_{sw}T_{sw} \tag{12}$$

$$i_{sw1}|_{peak} = \left(\frac{1}{L_i}+\frac{1}{L_{o1}}\right)V_m D_{sw}T_{sw} = \frac{V_m D_{sw}T_{sw}}{L_{eq}} \tag{13}$$

where $L_{\rm eq}$ is equivalent inductance seen from source and written as

$$L_{eq} = \frac{L_i \times L_{o1}}{L_i + L_{o1}}. \tag{14}$$

Similarly, peak current through diode $D_{o1}$ is as

$$i_{Do1}|_{peak} = i_{L_i}|_{peak} + i_{L_{o1}}|_{peak} = \frac{V_{dc1}}{L_i}D_{sw}T_{sw} + \frac{V_{dc1}}{L_{o1}}D_{sw}T_{sw} \tag{15}$$

$$i_{Do1}|_{peak} = \frac{V_{DC}}{L_{eq}}D_{sw}T_{sw}. \tag{16}$$

CCM functioning and current ripple at minimal supply voltage and maximum load condition are considered while designing input inductor. Table III shows estimated and selected $L_i$ values. Then, after output inductors are designed to operate in DICM with minimum supply voltage and minimum dc link to fulfill load requirement, the condition is considered as critical condition for DCM operation. Selected values of $L_{o1}/L_{o2}$ are one-fourth of the estimated value for ensured DICM operation. Calculation and selection of passive components are explained in Table III.

## V. Control of PFC Fed SRM Drive

Mainly, PFC control and SRM commutation control are constituted PFC-supported SRM drive control. Regulating dc link voltage and ensuring grid current power quality are two of primary functions of PFC controller. Commutation logic control based on rotor position is used for motoring operation of SRM. Both controls are briefly explained as follows.

### A. SRM Drive Control

A four-phase SR motor is operated based on rotor position. Rotor position ($\theta$) is generated by encoder signal. Then after, a commutation logic is used for sequential switching of SRM. For four-phase SRM, four pulses are generated and fed to four switches ($S_A$, $S_B$, $S_C$, and $S_D$) of MPC as shown in Fig. 3. Rotor pole pitch and stroke angle for six rotor poles are 60° and 15°. For $\theta_{\rm on}$ turn ON angle and $\theta_{\rm com}$ commutation angle, turn OFF angle is, $\theta_{\rm com}$–$\theta_{\rm on}$. Turn ON and turn OFF angles are compared with rotor position and after that logic is used for gate pulse generation. Fig. 10 shows control block schematic for gate signal of phase A. Phases B, C, and D gate driver signals are similarly generated using shifted rotor position. Table IV shows the position-based excited phase sequence.

### B. Control for Presented PFC Converter

A control for TPBLDO rectifier for an MPC-fed SRM drive is used to achieve dc voltage variations, ac supply fluctuations mitigations, and power quality improvement at grid side. TI Launchpad TMS320F28379D is used for digital control implementation. Single voltage controller-based controller is used for PFC converter.

In the presented TPBLDO rectifier, dc link voltage is sensed using a voltage sensor (LEM LV-25P) and given to analog and digital pins of digital signal processor (DSP) controller. The error signal ($e_v$), generated by comparison of sensed voltage ($V_{\rm dc\_s}$) with reference voltage ($V_r$), is given to proportional integrator (PI) controller. Then after modulating signal ($m_v$) is logically compared with 20 kHz carrier signal for pulse generation. Finally, generated pulses $S_1$ and $S_2$ are fed to PFC converter. The control block schematic of voltage controller using DSP is illustrated in Fig. 11 and is carried out as follows.

For sensed voltage at $k$th sampling, an error signal is expressed as

$$e_v(k) = V_r - V_{dc\_s}(k). \tag{17}$$

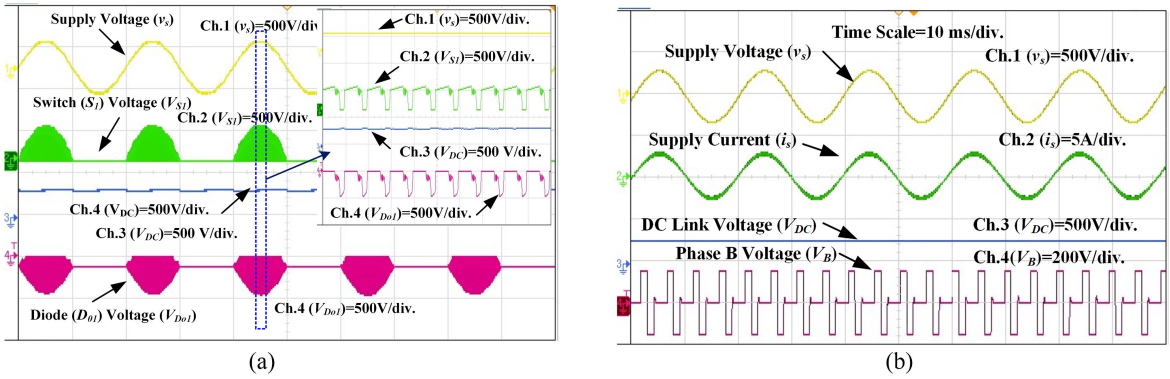


Fig. 16. Steady state parameters with rated dc link voltage. (a) $v_s$, $V_{S1}$, $V_{\rm DC}$, and $V_{Do1}$. (b) $v_s$, $i_s$, $V_{\rm DC}$, and $V_B$.

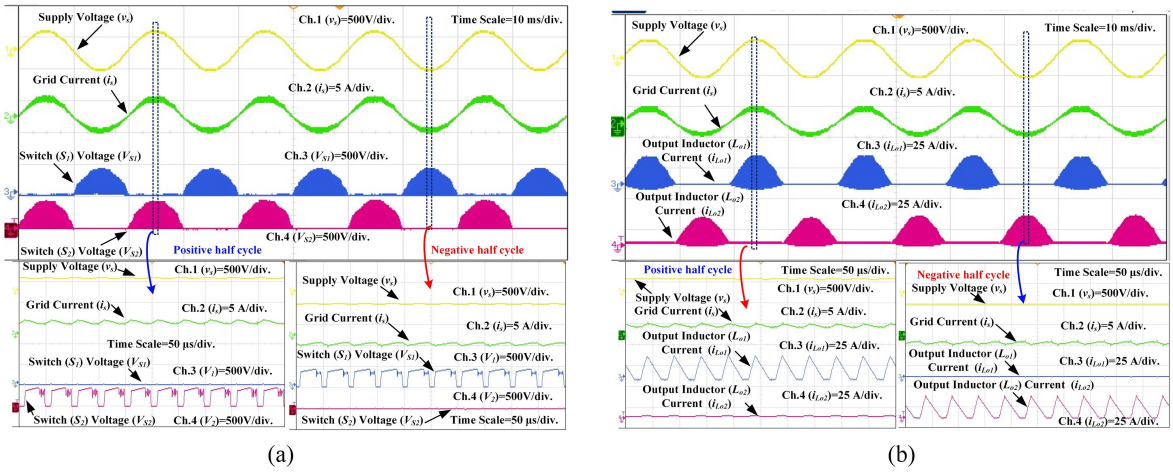


Fig. 17. TPBLDO converter's operation with grid voltage. (a) $v_s$, $i_s$, $V_{S1}$, and $V_{S2}$. (b) $v_s$, $i_s$, $i_{Lo1}$, and $i_{Lo2}$.

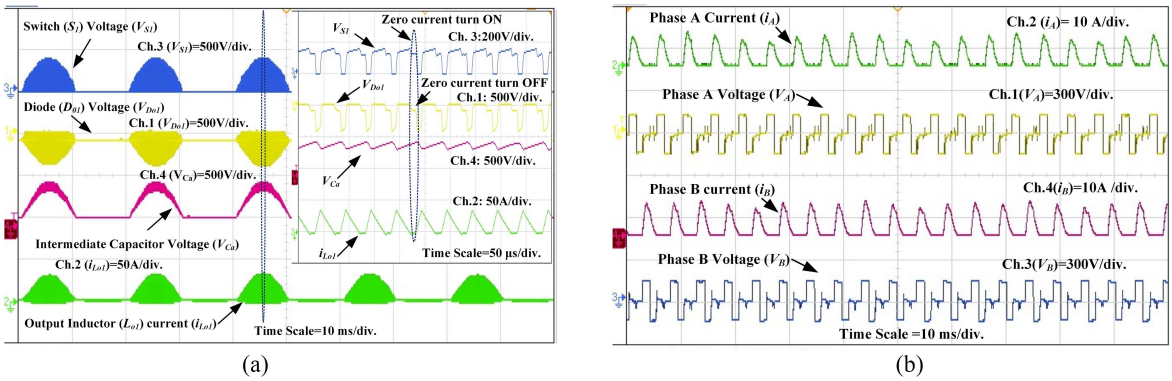


Fig. 18. (a) Passive components in positive half grid ($V_{S1}$, $V_{Do1}$, $V_{Ca}$, and $i_{Lo1}$). (b) Motor phase excitation and currents ($i_A$, $V_A$, $i_B$, and $V_B$).

Modulating signal, $m_V$ (k), samples are produced by a PI-controller having proportional gain $K_{\rm pv}$ and integral gain $K_{\rm iv}$, are represented as

$$m_v(k) = m_v(k-1) + K_{pv}[e_v(k) - e_v(k-1)] + \frac{K_{iv}T_s}{2}[e_v(k) + e_v(k-1)]. \quad (18)$$

After that gate pulses, $S_1$ and $S_2$, are generated by comparing carrier signal ($V_c$) of 20 kHz frequency and modulating signal ($m_v$) and given as

$$\left.\begin{array}{l} \text{If, } m_v(k) \rangle V_c(k) \Rightarrow \text{S}_1 \text{ and S}_2 \text{ are ON;} \\ \text{if, } m_v(k) \langle V_c(k) \Rightarrow \text{S}_1 \text{ and S}_2 \text{ are OFF;} \end{array}\right\}. \quad (19)$$

## VI. Result Validation and Discussion

First, design and performance validation of presented TP-BLDO rectifier-assisted low-power SRM drive under steady state and transient conditions are evaluated through simulations

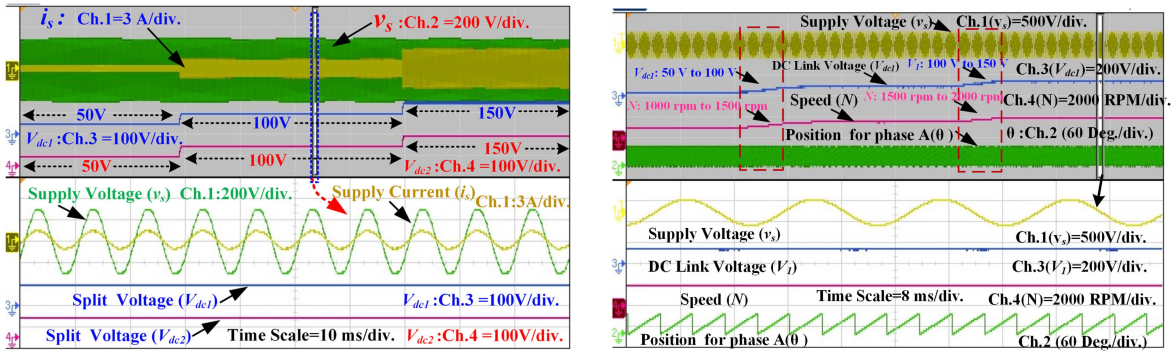


Fig. 19. TPBLDO converter's operation with grid voltage. (a) $v_s$, $i_s$, $V_{\rm dc1}$, and $V_{\rm dc2}$. (b) $v_s$, $V_{\rm dc1}$, Speed ($N$), and rotor position ($\theta$).

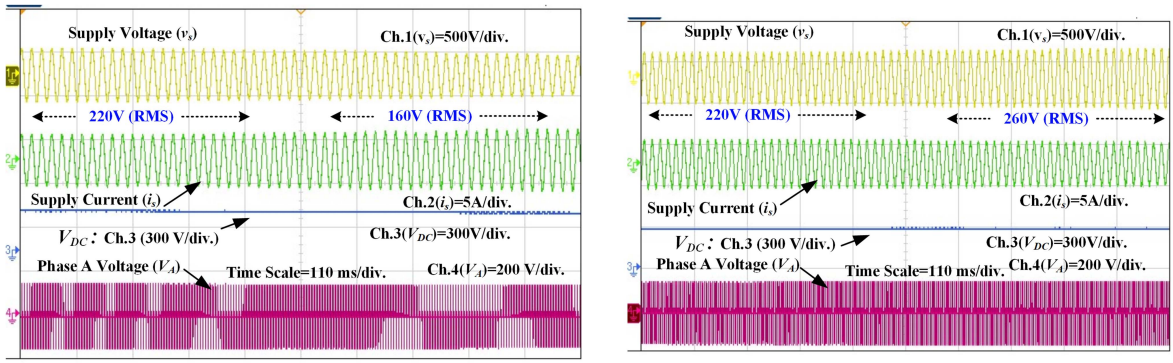


Fig. 20. TPBLDO converter's dynamic performance with grid voltage fluctuation. (a) Under voltage fluctuation: $v_s$, $i_s$, $V_{\rm DC}$, and $V_A$. (b) Over voltage fluctuation: $v_s$, $i_s$, $V_{\rm DC}$, and $V_A$.

in a MATLAB environment. Then-after verifications of outcomes for steady state and dynamic tests are carried out through a laboratory hardware test bench setup. A block diagram of PFC assisted SRM drive, and hardware setup photograph for experimental verification are showcased in Figs. 12 and 13, respectively. Finally, derived results at steady state and under various transients are explained and illustrated in Figs. 14–18.

### A. Simulation Results

In this section, the simulated performance of presented converter-fed SRM drive is analyzed, through the MATLAB Simulink platform, which is helpful for component design and power electronics device selection. A 400-W dual output rectifier performance under steady state and dynamic conditions is analyzed to verify drive performance. A 220 V, 50 Hz grid supply, and 300 V dc link voltage are maintained at a steady state. Steady-state converter and motor's performances are depicted in Fig. 14. In Fig. 14(a), supply voltage ($v_s$) and input current ($i_s$) at 300 V dc link voltage with motor's phase current ($i_A$), torque ($T_e$), and speed ($N$) are presented. Split capacitor voltages ($V_{\rm dc1}$ and $V_{\rm dc2}$) are equal and 150 V at steady state. Phase A peak current is approximately 6 A (peak) at 2000 r/min rated speed. Fig. 14(b) and (c) shows passive component's stress and the converter's operation with positive and negative grid supply. Input inductor current ($i_{Li}$) is in CCM and output inductor currents ($i_{Lo1}$ and $i_{Lo2}$) are in DCM with nearly 24 A peak current. Switch and energy transfer capacitor's voltage stresses ($V_{Ca}$ and $V_{Cb}$) are nearly 460 V as shown in Fig. 14(b). Fig. 14(d) represents passive components operation with positive grid supply in switching period, which validates output inductor's ($L_{o1}$) functioning in DCM and intermediate capacitor ($C_a$) and input inductor's ($L_i$) working in CCM.

### B. Experimental Results

Converter's performances are analyzed through an experimental setup under various working environments. Components used in the laboratory test bench setup are detailed in Table V. Converter-fed SRM drive operation, detailed under steady state and under supply and dc link voltage variations, are as follows.

*1) Performance Validation at Steady State:* Considering nominal condition with supply ($v_s$) at 220 V (rms) and dc link voltage ($V_{\rm DC}$) at 300 V, a 400-W SRM drive is validated. As shown in Fig. 15, supply end power quality is ensured at rated dc link voltage. Here, the grid voltage is in phase with supply current along with maintaining rated dc link for SR motor control.

Fig. 16(a) displays switch $S_1$ and diode $D_{o1}$ operation in the positive half-grid cycle at rated dc link voltage. Voltage stresses across $S_1$ and $D_{o1}$ are nearly $v_s$+$V_{\rm dc1}$, as discussed in design limits. SR motor phase B excitation, in single pulse control mode, is depicted in Fig. 16(b). Phase winding voltage is $V_{\rm DC}$/2 and applied according to position control logic. Moreover, both switches ($S_1$ and $S_2$) are operating in positive and negative half cycles sequentially as recorded in Fig. 17(a).

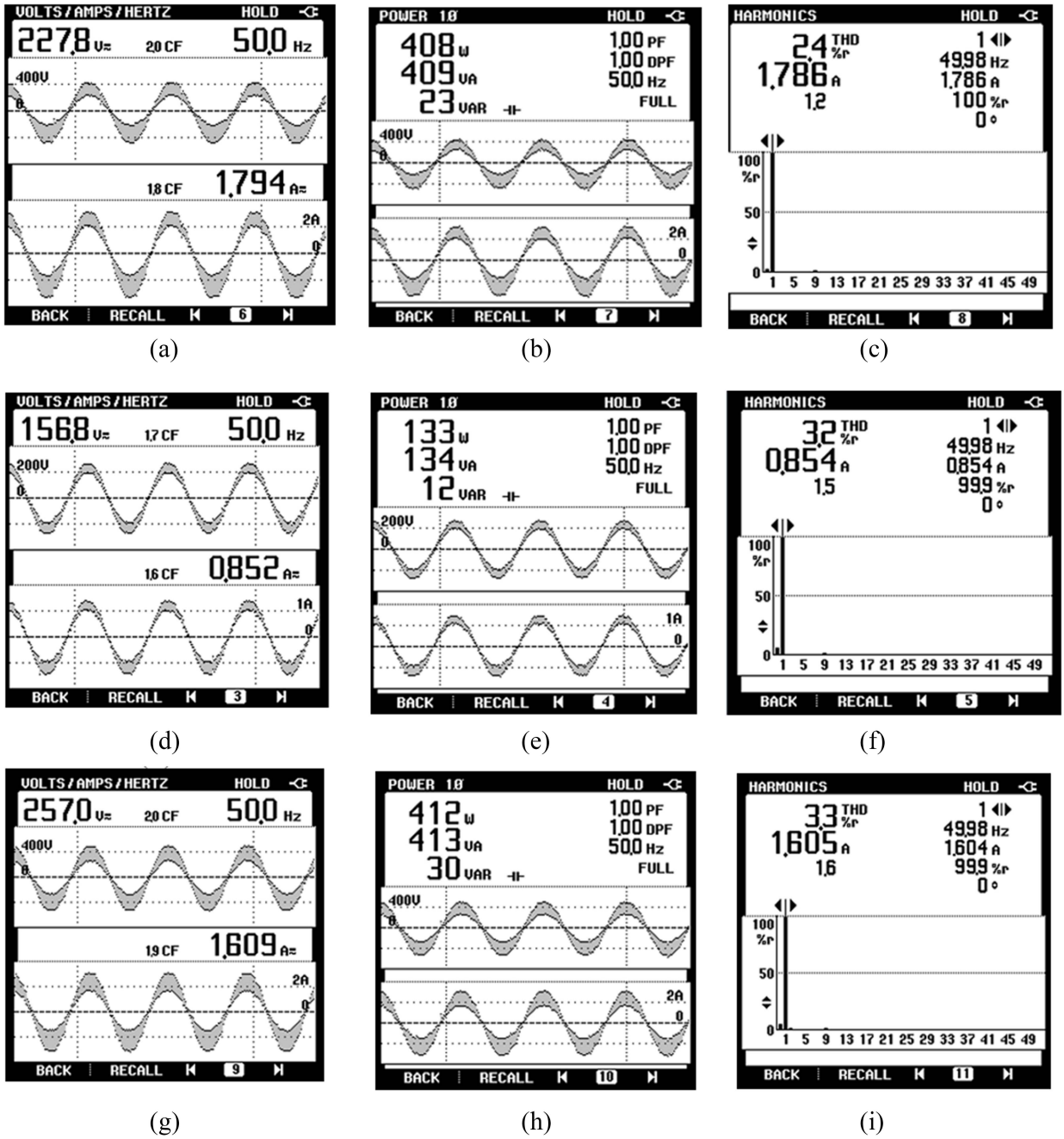


Fig. 21. Improved PQ performance of presented DOHBL converter fed SRM drive at (a)–(c) rated condition ($v_s$) = 227 V, and $V_{\rm DC}$ = 300 V, (d)–(f) $v_s$ = 156 V, and $V_{\rm DC}$ = 100 V, and (g)–(i) $v_s$ = 257 V, and $V_{\rm DC}$ = 300 V.

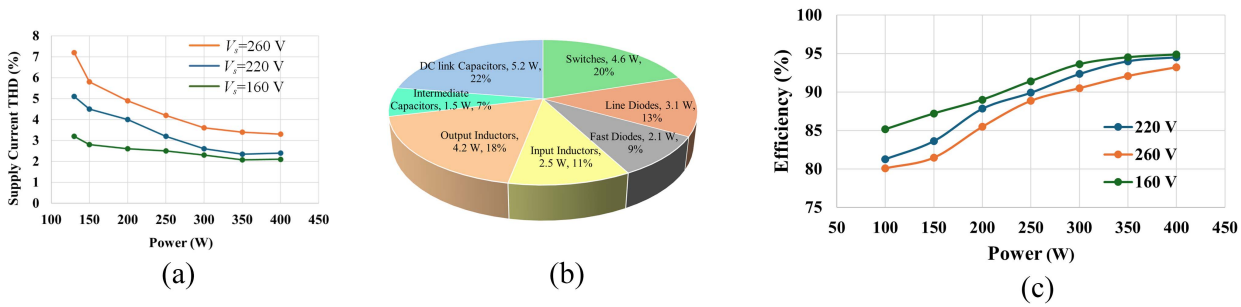


Fig. 22. PFC Converter Performance for various power and supply voltage. (a) Grid current THD. (b) Loss break down at rated conditions. (c) Efficiency plot.

TABLE VI
COMPARISON OF PRESENTED PFC CONVERTER WITH BL BUCK AND BUCK-BOOST PFC TOPOLOGY HAVING SINGLE AND DUAL OUTPUT

| *Characteristics* | *[19]* | *[17]* | *[37]* | *[38]* | *[43]* | *[39]* | *[40]* | [41] | *[42]* | *[22]* | *[46]* | *[47]* | *Present* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ***Topology*** | *BL-Cuk* | *BL-Cuk* | *BL-Cuk* | *BL-Buck* | *BL-Buck* | *RC* | *BL-SEPIC* | *BL-Cuk SEPIC* | *BL Buck-Boost* | *BL-Cuk* | *BL Buck-Boost* | *BL Buck-Boost* | *TP-BL* |
| ***Switches*** | 3 | 2 | 3 | 2 | 3 | 4 | 2 | 1 | 2 | 1 | 2 | 2 | 2 |
| ***FR diode/ SR diode*** | 3/4 | 2/2 | 1/2 | 4/0 | 6 | 2/2 | 4/0 | 1/4 | 2/2 | 2/0 | 4 | 4 | 2/2 |
| ***Inductors*** | 4 | 4 | 2 | 2 | 5 | 3 | 2 | 4 | 3 | 2 | 4 | 3 | 3 |
| ***Midway Capacitor/ DC Link Capacitor*** | 3/1 | 2/1 | 1/1 | 0/2 | 3/2 | 1 /2 | 2/2 | 3/2 | 1/2 | 1/2 | 2/2 | 2/2 | 2/2 |
| ***TC/ CCS*** | 18/11 | 13/10 | 10/8 | 10/6 | 19/9 | 13/7 | 14/9 | 15/10 | 12/8 | 9/6 | 14/7 | 13/8 | 13/8 |
| ***Input Voltage*** | 110V | 100V | 89–141 V | 85–264 V | 110 V | 85–530 V | 85–260 V | 170–250 V | 90–135 V | 90–120 V | 110–220 V | 220 | 160–260 V |
| ***Output Voltage (V)*** | 80 | 48 | 100 | B (160) | 48 | 400 | UB (30/60) | B (300) | 160 | B (400) | 50 | 400 | B (300) |
| ***AC Side Current Ripple*** | *Low* | *Low* | *Low* | *High* | *High* | *High* | *Low* | *Low* | *Low* | *Low* | *Low* | *Low* | *Low* |
| ***DC Side Current Ripple*** | *Low* | *Low* | *Low* | *Low* | *Low* | *High* | *High* | *Low* | *Low* | *High* | *High* | *High* | *Low* |
| ***Output Polarity*** | *Neg* | *Neg* | *Neg* | *Pos* | *Pos* | *Pos* | *Both* | *Neg* | *Neg* | *Pos* | *Pos* | *Pos* | *Neg* |
| ***Output Nature*** | *S* | *S* | *S* | *D* | *D* | *D* | *D* | *D* | *D* | *D* | *D* | *D* | *D* |
| ***Control*** | Sim | Sim | Sim | Com | Com | Com | Com | Sim | Sim | Sim | Sim | Sim | Sim |
| ***Voltage stress*** | $V_m$+ $V_o$ | $V_m$+ $V_o$ | $V_m$+ $V_o$ | $V_m$+ $V_o$/2 | $V_m$ | $V_m$+ $V_o$ | $V_m$+ $V_o$/2 | $V_m$+ $V_o$/2 | $V_m$+ $V_o$/2 | $V_m$+ $V_o$/2 | $V_m$+ $V_o$/2 | $V_m$+ $V_o$/2 | $V_m$+ $V_o$/2 |
| ***Gate driver*** | 2 | 1 | 1 | 2 | 2 | 2 | 2 | 1 | 1 | 1 | 1 | 1 | 1 |
| ***Mode*** | *DCM* | *DCM* | *DCM* | *CCM* | *DCM* | *DCM* | *BCM* | *DCM* | *DCM* | *DCM* | *DCM* | *DCM* | *DCM* |
| ***VS/CS*** | 2/1 | 1 | 1 | 1/1 | – | 1 | 3/1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ***Switching frequency*** | 100 kHz | 50 kHz | 40 kHz | 65 kHz | 100 kHz | – | 20 kHz | 20 kHz | 50 kHz | 50 kHz | – | 50 kHz | 20 kHz |
| ***Min. THD/ Peak PF*** | 2.1/ 0.99 | <2/- | -/0.99 | 43.4/ 0.88 | 3.3/ 0.99 | - /0.9999 | 14.8/ 0.99 | 4.5/ 0.99 | 3.2/ 0.99 | 3.49/ 0.99 | 32.4/ 0.91 | 2/ 0.99 | 2.4/ 0.99 |
| ***Power(W)/ Efficiency (%)*** | 200/ 95.8 | 150/ 93.2 | 100/ 96.40 | 700/ 96.4 | 120/ 92.7 | 1000/ 96 | 100/ 93.5 | 400/- | 100/ 91.1 | 1000/ 94.0 | 100/ 92 | 1000/ 95.7 | 400/ 94.52 |

*Totem pole: TP, Bridgeless: BL, RC: Reconfigurable Circuit, FR Diode: Fast recovery diode, SR Diode: Slow-rate diode, TC: Total Component, CCS: Component Conducting Simultaneously, Neg: Negative, Pos: Positive, PF: Power factor, VS: Voltage Sensor, CS: Current Sensor, BCM: Boundary conduction mode, UB: Unbalanced, B: Balanced, S: Single Output, D: Dual Output, Sim: Simple, Com: Complex,*

Notably, $L_{o1}$ and $L_{o2}$ satisfy DICM operation throughout positive half and negative half of $V_s$, respectively as displayed in Fig. 17(b). Converter components operating in positive half, $V_{\mathrm{sw1}}$, $V_{Ca}$, $V_{Do1}$, and $i_{Lo1}$, are displayed in Fig. 18(a). Here, energy transfer capacitor ($C_a$) is operating under CVCM. Both switches ($S_1$ and $S_2$) are turned ON under zero switching conditions leading to lower switching loss of switches. Moreover, diodes turning OFF with zero current contribute to significant loss reduction at switching time. Furthermore, supply side current confirms CICM operation of input inductor ($L_i$). Motor phase winding voltage along with phase current for phase A and phase B is illustrated in Fig. 18(b). Phase winding voltage is 150 V at rated condition and phase current is nearly 6 A peak. In general, PFC aided SRM drive has achieved good outcomes while running under normal circumstances and is consistent with design assumptions.

*2) Dynamic Performance Validation:* In this part, an analysis is performed on dynamic behavior of supply voltage as well as dc link voltage. The range of voltage variations that is taken into consideration for grid is from 220 V (rms) to 160 V (rms) for undervoltage fluctuations and from 220 V (rms) to 260 V (rms) for overvoltage uncertainties. SR motor speed control is achieved by changing dc link voltage. Split dc link voltages ($V_{\mathrm{dc1}}$ and $V_{\mathrm{dc2}}$) are half of dc link voltage. In Fig. 19(a), $V_{\mathrm{dc1}}$ and $V_{\mathrm{dc2}}$ vary for wide-speed SR motor control. Grid supply is fixed at 220 V and dc link varies from 100 to 300 V. Accordingly, split dc link voltages vary from 50 to 150 V as shown in Fig. 19(a). Grid current increases to maintain power balance between input and output. Motor speed changes from 1000 to 1500 r/min and then reaches 2000 r/min as $V_{\mathrm{dc1}}$ and $V_{\mathrm{dc2}}$ vary from 50 to 100 V and then to 150 V, respectively, as demonstrated in Fig. 19(b). Furthermore, supply voltage fluctuations are considered for drive performance analysis. In this, supply voltage is altered to 160 V from a rated condition for undervoltage fluctuation analysis. Fig. 20(a) shows under voltage supply (160 V) variation from 220 V. DC link voltage is maintained at rated 300 V. Moreover, phase voltage is 160 V with single pulse control. During instances of overvoltage supply fluctuation, supply voltage rises from 220 to 260 V. Drive power requirement remains constant at rated dc link voltage, and is achieved by regulating supply current, as illustrated in Fig. 20(b).

*3) Power Quality of Presented PFC-Fed SRM Drive:* Proposed TPBLDO front end converter for MPC assisted SRM drive is designed to control motor speed along with maintaining grid

power quality. At different levels of both voltage and power, power quality indexes such as distortion factor, displacement factor, THD, and PF are examined. Fig. 21(a)–(i) illustrates findings of a supply-side power quality assessment carried out through a single-phase power quality analyzer. Results presented in Fig. 21(a)–(c) show grid current THD at rated power 408 W with 227 V (rms) and 300 V dc link voltage. Grid current THD at nominal condition is 2.4% with unity PF. Other results outlined for supply under voltage fluctuation at lower power (156–100 V dc link voltage) and overvoltage fluctuation at rated power (257–300 V dc link voltage) clearly show $i_s$ and $v_s$ are in phase with each other. Grid current THD for under-voltage fluctuation and overvoltage fluctuations are 3.2% and 3.3% as depicted in Fig. 21(d)–(i), respectively.

The impact of load variations on grid current THD under different power supply as well as load conditions is thoroughly analyzed and illustrated in Fig. 22(a). Notably, the proposed PFC converter is designed to maintain a high-PF while effectively regulating current THD over a broad supply voltage range of 160 V RMS to 260 V RMS and across different power levels, as demonstrated in Fig. 22(a). This ensures stable and efficient operation under varying grid conditions, reducing power quality issues and enhancing system reliability. By minimizing harmonic distortions in supply current, converter adheres to international power quality standards, including IEC 61000-3-2 and IEEE 519 [36].

*4) Comparative Analysis:* This study provides a detailed analysis of BL dual output PFC converter, including design, its operation, and control for MPC-assisted SRM drive. A comparative analysis of the presented PFC converter with an available BL buck and buck boost type PFC converter is discussed in this section. Table VI elaborates a detailed comparison of proposed TPBLDO PFC converter with current counterparts, focusing on critical performance metrics such as total component count, simultaneously conducting component count, control complexity, supply voltage adaptability, output voltage with their polarity, switch stress, supply current THD, PF, operating ranges, and efficiency. However, in buck converters, when the input voltage is lower than output voltage, input current is zero, resulting in dead angle in input current, which leads to a poor PF and high level of input current THD of BL buck-based PFC converters [31], [44]. Moreover, to maintain grid power quality as per IEC standards, various methods are discussed in the literature, which increases the cost and complexity of BL buck PFC converter [38], [43], [45]. As system under consideration necessitates a front-end PFC converter, which is capable of broad range dc voltage (100–300 V) control along with significant supply fluctuations (160–260 V), buck converter is not a viable competitor to proposed dual output BL PFC converter. Furthermore, BL PFC converters designed with single and dual buck boost output are elaborated in [22], [39], [40], [41], [42], [46], [47], and [48]. Integrated PFC converter under consideration utilizes the voltage-doubler concept applied to single-phase SEPIC rectifier operating in DCM, as proposed in [47]. Considering dual output requirements, presented converter has lower component count as compared to [17], [19], [40] and [41]. Moreover, converters in [38] and [39] exhibit discontinuous input current, requiring reconfigurable input filters for PFC implementation. Unlike [22], Mahdavi et al. [39], Shen and Yang [40], Dah et al. [46], and Costa et al. [47] presented PFC converter has ripple free current at output side, which reduces dc link capacitor's size and prolongs capacitor's life span. A comprehensive loss analysis of proposed converter, including a breakdown of losses in each component, has been conducted and is provided in the Appendix section. Estimated efficiency of proposed PFC converter under rated conditions, utilizing components listed in Table V, is approximately 94.52%. Although overall performance of proposed rectifier is thoroughly validated through proof-of-concept prototyping in a laboratory environment, its efficiency remains consistently high and competes well with state-of-the-art wide-range PFC ac–dc converters [17], [22], [40], [41], [42], [47]. Consequently, design and optimization of presented PFC converter in commercial form undoubtedly guarantee greater efficiency than discussed alternatives.

Based on experimental outcomes, loss analysis, and comparison table review as demonstrated in Table VI, it is noticed that proposed converter facilitates several advantages such as dual output availability, fewer components, wide range supply voltage adaptability, broad range of output voltage, low supply current THD, unity PF, and higher efficiency.

## VII. Conclusion

This work presents a BL totem-pole dual-output PFC rectifier that supplies a SRM drive, tailored for low-power applications. The operation of converter in DCM is examined through detailed circuit analysis, supported by both theoretical and experimental validation. Converter components are designed considering a wide range output voltage variation along with large supply voltage fluctuations. This converter is reliable for low power SRM drives because of its affordable cost, straightforward control, and single-sensor necessity for DCM operation. In addition, the presented control scheme has enabled variable dual output balanced voltages for wide speed motor control, along with ensuring unity PFs at supply end. To verify the effectiveness of presented PFC converter under various operating conditions, a 400-W SRM drive laboratory prototype is tested. Notably, presented TPBLDO rectifier operates with almost unity PF (0.9996), reduced THD of 2.4% in grid current, and having 94.52% efficiency at rated condition, making it a suitable candidate for low-power applications requiring an SRM drive aided by a midpoint converter.

## Appendix

### A. Losses Break Down and Efficiency Analysis

Using current waveform as depicted in Fig. 9, average and RMS current in each active and passive component are estimated as discussed in (20)–(29). Power loss is calculated for line cycle, i.e, 50 Hz. Moreover, presented PFC converter is symmetrical for positive and negative line cycle, hence only positive half cycle loss analysis is sufficient for converter's efficiency. As the switch $S_1$ current is given as

$$i_{S_1}(t) = \begin{cases} i_{Li}(t) + i_{Lo1}(t), & 0 \le t \le D_{sw}T_{sw} \\ 0, & D_{sw}T_s \le t \le (D_{sw} + D_d)T_{sw} \end{cases} \tag{20}$$

i.e.,

$$i_{s1}(t) = \frac{v_s dt}{L_i} + \frac{v_s dt}{L_{o1}} = \left(\frac{1}{L_i} + \frac{1}{L_{o1}}\right) v_s dt = \frac{v_s dt}{L_{eq1}}. \tag{21}$$

$$i_{D_{o1}}(t) = \begin{cases} 0 & 0 \le t \le D_{sw}T_{sw} \\ i_{Li}(t) + i_{Lo1}(t) & D_{sw}T_{sw} \le t \le (D_{sw}+D_d)T_{sw} \\ 0 & (D_{sw}+D_d)T_{sw} \le t \le T_{sw} \end{cases} \quad \forall \text{ Positive half cycle.}$$

Switch $S_1$ peak current is mentioned in (13). For switching period, average switch current ($i_{S1(\text{avg})\text{SC}}$) is given as

$$\begin{aligned} i_{s_1(avg)}\big|_{SC} &= \frac{1}{T_{sw}} \int_0^{T_{on}} i_{S_1}(t)dt \\ &= \frac{1}{T_{sw}} \int_0^{D_{sw}T_{sw}} \frac{i_{S_1(peak)}}{D_{sw}T_{sw}} t dt \\ &= \frac{1}{T_{sw}} \times i_{S_1(peak)} \times \frac{D_{sw}T_{sw}}{2} = \frac{i_{S_1(peak)}D_{sw}}{2}. \end{aligned} \tag{22}$$

Furthermore, average value of $S_1$ current ($i_{s1\ (\text{avg})\text{LC}}$) over line cycle is calculated as

$$i_{S_1(avg)}\big|_{LC} = \frac{1}{T_l} \int_0^{T_l/2} i_{sw(avg)}\big|_{sc} dt. \tag{23}$$

The rms current of $S_1$ estimated in swicthing frequency is as

$$\begin{aligned} & i_{s1(\text{rms})}\big|_{\text{SC}} \\ &= \sqrt{\frac{1}{T_{\text{sw}}} \int_0^{\text{DT}_{\text{sw}}} i^2{}_{s1}(t)dt} = \sqrt{\frac{1}{T_{\text{sw}}} \int_0^{D_{\text{sw}}T_{\text{sw}}} \left(\frac{i_{s1(\text{peak})}}{D_{\text{sw}}T_{\text{sw}}} t\right)^2 dt} \\ &= \sqrt{\frac{1}{T_{\text{sw}}} \times \frac{i^2{}_{s1(\text{peak})}}{(D_{\text{sw}}T_{\text{sw}})^2} \times \frac{(D_{\text{sw}}T_{\text{sw}})^3}{3}} = i_{s1(\text{peak})} \sqrt{\frac{D_{\text{sw}}}{3}}. \end{aligned} \tag{24}$$

Furthermore, the rms value of $S_1$ current ($i_{s1\ (\text{avg})\text{LC}}$) over line cycle is calculated referring [31] and written as

$$i_{s1(\text{rms})}\big|_{\text{LC}} = \sqrt{\frac{1}{T_l} \int_0^{T_l/2} \left(i_{s1(\text{rms})}\big|_{\text{sc}}\right)^2 dt}. \tag{25}$$

Moreover, the diode $D_{o1}$ current is expresses as, unnumbered equation shown at the top of this page.

Using peak diode current ($i_{Do1(\text{peak})}$) as mentioned in (16), average diode current for switching frequency and line frequency are calculated as

$$i_{Do1(avg)}\big|_{SC} = \frac{1}{T_{sw}} \int_0^{T_{on}} i_{Do1}(t)dt = \frac{i_{D_{o1}(peak)}(D_d - D_{sw})}{2} \tag{26}$$

$$i_{Do1(avg)}\big|_{\text{LC}} = \frac{2}{T_l} \int_0^{T_l/2} i_{D_{o1}(\text{avg})}\big|_{\text{sc}} dt = \frac{D(D_1 - D)T_{\text{sw}}V_m}{\pi L_{\text{eq1}}}. \tag{27}$$

Similarly average and rms currents of $S_2$ and $D_{o2}$ current are calculated for negative half cycle for loss analysis. Input side inductor current is supply current whose rms value is well known. In addition, using inductor and load current, capacitor's rms current is estimated. Output dc link capacitor current ($i_{Co1}$) in positive half cycle is given as

TABLE VII
LOSS BREAKDOWN ESTIMATION OF PFC CONVERTER

| ***Active Component Losses*** |
|---|
| Switch ($S_1$/$S_2$) losses, (Switch loss= Conduction loss+ Switching loss) $P_{sw1/2\_c}(t) = v_{CE0} \cdot i_{sw1/2(avg)}(t) + r_{CE} \cdot i^2{}_{sw1/2(rms)}(t)$ $P_{sw1/2\_s} = V_{sw1/2(peak)} \cdot I_{sw1/2(avg)} \cdot (t_{fall}) \cdot f_{sw}$ |
| Line Diode ($D_1$/$D_2$) losses, $P_{D_1/D_2} = V_{THL} \cdot I_{D_1/D_2(avg)} + r_{T_l} \cdot I^2{}_{D_1/D_2(rms)}$ |
| Fast recovery Diode ($D_{o1}$/$D_{o2}$) losses, $P_{D_{o1}/D_{o2}} = V_{THF} \cdot I_{D_{o1}/D_{o2}(avg)} + r_{TF} \cdot I^2{}_{D_{o1}/D_{o2}(rms)}$ |
| ***Passive Component Losses*** |
| Input Inductor ($L_i$) Loss ($P_{Li}$), $P_{L_i\_copper} + P_{L_i\_core} = I^2_{Li(rms)} \cdot r_{L_i} + k_c f^{\alpha}{}_{sw} B^{\beta} V_{e\_L_i}$ |
| Output Inductors ($L_{o1}$/ $L_{o2}$) Losses ($P_{Lo1/Lo2}$), $P_{L_{o1}/L_{o2}(copper)} + P_{L_{o1}/L_{o2}(core)} = I^2_{L_{o1}/L_{o2}(rms)} \cdot r_{L_{o1}/L_{o2}} + k_c f^{\alpha}{}_{sw} B^{\beta} V_{e\_L_{o1}/L_{o2}}$ |
| Intermediate Capacitor ($C_a$/$C_b$) Losses, $P_{C_a/C_b} = I^2_{C_a/C_b\_rms} \times ESR\_C_a / C_b$ |
| DC Link Capacitors ($C_{o1}$/$C_{o2}$) Losses, $P_{C_{o1}/C_{o2}} = I^2_{C_{o1}/C_{o2}\_rms} \cdot ESR\_C_{o1} / C_{o2}$ |

$S_1$/$S_2$ forward voltage drop ($V_{\text{CEO}}$) = 1.2 V; $S_1$/$S_2$ forward resistance ($r_{\text{CE}}$) = 0.011 Ω; $S_1$/$S_2$ fall time ($t_{\text{fall}}$) = 60 ns; Switching frequency ($f_{\text{sw}}$) = 20 kHz; $D_1$/$D_2$ forward voltage drop ($V_{\text{THL}}$) = 0.8 V; $D_1$/$D_2$ on state resistance ($r_{Tl}$) = 0.010 Ω; $D_{o1}$/$D_{o2}$ forward voltage drop ($V_{\text{THF}}$) = 1.2 V; $D_{o1}$/$D_{o2}$ on state resistance ($r_{\text{TF}}$) = 0.010 Ω; ESR of $L_i$ ($r_{Li}$) = 0.3Ω, ESR of $L_{o1/o2}$ ($r_{Lo1/o2}$ ) = 0.03Ω,; ESR of $C_{a/b}$ (ESR_$C_a$/$C_b$) = 0.025Ω, ESR of $C_{o1/o2}$ (ESR_$C_a$/$C_b$) = 0.085 Ω; Psw_c and Psw_s are switch conduction losses and switching losses, respectively; $P_{Lo1/Lo2\_\text{copper}}$ are Copper losses, and $P_{Lo1\_\text{core}}$ is Core losses in $L_{o1}$ and $L_{o1}$, $\alpha$, $\beta$, and $k_c$, are material parameters; $B$ is peak flux density; $V_e$ is core volume.

Then rms current ($I_{Co1}$(rms)) in $C_{o1}$ is calculated as [31]

$$I_{C_{o1}(\text{rms})}\big|_{\text{LC}} = \sqrt{\frac{1}{T_l} \int_0^{T_l/2} \left(i_{C_{o1}}(t)\right)^2 d(\omega t)}. \tag{29}$$

Conduction and switching losses of PFC converter components are estimated using component's parameter along with mathmatical expressions as provided in Table VII. Moreover, based on expression as mentioned in Table VII, critical losses associated with major components are analyzed at rated conditions (i.e., $P = 400$ W, $v_s = 220$ V, $V_{\text{dc}} = 300$ V, $f_{\text{sw}} = 20$ kHz) and their breakdown is showcased in Fig. 22(b). Finally, efficiency variations under different loading conditions with supply voltage fluctuations are analysed and demonstated in Fig. 22(c). Peak efficiencies at rated load with 160 V and 260 V rms supply voltage are 94.86 W and 93.2 W, respectively. Notably, improved efficiency is observed at lower input voltages, which ensure reduces power losses, enhances thermal management, and extends component lifespan, in low-voltage conditions.

### B. SRM Motor's Parameters

Stator/rotor pole = 8/6, phases = 4, respectively, rated Voltage = 300 V, rated speed = 2000 r/min, per phase resistance = 0.98 Ω, unaligned inductance = 24.6 mH, aligned inductance = 5.90 mH.

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