Systematic Efficiency-Density Co-Optimization of 100 kW GaN Traction Inverter: Methodology and Integration

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***Abstract*—The increasing pursuit of high efficiency and power density in EV traction inverters is accelerating the deployment of the wide bandgap device, including silicon carbide (SiC) and gallium nitride (GaN). As the efficiency-density boundary of the SiC traction inverter has approached its limitation, the traction inverter utilizing GaN devices, with lower power loss and higher switching speed, is considered as a promising solution. Focusing on the GaN traction inverter for EV applications, this article proposes a design methodology considering the co-optimization of the pursued efficiency and power density objectives. Based on the created mathematical models of design concerns, including power loss, dc-link ripple, and thermal resistance, the efficiency-density design domain of the GaN inverter is established, upon which the optimal design space of the efficiency-density is determined through Pareto frontier analysis. Based on the co-optimization results, a 100 kW / 400 V GaN traction inverter prototype is compactly integrated, incorporating meticulously designed key components, including the GaN power module, dc-link capacitor, and heat sink. Experimental validation confirms the effectiveness of the proposed co-optimization methodology and demonstrates the feasibility of the integrated GaN inverter, achieving the high power density 62.1 kW/L and peak efficiency 99.3%.**

***Index Terms*—Coordination optimization, gallium nitride (GaN), high efficiency, high power density, integration design, traction inverter.**

I. INTRODUCTION

DRIVEN by global energy challenges and semiconductor technology breakthroughs, electric vehicles (EV) are experiencing unprecedented development [1], [2], [3]. The traction inverter (see Fig. 1) is the core of energy conversion in the EV, regulating the energy flow between the battery and the motor [4], [5]. Due to the demands of extended driving range and enhanced vehicle performance, the traction inverter is continuously pursuing higher efficiency and power density [6], [7], thus accelerating the adoption and development of wide bandgap (WBG) devices in EV [8], [9], [10]. Some commercialized traction inverters have employed silicon carbide (SiC) devices to replace traditional silicon (Si) counterparts, enhancing efficiency and power density [11], [12], [13], [14]. However, the efficiency-density limitation of the SiC traction inverter is being approached, and the high cost of devices constrains their broader deployment. Compared with SiC, gallium nitride (GaN) features a faster switching speed, lower power loss, and cost-reduction potential [15], [16], [17]. Therefore, the high-capacity GaN traction inverter emerges as a promising solution to surpass the existing SiC efficiency-density boundary, marking the technological frontier of the next-generation EV.

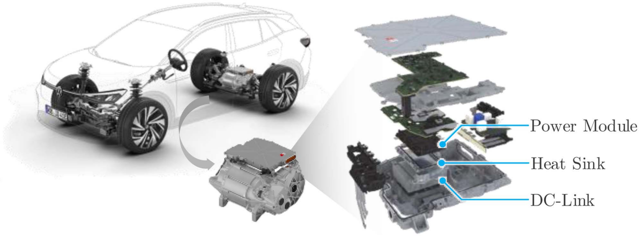

Fig. 1. Exploded structure of traction inverter in EV system.

Several research efforts have been explored for GaN traction inverters to enhance power density and improve efficiency, as well as to meet the high-power demands of EV traction systems. Regarding enhancing power density, the volume of the inverter is compressed through the miniaturization of active and passive components [18], [19]. To reduce the volume of GaN power modules, embedded packaging [20], 3D packaging [21], and integrated gate driver [22], [23] have been explored. Furthermore, some advanced high-density capacitor solutions, such as stacked ceramic capacitors [24], [25], hybrid electrolytic-film capacitors [26], and active switching capacitors [27], have replaced traditional large-sized film capacitors in dc-link. Besides, the current source inverter discards the capacitor in the topology [28], [29], which is conducive to miniaturization design.

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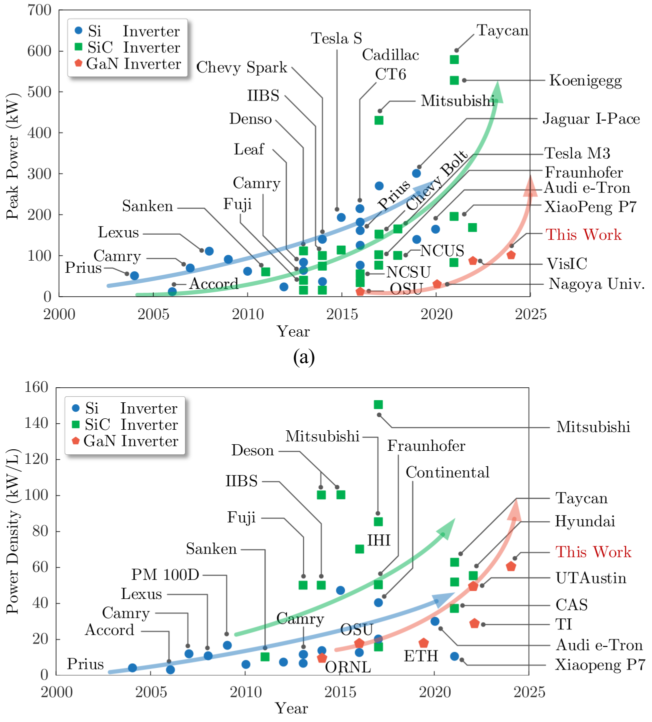
Additionally, the volume of heat sink is significantly reduced through employing high-heat-flux cooling techniques, including substrate microchannels cooling [30] and 3D printed microjets cooling [31], etc. Regarding improving efficiency, the primary focus is on reducing power losses at device-level and system-level. To minimize the switching losses of the GaN device, the additional p-GaN-layer process reduces the dynamic on-state resistance [32], and the active gate driver enhances the switching speed by regulating switching trajectory [33]. Since turn-ON losses dominate the power losses of GaN devices, achieving zero voltage switching mode through resonant networks can enhance the converter efficiency [34]. Besides, by applying adaptive dead-time technology [35], dynamic switching frequency regulation [36], and switching mode sequence control [37], the power losses under various operating conditions can be effectively decreased. The adoption of more efficient topologies, such as the dual-bridge inverter [38] and T-type three-level inverter [39], [40], is beneficial to the system efficiency. Moreover, multiobjective optimization methods for power electronic converters have also been developed [41], [42], [43], providing valuable references for optimizing the efficiency and power density of GaN-based systems. Regarding expanding power capacity, due to the limited current capacity of the single GaN device, multiple devices must be parallel connected to meet the high-power requirements of EV traction inverter [44]. In general, utilizing printed circuit board (PCB) to parallel connect GaN devices is a flexible and cost-effective solution [45]. The parallel connection of multiple devices increases the demand for heat dissipation, which can be effectively managed by employing the insulated-metal-substrate [46] and direct-bonded copper board [47], to establish a low-thermal-resistance pathway. In order to reduce the parasitic inductance in parallel, the direct parallel packaging of GaN bare chips can improve the parallel performance [48], [49]. In addition, some other novel packaging concepts have been introduced into GaN modules, which are conducive to improving the electrical and thermal performance, including silver sintering [50], flexible PCB [51], double-sided cooling [52], integrated filters [53], and center-symmetric layouts [54], etc. Thanks to the impetus of these researches, the efficiency-density performance and power capacity of GaN are enhancing, which is accelerating the adoption of GaN in EV traction inverters. However, due to the inherent trade-off between efficiency and power density, independent optimization alone cannot achieve the systematic optimal performance required for GaN inverters to surpass the existing efficiency-density limitation. Meanwhile, to meet the 100 kW-class power demand of EV traction inverters, the high-power integration of GaN devices is still scarce.

Motivated by these challenges, this article proposes a comprehensive design methodology for the efficiency-density co-optimization of high-capacity GaN traction inverter. Based on the derived analytic model of device power loss, dc-link capacitor, and heat sink thermal management, the frequency-based "efficiency-power density" design space for the GaN inverter is formulated. The Pareto frontier analysis is utilized to identify the optimal design point in terms of efficiency and power density. Finally, the stepwise design and integration of GaN traction inverter with high efficiency and high power density are conducted.



(a)

(b)

Fig. 2. State-of-the-art and trends of EV inverters. (a) Peak power and (b) volumetric power density.

The rest of this article is organized as follows. The current technological status, challenges and optimization approaches of the EV traction inverter are highlighted in Section II. Taking the power losses, dc-link, and heat sink into account, the model-based development of an "efficiency-power density" design space and co-optimization methodology for the GaN inverter are established in Section III. Based on the co-design results, details of the stepwise design and integration for the GaN traction inverter are demonstrated in Section IV. In Section V, the developed GaN inverter prototype is experimentally validated. Finally, Section VI concludes this article.

II. GAN TRACTION INVERTERS: STATE-OF-THE-ART, MAIN CHALLENGES AND SYSTEMATIC OPTIMIZATION APPROACHES

A. State-of-the-Art and Trends of EV Traction Inverter

The current development status and trends of EV traction inverters are illustrated in Fig. 2(a). As the power ratings of traction inverters continue to increase, this trend is accompanied by a rise in volume and total losses. Therefore, the challenge of jointly enhancing efficiency and power density has become progressively more prominent. The power density of traction inverters is summarized in Fig. 2(b). It is evident that the power density of traction inverters can be significantly improved through the utilization of SiC and GaN power devices.

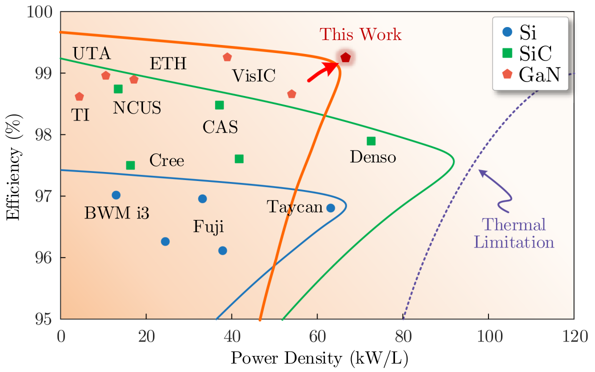


Fig. 3. “Efficiency-power density” boundary in EV traction inverters with various power devices.

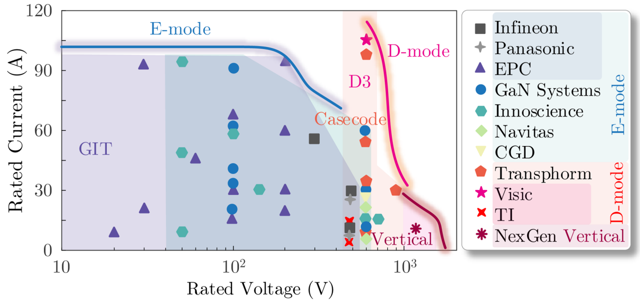


Fig. 4. Voltage-current rating distribution across various GaN devices.

Additionally, efficiency is another key factor that needs to be considered simultaneously. The efficiency and power density distribution of traction inverters are depicted in Fig. 3. The results demonstrate that, owing to the superior electrothermal properties, the WBG devices extends the “efficiency-density” frontier of the EV traction inverters in comparison with Si-based devices. Due to the high junction temperature tolerance of the SiC devices and the application development in recent years, the SiC inverters has performed outstandingly in terms of power density. However, their efficiency has approached the limitation. Benefiting from enhanced semiconductor properties, the GaN inverters demonstrates superior efficiency boundaries and exhibits promising high power density evolutionary trends. Thus, the GaN traction inverters is progressively pushing the existing “efficiency-density” frontier.

B. *Challenges of GaN Traction Inverters for EV Applications*

The voltage and current ratings of available GaN devices are statistically summarized in Fig. 4. On the one hand, the EV traction inverter imposes relatively high-power level demands, whereas commercially available GaN devices are rated for low-power levels, and there is a lack of mature high-current power module solutions. On the other hand, compared with Si and SiC devices, the GaN devices offer multiple technical variants with distinct characteristics. Consequently, for the GaN traction inverter applications, it is essential to carefully select the GaN device type and integrate the devices in parallel for the high-power module.

Furthermore, the volume of traction inverters is primarily composed of the power module, dc-link, and heat sink. However, in the current research on GaN inverters, the optimization and design of each component are usually presented in separate literature. In practice, the design parameters of these components are intricately linked to the switching frequency and output power of the inverter. Meanwhile, due to the dependency on switching frequency and the influence of output power, there is a fundamental trade-off between efficiency and power density. The design space for efficiency and power density is bounded by a fundamental frontier, as shown in Fig. 3. Therefore, to promote higher performance in GaN inverters, it is crucial to uniformly consider the design of the power module, dc-link, and heat sink comprehensively.

In light of the above issues, in order to achieve a breakthrough in efficiency-density of the next-generation GaN traction inverters, some challenges need to be overcome.

Challenge 1*:* How to comprehensively consider the impact of power module, dc-link capacitor, and heat sink on the “efficiency-power density” of GaN inverters?

Challenge 2*:* How to achieve the co-optimization of “efficiency and power density” in GaN inverters?

Challenge 3*:* How to select and integrate GaN devices in parallel for the high-power traction inverter applications?

C. *Systematic Optimization Methodology of GaN Traction Inverter*

To address the challenges currently encountered by GaN traction inverters, a systematic co-optimization methodology for “efficiency-density,” coupled with an integrated design framework, is proposed. This method accounts for the influence of all key components in the traction inverter, starting from the modeling of power modules, dc-link capacitors, and heatsinks, to construct a system-level efficiency-density design space, within which co-optimization is achieved. The optimization outcomes are then used to guide the design of each key component and the integration of the GaN traction inverter.

The proposed optimization methodology and integration for GaN traction inverter are systematically summarized and generalized into a flowchart, as shown in Fig. 5. In Section III, the “efficiency-density” co-optimization methodology is developed. Based on the optimization results, a 100 kW GaN prototype is stepwise designed and high density integrated in Section IV.

III. METHOD OF CO-OPTIMIZATION DESIGN FOR EFFICIENCY AND POWER DENSITY IN GAN TRACTION INVERTERS

In this section, the co-optimization methodology for efficiency-power density in GaN traction inverters will be elaborated in detail. First, a loss evaluation model for the GaN inverter is established, and candidate GaN devices are assessed and selected. Second, the volume-switching frequency relationship of the dc-link capacitor and the thermal resistance-switching frequency constraint of the heat sink are separately formulated. Finally, based on these models, the “efficiency-power density” design space of the GaN inverter is constructed, and the optimal

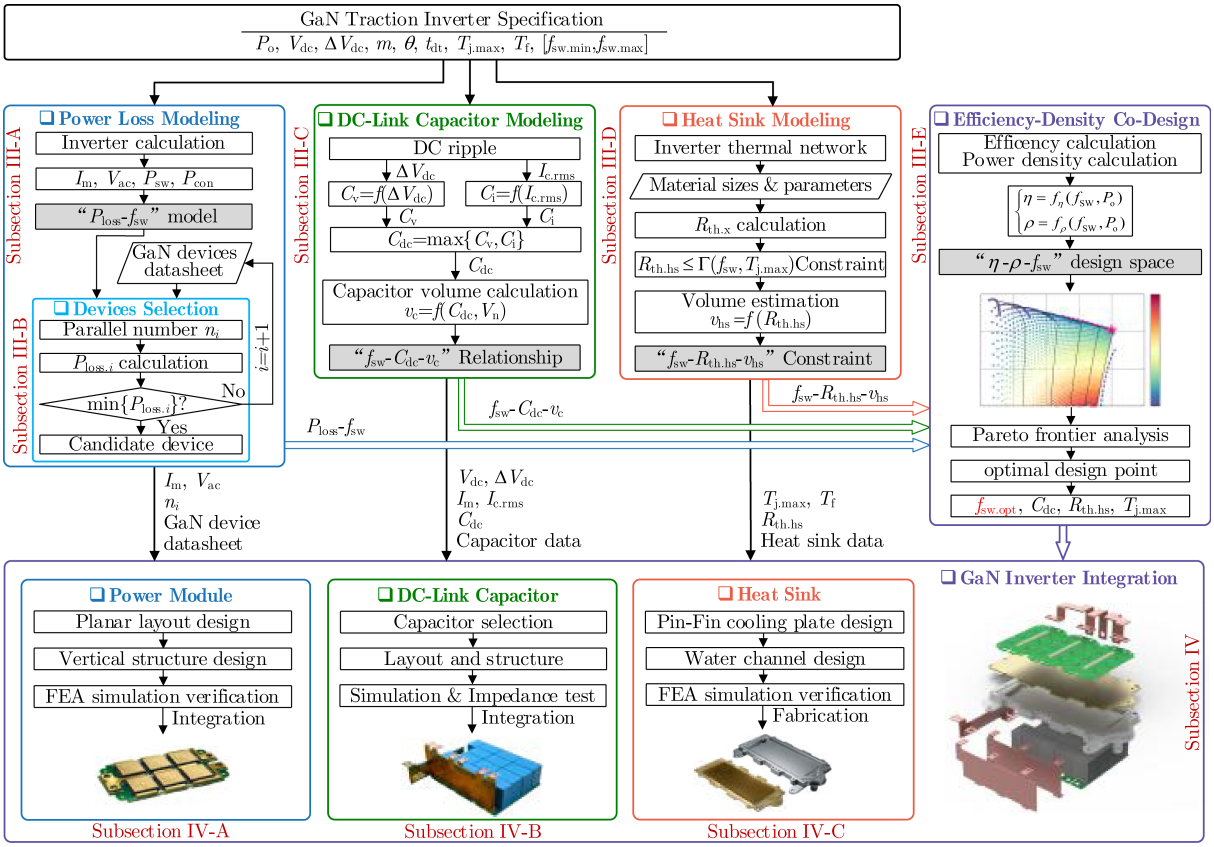


Fig. 5 Flowchart of co-optimization method and integration for GaN traction inverter.

design points for achieving both high efficiency and high power density are identified through the Pareto frontier analysis.

A. Power Losses Modeling of GaN Traction Inverter

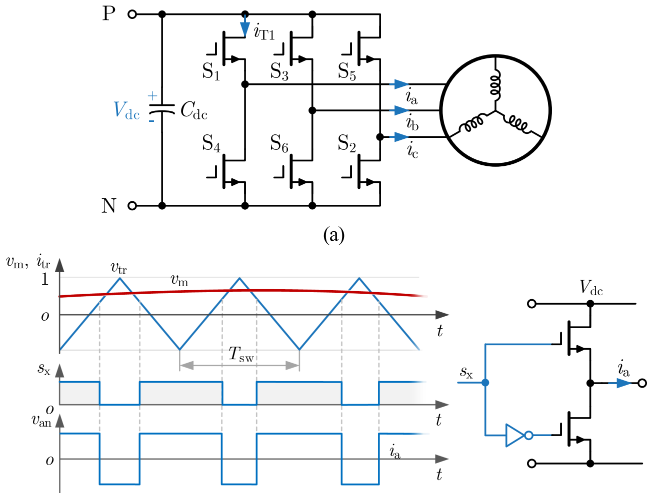
Evaluation of power loss is a critical aspect of inverter design, as it not only influences the conversion efficiency of the inverter, but also significantly impacts the thermal design of the system. In this article, the three-phase two-level topology, a fundamental and widely used configuration for traction inverters in EVs, is utilized, as depicted in Fig. 6(a). In addition, the dc-link bus voltage of 400 V and the maximum output power of 100 kW are taken as the design objectives in this article.

According to the inverter topology, the output power of the inverter is related to the output voltage and the phase leg currents, which can be expressed as

$$P_o = \sqrt{3}V_{ac}I_{\text{rms}}=\sqrt{3}V_{ac}I_m/\sqrt{2} \tag{1}$$

where P_o is the output power. V_{ac} is the root mean square (RMS) value of output line-line voltage. I_{rms} and I_m represent the RMS and amplitude value of the output current for phase-leg, respectively. The output voltage V_{ac} is determined by the dc-link voltage V_{dc}, the modulation method, and modulation ratio m. Considering the classical SPWM modulation shown in Fig. 6(b), the amplitude of phase-leg output current can be written as

$$I_m = \frac{\sqrt{6}P_o}{3mV_{\text{ac}}} = \frac{4P_o}{3mV_{dc}} \tag{2}$$



(a)

(b)

Fig. 6. Schematic of GaN traction inverter. (a) Topology of inverter and (b) modulation principle of phase-leg.

where $m = \sqrt{2}\ V_{\text{ac}}/V_{\text{dc}}$ is modulation ratio. Based on the operating conditions of the inverter and the characteristics of the devices, the power losses can be evaluated.

The power losses of GaN devices consist of conduction loss and switching loss. To evaluate the losses of GaN devices in the inverter, the average power losses over one sinusoidal cycle are consistently used as a standard metric for assessment.

1) Conduction Loss: For high-power level inverters, the loss calculation is conducted based on a phase-leg switch consisting of *n* parallel-connected GaN devices. Additionally, to account for the impact of the dead time in the phase-leg, the conduction loss is analyzed and calculated for the entire phase-leg as a whole [19]. In a phase-leg, the conduction loss of an individual GaN device in the high-side switch S_1 or the low-side switch S_4 can be expressed respectively as

$$\begin{cases} P_{\mathrm{con}.H} = \frac{I_m^2}{n^2}\left(\frac{1}{8} + \frac{m\cos\varphi}{3\pi}\right)R_{\mathrm{ds.on}} \\ P_{\mathrm{con}.L} = \frac{I_m^2}{n^2}\left(\frac{1}{8} - \frac{m\cos\varphi}{3\pi}\right)R_{\mathrm{ds.on}} \end{cases} \tag{3}$$

where $R_{\mathrm{ds.on}}$ is ON-state resistance of GaN device. In particular, due to the self-commutated reverse conduction mechanism of GaN HEMT, the increased conduction loss during dead-time needs to be taken into consideration. The conduction loss of a phase-leg during the dead time can be represented as

$$P_{\mathrm{con}.dt} = \frac{t_{dt}f_{\mathrm{sw}}}{\pi}\left(\frac{\pi}{2}R_F\frac{I_m^2}{n^2} + 2V_F\frac{I_m}{n}\right) \tag{4}$$

where V_F and R_F stand for equivalent reverse voltage drop and reverse conduction resistance, respectively. t_{dt} is dead-time. f_{sw} is switching frequency. Considering the dead-time, the portion of the aforementioned conduction loss occurring during this period should be reduced accordingly for the necessary adjustment. This process can be described as

$$P_{\mathrm{con.red}} = \frac{1}{2}\frac{I_m^2}{n^2}R_{\mathrm{ds.on}}t_{dt}f_{\mathrm{sw}}. \tag{5}$$

Based on (3) to (5), the total conduction loss of a phase-leg with *n* parallel GaN devices can be expressed as

$$P_{\mathrm{con}} = n(P_{\mathrm{con}.H} + P_{\mathrm{con}.L} + P_{\mathrm{con}.td} - P_{\mathrm{con.red}}). \tag{6}$$

2) Switching Loss: The losses during the switching transient of the device include turn-ON loss, turn-OFF loss, output capacitance loss and gate loss. The turn-ON and turn-OFF losses can be respectively written as

$$\begin{cases} P_{\mathrm{sw.on}} = E_{\mathrm{on}}\frac{f_{\mathrm{sw}}}{\pi}\frac{V_{\mathrm{dc}}I_m}{nV_nI_n} \\ P_{\mathrm{sw.off}} = E_{\mathrm{off}}\frac{f_{\mathrm{sw}}}{\pi}\frac{V_{\mathrm{dc}}I_m}{nV_nI_n} \end{cases} \tag{7}$$

where E_{on} and E_{off} are the turn-ON and turn-OFF losses of the device under the rated test conditions, respectively. V_n and I_n represent the rated voltage and current of the device, respectively. Operating as a free continuation device, the reverse recovery loss can be yielded as

$$P_{\mathrm{rec}} = E_{\mathrm{rec}}\frac{f_{\mathrm{sw}}}{\pi}\frac{V_{\mathrm{dc}}I_m}{nV_nI_n} \tag{8}$$

where E_{rec} is the recovery loss of the device at the rated test conditions. With the exception of Cascode GaN devices, the reverse recovery loss in other GaN HEMT is negligible because the reverse recovery charge is almost zero. Along with the switching transient, the charging and discharging loss of the output capacitor can be expressed as

$$P_{\mathrm{oss}} = V_{\mathrm{dc}}Q_{\mathrm{oss}}f_{\mathrm{sw}} \tag{9}$$

where Q_{oss} is the output charge of the GaN device. The corresponding loss induced by the charging and discharging of the gate charge can be expressed as

$$P_g = (V_C - V_E)Q_{g.\mathrm{tot}}f_{\mathrm{sw}} \tag{10}$$

where $Q_{g.\mathrm{tot}}$ is the total gate charge of the GaN device. V_C and V_E are the turn-ON and turn-OFF driving voltages, respectively. According to (7) to (10), the total switching loss of a switch with *n* parallel GaN devices can be written as

$$P_{\mathrm{sw}} = n(P_{\mathrm{sw.on}} + P_{\mathrm{sw.off}} + P_{\mathrm{rec}} + P_{\mathrm{oss}} + P_g). \tag{11}$$

3) Total Power Loss: Based on (6) and (11), in a phase-leg, the total power loss in its high side and low side devices can be expressed as

$$P_{\mathrm{loss.ph}} = P_{\mathrm{con}} + 2P_{\mathrm{sw}}. \tag{12}$$

In addition to the power devices, the dc-link capacitor loss $P_{\mathrm{loss.dc}}$ should be considered in the inverter loss analysis

$$P_{\mathrm{loss.dc}} = I_{c.\mathrm{rms}}^2 \cdot \mathrm{ESR}(f) \tag{13}$$

where $I_{c,\mathrm{rms}}$ is the ripple current RMS value of the dc-link capacitor. ESR (*f*) is the frequency-dependent equivalent series resistance of the capacitor, which can be taken from datasheets at the principal ripple frequency.

Therefore, the total power loss of the three-phase inverter can be expressed as

$$P_{\mathrm{loss.inv}} = 3P_{\mathrm{loss.ph}} + P_{\mathrm{loss.dc}} = 3P_{\mathrm{con}} + 6P_{\mathrm{sw}} + P_{\mathrm{loss.dc}}. \tag{14}$$

B. Selection and Evaluation of GaN Devices

1) Candidate GaN Devices: Selection of the appropriate GaN power device according to the design objectives of the inverter is an essential step for the subsequent design. First of all, the device is required to meet the voltage and current stress requirements. For voltage stress, the 650 V nominal voltage of conventional GaN devices already meets the 400 V dc-link voltage requirement. However, for current stress, according to (2), the current amplitude is $I_m = 370$ A, and currently, there are no commercially available GaN products that meet this current rating. Therefore, the proposed GaN inverter requires a solution with multiple GaN devices in parallel. In order to reduce the number of chips in parallel to reduce the size of the power module, GaN devices with high current rating are therefore prioritized. Among the existing commercially GaN HEMTs, GS66516T (GaN Systems) and V08TC65S1A2 (VisIC) are the devices with the largest current rating in E-mode and D-mode, respectively, and TP65H015G5WS (Transphorm) is the Cascode device with the largest current rating. Thus, the above three devices are taken as candidates, and their information is given in Table I.

2) Number of Parallel Devices: Based on the phase-leg current amplitude I_m, and the current rating of the devices, the number of GaN devices in parallel in a phase-leg switch can be determined. In addition, thermal and current margins should also be considered to expand the safe operating area and improve the

TABLE I
PARAMETERS OF CANDIDATE GAN DEVICES

Device		**Device 1**	**Device 2**	**Device 3**
Manufacturer		VisIC	GaN Systems	Transphorm
Part Number		V08TC65S1A2	GS66516T	TP65H015 G5WS
Device Type		D-mode	E-mode	Cascode
V_{DS}		650 V	650 V	650 V
I_D	25°C	200 A	60 A	95 A
	100°C	145 A	47 A	60 A
$R_{DS.on}$		7.8 mΩ	25 mΩ	19 mΩ
$Q_{g.tot}$		110 nC	14.2 nC	74 nC
C_{oss}		500 pF	126 pF	307 pF
Size		23×21 mm^2	9×7.64 mm^2	16×21 mm^2

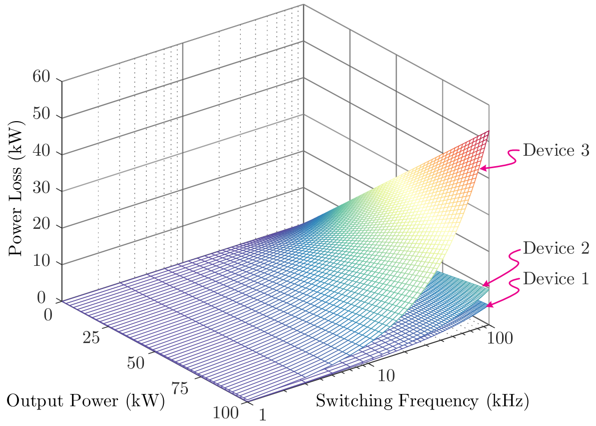


Fig. 7. Total power loss of GaN devices at different output powers and switching frequencies.

capability to handle overload conditions. Considering the derating of device current due to increased operating temperature, the number of parallels can be calculated as

$$n = \left\lceil \frac{I_m k_T k_I}{I_D} \right\rceil \tag{15}$$

where $k_T = I_{D.@25°C} / I_{D.@\ 100°C}$ is the current derating factor with temperature rise of device. k_I is the current margin factor, which is taken as 1.2 in this design. Therefore, the number of parallel devices required for candidate GaN devices are $n_1 = 3$ (Device 1, V08TC065S1), $n_2 = 10$ (Device 2, GS66516T), $n_3 = 8$ (Device 3, TP65H015G5WS).

3) Power Loss and Efficiency: Based on the above power losses assessment model and the number of parallel devices, the total power losses of the candidate GaN devices at different output powers and switching frequencies are given in Fig. 7. Device 1 maintains the lowest total power loss under different operating conditions. In addition, the various power losses of candidate devices at full load conditions are calculated and shown in Fig. 8. The conduction losses P_{con} of each candidate device are relatively similar. Meanwhile, for switching loss, device 1 has the lowest turn-ON loss, which is only 53% of that of device 2. The turn-OFF loss $P_{\text{sw.off}}$ of device 1 and device 2 are similar and significantly lower than that of device 3. Device 3 experiences reverse recovery loss, whereas device 1 and device 2 have little to none. Overall, device 1 exhibits the lowest total power loss among candidate GaN devices.

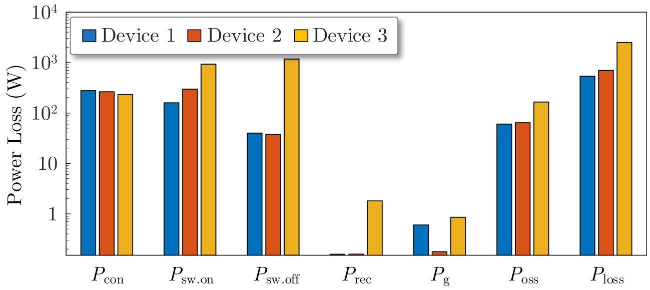


Fig. 8. Comparison of various power losses in candidate GaN devices under full-load conditions.

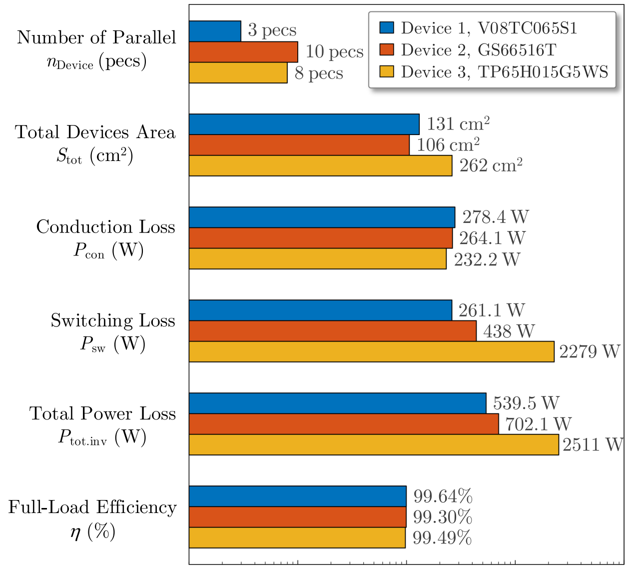


Fig. 9. Detailed power loss comparison of candidate GaN devices.

4) Comprehensive Comparison of GaN Devices: The comprehensive comparison results of candidate GaN devices are given in Fig. 9 to help in selecting a suitable device for designing high density inverters. Device 1 features the fewest parallel connections, aiding in the reduction of parasitic inductance and facilitating current balancing. Besides, the total areas of the parallel devices are calculated. It is found that the total area of the device 3 configuration is the largest, approximately twice that of the device 1 or device 2 configurations. Moreover, device 1 demonstrates the lowest total power loss and achieves the highest theoretical full-load peak efficiency of 99.64%. Consequently, summarizing the above comparisons, the device 1 (VisIC, V08TC065S1) is selected for the inverter design in this article.

C. f_{sw}-C_{dc}-*Volume Modeling of DC-Link Capacitor*

The dc-link capacitor in the inverter stabilizes the dc-link voltage and absorbs the ripple current. Thus, the design of dc-link capacitor needs to simultaneously satisfy the requirements of

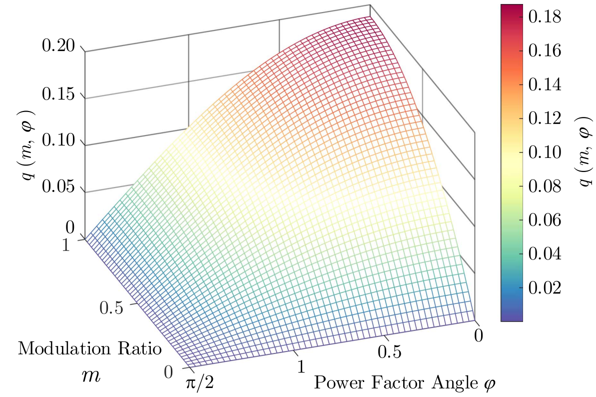


Fig. 10. Graph of function $q(m,\varphi)$in $m \in (0,1), \varphi \in (0,\pi/2)$.

ripple voltage and ripple current, which can be expressed as

$$C_{\text{dc}} = \max(C_v, C_i) \tag{16}$$

where C_v and C_i are the minimum capacitance to support ripple voltage and ripple current, respectively. The calculation of C_v and C_i are derived as follows

1) Capacitance for Ripple Voltage: DC-link capacitors are essential for absorbing voltage ripple to ensure the stability of the dc voltage. The ripple voltage $\Delta V_{\text{dc, pp}}$ is related to the peak-to-peak charge ΔQ_{c} of the capacitor [55], [56], which can be expressed as

$$\Delta V_{\text{dc,pp}} = \frac{\Delta Q_c}{C_v} = \frac{I_m}{C_v f_{\text{sw}}} q(m,\varphi) \tag{17}$$

where $q\,(m, \varphi)$ is a coefficient function of the capacitor charge with respect to the modulation ratio m and power factor angle φ. Considering the effective operating area of the EV inverter, i.e., $m \in (0, 1)$, $\varphi \in (0, \pi/2)$, the graph of the function $q\,(m, \varphi)$ is displayed in Fig. 10. In order to meet the maximum voltage ripple requirements, the worst operating conditions are obtained when $m = 1$, $\varphi = \pi/2$, while considering the margin of voltage ripple, the capacitance to support ripple voltage C_v can be expressed as

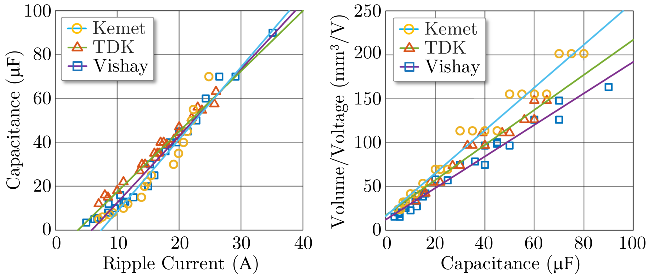
$$C_v \approx \frac{I_m}{5 f_{\text{sw}} \Delta V_{\text{dc,pp}}}. \tag{18}$$

In this design, a 5% ripple voltage margin is considered, i.e., $\Delta V_{\text{dc,pp}} = 5\% V_{\text{dc}}$.

2) Capacitance for Ripple Current: The minimum ripple current capability $I_{c\text{.rms}}$ required by the dc-link capacitor is determined by the ac output current amplitude I_m, modulation ratio m, and power factor angle φ [25], [56], which can be calculated as

$$I_{c\text{.rms}} = I_m \sqrt{2m \left[\frac{\sqrt{3}}{4\pi} + \cos^2(\varphi) \left(\frac{\sqrt{3}}{\pi} - \frac{9}{16} m \right) \right]}. \tag{19}$$

Owing to the superior reliability and cost-effectiveness of film capacitors, they are preferentially employed in the dc-link of EV inverter. The ripple current tolerance and capacitance of film capacitors from TDK, Kemet, and Vishay are concluded and illustrated in Fig. 11(a). Based on the statistical analysis of commercially available capacitors, it is evident that there is a positive correlation between ripple current tolerance and capacitance. This relationship can be fitted and expressed as



(a) (b)

Fig. 11. Characteristics of various capacitors. (a) Current-capacitance and (b) capacitance-volume.

TABLE II
PARAMETERS OF CAPACITOR CURRENT-CAPACITANCE AND CAPACITANCE-VOLUME MODELS

Capacitor	Current-Capacitance		Capacitance-Volume	
	k_{C1} (μF/A)	k_{C2} (μF)	k_{V1} (mm³/V·μF)	k_{V2} (mm³/V)
Kemet	3.0	–17.8	1.8	12.2
TDK	2.4	–10.1	2.0	17.3
Vishay	3.3	–24.3	2.4	16.4

$$C_i = k_{C1} I_{c\text{.rms}} + k_{C2} \tag{20}$$

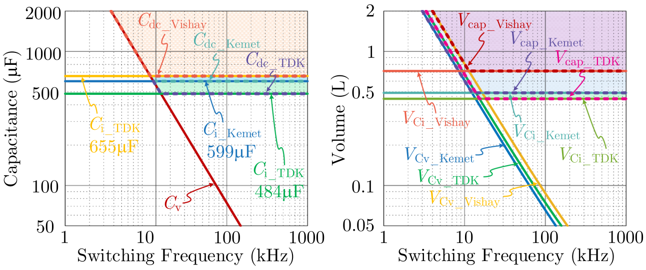
where k_{C1} and k_{C2} denote the current-capacitance coefficients. According to the samples show in Fig. 11(a), these coefficients can be estimated, as given in Table II. It is noted that TDK exhibits the highest current-capacitance density among the film capacitor candidates. This characteristic will be advantageous in reducing the capacitance necessary for ripple currents, consequently minimizing the overall volume of the capacitor.

3) Volume of Capacitors: The volume of the dc-link capacitor is dependent on both rated voltage and capacitance, which are constrained by the manufacturing processes and film insulation distances. The relationships of capacitance-volume-voltage from manufacturers TDK, Kemet, and Vishay, are shown in Fig. 11(b). The capacitance is positively correlated with volume/voltage, which can be expressed as

$$v_c = (k_{V1} C_{\text{dc}} + k_{V2}) V_n \tag{21}$$

where v_c is the volume of the capacitor. k_{V1} and k_{V2} are coefficients of calculating capacitor volume. V_n is rated voltage of the capacitor. According to the samples shown in Fig. 11(b), these coefficients can be estimated, as given in Table II.

Based on (16), (18), and (20), the ripple voltage capacitance C_v and ripple current capacitance C_i can be computed for various switching frequency operating scenarios. These calculations enable the establishment of "switching frequency-capacitance" boundary for the dc-link capacitance, i.e., f_{sw}-C_{dc}, as shown in Fig. 12(a). It can be observed that the dc-link capacitance is dominated by the ripple voltage capacitance C_v at low frequencies. As the frequency rises, the dc-link capacitance gradually



(a) (b)

Fig. 12. (a) Current-capacitance and (b) capacitance-volume characteristics of commercial capacitors.

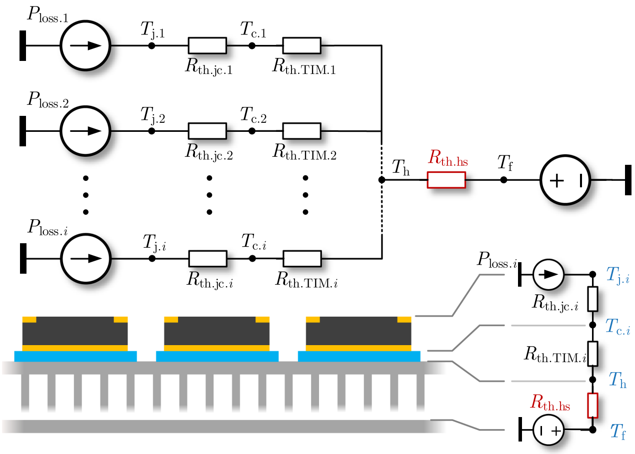


Fig. 13. Thermal circuit model of phase-leg with n parallel chips.

decreases and ultimately becomes defined by the current ripple capacitance C_i at high frequencies. According to (21), the "switching frequency-volume" boundary of the dc-link capacitor, i.e., f_{sw}-v_c, can be obtained in Fig. 12(b). In conclusion, the f_{sw}-C_{dc}-v_c model for the dc-link capacitor has been established, which can be applicable for calculating the capacitance value and estimating the volume of the dc-link capacitor in GaN inverters. Among the results, the TDK film capacitor exhibits the lowest volume boundary and is therefore selected for this design.

D. f$_{sw}$-R$_{th}$-Volume Modeling of Heat Sink

The power losses P_{loss} generated by the GaN devices in the inverter are dissipated via the heat sink, ensuring that the chip junction temperature T_j remains below the maximum allowable junction temperature $T_{j.\mathrm{max}}$, thereby maintaining device thermal stability. The thermal resistance of the thermal path consists of the junction-to-case resistance $R_{\mathrm{th.jc}}$ of the GaN device, the thermal interface material (TIM) resistance $R_{\mathrm{th.TIM}}$, and the heat sink resistance $R_{\mathrm{th.hs}}$. Based on the path of heat dissipation, for a phase-leg with n parallel devices, the thermal circuit model is shown in Fig. 13.

In practice, device power loss $P_{\mathrm{loss.}i}$ and heat sink thermal resistance $R_{\mathrm{th.hs}}$ play significant roles in junction temperature T_{j} due to the basically fixed thermal resistance of device junction-to-case $R_{\mathrm{th.jc}}$ and TIM $R_{\mathrm{th.TIM}}$. Device power loss vary with switching frequency and output power. Based on the power loss model presented in Section II-A, the power loss of single GaN device can be formulated as

TABLE III

STRUCTURE SIZE AND MATERIAL CHARACTERISTIC PARAMETERS FOR THERMAL MODELS

	Material	λ_T [W/(m·K)]	h_T (mm)	A_T (mm^2)	R_{th} (K/W)
GaN Device	—	—	—	23 × 21	0.1
TIM	SAC305	63.2	0.1	23 × 21	0.003
Heat Sink	Copper	380	—	>(23 × 21)	$R_{\mathrm{th.hs}}$

$$P_{\mathrm{loss}.i} = \frac{1}{2n} P_{\mathrm{loss.ph}} \tag{22}$$

where $i = 1, 2, \ldots, n$ denotes the device index in a phase-leg with n parallel devices. The relationship between the device junction temperature T_j and heat sink temperature T_h can be denoted as

$$T_{j.i} - T_h = P_{\mathrm{loss}.i}(R_{\mathrm{th.jc}.i} + R_{\mathrm{th.TIM}.i}). \tag{23}$$

Through the thermal circuit model, the relationship between the heat sink temperature T_h and the cooling fluid temperature T_f can be derived as

$$T_h - T_f = R_{\mathrm{th.hs}} \sum_{i=1}^{2n} P_{\mathrm{loss}.i}. \tag{24}$$

Substituting (22) and (24) into (23), the thermal resistance limit constraint of the heat sink can be obtained as

$$R_{\mathrm{th.hs}} \leq \frac{T_{j.\mathrm{max}} - T_f - P_{\mathrm{loss}.i}(R_{\mathrm{th.jc}} + R_{\mathrm{th.TIM}})}{\sum\limits_{i=1}^{2n} P_{\mathrm{loss}.i}}. \tag{25}$$

In the thermal model, the junction-to-case thermal resistance and the maximum junction temperature of the GaN device can be obtained from the device datasheet, i.e., $R_{\mathrm{th.jc}} = 0.1$ K/W, $T_{j.\mathrm{max}} = 150\,^{\circ}\mathrm{C}$. The structural size and material characteristics of each layer in the thermal model are detailed in Table III. The thermal resistance $R_{\mathrm{th.TIM}}$ of the TIM layer can be calculated as

$$R_{\mathrm{th.TIM}} = \frac{h_{\mathrm{TIM}}}{\lambda_{\mathrm{TIM}} A_{\mathrm{TIM}}}. \tag{26}$$

The thermal resistance $R_{\mathrm{th.hs}}$ of the heat sink plays a crucial role in determining the overall heat dissipation performance of the system, especially considering the relatively fixed thermal resistances of the device $R_{\mathrm{th.jc}}$ and the TIM $R_{\mathrm{th.TIM}}$. Based on (25), the distribution of thermal resistance $R_{\mathrm{th.hs}}$ and junction temperature T_{j} under different switching frequencies, i.e., f_{sw}-T_j-$R_{\mathrm{th.hs}}$, is shown in Fig. 14(a). In practical design considerations, an adequate temperature margin needs to be guaranteed, so the maximum operational junction temperature $T_{j.\mathrm{max}}$ is set at 125 °C.

Upon collecting the data, the thermal resistance and volume of the heat sink are intricately related to the heat dissipation method. Some typical samples of natural air cooling, forced air cooling, and liquid cooling are presented in Fig. 14(b). Under the same heat dissipation method, the volume of the heatsink

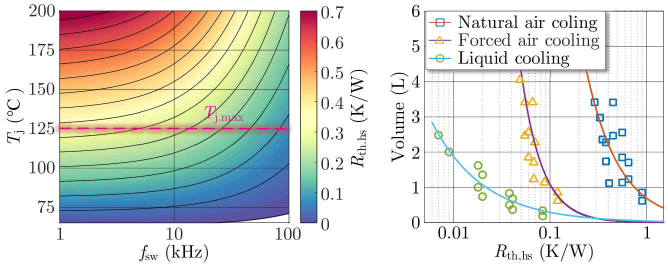


Fig. 14. Thermal resistance modeling of heat sink. (a) f_{sw}-T_j-$R_{\mathrm{th.hs}}$ distribution and (b) $R_{\mathrm{th.hs}}$-volume relationship for different cooling methods.

TABLE IV
PARAMETERS OF THERMAL RESISTANCE-VOLUME MODELS

	Natural Air Cooling	Forced Air Cooling	Liquid Cooling
k_{hs} (L·W/K)	0.694	0.011	0.045
α_{hs}	–1.276	–1.993	–0.809

v_{hs} is negatively correlated with its thermal resistance $R_{\mathrm{th.hs}}$. As the volume of the heat sink increases, its heat dissipation performance enhances, and its thermal resistance decreases. Based on the data in Fig. 14(b), the relationship between the thermal resistance $R_{\mathrm{th.hs}}$ of the heat sink and the volume v_{hs} of the heat sink is fitted and can be approximated as

$$v_{\mathrm{hs}} = k_{\mathrm{hs}}(R_{\mathrm{th.hs}})^{\alpha_{\mathrm{hs}}} \tag{27}$$

where k_{hs} and α_{hs} are coefficients of calculating heat sink volume, respectively. The coefficients for volume calculation associated with different types of heat sinks are given in Table IV.

It is evident that, under identical thermal resistance conditions, the volume of the heat sink required for liquid cooling is minimized. Consequently, liquid cooling heat sinks are highly effective in enhancing the power density of inverters and are given primary consideration in EV. In summary, based on the models depicted in Fig. 14(a) and (b), the "switching frequency-thermal resistance-volume" constraint of the heat sink, i.e., f_{sw}-$R_{\mathrm{th.hs}}$-v_{hs}, is established.

E. Efficiency-Density Space and Pareto Frontier Co-Optimization

Based on the power loss model of inverter, the f_{sw}-C_{dc}-v_c model of dc-link capacitor, and f_{sw}-$R_{\mathrm{th.hs}}$-v_{hs} constraint of heat sink, the "efficiency-power density" (η–ρ) model for the GaN traction inverter is formulated.

1) Efficiency of GaN Inverter: According to the power loss model, inverter efficiency η can be expressed as

$$\eta = \frac{P_o}{P_{\mathrm{in}}} = \frac{P_o}{P_o + P_{\mathrm{loss.inv}}} \tag{28}$$

where P_{in} is the dc-link input power. P_o represents the rated output power as specified in the system design. The total inverter power loss $P_{\mathrm{loss.inv}}$, which was previously discussed in (14), exhibits a significant dependence on both the switching frequency f_{sw}, and the rated power P_o, denoted as $P_{\mathrm{loss.inv}}$ (f_{sw}, P_o). Therefore, based on (14) and (28), the inverter efficiency η can be characterized as a function of switching frequency and rated power, denoted as η (f_{sw}, P_o).

2) Power Density of GaN Inverter: The volume of the GaN inverter is primarily determined by the GaN power module, dc-link capacitor, and heat sink. The power density ρ is given by

$$\rho = \frac{P_o}{v_{\mathrm{tot}}} = \frac{P_o}{v_M + v_c + v_{\mathrm{hs}} + v_{\mathrm{other}}} \tag{29}$$

where v_{tot} is the total volume of inverter. v_{other} is the additional volume attributed to other components and is considered a fixed value. Considering the relationship between the rated current and the number of parallel-connected devices, the volume of the power module is correlated with the rated power P_o, i.e., v_M (P_o). Based on the f_{sw}-C_{dc}-v_c model for the dc-link, the volume of the dc-link capacitor is determined by the switching frequency and the rated power, i.e., v_c (f_{sw}, P_o). According to the f_{sw}-$R_{\mathrm{th.hs}}$-v_{hs} constraint relationship of the heat sink, the volume of the heat sink is related to the switching frequency and the rated power, i.e, v_{hs} (f_{sw}, P_o). Therefore, the power density of the GaN inverter is determined by the switching frequency and the rated power, denoted as ρ (f_{sw}, P_o).

3) Efficiency-Power Density Design Space: Based on the aforementioned analysis, both efficiency η and power density ρ of GaN inverters are interdependent functions of switching frequency f_{sw} and rated power P_o, which can be collectively expressed as

$$\begin{cases} \eta = f_\eta(f_{\mathrm{SW}}, P_o) \\ \rho = f_\rho(f_{\mathrm{SW}}, P_o) \end{cases} \tag{30}$$

The "efficiency-power density" distribution of the GaN traction inverter, under varying switching frequencies (1 to 200 kHz) and rated power (1 to 100 kW), is illustrated in the f_{sw}–P_o operating space, as depicted in Fig. 15(a). It can be observed that the inverter exhibits excellent efficiency and power density in certain regions. However, the optimal "efficiency-power density" design point is inconvenient to determine under the f_{sw}–P_o coordinate. Therefore, the relationship between efficiency, power density and switching frequency is re-expressed in the $\boldsymbol{\eta}$**–**$\boldsymbol{\rho}$**–**$\boldsymbol{f_{\mathrm{sw}}}$ space, as shown in Fig. 15(b). The η–ρ upper convex envelope clearly identifies the Pareto frontier. The knee point of this frontier corresponds to the optimal design point $f_{\mathrm{sw.opt}} = 16$ kHz, where both efficiency and power density are maximized. Additionally, the 3D space representing the η–ρ–f_{sw} relationship is shown in Fig. 15(c). This multidimensional representation reveals the trend variations in design objectives through their orthogonal projections.

1) *Front View Projection:* Fig. 15(d) depicts the f_{sw}–η relationship under rated power conditions, demonstrating the efficiency degradation trend at higher switching frequencies.
2) *Top View Projection:* Fig. 15(e) illustrates the f_{sw}–ρ relationship, showing a distinct peak power density achievable at $f_{\mathrm{sw.opt}} = 16$ kHz.

Notably, the Pareto-optimal solution lies at this critical frequency point $f_{\mathrm{sw.opt}}$, where the theoretical maximum power density ($\rho_{\mathrm{max.theory}} = 80$ kW/L) is achieved while maintaining an

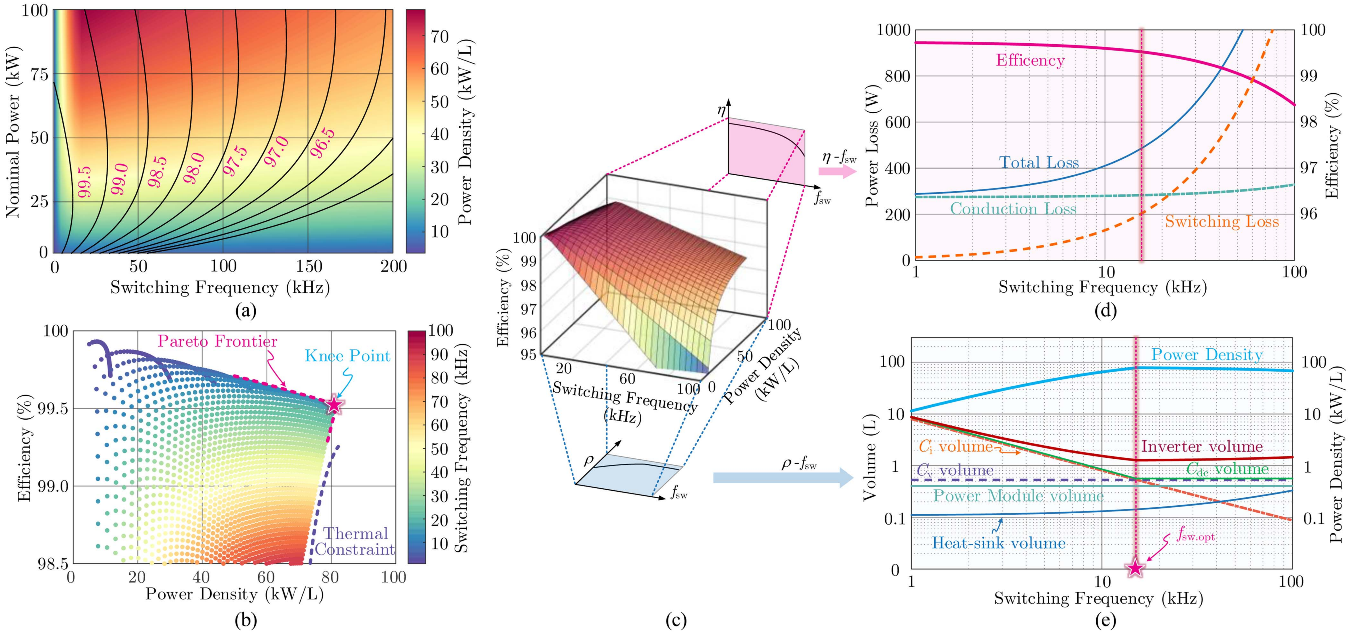


Fig. 15. GaN inverter efficiency-power density design space. (a) Efficiency-power density distribution at varying switching frequencies and rated powers. (b) Pareto frontier analysis of efficiency-power density. (c) 3D design space visualization of η–ρ–f_{sw} relationships. (d) f_{sw} –η projection at rated power conditions. (e) f_{sw} -ρ projection at rated power conditions.

TABLE V
OPTIMIZED DESIGN PARAMETERS OF GAN INVERTER

Parameters	Design value
DC-Link Voltage	400 V
Rated Power	100 kW
Phase Current	260 Arms
Switching Frequency	16 kHz
AC output Frequency	50 – 600 Hz
Heat Sink	Liquid Cooling, $R_{\mathrm{th.hs}} \leq 0.135$ K/W
DC-Link Capacitor	$\geq 484\,\mu$F

exceptional theoretical peak efficiency ($\eta_{\mathrm{max.theory}} = 99.5\%$). Based on the co-design, the parameters of the proposed GaN traction inverter are given in Table V.

IV. INTEGRATION OF GAN TRACTION INVERTER: POWER MODULE, DC-LINK, HEAT SINK, AND PROTOTYPE

The GaN inverter prototype is fabricated and integrated in this section. The design and manufacture of each component are based on the co-optimization results in Section III, with $f_{\mathrm{sw.opt}} =$ 16 kHz, $P_o = 100$ kW. The details of the design and integration are elaborated as follows.

A. Integration of High-Power GaN Module

As a result of the selection of GaN devices, a direct-drive D-mode GaN device V08TC65S1A2 from VisIC Technology is employed in the traction inverter design. Based on the co-design results, to achieve the target power level $P_o = 100$ kW, a half-bridge unit is implemented by paralleling three GaN devices (V08TC65S1A2). The three-phase inverter topology, composed of three half-bridge modules, offers a flexible and easily integrated solution.

1) Planar Layout of GaN Power Module: The layout and form factor of the module have been meticulously designed based on several critical considerations. *First*, the dimensions of the half-bridge module must be carefully designed to accommodate the spatial requirements for six GaN devices while ensuring sufficient spacing between the chips. *Second*, considering the high power density of the integrated half-bridge module, an "I-shaped" layout of parallel chips is employed to achieve a more compact inverter design. *Third*, the outer contour of the GaN module is designed with reference to existing commercial power modules, ensuring compatibility with standard installation and application requirements. Based on the area of the GaN device (21 mm × 23 mm) and the number of parallel devices ($n = 3$), the width and power terminal configuration of the designed module are modeled after the EconDual packaging. The GaN devices are integrated into the power module using a PCB as the interconnection carrier. To enhance current-carrying capacity and reduce parasitic inductance, copper blocks are embedded in the PCB for the dc+, dc–, and ac power paths. The planar layout of the designed power module is illustrated in Fig. 16(a) and (b). The current density distribution is obtained through the finite-element analysis (FEA) simulation, as shown in Fig. 16(c). Based on the simulation results, the parasitic inductance of the power loop in the designed power module is 6.4 nH.

2) Vertical Structure of GaN Power Module: The designed power module features a vertically integrated "*Sandwich*" structure, as shown in Fig. 17(a). The structure consists of three layers, from top to bottom: the driver isolation stage, the driver output stage, and the power stage. **The power stage** is integrated onto

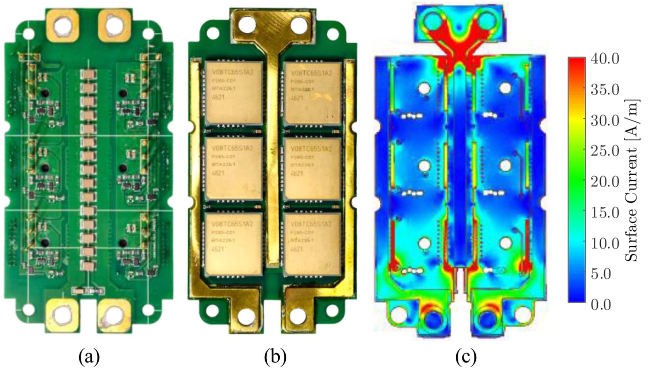


Fig. 16. Designed GaN power module layout and FEA-based simulation. (a) Top view, (b) bottom view, and (c) current density distribution.

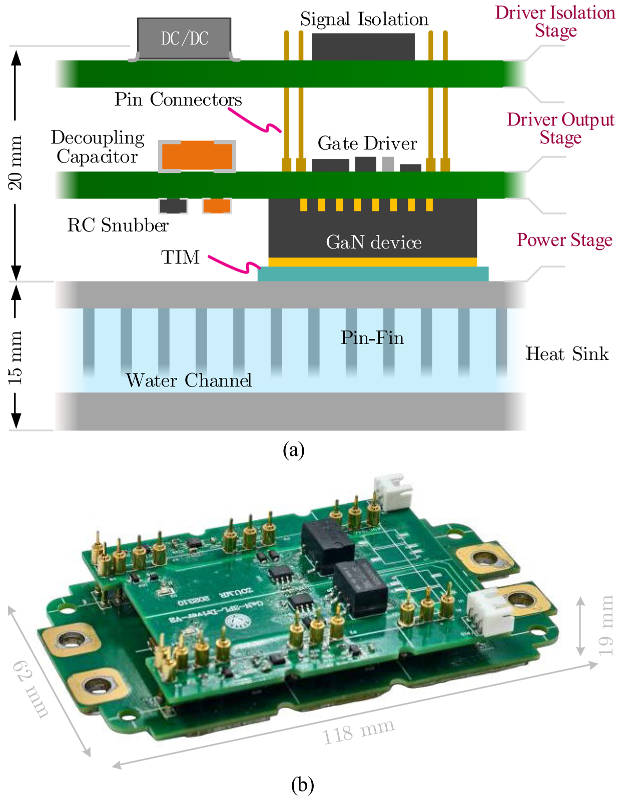


Fig. 17. Designed GaN power module. (a) Vertical structure schematic diagram and (b) fabricated prototype.

the bottom surface of the PCB module, making direct contact with the heat sink to minimize the thermal resistance of the thermal path. **The driver output stage** is integrated onto the top surface of the PCB module, thereby minimizing the parasitic inductance in the gate loop as much as possible and achieving a high degree of integration. The gate loop is carefully laid out, with the projection of driver output on the PCB nearly overlapping the gate and source pads of the GaN device. The output of the driver totem-pole is directly connected to the GaN gate through PCB vias, ensuring a gate drive path length of less than 2 mm. Based on the FEA, the loop inductance of the gate drive path is as low as 1.4 nH. Moreover, the decoupling capacitors and RC snubber circuits are also integrated into the PCB module. **The driver isolation stage** is implemented on a daughter-board at the top of the GaN module, connected to the GaN module via Pin headers, ensuring the delivery of driving signals and isolated power supply. The fabricated prototype of the designed GaN module is shown in Fig. 17(b).

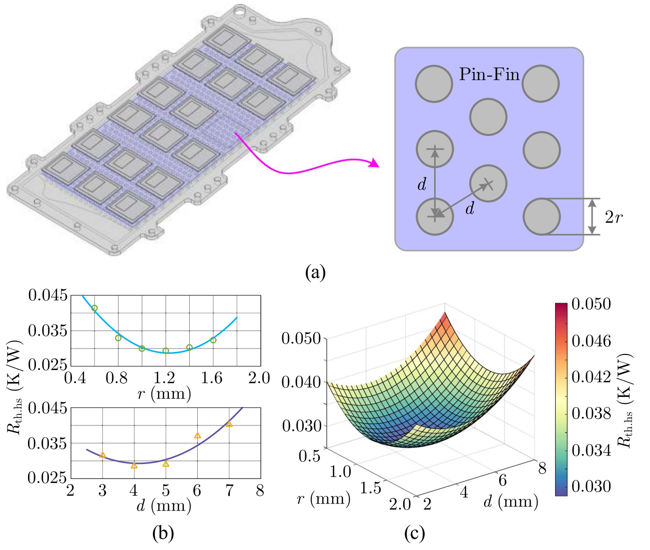


Fig. 18. Parameter design and optimization of the pin-fin heat sink. (a) Definition of structural parameters. (b) Simulation results under different values of d and r. (c) fitted thermal resistance surface within the design domain.

B. Design of Low Thermal Resistance Liquid Cooling Heat Sink

Based on the optimization outcomes from the co-design process, the heat sink of the GaN inverter utilizes the liquid cooling solution. The pin-fin liquid cooling is selected for this design due to its high heat flux and high density, as well as its superior performance in commercial power modules. Optimizing the layout of the pin-fin array can effectively enhance heat dissipation performance. The geometry of the pin-fin structure is primarily defined by two parameters: the pin spacing d and radius r, as illustrated in Fig. 18(a). Considering manufacturing feasibility and referencing typical values from commercial pin-fin designs, the design range for the pin-fin parameters is set as: 2 mm $\leq d \leq$ 8 mm, 0.5 mm $\leq r \leq$ 2 mm. To avoid design conflicts, such as pin overlap, a constraint must be applied to the design: $r < d\,/\,2$. The pin height, which has relatively little influence on thermal performance, is fixed at a typical value of 5.5 mm. Starting from a set of typical commercial values ($d = 5$ mm, $r = 1$ mm) as the initial parameters, FEA-based simulations are conducted for pin-fin heat sinks with varying pin radius r and spacing d. The corresponding thermal resistances are extracted, and the simulation results are shown in Fig. 18(b). Based on the simulation results, regression analysis is performed to fit a parametric surface of the heat sink thermal resistance within the design domain, as shown in Fig. 18(c). Due to the high heat flux capability of pin-fin liquid cooling, the thermal design constraints are generally satisfied across the design space.

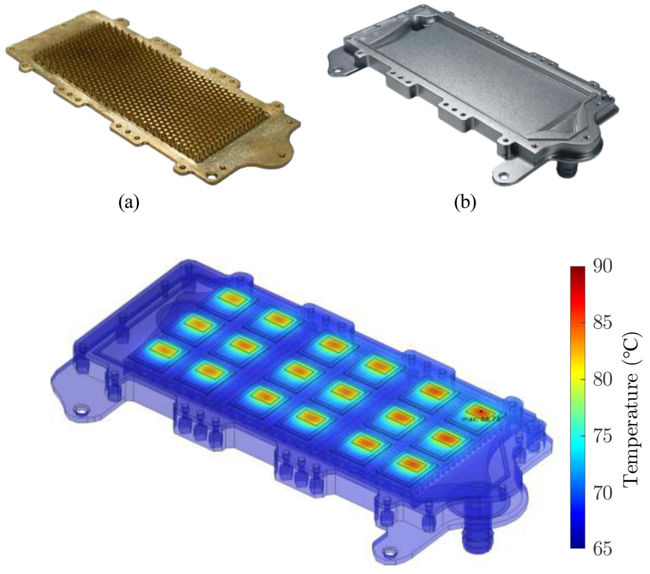


Fig. 19. Designed heat sink prototype and its FEA-based simulation. (a) Pin-Fin cooling plate, (b) water channel, and (c) thermal distribution.

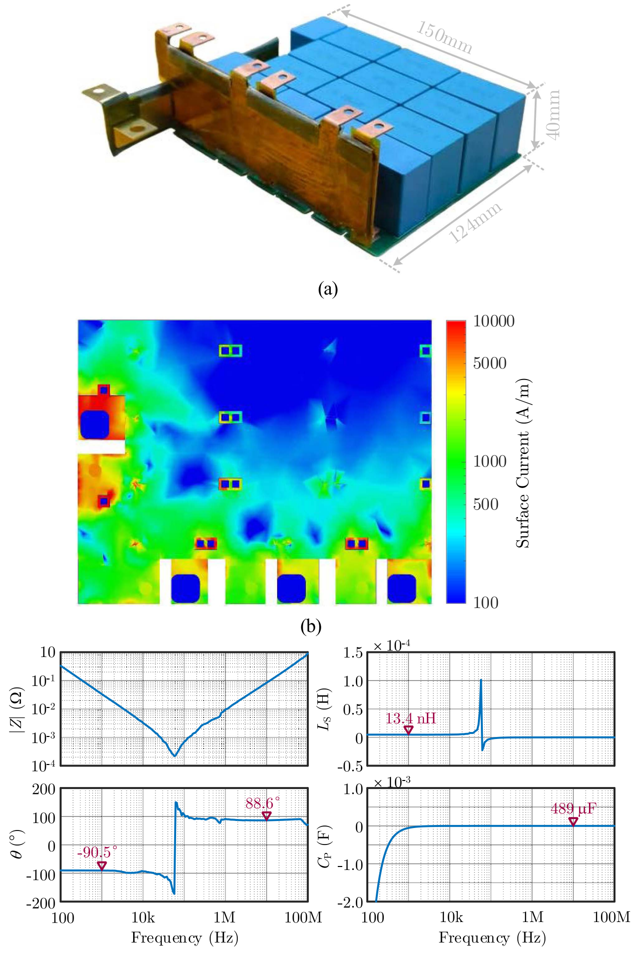


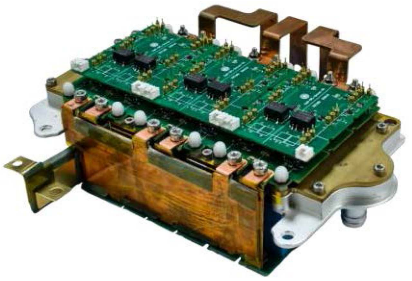
Fig. 20. Designed DC-link capacitor. (a) Prototype. (b) Current distribution FEA- based simulation. (c) Measured impedance parameters.

However, selecting the lowest point on the fitted surface can further enhance heat sink performance. Therefore, considering manufacturing tolerances and design constraints, the optimized pin-fin parameters of $d = 4.2$ mm, $r = 1.2$ mm are adopted near the surface minimum.

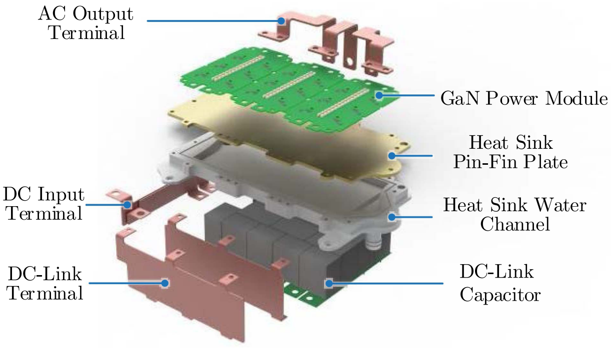
The designed heat sink consists of two main components: a pin-fin cooling plate and a water channel, as shown in Fig. 19(a) and (b), respectively. The pin-fin cooling plate is directly interfaced with the heat dissipation surface of GaN devices, establishing a thermal conduction pathway with low thermal resistance. The pin-fin design area encompasses the entire region beneath the GaN devices layout of the power module. Furthermore, the heat sink is designed with multiple precision-engineered mechanical mounting holes to facilitate convenient and secure installation and fastening. Validated through FEA-based simulation models, the heatsink demonstrates a thermal resistance of 0.029 K/W, meeting the thermal resistance design requirements under the maximum junction temperature constraint of co-design, i.e., $R_{\mathrm{th.hs}} \leq 0.135$ K/W (according to Section III-D). Under a 100 kW full-load current condition, the GaN device reaches a steady-state junction temperature of 86.7 °C. The thermal simulation results of the temperature distribution are shown in Fig. 19(c).

C. Integration of High Volume Density DC-Link

Through the calculations and comparisons in the Section III, the TDK capacitors are employed in the dc-link. Based on the co-design results, the dc-link capacitor exceeds 484 μF to ensure sufficient absorption of current ripples and support for the dc-link voltage. Furthermore, considering the dc-link capacitor vertically positioned beneath the module and heatsink, its projection area should closely match the footprint of the three-phase power module. This design ensures that the GaN inverter system attains high power density and a compact form factor. Therefore, based on the datasheet of the TDK film capacitor [57], the selection and design are as follows: with the voltage rating of 500 V@85 °C, 40 μF capacitors are arranged in a 3×3 configuration, and 22 μF capacitors are arranged in a 1×6 configuration. This design achieves a total capacitance of 492 μF ($\geq$ 484 μF) with dimensions of 150 mm × 124 mm × 40 mm, thereby fulfilling the specified requirements for dc-link capacitance. Furthermore, in the dc-link design, the input terminals, output terminals, and PCB layout, all adopt a stack-up design for dc+ and dc– to ensure minimal parasitic inductance. The fabricated prototype of the dc-link capacitor is shown in Fig. 20(a). The FEA-based simulation results of the dc-link current density distribution are shown in Fig. 20(b). Finally, the designed dc-link capacitor is measured using an impedance analyzer, with the resulting test curve shown in the Fig. 20(c). The measured capacitance is 489 μF, meeting the design target, while the parasitic inductance is as low as 13.4 nH.



(a)



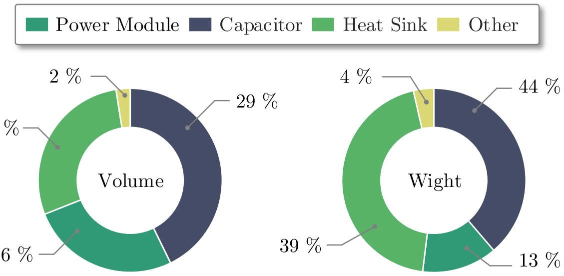
(b)

Fig. 21. Designed GaN traction inverter. (a) Prototype and (b) 3D exploded view.

Fig. 22. Installation of designed GaN traction inverter into a housing.

D. High Density Integration of GaN Traction Inverter

The designed GaN traction inverter is composed of GaN power modules, a dc-link capacitor, and a liquid cooling heat sink, all of which are vertically integrated into a compact stack. The prototype and exploded view of the designed GaN traction inverter are shown in Fig. 21(a) and (b), respectively. This integrated approach can enhance the compactness of the inverter prototype, thereby ensuring a high power density. The volume of the GaN traction inverter prototype, calculated based on its external contour, is 1.61 L. At the rated output power of 100 kW, the power density of the prototype is 62.1 kW/L. Additionally, Fig. 22 illustrates a demonstration of the assembled GaN inverter within a commercial traction inverter housing. Finally, the volume and weight distribution of various components in the GaN traction inverter prototype are summarized in Fig. 23.



(a) (b)

Fig. 23. Designed GaN traction inverter. (a) Volume distribution. (b) Weight distribution.

V. EXPERIMENTAL RESULTS AND ANALYSES

This section conducts switching characteristic tests on the designed GaN power module and performs power loading tests along with efficiency evaluations on the GaN traction inverter prototype. These experiments validate the efficiency and correctness of the proposed "efficiency-power density" co-design methodology, as well as demonstrate the feasibility and potential of the GaN traction inverter prototype.

A. Comprehensive Assessment of Dynamic Switching Performance for Designed GaN Module

The designed GaN power module, serving as the pivotal component of the GaN inverter prototype, necessitates dynamic characteristic evaluation across a range of conditions. A representative set of dynamic switching waveforms is shown in Fig. 24(a). Under a dc-link voltage $V_{\mathrm{dc}} = 400$ V and a junction temperature $T_{\mathrm{j}} = 25\,^{\circ}$C, Fig. 24(b) illustrates the measured turn-ON and turn-OFF trajectories of the GaN power module for load currents ranging from 150 to 600 A. Besides, under the conditions of load currents $I_d = 600$ A and junction temperature $T_j = 25\,^{\circ}$C, Fig. 24(c) presents the experimental switching trajectories for various dc-link voltages ranging from 200 to 400 V. It can be observed that the GaN module exhibits extremely fast switching speed, with current rise/fall times within 15 ns. Additionally, the switching time increases with the increasing load current and dc-link voltage.

Furthermore, the switching waveforms of the GaN module at various junction temperatures T_j from 25 to 125 °C, while maintaining the dc-link voltage $V_{\mathrm{dc}} = 400$ V and load current $I_d = 600$ A, are shown in Fig. 24(d). The test results show that as the junction temperature T_j rises, the turn-ON speed slightly decreases, whereas the turn-OFF remains virtually unaffected. Therefore, switching losses are also influenced by the junction temperature.

The measurement results of the switching loss varying with junction temperature under different load currents are shown in Fig. 25(a) and (b). The turn-ON loss increases with the rise of junction temperature, while the turn-OFF loss changes slightly. The turn-ON loss exhibits a significant increase as

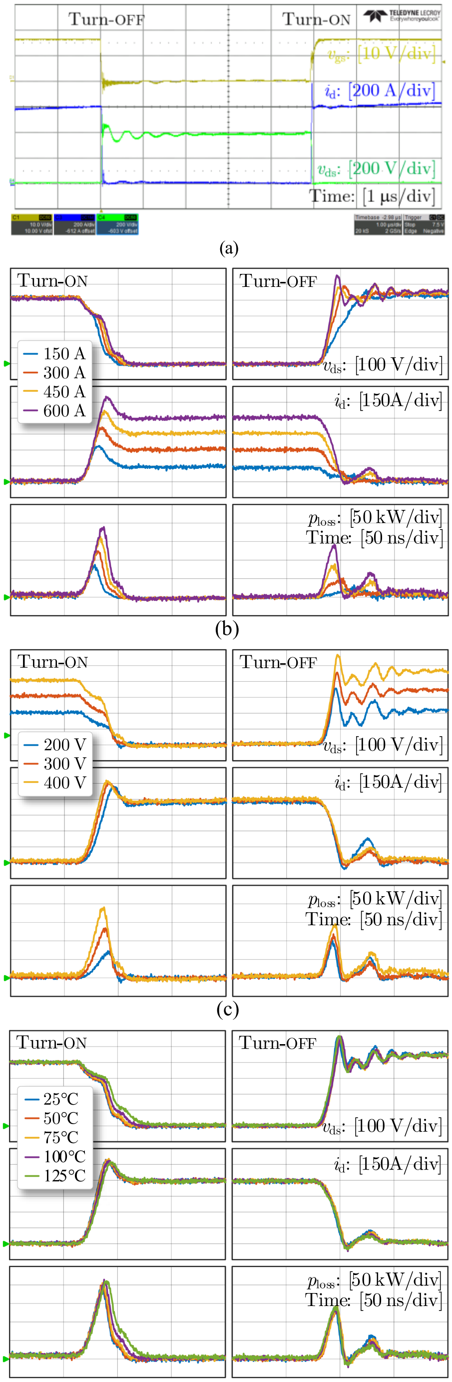


Fig. 24. (a) Representative switching waveforms of the fabricated GaN power module at 400 V/600 A, and measured switching behaviors under different. (b) Load currents. (c) DC-link voltages. (d) Junction temperatures.

the junction temperature rises, whereas the turn-OFF loss remains relatively unchanged. Furthermore, as the load current increases, the dependence of the loss on the junction temperature becomes increasingly significant. Therefore, optimal heat dissipation and a low operation junction temperature are beneficial for enhancing the efficiency of the GaN inverter.

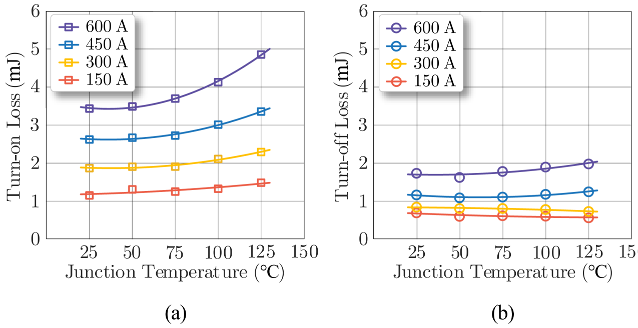


Fig. 25. Measured (a) turn-ON and (b) turn-OFF losses of GaN power module under different load currents and junction temperatures.

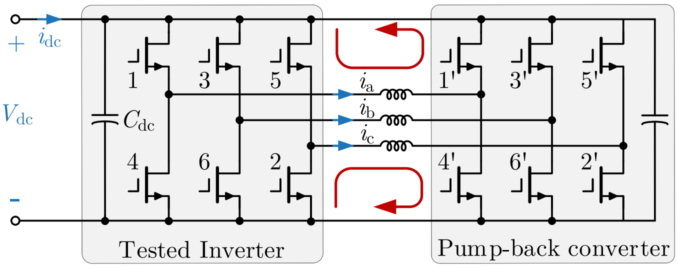


Fig. 26. Topology of power test circuit.

TABLE VI
PARAMETER SETUP OF TEST RIG

Devices	Specifications
Inverter	Rating 600 A / 400 V, switching frequency 16 kHz
Controller	TI TMS320F28335, modulation frequency 50 - 600 Hz
Heating Circulator	Water temperature 65°C, fluid flux 10 L/min
Load Inductor	0.5 mH, 300 A

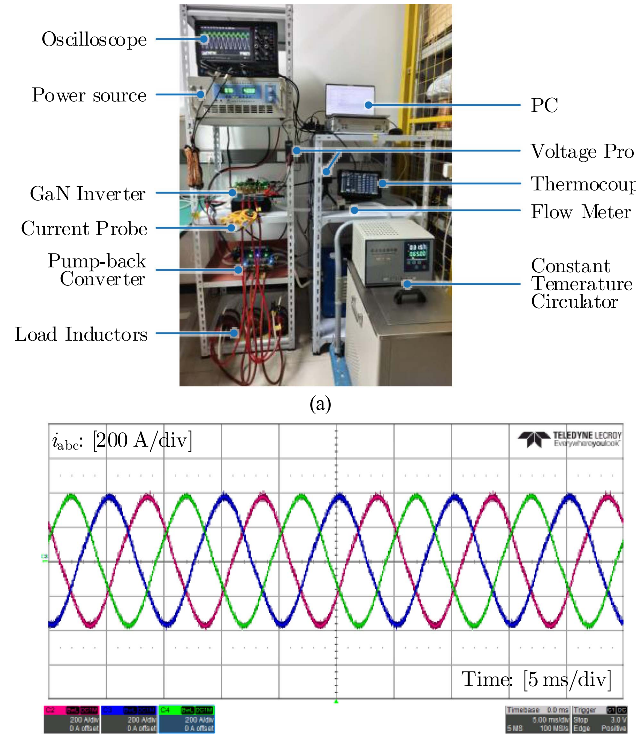
B. Performance Evaluation of the Designed GaN Inverter Under Operational Conditions

To assess the load-carrying performance of the designed GaN inverter prototype, a power pump-back circuit based on the front-to-front topology is utilized for power testing, as shown in Fig. 26. Meanwhile, the test bench has been set up, as shown in Fig. 27, and its parameter configuration is given in Table VI.

Startup and Shutdown Waveforms: Under the dc-link voltage of $V_{\text{dc}} = 400$ V and half-load current of $I_d = 130$ Arms, the overall waveforms of the line voltage v_{ab} and phase current i_a during the startup and shutdown of the GaN inverter are shown in Fig. 28(a). The detailed zoomed-in waveforms are shown in Fig. 28(b).

Additionally, the startup waveforms under full-load current of $I_d = 260$ Arms, along with the detailed views, are presented in Fig. 29(a) and (b), respectively.

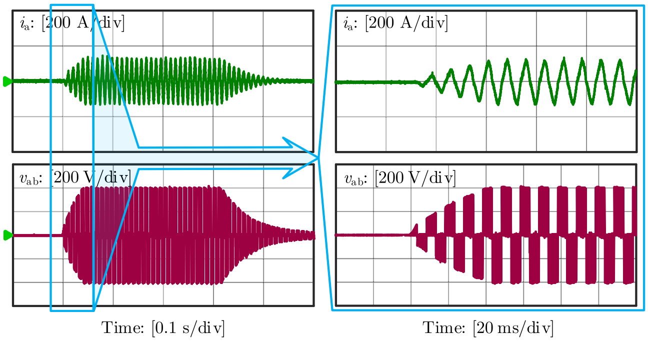
Full-Load Continuous Waveform: The designed GaN inverter achieves a full power output $P_o = 100$ kW, with the dc-link voltage of $V_{\text{dc}} = 400$ V and a phase current RMS reaching $I_d = 260$ A. The full-load continuous operation waveforms are illustrated in Fig. 30, providing detailed views of the line voltage and three-phase currents.



(a)

(b)

Fig. 27. Power test. (a) Configuration of test rig and (b) output current waveform.



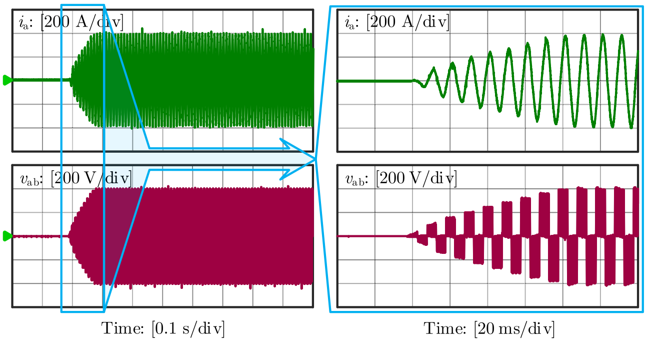
(a)

(b)

Fig. 28. Experimental results of proposed GaN inverter under half-load condition. (a) Startup and shutdown waveforms. (b) Zoomed-in startup waveforms.

C. *Efficiency Assessment of Designed GaN Inverter Under Various Operation Points*

Under the dc-link voltage of $V_{dc} = 400$ V, efficiency measurements are performed at various output power points across ac output frequencies ranging from 50 to 600 Hz. The resulting efficiency curves of the GaN traction inverter under different output frequencies and power levels are plotted in Fig. 31. Meanwhile, these efficiency curves can be transformed into an efficiency map in “ac frequency and output power” coordinate system, as illustrated in Fig. 32.



(a)

(b)

Fig. 29. Experimental results of proposed GaN inverter under full-load condition. (a) Overall startup waveforms. (b) Zoomed-in startup waveforms.

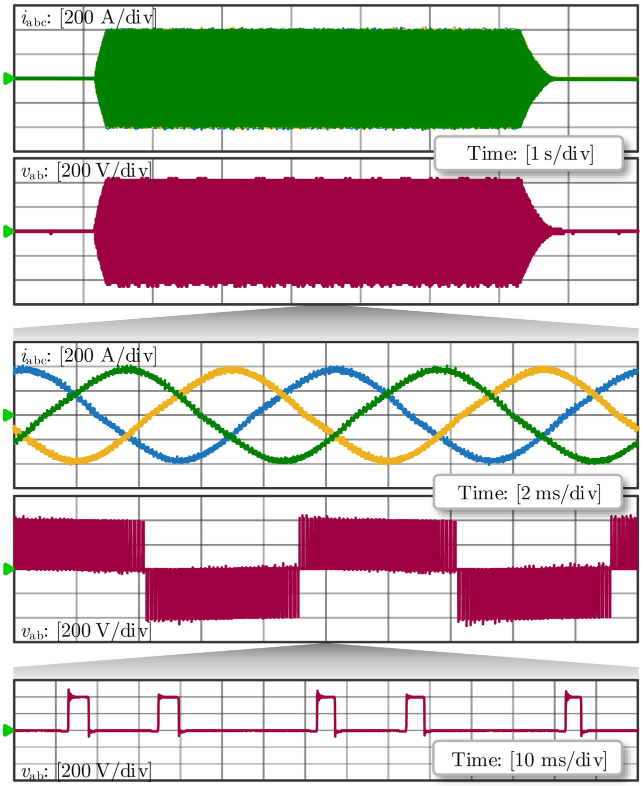


Fig. 30. Line voltage and phase current waveforms and details under full-load steady-state operation.

Based on the efficiency test results, the GaN inverter demonstrates a high-efficiency operating state even under light load conditions. As the output ac frequency increases, the efficiency improves and reaches the peak at 500 Hz, after which it begins to decline slightly. At the ac output frequency of 500 Hz and under a light load condition, efficiency reaches the peak $\eta_{\max} = 99.3\%$. Within the measured range of the experiment, the efficiency exceeds 98% across 79.3% of the efficiency MAP area. The GaN inverter showcases remarkable peak efficiency and consistently high performance across the entire mission profiles.

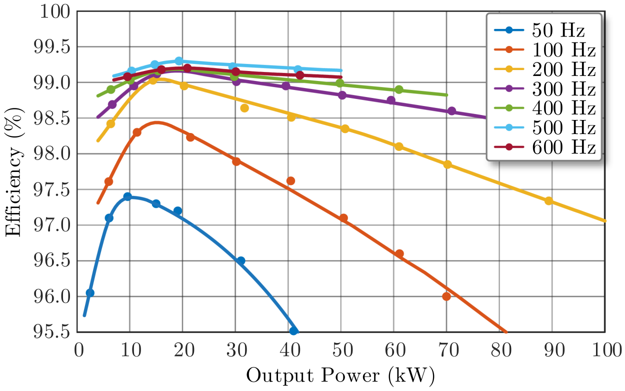


Fig. 31. Measured efficiency results of designed GaN traction inverter.

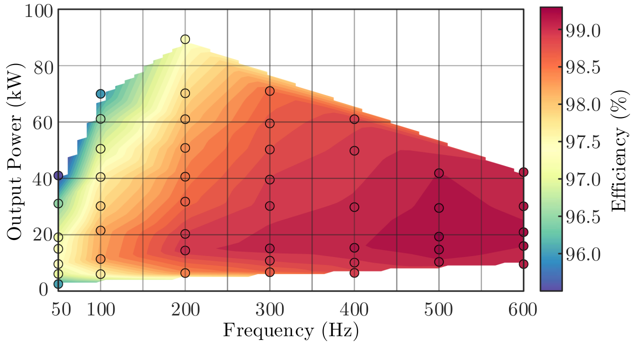


Fig. 32. Experimental efficiency map of designed GaN traction inverter.

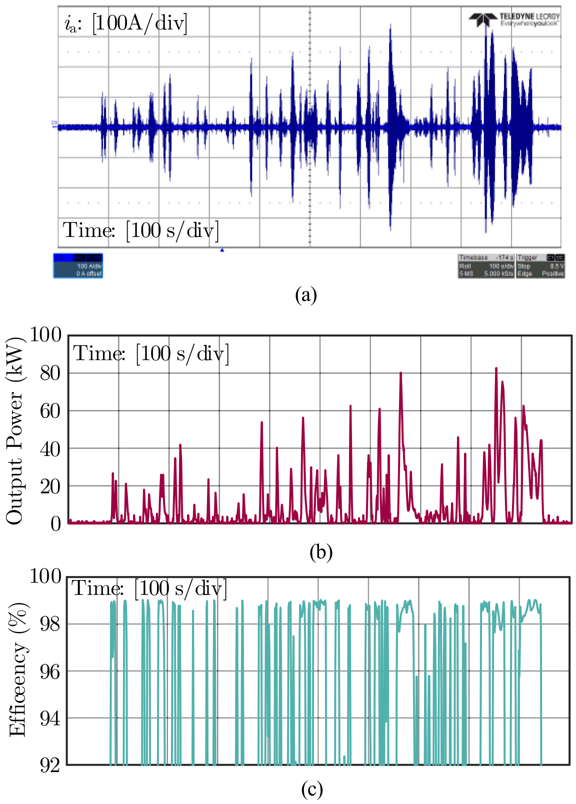


Fig. 33. WLTP driving cycle test results of the GaN inverter. (a) Output current waveform. (b) Output power curve. (c) Efficiency curve.

D. WLTP Standard Drive Cycle Testing of the GaN Traction Inverter

The Worldwide harmonized Light vehicles Test Procedure (WLTP) is a globally adopted automotive testing standard. By conducting WLTP drive cycle tests, the actual operating performance of the designed GaN inverter prototype can be effectively evaluated. Based on the rated power of prototype, the equivalent WLTP operating control for the inverter is derived and configured using vehicle dynamics model. Under the WLTP drive cycle, the output current waveform of the designed GaN inverter is shown in Fig. 33(a). The corresponding output power and efficiency curves are recorded and presented in Fig. 33(b) and (c), respectively.

The test results validate the feasibility of the designed prototype under cyclic driving conditions. Moreover, the efficiency curve demonstrates the of GaN traction inverter rapid responsiveness in reaching the high-efficiency region across a wide range of conditions.

E. Comparisons and Discussions

To ensure the effectiveness of the proposed co-design method and demonstrate the advancements of the designed GaN prototype, key parameters from several commercial and prototype-level traction inverters are compared in Table VII, revealing notable contrasts.

Regarding power density, current SiC experimental prototypes demonstrate a clear advantage—for example, the MARC·100 (70 kW/L) [55] and the UArk Prototype (86 kVA/L) [58]. This may be attributed to the high-voltage and high-temperature capabilities of SiC devices, as well as their more mature technological development compared to GaN devices. The proposed GaN prototype achieves a power density of 62.1 kW/L, closely approaching the first-tier SiC designs and comparable to the commercial benchmark Porsche Taycan inverter (62.3kW/L). Moreover, it significantly outperforms most commercial SiC inverters, indicating that GaN traction inverters have strong potential to compete with SiC in high-density integration. ***Regarding efficiency***, the proposed GaN inverter achieves a significant breakthrough enabled by the high-speed and low-loss characteristics of GaN devices. The prototype reaches a peak efficiency of 99.3%, surpassing the other compared automotive traction inverters. Moreover, among all full-power device types listed in the table, GaN is the only one to exceed the 99% efficiency boundary for traction inverters. ***Regarding simultaneous improvements in efficiency and power density***, the proposed GaN traction inverter in this article represents a core advancement. Traditionally, a tradeoff is often required between high power density and high efficiency. However, this article introduces a system-level "efficiency-density" co-optimization methodology. The optimization and integrated design enable the GaN traction inverter to maintain a high power density of 62.1 kW/L while achieving a peak efficiency of 99.3%. These results

TABLE VII
COMPARISONS OF COMMERCIAL AND PROTOTYPE-LEVEL TRACTION INVERTER AND PROPOSED GAN INVERTER PROTOTYPE

Inverter	Audi eTron 	Porsche Taycan 	Tesla M3 	Wolfspeed Prototype [11] 	MARC 100 [55] 	UArk Prototype [58] 	UTA Prototype [59] 	**This article** 
Power Device	Si	Si	SiC	SiC	SiC	SiC	GaN	GaN
DC-Link Voltage	150-460 V	450-800 V	345 V	650 V	800 V	800 V	800 V	400 V
Rated Power	165 kW	175 kW	220 kW	110 kW	100 kW	150 kW	10 kW	100 kW
Power Density	30 kW/L	62.3 kW/L	27.4 kW/L	17 kW/L	70 kW/L	86 kVA/L	16.5 kW/L	**62.1 kW/L**
Peak Efficiency	97%	98%	98%	97.4%	—†	—†	98.9%	**99.3%**

† *Data not publicly available.*

demonstrate the technical feasibility of GaN power devices in high-efficiency, high-density EV applications, offering a new paradigm for next-generation advanced inverters.

VI. CONCLUSION

This article introduces a co-design methodology of efficiency and power density for the GaN traction inverter in EV applications, considering the design and integration of the key component. GaN are a potential solution to break through the efficiency and power density boundaries of SiC, whereas the utilization of GaN devices in traction inverters remains underdeveloped in terms of systematic design and integration. To overcome these challenges, an "efficiency-density" co-design methodology for GaN traction inverter is proposed, incorporating a comprehensive analysis of key components. The "η–ρ–$f_{\rm sw}$" design space of the GaN inverter is systematically constructed, based on the derived the "$f_{\rm sw}$–$P_{\rm loss}$" model of the inverter, the "$f_{\rm sw}$–$C_{\rm dc}$–v_c" relationship of the dc-link capacitor, and the "$f_{\rm sw}$–$R_{\rm thhs}$–$v_{\rm hs}$" constraint of the heat sink. Through pareto frontier analysis, the co-optimization design point of efficiency and power density is determined. Based on the co-design results, key components are developed and integrated, including the high-power GaN module with integrated gate driver, a dc-link capacitor with high volume density, and a pin-fin liquid cooling heat sink. Ultimately, a 400 V / 100 kW GaN traction inverter prototype is high-density integrated, utilizing a vertical stack structure of "power module-heat sink-capacitor". Experimental validation confirmed the superior performance of the designed prototype, achieving a full-load power density of 62.1 kW/L and a peak efficiency of 99.3%, thereby surpassing the existing "efficiency-density" boundary of EV traction inverters (see Fig. 3). This research serves as a valuable reference for the application of GaN devices in EV. It offers significant insights and practical value for advancing the next generation of EV traction inverter technology.

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