Phase-Shift Controlled Push-Pull Class-E Inverter With Diode Balance for Load Impedance Variations

Yutaro Komiyama, *Graduate Student Member, IEEE*, Wenqi Zhu, *Member, IEEE*, Akihiro Konishi, *Member, IEEE*, Ayano Komanaka, *Graduate Student Member, IEEE*, Yinchen Xie, *Graduate Student Member, IEEE*, Kien Nguyen, *Senior Member, IEEE*, Hiroo Sekiya, *Senior Member, IEEE*, and Tatsuya Ikenari

***Abstract*—This article proposes a phase-shift controlled push-pull class-E inverter with diode balance for load impedance variations, along with its design method. The diode clamp absorbs the asymmetric inductive and capacitive impedance changes that occur as a side effect of the phase-shift control. As a result, the proposed inverter maintains the symmetrical waveforms between the single-ended inverters, achieving Zero-Voltage Switching under the phase-shift control. A general design framework for the phase-shift controlled push-pull class-E inverter is established with a circuit equation solver and a heuristic optimization algorithm. The design method eliminates the complex analysis for the asymmetric operation of the push-pull class-E inverter because the optimal circuit parameters are automatically explored by maximizing an objective function. This article gives the design example and performs an experiment with a prototype inverter operating at 13.56 MHz and 500 W output power. The prototype inverter achieved 87.8 % –89.0 % efficiency against resistive, inductive, and capacitive load impedance variations on the Voltage Standing Wave Ratio 2:1. The experimental results demonstrate the validity and effectiveness of the proposed inverter.**

***Index Terms*—Class-E inverter, load variations, particle swarm optimization, phase-shift control, zero-voltage switching (ZVS).**

I. Introduction

HIGH-FREQUENCY circuit operation beyond tens of MHz has become practical owing to the wide-bandgap power semiconductor devices [1]. Mainly, research on high-frequency inverters at Industrial, Scientific, and Medical (ISM) band frequencies, such as 13.56 MHz and 27.12 MHz, has been focused on potential applications in plasma generation [2], [3], [4] and wireless power transfer systems [5], [6], [7]. In such high-frequency applications, achieving Zero-Voltage Switching (ZVS) becomes an essential design objective to reduce the switching losses. Within this context, the class-E ZVS inverter [1], [3], [4], [5], [6], [7], [8] is widely adopted in high-frequency applications. One major issue in the class-E inverter is its high sensitivity against load impedance variations [9], [10]. When the load impedance changes resistively, inductively, or capacitively, the output power varies, and also ZVS cannot be ensured.

Phase-shift control [11], [12], [13], [14], [15], [16] is a typical control method in the class-E inverter to achieve output power regulation against load impedance variations. In the phase-shift control, two class-E inverters are connected in series or parallel to the load, and the output power is controlled by changing the phase shift between the single-ended inverters. Since there is only a single control parameter in the phase-shift control, it is hard to achieve the output power control and ZVS simultaneously. In addition, the phase shift makes one of the single-ended inverters change inductively while the other changes capacitively. This operation poses a challenge to achieving ZVS in both two single-ended inverters. Hence, the phase-shift controlled class-E inverter cannot apply for wide load impedance variations that require large phase shifts. In order to expand the load variation range, various efforts have been made, including passive combiners that mitigate load variations [11], [12], asymmetric circuit configuration [13], and modular ON/OFF control with phase-shift control [14], [15], [16]. Although these methods expand the resistive or inductive load variation range, no research has been reported that addresses all resistive, inductive, and capacitive load impedance variations. With the growing applications of high-frequency inverters, it is crucial to consider various types of load variations. This serves as the motivation for developing the phase-shift controlled class-E inverter that ensures ZVS across resistive, inductive, and capacitive load variations.

This article proposes a phase-shift controlled push-pull class-E inverter with diode balance, along with its design method. The proposed inverter maintains symmetrical waveforms between the single-ended inverters owing to the diode clamps. Namely, the asymmetric inductive and capacitive impedance changes due to the phase-shift control, as well as the load impedance

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Yutaro Komiyama, Ayano Komanaka, and Yinchen Xie are with the Department of Applied and Cognitive Informatics, Chiba University, Chiba 263-8522, Japan (e-mail: y.komiyama@chiba-u.jp).

Wenqi Zhu is with the Department of Electrical Engineering, Tokyo University of Science, Tokyo 162-8601, Japan.

Akihiro Konishi, Kien Nguyen, and Hiroo Sekiya are with the Department of Informatics, Chiba University, Chiba 263-8522, Japan (e-mail: sekiya@faculty.chiba-u.jp).

Tatsuya Ikenari is with Plasma System Division DAIHEN Corporation, Osaka 532-8512, Japan.

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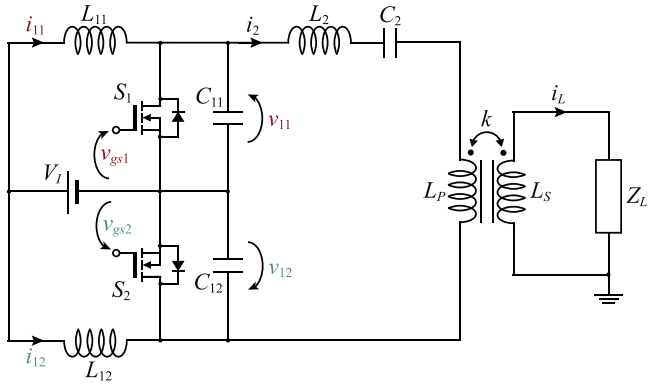

Fig. 1. Circuit topology of the conventional inverter.

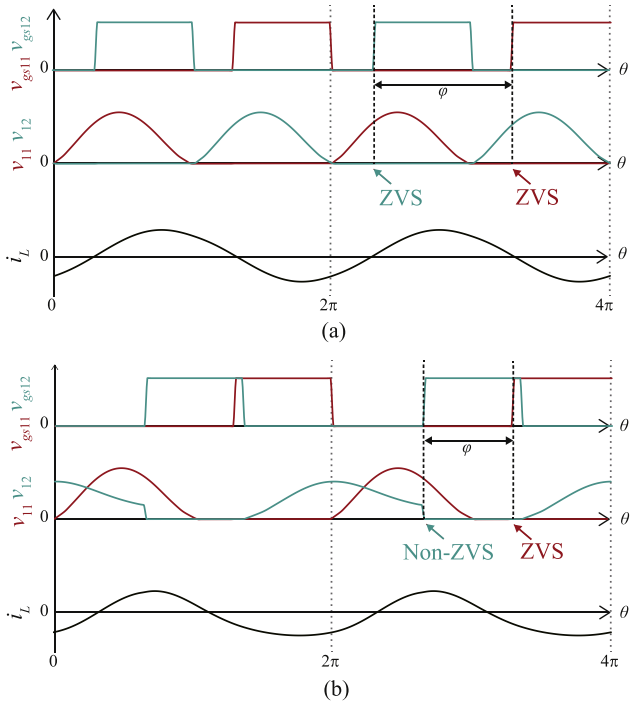

Fig. 2. Example waveforms of the conventional inverter. (a) For $\varphi = \pi$. (b) For load impedance variations.

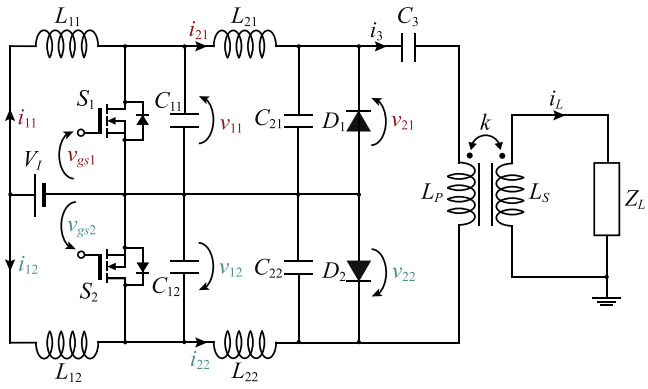

Fig. 3. Circuit topology of the proposed inverter.

variations, can be alleviated. Consequently, the proposed inverter simultaneously achieves the output power regulation and ZVS against resistive, inductive, and capacitive load impedance variations. A circuit equation solver and a heuristic optimization algorithm are combined to design the inverter. The circuit equation solver derives the steady-state waveforms under the phase-shift control. Also, the heuristic optimization automatically explores the circuit parameters that maximize an objective function. This article provides experimental verifications with the optimized proposed inverter under a 13.56 MHz operating frequency and a 500 W output power. The validity of the experimental results was confirmed by the quantitative agreement between the waveforms obtained from the circuit equation solver and the experiment.

II. Phase-Shift Controlled Push-Pull Class-E Inverter

A. Conventional Circuit

Fig. 1 shows the circuit topology of the typical push-pull class-E inverter [8], which is consisted of the input voltage source V_I, input inductors L_{11} and L_{12}, shunt capacitors C_{11} and C_{12}, and series resonant filter L_2-C_2. The transformer L_P-L_S, with a sufficiently high coupling coefficient k, isolates the inverter from the load Z_L.

Since the output power of the push-pull class-E inverter is highly sensitive against load impedance variations, the phase-shift control is commonly applied to maintain the desired output power. The phase-shift control changes the phase shift between the switches S_1 and S_2 depending on the load impedance. Fig. 2 shows the example waveforms of the phase-shift controlled push-pull class-E inverter, where $\theta = \omega t = 2\pi f t$ represents angular time, ω is angular operating frequency, and f denotes the operating frequency. For $\varphi = \pi$, the inverter works symmetrically, as shown in Fig. 2(a). Therefore, both switch voltages v_{11} and v_{12} achieve ZVS. When the load impedance varies, the output power regulation is performed by changing the phase shift φ. However, it is challenging to achieve ZVS under the phase-shift control. This is because the phase-shift control utilizes only a single adjustable variable φ for output power regulation, and the inherent ZVS region is limited in the class-E inverter. Furthermore, the impedances seen from two single-ended inverters change differently in inductive and capacitive due to the phase shift. Even if one of the switches achieves ZVS, the other side cannot achieve ZVS, as shown in Fig. 2(b). Non-ZVS waveform seriously deteriorates the power-conversion efficiency in high-frequency operation. Therefore, this article aims to develop the phase-shift controlled class-E inverter that achieves ZVS for both switches with the output power regulation.

B. Proposed Circuit

Fig. 3 shows the circuit topology of the proposed phase-shift controlled push-pull class-E inverter. Compared with the conventional circuit topology, the proposed inverter adds inductors L_{21} and L_{22}, capacitors C_{21} and C_{22}, and diodes D_1 and D_2. The

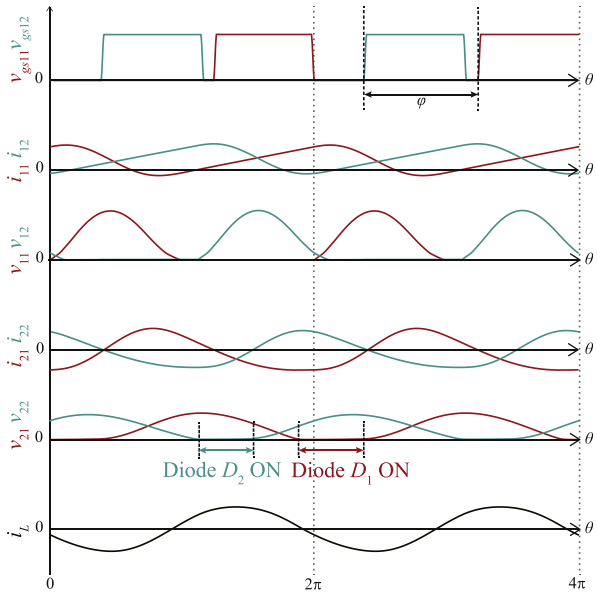

Fig. 4. Example waveforms of the proposed inverter.

diodes D_1 and D_2 are used to keep the symmetric waveforms between the single-ended inverters.

The capacitors C_{21} and C_{22} are employed to absorb the nonlinear parasitic capacitance of the diodes. Without the capacitors C_{21} and C_{22}, the circuit operation becomes highly dependent on the nonlinear characteristics, affecting ZVS, output voltage stability, and overall efficiency.

Fig. 4 shows the example waveforms of the proposed inverter. The proposed inverter regulates the output power using the phase-shift control. The proposed inverter can maintain the symmetric operating waveforms between the single-ended inverters even when the load impedance variations and phase shifts occur. As the diodes inherently clamp the negative voltage, as shown in Fig. 4, it prevents the excessive voltage from applying on only one side of the single-ended inverters. Consequently, the voltage and current are balanced in the push-pull configuration during the phase-shift control.

Fig. 5 shows the proposed inverter during diode turn-ON and OFF states. When the diode turns OFF, the current flows through the capacitor C_{21}. Namely, the circuit topology becomes the class-E inverter with LCCL filter, as shown in Fig. 5(a). With a specific set of circuit parameters, the class-E inverter with LCCL filter achieves ZVS across a wide range of resistive load variations [6]. On the other hand, when the diode turns ON, the inductor L_{21} is shorted out, as shown in Fig. 5(b). Namely, the equivalent impedance seen from the switch S_1 becomes inductive. Consequently, the diode-clamp operation increases the inductive impedance as seen from the switch, promoting the discharge of the capacitor C_{11}. For this reason, the proposed topology is capable of maintaining ZVS across a wide range of load impedance variations. Indeed, the analysis of the single-ended diode-clamp inverter has been presented in [17], where it is shown that the diode-clamp operation increases the imaginary part of the equivalent impedance as seen from the switch.

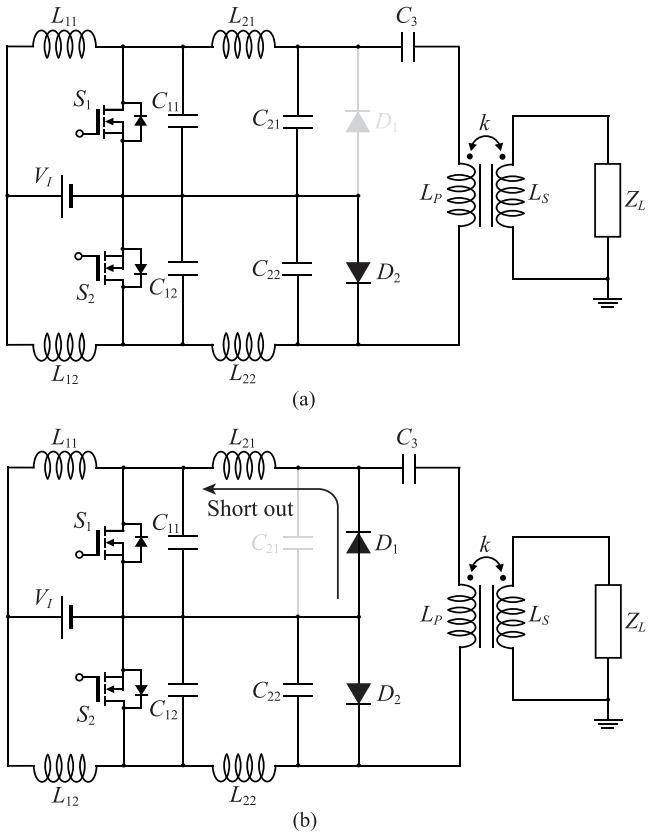

Fig. 5. Proposed inverter. (a) Diode turn-OFF state. (b) Diode turn-ON state.

III. General Design Framework

For designing the class-E inverters, analytical approaches are generally employed [5], [18]. However, phase-shift controlled push-pull class-E inverters involve asymmetric operation, which inevitably complicates the analytical expressions. Therefore, this article adopts a numerical approach for designing the phase-shift controlled class-E inverters. Fig. 6 shows the overview of the general design framework for the phase-shift controlled push-pull class-E inverter. The design framework comprises a heuristic optimization algorithm in the outer loop of the circuit equation solver. The circuit equation solver derives the steady-state waveforms. The circuit-design parameters are optimized using the heuristic optimization algorithm by evaluating the steady-state waveforms.

A. Optimization Algorithm

In this article, Particle Swarm Optimization (PSO) [19] is applied to optimize the component values and circuit parameters. The PSO is based on multipoint search, where candidate solutions, represented as particles, explore the parameter space to find the optimal solution. The optimization is performed by sharing the information about the best solution among the particles. According to the position of the best solution in the parameter space, the particles converge toward the optimal solution.

In the PSO algorithm, I particles are initially prepared with a position vector $\boldsymbol{x}_i^{(0)}$ and a velocity vector $\boldsymbol{v}_i^{(0)}$, which are given

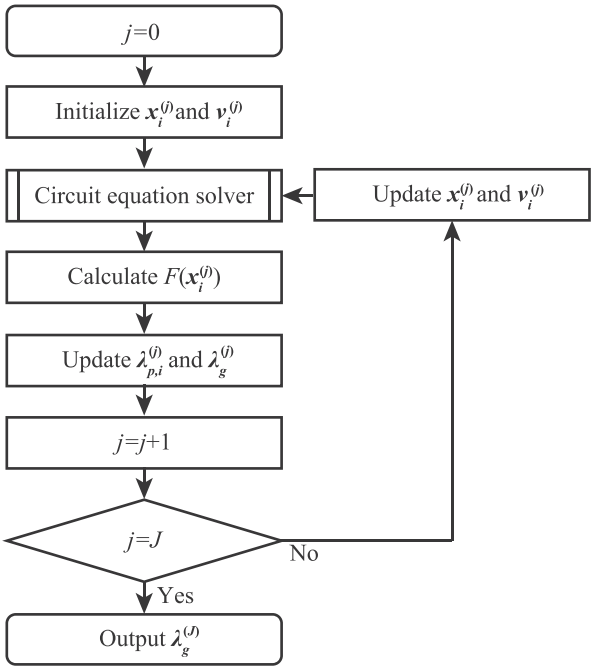

Fig. 6. Overall flowchart of the general design framework for the phase-shift controlled push-pull class-E inverter.

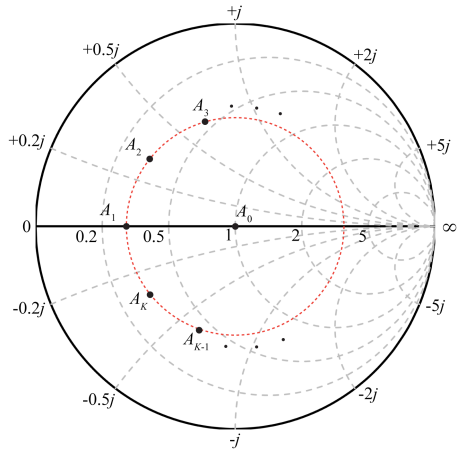

Fig. 7. Optimization points on the Smith chart.

randomly. Here, $i \in [1, I]$ represents the index number of the particle. Within J iterations, the position and velocity vectors of each particle are updated according to the best solution. Every single particle keeps the local best solution, which is the best solution found in the search on each particle. Additionally, all particles share the information about the global best solution, which is the best solution in the local best solutions. The position and velocity vectors are updated based on local and global best solutions.

As shown in Fig. 6, the objective function $F(\boldsymbol{x}_i^{(j)})$ is calculated in the j-th iteration. Subsequently, the local best solution $\boldsymbol{\lambda}_{p,i}^{(j)}$ and global best solution $\boldsymbol{\lambda}_{g,i}^{(j)}$ are updated. The position vector of ith particle is updated as

$$\boldsymbol{x}_i^{(j+1)} = \boldsymbol{x}_i^{(j)} + \boldsymbol{v}_i^{(j+1)}. \tag{1}$$

Also, the velocity vector is updated as

$$\boldsymbol{v}_i^{(j+1)} = a_1 \boldsymbol{v}_i^{(j)} + a_2 u_2 \left(\boldsymbol{\lambda}_{p,i}^{(j)} - \boldsymbol{x}_i^{(j)}\right) + a_3 u_3 \left(\boldsymbol{\lambda}_g^{(j)} - \boldsymbol{x}_i^{(j)}\right) \tag{2}$$

where u_2 and u_3 are random values between 0 to 1. The weight parameters $a_1 = 0.729$ and $a_2 = a_3 = 1.50$ are typically used in the PSO alghorithm [20]. After J iterations, the global best position vector is output as the optimal solution.

B. Objective Function

This research aims to design the phase-shift controlled push-pull class-E inverter, which achieves high power-conversion efficiency and constant output power against load impedance variations. Therefore, it is necessary to evaluate circuit operation under load variations as well as the rated load condition.

Fig. 7 shows the evaluation points of the circuit operation on the Smith chart. The rated load condition A_0 and the boundary of the given load variation range A_1-A_K are specified as the evaluation points. The design points can be flexibly changed depending on the design specifications and applications. The objective function is given as

$$F = w_\eta \sum_{k=0}^{K} \eta_k + w_{P_O} \sum_{k=0}^{K} \exp\left(-\left|1 - \frac{P_{Ok}}{P_{Or}}\right|\right) \tag{3}$$

where P_{Or} is the desired output power, and η_k and P_{Ok} are the power-conversion efficiency and output power at the evaluation point A_k, respectively. Besides, w_η and w_{P_O} are the weight parameters. We can see from (3) that the first term increases as the power-conversion efficiencies increase. Also, the second term increases as the output power P_{Ok} is closer to the desired output power P_{Or}. Hence, the circuit optimization can be performed by maximizing the objective function.

C. Circuit Equation Solver

In order to calculate the objective function given in (3), operating waveforms of the phase-shift controlled push-pull class-E inverter need to be derived. This article adopts a transient analysis to obtain the steady-state waveforms. By solving the circuit equations with a numerical integration for a sufficiently long period, steady-state waveforms can be obtained [21]. This section specifically describes how to derive the waveforms under the phase-shift control.

Fig. 8 shows the flowchart for obtaining the steady-state waveform of the phase-shift controlled push-pull inverter. We assume that the phase-shift controlled push-pull inverter exhibits a monotonic increase in output power against the phase shift, with minimum power at $\varphi = 0$ and maximum power at $\varphi = \pi$. By utilizing the monotonic increasing nature, the phase shift that achieves the desired output power can be obtained by the bisection method. In the bisection method, the boundary phase shifts $\varphi_l^{(0)} = 0$ and $\varphi_h^{(0)} = \pi$ are firstly given. In each iteration,

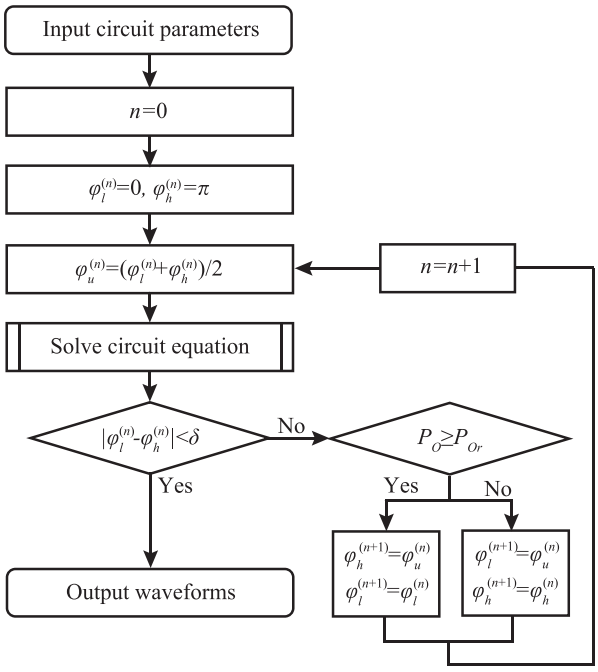

Fig. 8. Flowchart of the waveform derivation algorithm.

the intermediate point between $\varphi_l^{(n)}$ and $\varphi_h^{(n)}$, namely

$$\varphi_u^{(n)} = \frac{\varphi_l^{(n)} + \varphi_h^{(n)}}{2} \tag{4}$$

becomes a candidate for the optimal phase shift to achieve the desired output power. By numerically solving the circuit equation with the phase shift $\varphi_u^{(n)}$, the circuit waveforms and their output power P_O can be obtained. The boundary phase shifts are updated as

$$\begin{cases} \varphi_h^{(n+1)} = \varphi_u^{(n)} & \text{and} \quad \varphi_l^{(n+1)} = \varphi_l^{(n)} \quad \text{if } P_O \geq P_{Or}, \\ \varphi_h^{(n+1)} = \varphi_h^{(n)} & \text{and} \quad \varphi_h^{(n+1)} = \varphi_u^{(n)} \quad \text{if } P_O < P_{Or}. \end{cases} \tag{5}$$

By iterating this operation, the calculated output power P_O gradually approaches the desired output power P_{Or}. When the boundary phases satisfy

$$|\varphi_l^{(n)} - \varphi_h^{(n)}| < \delta \tag{6}$$

for a sufficiently small δ, the steady-state waveforms with the desired output power can be obtained for given circuit parameters. Note that when the desired output power P_{Or} cannot be achieved for any phase shift φ under the given circuit parameters, the maximum available output power with $\varphi = \pi$ is obtained in this algorithm.

D. Modeling of Circuit

In order to formulate the circuit equations, we provide a circuit model for the inverter. Each circuit component is modeled separately, and finally, the overall circuit model for the inverter is derived.

1) Switching Device: Fig. 9(a) shows the circuit model of the switching device. The switching device is modeled

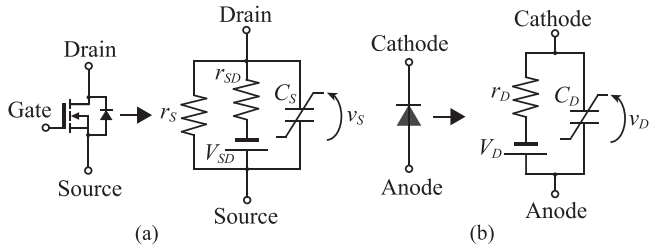

Fig. 9. Model of the devices. (a) Switching device. (b) Diode.

with resistances r_S and r_{SD}, output parasitic capacitance C_S, and reverse voltage drop V_{SD}. The resistance r_S expresses the turn-ON and OFF operations by changing the resistance value as

$$r_S = \begin{cases} \infty & \text{for } 0 \leq \theta < 2\pi D_S \\ r_{Son} & \text{for } 2\pi D_S \leq \theta < 2\pi \end{cases} \tag{7}$$

where r_{Son} is ON-resistance and D_S is the OFF-duty ratio. Besides, the resistance r_{SD} expresses the reverse conduction as

$$r_{SD} = \begin{cases} r_{SDon} & \text{for } 0 \leq \theta < 2\pi D_S \cap v_S \leq -V_{SD} \\ \infty & \text{otherwise.} \end{cases} \tag{8}$$

The switching devices have an output capacitance with voltage-dependent characteristics, which can be included in the calculation by expressing the capacitance as a function of the switch voltage.

2) Diode: Fig. 9(b) shows the circuit model of the diode. The diode is modeled as a resistance r_D, forward voltage V_F, and output parasitic capacitance C_D. The resistance r_D expresses the operation of the diode as

$$r_D = \begin{cases} r_{Don} & (v_D \leq -V_F) \\ \infty & (v_D > -V_F) \end{cases} \tag{9}$$

where r_{Don} is ON-resistance of the diode. The output capacitance of the diode can also be given as a function of the voltage across the diode v_D.

3) Inductor: The inductors are modeled as a series connection of the self-inductance and the Equivalent Series Resistance (ESR). These values can be obtained from measurements. Meanwhile, it is more beneficial to derive the self-inductance and the ESR from the geometric parameters of the inductor. This is because we intend to optimize the geometric parameters of the inductors. This article provides the model of an air-core solenoid inductor.

Fig. 10 shows the diagram of the air-core inductor, where d is the diameter of the coil, l is the length of the coil, w is bare wire diameter, p is wire-winding distance, and N is turn number. The self-inductance of the finite solenoid coil can be obtained from

$$L = K_L \frac{\mu_0 \pi d^2 N^2}{4l} \tag{10}$$

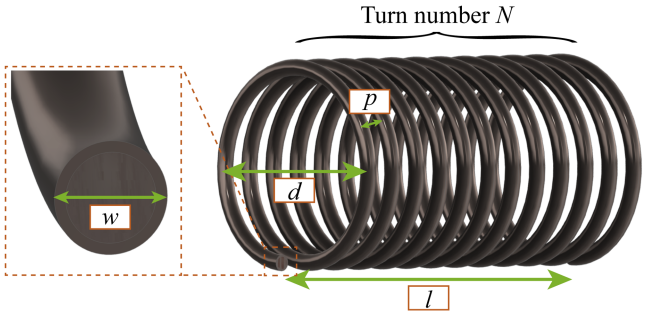

Fig. 10. Diagram of the air-core solenoid coil.

where K_L is Nagaoka's coefficient [22] and μ_0 is vacuume permeability. The Nagaoka's coefficient is derived from

$$K_L = \frac{4}{3\pi\sqrt{1-z^2}}\left[\frac{1-z^2}{z^2}K(z) - \frac{1-2z^2}{z^2}E(z) - z\right] \quad (11)$$

where z is defined as

$$z = \frac{d}{\sqrt{d^2+l^2}}. \quad (12)$$

Besides

$$K(z) = \int_0^{\frac{\pi}{2}} \frac{1}{\sqrt{1-z^2\sin^2\theta'}} d\theta' \quad (13)$$

and

$$E(z) = \int_0^{\frac{\pi}{2}} \sqrt{1-z^2\sin^2\theta'}\, d\theta' \quad (14)$$

are complete elliptic integrals of the first and second kinds.

The ESR of the inductor can be obtained from Dowell's equation [23] as

$$r = \frac{4\rho d N X}{w^2}\frac{\sinh(2X)+\sin(2X)}{\cosh(2X)-\cos(2X)} \quad (15)$$

where X is derived from

$$X = \left(\frac{\pi}{4}\right)^{\frac{3}{4}} \frac{w}{\sqrt{\frac{\rho}{\pi\mu_0 f}}}\sqrt{\frac{w}{p}} \quad (16)$$

and $\rho = 1.724\ \mu\Omega\cdot$m is the copper resistivity. We can see from (10)–(14) and (15)–(16) that the self-inductance and the ESR can be determined by giving the geometric parameters denoted in Fig. 10.

4) Capacitor: In this article, the capacitors are modeled as a capacitance with no ESR. This is because the ESR of the capacitors is small enough compared with the inductors and can be ignored.

IV. Design Example

A. Circuit Equation

Fig. 11 shows the overall circuit model of the proposed inverter, which is obtained using the component models described in Section III-D. The inductors L_{11}, L_{12}, L_{21}, L_{22}, and L_3 are implemented as the air-core solenoid coil, which can be modeled using the inductor model given in Section III-D3. The transformer L_P-L_S is modeled with self-inductances L_P and L_S, ESRs r_{L_P} and r_{L_S}, and coupling coefficient k, where the measured values are used in this article. The load impedance Z_L is modeled with a series connection of inductance L_L, capacitance C_L, and resistance R_L to express resistive, inductive, and capacitive load impedance variations.

From Fig. 11, the circuit equation can be formulated as shown in (17) shown at the bottom of the next page, where $L_M = k\sqrt{L_P L_S}$ is a mutual inductance of the transformer.

TABLE I
Specifications of the Phase-Shift Controlled Push-Pull Class-E Inverter

Parameter		Specification
Input DC-voltage V_I		130 V
Switching frequency f		13.56 MHz
Rated output power P_{Or}		500 W
Rated load impedance Z_{Lr}		50 Ω
Load impedance range		VSWR 2:1
Diameter of air-core coils		10 mm
Transformer L_P-L_S	Core material	67 (Fair-rite)
	Winding wire	DFS017 (Junkosha)
	Self inductance L_P (measured)	2.02 μH
	Self inductance L_S (measured)	1.97 μH
	Coupling coefficient k (measured)	0.981
	ESR r_P (measured)	550 mΩ
	ESR r_S (measured)	363 mΩ

B. Design Specifications

The design specifications of the inverter are given in Table I. The transformer L_P-L_S is made prior to circuit optimization, details of which are also given in Table I. In addition, all the air-core inductors are wound evenly with intervals equal to the wire diameter.

Based on the design specifications, the GS66508 T 650 V Enhancement Mode GaN Transistor from Infineon is selected for the switches S_1 and S_2, whose output capacitance is expressed as [24]

$$C_S(v_S) = 80 + \frac{240}{1+\exp\left[0.15(v_S-68)\right]} + \frac{87.4}{1+\exp\left[0.03(v_S-180)\right]} - \frac{20.3\exp\left[0.77(-v_S+4.3)\right]}{\{1+\exp\left[0.15(-v_S+4.3)\right]\}^2} \ \text{pF} \quad (18)$$

which is plotted as shown in Fig. 12(a).

The C6D20065 G Silicon Carbide Schottky Diode from Wolfspeed is used for the diodes D_1 and D_2, whose junction capacitance is expressed as [25]

$$C_D(v_D) = \frac{850}{1+\left[\frac{\max(\min(v_D,450),0)}{0.950}\right]^{0.450}} \ \text{pF} \quad (19)$$

which is plotted as shown in Fig. 12(b).

The parameter set for the optimization is given as

$$\boldsymbol{x} = [C_1, C_2, C_3, N_1, N_2, N_3, w_1, w_2, w_3, D_S]^T \quad (20)$$

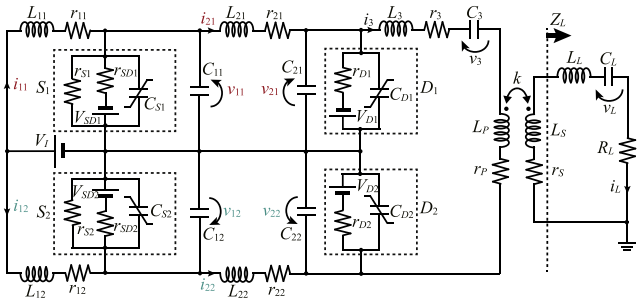

Fig. 11. Overall circuit model of the proposed inverter.

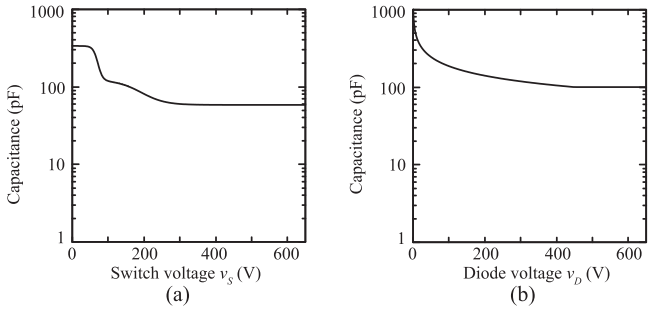

Fig. 12. Parasitic capacitance as a function of the voltage across the device. (a) Output capacitance of GS66508 T. (b) Junction capacitance of C6D20065 G.

TABLE II
DEFINITION OF THE OPTIMIZED PARAMETERS AND THEIR OPTIMIZED VALUES

Symbol	Definition	Optimized value
C_1	Capacitances of C_{11} and C_{12}	159 pF
C_2	Capacitances of C_{21} and C_{22}	542 pF
C_3	Capacitance of C_3	1878 pF
N_1	Turn numbers of L_{11} and L_{12}	15
N_2	Turn numbers of L_{21} and L_{22}	10
N_3	Turn number of L_3	3
w_1	Wire diameters of L_{11} and L_{12}	1.6 mm
w_2	Wire diameters of L_{21} and L_{22}	1.8 mm
w_3	Wire diameter of L_3	1.3 mm
D_S	OFF-duty ratios of S_1 and S_2	0.544

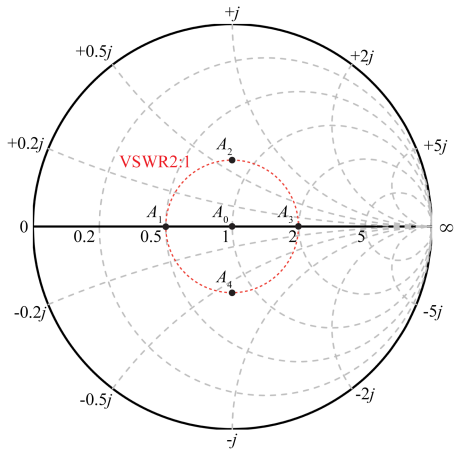

Fig. 13. Optimization points on the design example.

where the definition of each parameter is given in Table II. The circuit waveforms are determined uniquely when a specific $\boldsymbol{x}$ is given under the above design specifications.

C. Objective Function

Based on the design specifications for the load impedance given in Table I, the circuit waveforms at the rated 50 Ω load and four representative points on VSWR2:1, as shown in Fig. 13 are selected as the evaluation points. Accordingly, the objective function given in (3) is applied for these evaluation points, where $w_\eta = 0.3$ and $w_{P_O} = 0.7$ are used in this article.

The output power of the inverter is evaluated for the fundamental frequency component, which is calculated as

$$P_O = \frac{1}{2} R_L I_{Lfund}^2 \tag{21}$$

where I_{Lfund} is the amplitude of the output current in the fundamental frequency component. The I_{Lfund} can be obtained

$$\begin{cases}
\frac{di_{11}}{d\theta} = V_I - \frac{1}{\omega L_{11}}\left(r_{11} i_{11} + v_{11}\right) \\
\frac{dv_{11}}{d\theta} = \frac{1}{\omega C_{11}}\left[i_{11} - v_{11}\left(\frac{1}{r_{S1}} + \frac{1}{r_{SD1}}\right) - \frac{V_{SD1}}{r_{SD1}} - i_{21}\right] \\
\frac{di_{21}}{d\theta} = \frac{1}{\omega L_{21}}\left(v_{11} - r_{21} i_{21} - v_{21}\right) \\
\frac{dv_{21}}{d\theta} = \frac{1}{\omega C_{21}}\left(i_{21} - \frac{v_{21}+V_{D1}}{r_{D1}} - i_3\right) \\
\frac{di_{12}}{d\theta} = V_I - \frac{1}{\omega L_{12}}\left(r_{12} i_{12} + v_{12}\right) \\
\frac{dv_{12}}{d\theta} = \frac{1}{\omega C_{12}}\left[i_{12} - v_{12}\left(\frac{1}{r_{S2}} + \frac{1}{r_{SD2}}\right) - \frac{V_{SD2}}{r_{SD2}} - i_{22}\right] \\
\frac{di_{22}}{d\theta} = \frac{1}{\omega L_{22}}\left(v_{12} - r_{22} i_{22} - v_{22}\right) \\
\frac{dv_{22}}{d\theta} = \frac{1}{\omega C_{22}}\left(i_{22} - \frac{v_{22}+V_{D2}}{r_{D2}} + i_3\right) \\
\frac{di_3}{d\theta} = \frac{L_L+L_S}{\omega(L_3+L_P)(L_L+L_S)-\omega L_M^2}\left[v_{21} - v_{22} - (r_3+r_P) i_3 - v_3 - \frac{L_M(R_L+r_S)}{L_L+L_S} i_L - \frac{L_M}{L_L+L_S} v_L\right] \\
\frac{dv_3}{d\theta} = \frac{i_3}{\omega C_3} \\
\frac{di_L}{d\theta} = \frac{L_M}{\omega(L_3+L_P)(L_L+L_S)-\omega L_M^2}\left[v_{21} - v_{22} - (r_3+r_P) i_3 - v_3 - \frac{(R_L+r_S)(L_3+L_P)}{L_M} i_L - \frac{L_3+L_P}{L_M} v_L\right] \\
\frac{dv_L}{d\theta} = \frac{i_L}{\omega C_L}.
\end{cases} \tag{17}$$

from the Fourier Transform as

$$I_{Lfund} = \frac{1}{2\pi}\sqrt{\left(\int_0^{2\pi} i_L \cos\theta d\theta\right)^2 + \left(\int_0^{2\pi} i_L \sin\theta d\theta\right)^2}. \tag{22}$$

The power-conversion efficiency can also be calculated using the circuit waveforms. The conduction losses of components and voltage drop losses in the switches and diodes are inherently included in the circuit model in Fig. 11. In addition, we consider the C_{OSS} hysteresis loss of the GaN HEMT [26], which is not included in the circuit model. The C_{OSS} loss can be calculated as

$$P_{OSSi} = k_O f^{\alpha_O} V_{S_i}^{\beta_O} \tag{23}$$

where V_{S_i} is the maximum voltage across the switch S_i, and coefficients $k_O = 1.4 \times 10^{-15}$, $\alpha_O = 1.6$, and $\beta_O = 1.6$ are used for GS66508 T. The power-conversion efficiency η can be calculated as

$$\eta = \frac{P_O}{P_I + P_{OSS1} + P_{OSS2}} \tag{24}$$

where the input power P_I can be calculated as

$$P_I = \frac{V_I}{2\pi}\int_0^{2\pi} i_{11} + i_{12}\, d\theta. \tag{25}$$

D. Optimization Execution

The optimization for the proposed inverter was carried out with the PSO iteration of $J = 100$ and particle number of $I = 200$. To investigate the parameter selection of a_1, a_2, and a_3 in (2), we performed five optimization runs for different weighting parameter sets.

Fig. 14 shows the value of the objective function for the global best solution as a function of the generation number. It can be observed from Fig. 14(a)–(c) and (d)–(f) that the cases with $a_1 = 0.729$ achieve higher values of objective function compared to those with $a_1 = 0.4$. However, the cases with $a_1 = 0.4$ exhibit smaller variations across the five runs, indicating more consistent performance. These results suggest that a larger a_1 promotes better global exploration at the expense of slower convergence. Furthermore, it can be seen from Fig. 14(b) and (e) that increasing a_2 leads to greater variation in the solutions, as particles are more strongly influenced by their personal best solutions. Additionally, it can be seen from Fig. 14(c) and (f) that a larger a_3 results in faster convergence. Although variations in PSO weighting parameters affected convergence speed and objective function values, practical solutions for designing the inverter were obtained in all cases. The maximum value of the objective function $F = 0.965$ was obtained with $a_1 = 0.729$, $a_2 = 1.5$, and $a_3 = 1.5$, whose parameter set is given in Table II.

Fig. 15 shows the values of the objective function calculated during the PSO search as a function of the normalized capacitances. It can be seen from Fig. 15(a) that there exists an optimal design point with a high objective function value within the solution space of C_1 and C_2. It can also be seen from Fig. 15(b) that the the objective function values are unaffected by C_3 when $1/(\omega C_3 Z_{Lr}) < 1$. This is because C_3 forms a resonant pair with L_3, which allows any combination under the same resonant frequency.

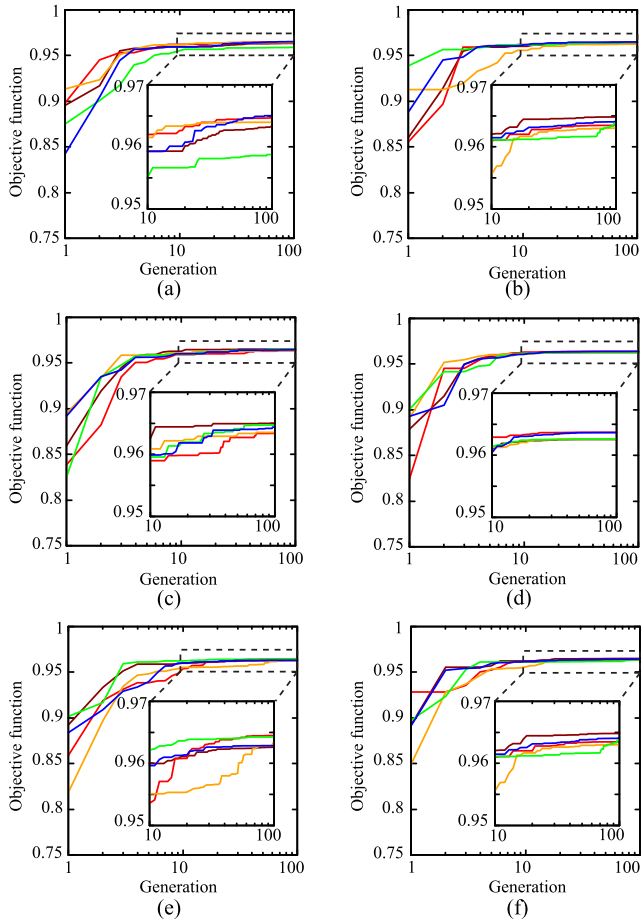

Fig. 14. Value of the objective function for the global best solution as a function of the generation number. (a) $a_1 = 0.729$ and $a_2 = a_3 = 1.5$. (b) $a_1 = 0.729$, and $a_2 = 2.5$, and $a_3 = 1.5$. (c) $a_1 = 0.729$, and $a_2 = 1.5$, and $a_3 = 2.5$. (d) $a_1 = 0.400$ and $a_2 = a_3 = 1.5$. (e) $a_1 = 0.400$, and $a_2 = 2.5$, and $a_3 = 1.5$. (f) $a_1 = 0.400$, and $a_2 = 1.5$, and $a_3 = 2.5$.

Based on these results, it can be said that there are no notable local maximum solutions in the parameter space of the proposed inverter. However, solutions with high objective function values are densely clustered near the optimal solution. Therefore, setting $a_2 < a_3$ is considered to facilitate the search for the optimal solution.

V. Experimental Verification

The experimental verification of the proposed inverter was carried out with the optimization results given in Section IV-D. A discussion for the conventional push-pull class-E inverter introduced in section II is also provided for comparison.

A. Experimental Setup

Fig. 16 shows the experimental circuit configuration to perform the load impedance variations, where the 500-WT-FN convection-cooled dry termination was used as the 50 Ω load resistance. The load impedance Z_L consists of a coaxial cable

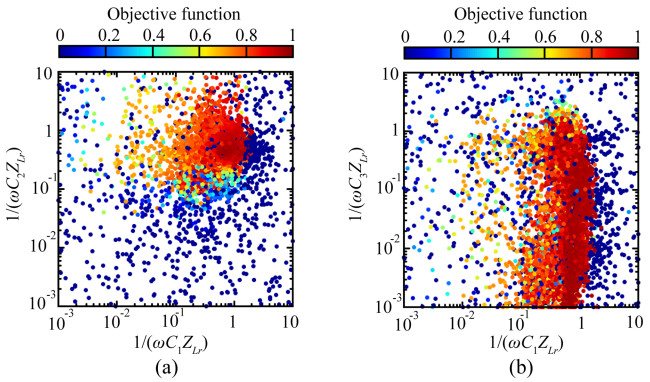

Fig. 15. Objective function values calculated during the PSO search as a function of the normalized capacitances. (a) For $1/(\omega C_1 Z_{Lr})$ and $1/(\omega C_2 Z_{Lr})$. (b) For $1/(\omega C_1 Z_{Lr})$ and $1/(\omega C_3 Z_{Lr})$.

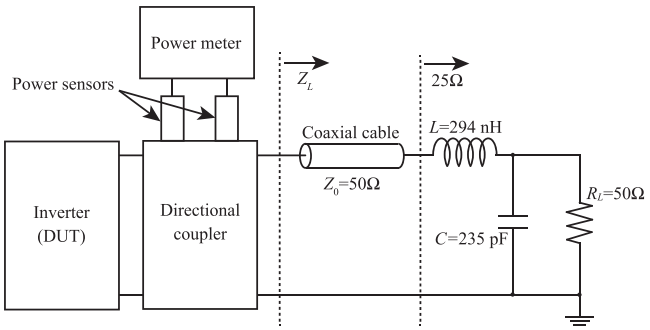

Fig. 16. The experimental circuit configuration.

TABLE III
LOAD IMPEDANCE AND CORRESPONDING COAXIAL CABLE LENGTH

Evaluation point	Load impedance Z_L	Coaxial cable length
A_1	25 Ω	0 m
A_2	$40+30j$ Ω	1.85 m
A_3	100 Ω	3.70 m
A_4	$40-30j$ Ω	5.56 m

with a characteristic impedance of $Z_0 = 50$ Ω and a 25 Ω matching circuit. Due to the impedance mismatch between the coaxial cable and the 25 Ω matching circuit, the load impedance Z_L can vary within the same VSWR by changing the length of the coaxial cable. As the circuit is evaluated under a fixed VSWR, it is convenient to vary the load impedance simply by swapping the cable. The relationship between the impedance Z_L and length of coaxial cable l can be expressed as

$$Z_L(l) = Z_0 \frac{R_L + jZ_0 \tan(\beta l)}{Z_0 + jR_L \tan(\beta l)} = \frac{25 + 50j \tan(\beta l)}{2 + j \tan(\beta l)} \quad (26)$$

where $\beta = 2\pi/\lambda$ is the phase constant, and λ is the wavelength of electromagnetic waves. Table III gives the load impedance and corresponding coaxial cable length used in the experiment.

The output power of the inverter was measured with C2671-20 Dual Directional Coupler from Werlatone, 8482 A Power Sensor from Keysight, and E4419B Dual-Channel Power Meter from Keysight, as shown in Fig. 16. The power meter measures the forward ac power P_{OF} and reflected ac power P_{OR}. The experimental output power P_O was measured as

$$P_O = P_{OF} - P_{OR}. \quad (27)$$

TABLE IV
CIRCUIT PARAMETERS OF THE INVERTERS

Proposed		Conventional	
Symbol	Parameter	Symbol	Parameter
C_{11}	159 pF	C_{11}	388 pF
C_{12}	159 pF	C_{12}	388 pF
C_{21}	542 pF	C_3	173 pF
C_{22}	542 pF	L_{11}	198 nH
C_3	1878 pF	L_{12}	198 nH
L_{11}	736 nH	L_2	1132 nH
L_{12}	736 nH	r_{11}	93 mΩ
L_{21}	452 nH	r_{12}	93 mΩ
L_{22}	452 nH	r_3	527 mΩ
L_3	129 nH	D_S	0.750
r_{11}	262 mΩ	–	–
r_{12}	262 mΩ	–	–
r_{21}	159 mΩ	–	–
r_{22}	159 mΩ	–	–
r_3	63 mΩ	–	–
D_S	0.544	–	–

TABLE V
INDUCTANCES AND THEIR ESRS

Symbol	Theoretical	Measured	Error
L_{11}	736 nH	736 nH	0.0 %
L_{12}	736 nH	736 nH	0.0 %
L_{21}	452 nH	442 nH	−2.1 %
L_{21}	452 nH	452 nH	0.3 %
L_3	129 nH	125 nH	−3.3 %
r_{11}	262 mΩ	257 mΩ	−2.0 %
r_{12}	262 mΩ	256 mΩ	−2.5 %
r_{21}	159 mΩ	153 mΩ	−3.7 %
r_{22}	159 mΩ	163 mΩ	−3.4 %
r_3	63 mΩ	80 mΩ	21.7 %

Table IV gives the circuit parameters of the proposed and conventional inverters. The conventional inverter described in Section II is designed with the same specifications given in Table I and design procedure as the proposed inverter. Table V gives the inductances and their ESRs, where the experimental component values were measured by the E4990 A Impedance Analyzer. We can see from Table V that the theoretical and measured inductances are in good agreement. However, there is a 21.7 % error between theoretical and measured ESRs of the inductor L_3. This is because Dowell's equation in (15) assumes that the length of the coil is significantly large against its radius so that the end effects are taken as negligible [27]. Meanwhile, the inductor L_3 has only 3 turns against a 5.0 mm radius. As a result, the ESR of L_3 is underestimated in the Dowell's equation. On the other hand, the absolute difference between theoretical and measured ESR of L_3 is only 23 mΩ, which does not significantly affect the waveform and efficiency estimations in the proposed design method. Therefore, we consider the ESR estimation by Dowell's equation to be practically acceptable in this article. Fig. 17 shows a photograph of the implemented proposed inverter.

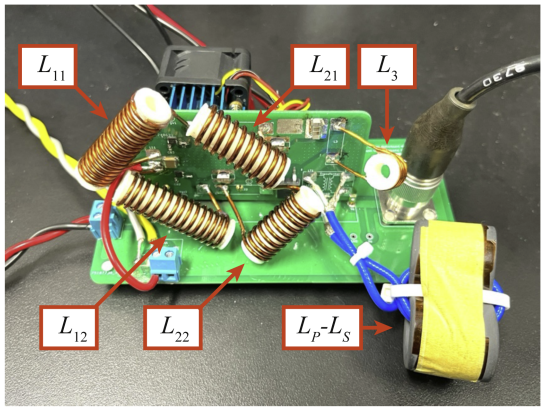

Fig. 17. Photograph of the implemented proposed push-pull class-E inverter.

B. Circuit Waveforms

1) Conventional Inverter for Load Impedance Variations: Fig. 18(a)–(e) shows the theoretical waveforms of the conventional phase-shift controlled push-pull class-E inverter. It can be seen from Fig. 18(a)–(e) that the conventional inverter needs to change the phase shift φ from 0.582π to π to achieve the output power regulation against load impedance variations. The large phase shift not only increases reactive current, but also has a significant effect on the switch voltage waveforms. It can be observed that the switch voltage v_{11} achieves ZVS in all the load conditions. However, non-ZVS waveforms appear in another switch voltage v_{12} for $Z_L = 50\ \Omega$, $Z_L = 25\ \Omega$, and $Z_L = 40 - 30j\ \Omega$. This is because the impedance seen from the switch S_2 becomes capacitive due to the load impedance variations and the phase-shift control. Conversely, the impedance seen from the switch S_1 becomes excessively inductive, resulting in the long reverse conduction time of the switch S_1. Due to the increased switching losses and the reverse conduction losses, the power-conversion efficiency deteriorates to 86.7%, 83.5%, and 81.0% for $Z_L = 50\,\Omega$, $Z_L = 25\,\Omega$, and $Z_L = 40 - 30j\,\Omega$, respectively. From these results, we can state that the conventional inverter is highly sensitive to load impedance variations. Although we attempted to experiment with the conventional inverter, the GaN switching device was damaged due to the non-ZVS. In addition, significant noise was introduced into the gate voltage due to non-ZVS, and circuit operation at 13.56 MHz and 500 W was challenging.

2) Proposed Inverter for Load Impedance Variations: Fig. 18(f)–(o) shows the theoretical and experimental waveforms of the proposed inverter. It can be seen from Fig. 18(f)–(o) that the phase-shift control for the output power regulation was performed in the smaller range of $0.833\pi \leq \varphi \leq \pi$ compared with the conventional inverter. We consider this to be the effect of the diode balance. The voltage clamp of diodes D_1 and D_2 prevents high voltage from being applied on one side of the single-ended inverter excessively. As a result, the impedance variations caused by load variations and the phase-shift control are alleviated. We can confirm that both switch voltages v_{11} and v_{12} achieved ZVS in all the load conditions. Moreover, the reverse conduction time in the switch during the turn-OFF period is reduced compared with the conventional inverter, which contributes to mitigating the reverse conduction losses of the GaN switching devices.

The proposed inverter achieved slightly lower efficiency than the conventional inverter when the conventional inverter achieved ZVS, as shown in Fig. 18(c), (d), (h), and (i). This is because the conventional inverter uses fewer inductors and diodes, resulting in lower conduction losses. However, the conventional inverter causes significant efficiency degradation under non-ZVS conditions in Fig. 18(a), (c), and (e). Therefore, the proposed inverter has an advantage in keeping consistently high efficiency across all the load impedances. The proposed inverter maintained power-conversion efficiency within 87.8% to 89.0% even against resistive, inductive, and capacitive load variations.

We confirm from the experimental results that the proposed inverter obtains robustness against load impedance variations owing to the diode balance. In addition, the experimental and theoretical waveforms are quantitatively agreed upon, which substantiates the validity of the experiment.

3) Proposed Inverter for Phase-Shift Modulation: Fig. 19 shows the circuit waveforms of the proposed inverter for fixed phase shift. We varied the phase shift between S_1 and S_2 at the load impedance of $Z_L = 50\ \Omega$. It is seen from Fig. 19 that the proposed inverter achieved ZVS in both v_{11} and v_{12} for all the phase shift conditions. The phase shift can cause an excessive reactive loading for the inverter. Therefore, it is challenging to keep ZVS over a wide range of phase shifts in the class-E inverters. Nevertheless, the proposed inverter maintained the ZVS because the diode clamp increases the inductive impedance seen from the switch. In these measurements, the output power of the inverter varied from 2 W to 500 W over a phase shift from 0 to 0.833π.

C. Circuit Characteristics

Fig. 20 shows the power loss breakdown of conventional and proposed inverters. The power losses are calculated using the theoretical waveforms and the circuit model shown in Fig. 11. The detailed equations and definitions for the power-loss factor are given in Appendix. We can see from Fig. 20(a) that power loss in the switching devices is the dominant power loss factor in the conventional inverter. Especially, the ON-resistance loss in the switch S_2 for the load condition of A_4 reaches 47 W due to non-ZVS. In addition, the ESR losses in the inductors are also a large loss factor. The conventional inverter is highly sensitive to load impedance variations. Consequently, large reactive currents are introduced to reduce the switching losses. It is known that in the class-E inverters, the load impedance range for achieving ZVS can be expanded by introducing ripples in the input current [28]. The currents flowing through L_{11} and L_{12} reach 9.47 A RMS and 8.99 A RMS, respectively, in A_0, which increases the ESR losses. On the other hand, we can see from Fig. 20(b) that the proposed inverter effectively reduces the power losses in the switches S_1 and S_2. Besides, the ESR losses in the inductors are also reduced compared with the conventional inverter. This is because the proposed inverter is unnecessary to have a large reactive current to achieve ZVS due to the clamp diode. The

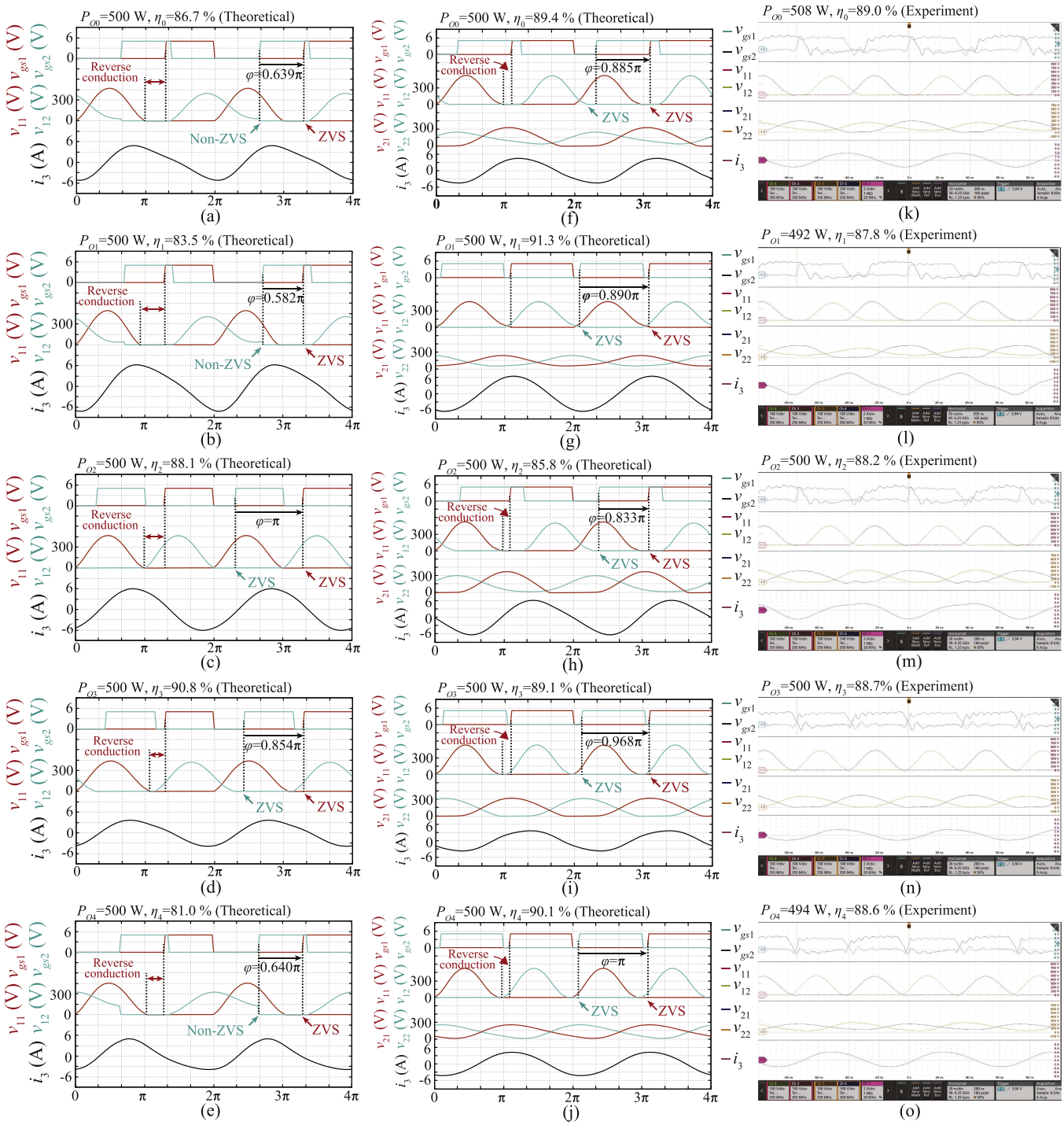

Fig. 18. Circuit waveforms. (a)–(e) Theoretical waveforms of conventional inverter. (f)–(j) Theoretical waveforms of proposed inverter. (k)–(o) Experimental waveforms of proposed inverter. (a), (f), (k) $A_0 : Z_L = 50\ \Omega$. (b), (g), (l) $A_1 : Z_L = 25\ \Omega$. (c), (h), (m) $A_2 : Z_L = 40 + 30j\ \Omega$. (d), (i), (n) $A_3 : Z_L = 100\ \Omega$. (e), (j), and (o) $A_4 : Z_L = 40 - 30j\ \Omega$.

currents flowing through L_{11} and L_{12} is 3.47 A RMS and 3.20 A RMS, respectively, in A_0. Despite the addition of the diodes and inductors, the proposed inverter reduces the total power losses, demonstrating the effectiveness of the diode clamp.

Fig. 21 shows the circuit characteristics as functions of the output power for the load impedance of $Z_L = 50\ \Omega$. We can see from Fig. 21(a) that the proposed inverter improves the power-conversion efficiency in heaby load range of output power compared with the conventional one. This is because the proposed inverter can maintain ZVS even when reactive loading occurs due to the phase shift. It is seen from Fig. 21(b) that the proposed inverter uses a larger phase shift to obtain the same output power compared with the conventional one. This indicates that the output power of the proposed inverter is less sensitive to phase shifts and reactive load variations than the conventional one. The theoretical predictions and experimental

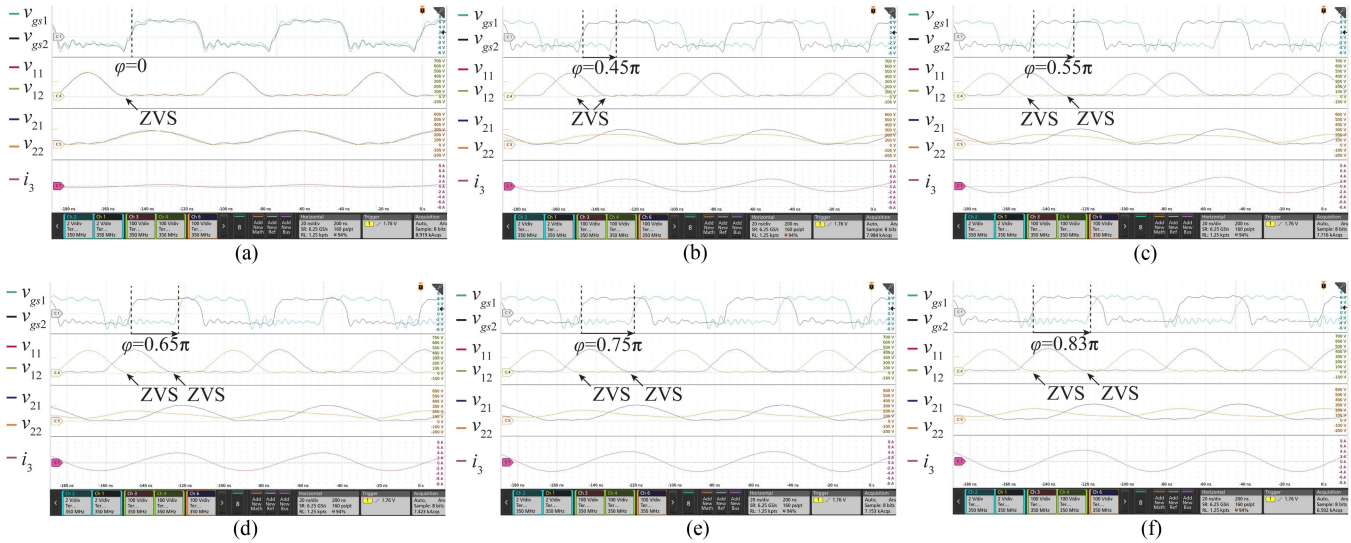

Fig. 19. Circuit waveforms of the proposed inverter for fixed phase shift. (a) For $\varphi = 0$ and 2 W. (b) For $\varphi = 0.45\pi$ and 102 W. (c) For $\varphi = 0.55\pi$ and 202 W. (d) For $\varphi = 0.65\pi$ and 290 W. (e) For $\varphi = 0.75\pi$ and 402 W. (f) For $\varphi = 0.83\pi$ and 500 W.

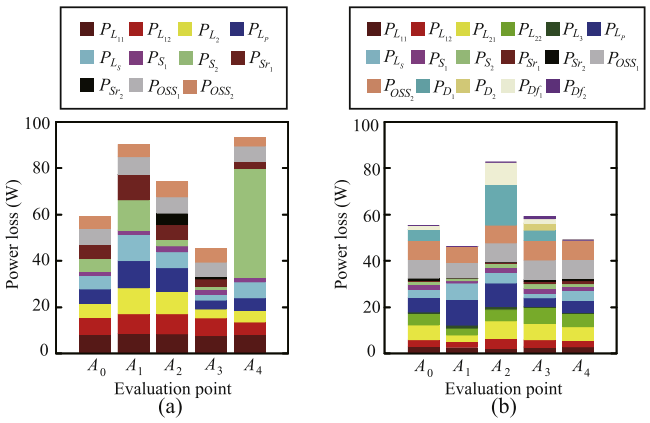

Fig. 20. Power loss breakdown. (a) For the conventional inverter. (b) For the proposed inverter.

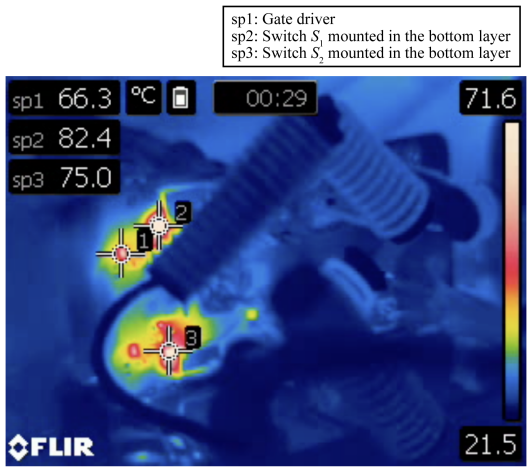

Fig. 22. Thermal image of the implemented inverter at 500 W.

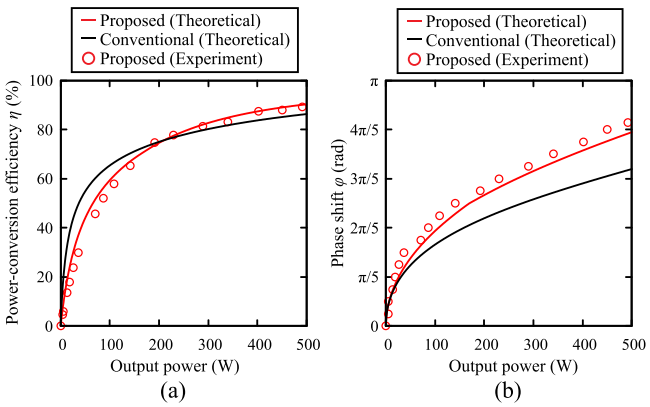

Fig. 21. Circuit characteristics as functions of the output power. (a) Power-conversion efficiency. (b) Phase shift φ.

results are in good agreement, which confirms the validity of the experiment and the accuracy of the model.

Fig. 22 shows the thermal image of the implemented inverter on the top layer at 500 W. It can be seen that the temperatures of the switches S_1 and S_2 reach 82.4 °C and 75.0 °C, respectively. The switches operate within the operating temperature range of –55 °C to 150 °C. The heat dissipation of the switches is performed using a heatsink and a fan from the bottom side of the PCB. Also, the temperature of the gate driver reaches 66.3 °C at 13.56 MHz. The gate drivers operate within the operating temperature range of –40 °C to 140 °C.

VI. Comparison With Previous Research

Table VI gives the comparison table with the conventional phase-shift controlled inverters. A phase-shift controlled

TABLE VI
COMPARISON WITH THE CONVENTIONAL PHASE-SHIFT CONTROLLED INVERTERS

	Designed inverter	Isolation	Component number S	D	L	C	Load impedance	Frequency	Output power	Efficiency
[11]	Interleave class-E	No	4	0	9	9	Resistive	27.12 MHz	100 W	40 %–85 %
[12]	Interleave class-D	No	5	0	4	6	Resistive and inductive	13.56 MHz	100 W	62 %–87 %
[14]	Interleave class-Φ_2	No	4	0	13	17	Resistive	13.56 MHz	200 W	82 %–93.5 %
[15]	Interleave class-E	No	6	0	13	19	Resistive	13.56 MHz	1500 W	83 %–93 %
[16]	Interleave class-E	No	4	0	9	17	Resistive	13.56 MHz	200 W	76 %–89 %
This work	Push-pull class-E	Yes	2	2	5	5	Resistive, inductive, and capacitive	13.56 MHz	500 W	87.8 %–89.0 %

inverter with a lossless multiway power combiner has been proposed [11], [12]. The power combiners are composed of passive *LC* components, absorbing the reactive loading caused by the phase-shift control. However, the combiners are highly sensitive to the reactive component variations. The modular ON/OFF control with phase-shift controls has been proposed [14], [15], [16]. In the modular ON/OFF control, multiple inverters are connected in parallel. Some of them work as phase-shift controlled inverters, and the others are turned OFF. As a result, the system can achieve output-power regulation with high efficiency over a wide range of load impedance variations. However, such solutions require a large number of components, leading to increased system complexity and scale. The proposed inverter achieves ZVS for all types of load impedance variations using only additional 2 diodes, 2 inductors, and 2 capacitors from the original push-pull class-E inverter.

VII. CONCLUSION

This article has proposed a phase-shift controlled push-pull class-E inverter with diode balance, along with its design method. Due to the diode clamps, the proposed inverter maintains symmetrical waveforms between the single-ended inverters. Consequently, the proposed inverter achieves the output power regulation and ZVS against resistive, inductive, and capacitive load impedance variations. The general design framework for the phase-shift controlled push-pull class-E inverter has been established, and it can adopt various design specifications and load impedance ranges. The experimental verifications for the proposed inverter were conducted with a 13.56 MHz operating frequency and a 500 W output power. The prototype inverter achieved 87.8% –89.0% power-conversion efficiency against resistive, inductive, and capacitive load impedance variations on the VSWR 2:1, confirming the effectiveness of the proposed inverter.

APPENDIX

We provide the equations for predicting the power losses in the proposed inverter. The power losses are calculated using the circuit model shown in Fig. 11 and its waveforms obtained by numerically solving (17).

The power losses due to the ESRs of the inductors are calculated as

$$P_{L_{ij}} = \frac{r_{ij}}{2\pi}\int_0^{2\pi} i_{ij}(\theta)^2 d\theta, \quad (i = 1, 2 \text{ and } j = 1, 2) \tag{28}$$

and

$$P_{L_3} = \frac{r_3}{2\pi}\int_0^{2\pi} i_3(\theta)^2 d\theta \tag{29}$$

where P_{ij} and P_{L_3} are the power losses in the ESRs of r_{ij} and r_3, respectively.

The power losses due to the ON-resistances of the switch and the diode can be obtained as

$$P_{S_j} = \frac{1}{2\pi r_{Sj}}\int_0^{2\pi} v_{1j}(\theta)^2 d\theta, \quad (j = 1, 2) \tag{30}$$

and

$$P_{D_j} = \frac{1}{2\pi r_{Dj}}\int_0^{2\pi} v_{2j}(\theta)^2 d\theta, \quad (j = 1, 2) \tag{31}$$

where P_{S_j} and P_{D_j} are the power losses in the ON-resistances of the switch S_j and diode D_j, respectively.

The power loss due to the reverse conduction in the switch can be derived as

$$\begin{aligned} P_{Sr_j} &= \frac{1}{2\pi}\int_0^{2\pi} V_{SDj} i_{SDj}(\theta) d\theta + \frac{r_{SDj}}{2\pi}\int_0^{2\pi} i_{SDj}(\theta)^2 d\theta \\ &= \frac{1}{2\pi r_{SDj}}\int_0^{2\pi} [v_{1j}(\theta) + V_{SDj}][v_{1j}(\theta) + 2V_{SDj}] d\theta, \\ &\quad (j = 1, 2) \end{aligned} \tag{32}$$

where i_{SDj} is the current flowing through r_{SDj} and P_{Sr_j} is the power loss due to the reverse conduction in the switch S_j.

The power loss due to the forward voltage drop in the diode is obtained as

$$\begin{aligned} P_{Df_j} &= \frac{1}{2\pi r_{Dj}}\int_0^{2\pi} i_{Dj}(\theta) V_{Dj} d\theta \\ &= \frac{V_{Dj}}{2\pi r_{Dj}}\int_0^{2\pi} v_{2j}(\theta) d\theta + \frac{V_{Dj}^2}{r_{Dj}}, \quad (j = 1, 2) \end{aligned} \tag{33}$$

where i_{Dj} is the current flowing through the diode D_j and P_{Df_j} are the power losses due to the forward voltage drop in the diode D_j, respectively.

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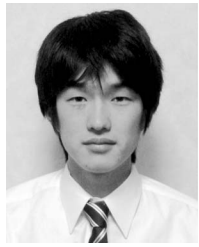
Yutaro Komiyama (Graduate Student Member, IEEE) received the B.E. and M.E. degrees in mathematics and informatics, in 2021 and 2022, respectively, from Chiba University, Japan, where he is currently working toward the Ph.D. degree in mathematics and informatics with the Graduate School of Science and Engineering.

Since 2022, he has been, Chiba University. He is a research fellow with the Japan Society for the Promotion of Science (JSPS). His research interests include high-frequency inverters, rectifiers, and wireless power transfer systems.

Wenqi Zhu (Member, IEEE) received the B.E. degree in electrical engineering and automation from Anhui University, China, in 2016, and the M.E. and Ph.D. degrees in mathematics and informatics from Chiba University, Japan in 2020 and 2022, respectively.

From 2022 to 2024, he was a Research Fellow with the Japan Society for the Promotion of Science (JSPS). He is currently an Assistant Professor with the Tokyo University of Science, Tokyo, Japan. His current research interests include resonant power converters and wireless power transfer systems.



Akihiro Konishi (Member, IEEE) received the M.S. and Ph.D. degrees in electrical engineering from Okayama University, Okayama, Japan, in 2019 and 2023, respectively.

From 2023 to 2024, he was a Project Assistant Professor with Chiba University, Chiba, Japan. Since 2025, he has been an Assistant Professor with the Faculty of Computer and Information Sciences, Sojo University, Kumamoto, Japan. His current research interests include power electronics and AI-assisted optimization of power converters.

Ayano Komanaka (Graduate Student Member, IEEE) was born in Aichi, Japan, on August 21, 1997. She received the B.E. and M.E. degrees in mathematics and informatics, in 2020 and 2022, respectively, from Chiba University, Chiba, Japan, where she is currently working toward the Ph.D. degree in mathematics and informatics with the Graduate School of Science and Engineering.

Her research interests include high-frequency and high-efficiency inverters.

Yinchen Xie (Graduate Student Member, IEEE) received the B.E. degree in information engineering from the School of Information Engineering, Hangzhou Dianzi University, Hangzhou, China, in 2020, and the M.E. degree in mathematics and informatics, in 2023, from Chiba University, Japan, where he is currently working toward the Ph.D. degree in information engineering.

His research interests include high-frequency inverters and rectifiers.

Kien Nguyen (Senior Member, IEEE) received the B.E. degree in electronics and telecommunication from Hanoi University of Science and Technology (HUST), Vietnam, in 2004, and the Ph.D. degree in informatics from the Graduate University for Advanced Studies, Japan, in 2012.

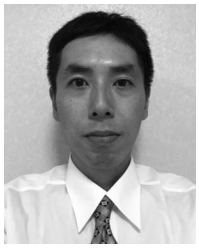
From 2014 to 2018, he was a Researcher with the National Institute of Information and Communication Technology (NICT), Japan. Since 2018, he has been with the Graduate School of Informatics, Chiba University, where he is currently an Associate Professor. His research covers a wide range of topics in networking and distributed systems, including the Internet, the Internet of Things technologies, and distributed ledger technologies. His research achievements have been disseminated in three patents, several IETF Internet drafts, and more than 180 publications in peer-reviewed journals and conferences.

Dr. Nguyen is a Member of the Institute of Electronics, Information, and Communication Engineers (IEICE) of Japan.

Hiroo Sekiya (Senior Member, IEEE) received the B.E., M.E., and Ph.D. degrees in electrical engineering from Keio University, Yokohama, Japan, in 1996, 1998, and 2001, respectively.

Since 2001, he has been with Chiba University, Chiba, Japan, where he is currently a Professor with the Graduate School of Informatics. His research interests include high-frequency inverters, wireless power transfer systems, and wireless communication systems.

Dr. Sekiya is a Fellow of IEICE, Japan, and a Member of IEEJ and the Electrochemical Society of Japan (EPSJ). He served on the IEEE Circuits and Systems Society Board of Governors from 2020 to 2022 and from 2023 to 2025. He serves as an Associate Editor for IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS and IET CIRCUITS, DEVICES AND SYSTEMS.



Tatsuya Ikenari was born in Hyogo, Japan, on March 5, 1972. He received the B.E. degree in electrical engineering from the Department of Electrical and Electronic Engineering, Faculty of Engineering, Tottori University, Japan, in 1994.

Since 1994, he has been engaged in the development and design of high-frequency power supplies for plasma generation at DAIHEN Corporation.