Discrete-Time State Feedback Design Approach in a Digitally Current Mode Controlled Boost Converter for Improving Transient Performance and Stability

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***Abstract*—The design tradeoff between the phase margin and the gain crossover frequency (ω_c) remains a challenge using an output feedback-based design approach in a current mode controlled (CMC) boost converter, primarily due to the presence of a right-half-plane (RHP) zero in its control-to-output transfer function. A state feedback (SF) design approach is an effective alternative in a digital CMC (DCMC) boost converter. Using discrete-time (DT) models, this article presents a direct SF-based design approach to optimize the converter's dynamic performance at higher ω_c in the presence of constraints on voltage/current overshoot/undershoot, irrespective of the type of load. The DT closed-loop model is shown to be valid for a higher ω_c and able to accurately predict the fast-scale instability due to the sampling delay under higher controller gains. A boost converter laboratory prototype is made, and the DCMC is implemented using an FPGA device. Superior transient performance using the proposed design approach at higher bandwidths, $\omega_c \in [0.5\,\omega_{\rm rhp},\ \omega_{\rm rhp}]$, is demonstrated using simulation and experimental results under constant resistive load, constant current load, and constant power load. The controllability property of the proposed design approach ensures the system's robustness and insensitivity against parameter variations and input voltage disturbance.**

***Index Terms*—Boost converter, constant current, current mode, constant power load (CPL), digital control, discrete-time state feedback, output/state feedback design, stability.**

I. Introduction

THE RHP zero ($\omega_{\rm rhp}$) in a boost converter comes closer to the imaginary axis of the complex "s" plane with increasing voltage gain and/or load current under continuous conduction mode (CCM) [1], [2]. The RHP zero problem, analogous to the effects of time delay, restricts the achievable closed-loop control bandwidth (BW) [3], regardless of the control techniques, thereby posing design challenges under a wide operating range. The achievable closed-loop BW (ω_c) is limited to $\omega_c = \omega_{\rm rhp}/5$ under voltage mode control, which can be enhanced up to $\omega_c = \omega_{\rm rhp}/3$ using CMC [4]. Under CMC, an output feedback (OF) approach is typically followed to design a type-II compensator or a PI controller [5]. Generally, a higher BW tends to reduce the phase margin (PM) [4]; thus, the worst-case design of a fixed gain controller results in slower transient performance in a boost converter for a wide operating range.

Nonlinear control methods, such as boundary control [6], [7], sliding-mode control [8], model predictive control [9], feedback linearization [10], etc., can achieve fast dynamic performance. However, due to the implementation complexity and challenges of variable frequency operations, the majority of low-power commercial products are still dominated by fixed-frequency controls. Digital CMC (DCMC) techniques have been gaining increasing attention because of real-time optimization [11] and tuning for achieving improved performance and efficiency [4], [12], [13], [14], [15], [16], [17]. Even so, the frequency-domain controller design approach using single-frequency small-signal models (SSM) cannot predict fast-scale instability and is not useful for performance exploration at higher BW under a variety of loads. Multifrequency modeling approaches [18], [19] and discrete-time (DT) modeling approaches are useful alternatives [20]. In contrast, the DT model can accurately capture the small-signal behavior while attempting to increase the control BW during transients, which offers an opportunity to overcome the BW barrier under CMC. However, the scope for further performance improvement remains difficult using an OF design approach due to the design tradeoff between PM and BW [21]. Also, the sampling delay along with the effective series resistance (ESR) of the output capacitance adversely affects the PM and cycle-by-cycle stability [22], [23], [24].

The SF-based design approach in [4] is useful in CMC by normalizing the SF gains to design the voltage loop PI controller. This is different from a full state-feedback realization [25]. The technique is applied to a DCMC boost converter [26]; however, the impact of the sampling delay while driving a dc load is not considered. Apart from a resistive load, it is also important to consider constant current load (CCL) and constant power load

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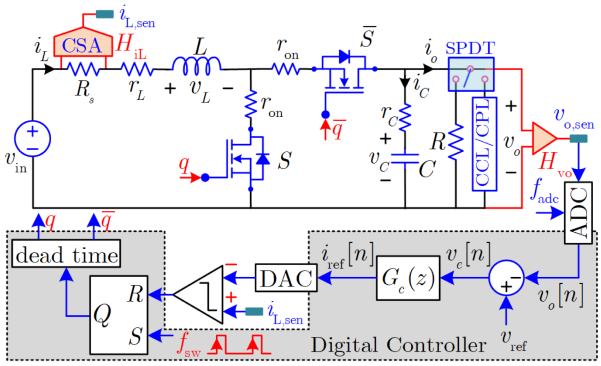


Fig. 1. Schematic of synchronous boost converter under DCMC.

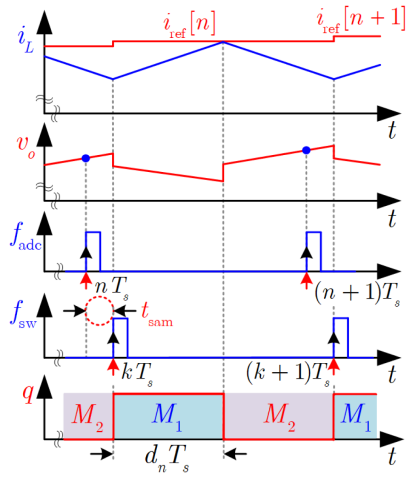


Fig. 2. Control waveforms of a boost converter under DCMC.

(CPL) for various applications. A CPL may lead to instability due to an incremental negative impedance effect, and various control techniques were reported in the past [27], [28], [29]. A fast transient DCMC technique was reported for a buck converter driving a CPL [30]. However, a suitable analysis and design framework is not readily available in a DCMC boost converter driving a CPL and other dc loads with optimized dynamic performance at higher BW.

The dc–dc converters belong to the class of switched linear systems, and a closed-loop switching scheme can be developed by combining SF realization and switching manifolds [31], such as sliding mode control [32], geometric control [33], etc. The implementation may include direct state-dependent switching, or a combination of time- and state-driven switching in a dc–dc converter [31], [32], [33], [34]. In this article, the switching surface concept and basic SF realization are retained in a DCMC boost converter. Further attempts are made to 1) develop accurate DT modeling to capture the sampling delay effect on closed-loop stability, 2) summarize steps for DCMC design in a boost converter for a variety of loads, such as constant resistive load, CCL, and CPL, and finally 3) demonstrate the usefulness of using accurate DT models and SF design framework to achieve a much higher BW with well-damped response and to retain cycle-by-cycle stability.

The rest of this article is organized as follows. Section II describes the small-signal modeling and DT output feedback (DTOF)-based controller design for a DCMC boost converter. Section III presents the proposed DTSF design approach in a DCMC boost converter driving various dc loads. Simulated case studies, comparing the performance using two design techniques, are presented in Section IV. Section V demonstrates the effectiveness of the proposed design technique using experimental results. Finally, Section VI concludes the article.

II. Modeling and of Based Controller Design in DCMC Boost Converter

Fig. 1 illustrates the schematic of a synchronous boost converter operating under DCMC and driving a dc load that may be a constant resistive load, CCL, CPL, or their combination. A mixed-signal implementation is used for the DCMC architecture [35], which consists of digital voltage and analog current loops. An analog-to-digital converter (ADC) is employed to sample the output voltage (v_o) using the sampling clock $f_{\rm adc}$ in sync with the switching clock $f_{\rm sw}$. A delay ($t_{\rm sam} \in (0,\ T_s]$) is used to capture clean voltage samples and to account for the ADC conversion and controller computation time. A digital PI controller G_c is considered, and its output is converted into an analog current reference $i_{\rm ref}$ using a digital-to-analog converter. The inductor current is sensed using a shunt R_s, which is compared with $i_{\rm ref}$ using an analog comparator. The comparator output is used to generate the gate signals (q, $\bar{q}$) using the latch and deadtime circuits as shown in Fig. 1. Fig. 2 shows the key control waveforms in a DCMC boost converter within a switching cycle. During mode-1 (M_1), the switch S is ON, and the inductor current (i_L) rises. During mode-2 (M_2), the switch S is OFF, and i_L falls.

A. Continuous-Time (CT) SSM

In Fig. 1, r_L, $r_{\rm ON}$, r_C, and R represent the dc resistance of the inductor, the ON-resistance of individual MOSFETs, ESR of the output capacitor, and the load resistance, respectively. The perturbed duty ratio can be obtained from the averaged linearized current loop model by applying small-signal perturbation as $\tilde{d} = F_{\rm mc}([-1\ \ 0]\tilde{x} + \tilde{i}_{\rm ref} - F_i\tilde{v}_{\rm in})$. From the equivalent circuit of a synchronous boost converter driving a dc load, considering the inductor current (i_L) and output capacitor voltage (v_C) as state variables, the perturbed state-space model can be written as follows:

$$\dot{\tilde{x}} = \begin{bmatrix} -\beta_{c2} & -\alpha D'/L \\ \beta_{c3} & -\gamma_{c3} \end{bmatrix} \tilde{x} + \begin{bmatrix} \beta_{c2} \\ -\gamma_{c2} \end{bmatrix} \tilde{i}_{\rm ref} + \begin{bmatrix} \beta_{c4} \\ \gamma_{c2}F_i \end{bmatrix} \tilde{v}_{\rm in} \quad (1)$$

where $F_i = DT_s/2L$, $\beta_{c2} = \beta_{c1}(1 + r'_C\gamma_{c1})$, $r'_C = r_C/D'$, $\beta_{c1} = F_{\rm mc}\alpha V_o/L$, $F_{\rm mc} = 2/m_1T_s$, $\beta_{c3} = k_\alpha/C' + \gamma_{c2}$, $C' = C/D'$, $\beta_{c4} = 1/L - \beta_{c1}F_i$, $D' = 1 - D$ (D is steady state duty ratio), $\alpha = R_{\rm leq}/(R_{\rm leq} + r_C)$, and the other coefficients are defined in Table I. In the generalized state-space model, $I_{\rm con}$ and $P_{\rm con}$ are considered as nominal values of constant load current and load power, respectively. The CT control-to-output transfer function (TF) of a CCM boost converter driving a dc load under

TABLE I
EXPRESSIONS OF THE COEFFICIENTS IN (1) AND (2) DEPENDING ON THE TYPE OF LOAD

Loads	k_α	γ_{c1}	γ_{c2}	γ_{c3}	γ_{c4}	R_{leq}
resistive	α	0	$F_{mc}\alpha V_o/D'RC$	α/RC	$2F_{mc}\alpha V_o/R$	R
CCL	1	I_{con}/V_o	$F_{mc}I_{con}/D'C$	0	$F_{mc}I_{con}$	V_o/I_{con}
CPL	1	P_{con}/V_o^2	$F_{mc}P_{con}/D'V_oC$	$P_{con}\alpha/V_o^2C$	0	V_o^2/P_{con}

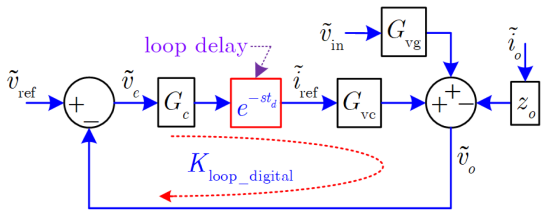


Fig. 3. Small-signal block diagram of boost converter under DCMC.

CMC with closed current loop can be expressed as follows:

$$G_{vc}(s)=\frac{D'\alpha F_{mc}V_o k_\alpha\left(1-s/\omega_{rhp}\right)}{LCs^2+\left(\alpha F_{mc}V_o+\gamma_{c3}L\right)Cs+\alpha\left(k_\alpha D'^2+\gamma_{c4}\right)} \tag{2}$$

where, $\omega_{rhp}=D'^2\alpha R_{leq}/L$, and the expressions of k_α, R_{leq}, and γ_{c4} are provided in Table I. The control-to-output TF in (2) can be approximated as a first-order system with a single load-dependent pole at ω_{pl}, since one of the poles is located far away on the negative real axis in the complex "s"-plane. The primary objective of SSM analysis is to design an appropriate controller (G_c) shaping the compensated loop gain, $K_{loop\_analog}(s)=G_c(s)G_{vc}(s)$, at the desired operating point to meet both transient and steady-state specifications. For the DCMC boost converter under a constant resistive load ($R_{leq}=R$), the PI controller needs to be designed by considering the closed-loop output impedance (z_{oc}) with the objectives to 1) operate at a higher closed-loop BW with stable periodic behavior, 2) reduce current/voltage overshoot/undershoot, 3) ensure cycle-by-cycle stability, 4) achieve well-damped response and robustness against parameters, and 5) minimize output voltage sensitivity to load variations. Thus, the closed-loop output impedance can be written as follows:

$$z_{oc}=\frac{z_o}{1+K_{loop\_analog}(s)};\ z_o=\frac{R}{2}\times\frac{(1+s/\omega_z)}{(1+s/\omega_p)} \tag{3}$$

where $\omega_z=1/r_CC$, and $\omega_p=2/(R+2r_C)C$. In addition, under DCMC, a loop delay t_d is considered in the forward path of the CT loop gain in Fig. 3, which is the sum of the sampling delay t_{sam} and the modulator delay t_{DPWM}. Thus, the overall CT loop gain of the DCMC boost converter can be written as $K_{loop\_digital}(s)=K_{loop\_analog}(s)\times e^{-st_d}$, which can be approximated using first-order Padé approximation as follows:

$$K_{loop\_digital}(s)\approx G_c(s)G_{vc}(s)\times\frac{(1-st_d/2)}{(1+st_d/2)}. \tag{4}$$

B. DT SSM Under DCMC

Considering the state vector as $x=[i_L\ \ v_C]^T$, and the input vector as $u=[v_{in}\ \ i_o]^T$, the state-space model of a boost converter driving a dc load can be expressed as follows:

$$\begin{aligned}&\dot{x}=A_mx+B_mu;\quad v_o=C_mx-\alpha_{DT}r_Ci_o\\&A_m=\begin{bmatrix}a_{11}&a_{12}\\a_{21}&a_{22}\end{bmatrix};\quad B_m=[B_{m1}\ \ B_{m2}]\\&B_{m1}=[1/L\ \ 0]^T;\quad B_{m2}=\alpha_{DT}[q'r_C/L\quad -1/C]^T\\&C_m=\alpha_{DT}\,[q'r_C\ \ 1];\quad m\in\{1,\ 2\}\end{aligned} \tag{5}$$

where $a_{11}=-[r_{eq}+q'\alpha_{DT}r_C]/L$, $a_{12}=-q'\alpha_{DT}/L$, $a_{21}=q'\alpha_{DT}/C$, $a_{22}=-\alpha_{DT}/R_lC$, $q'=1-q$, $r_{eq}=r_L+r_{on}$, $\alpha_{DT}=R_l/(R_l+r_C)$, and R_l depends on the type of load. The generic solution of (5) can be obtained as follows:

$$x(t)=e^{A_m(t-t_0)}x\left(t_0\right)+\Gamma_m\left(t-t_0\right)B_mu \tag{6}$$

where t_0 and $x(t_0)$ are the initial time and initial state vector for the mth mode, respectively, depending on the switching states (ON or OFF-state) and $\Gamma_m(\tau)=[e^{A_m\tau}-I]A_m^{-1}$. The overall DT model [36] between two consecutive sampling instants, nT_s and $(n+1)T_s$, can be obtained as follows:

$$\begin{aligned}x_{n+1}=&\,e^{A_2t_1}e^{A_1t_{ON}}e^{A_2t_{sam}}x_n+[e^{A_2t_1}\Gamma_1(t_{ON})B_1\\&+e^{A_2t_1}e^{A_1t_{ON}}\Gamma_2(t_{sam})B_2+\Gamma_2(t_1)B_2]u\end{aligned} \tag{7}$$

where $t_1=T_s-t_{ON}-t_{sam}$ and $t_{ON}=d_nT_s$. The DT SSM can be obtained by considering small perturbations $\tilde{x}_n$ and $\tilde{d}_n$ around the steady-state operating conditions x_{ss} and D, and applying Taylor series linearization [20] in (7) as follows:

$$\begin{aligned}&\tilde{x}_{n+1}=A_{eq}\tilde{x}_n+B_{eq}\tilde{d}_n+E_{eq}\tilde{i}_{o,n}\\&\tilde{v}_{o,n}=C_{eq}\tilde{x}_n-\alpha_{DT}r_C\tilde{i}_{o,n};\ \ C_{eq}=[\alpha_{DT}r_C\ \ \alpha_{DT}]\end{aligned} \tag{8}$$

where
$$\begin{aligned}A_{eq}&=e^{A_2(D'T_s-t_{sam})}e^{A_1T_{on}}e^{A_2t_{sam}}\\B_{eq}&=e^{A_2(D'T_s-t_{sam})}\times(A_1-A_2)\times B_{ss}\\E_{eq}&=e^{A_2(D'T_s-t_{sam})}E_{ss}+\Gamma_2(D'T_s-t_{sam})B_{22}\end{aligned}$$

where $B_{ss}=[x_{ss}+BV_{in}(DT_s+t_{sam})]T_s$, $B_{11}=B_{12}=B$, and $E_{ss}=e^{A_1T_{on}}\Gamma_2(t_{sam})B_{22}+\Gamma_1(T_{on})B_{12}$. The DT control-to-output TF and open-loop output impedance of a boost converter driving a resistive load ($R_l=R$) can be derived by substituting the expression of perturbed duty ratio, $\tilde{d}_n=F_m(\tilde{i}_{ref}[n]-\tilde{i}_{L,n})$, in (8) as follows:

$$\begin{aligned}G_{vc}(z)&=C_{eq}(zI-A_{DT})^{-1}B_{DT}\\z_o(z)&=C_{eq}(zI-A_{eq})^{-1}E_{eq}-\alpha_{DT}r_C\end{aligned} \tag{9}$$

where $A_{DT}=A_{eq}-F_mB_{eq}P_{eq}$, $P_{eq}=[1\ 0]e^{A_2t_{sam}}$, $B_{DT}=F_mB_{eq}$, and $F_m=1/m_1T_s$, where m_1 is rising slope of i_L.

C. Achieving Higher Control BW Using DT SSM

Fig. 4 shows that the CT SSM with a delay cannot capture the small-signal behavior with adequate accuracy while attempting

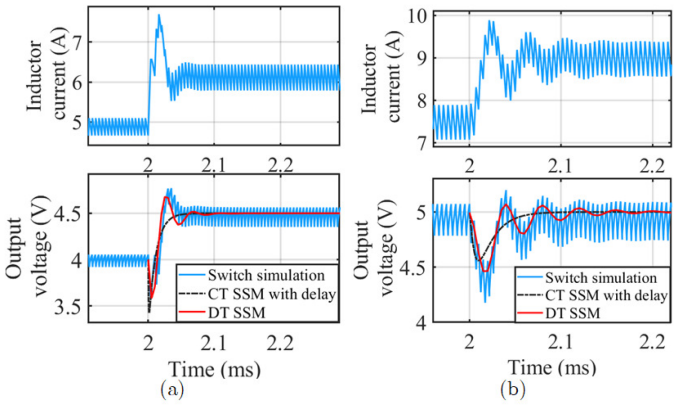


Fig. 4. (a) Step-up reference transient performance with model matching for a step change in $v_{\rm ref}$ from 4 V to 4.5 V using $\omega_c = 0.7\,\omega_{\rm rhp}$. (b) Step-up load transient with control BW $\omega_c = \omega_{\rm rhp}$ for a load step size of 1 A.

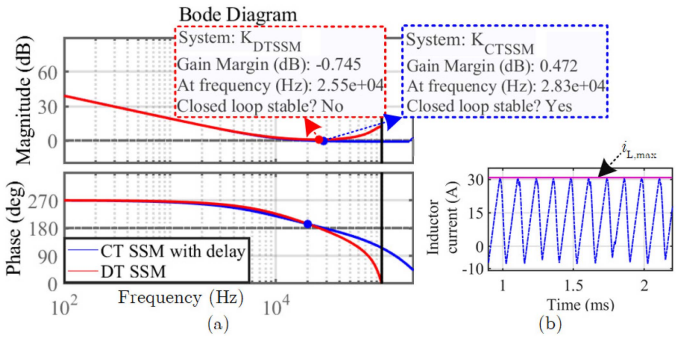


Fig. 5. Frequency response of the compensated CT loop gain in (a) fails to predict fast-scale instability (at $\omega_c = \omega_{\rm sw}/10$), as evident from the (b) inductor current trace, which can be predicted using the (a) DT loop gain.

to increase the control BW during reference and load transients. In contrast, the DT model offers superior accuracy and precisely captures overshoot and undershoot, as shown in Fig. 4. Thus, the DT model can be used to further improve the BW and to predict fast-scale instability. The DT compensated loop gain can be expressed as $K_{\rm ld\_digital}(z) = G_c(z) \times G_{\rm vc}(z)$, where $G_c(z)$ represents a digital PI controller.

D. Current Loop Stability Analysis Using CT and DT SSMs

A comparative study of the frequency response using the CT and DT SSMs is shown in Fig. 5. The figure shows that for the gain crossover frequency of the loop gain, $\omega_c = \omega_{\rm sw}/10$, the DT model correctly predicts the onset of instability, which is consistent with the switch simulation, whereas the loop gain using the CT model fails to capture instability. In addition, the location of the closed-loop poles for varying proportional gain $k_{\rm pd}$ is plotted in the complex z-plane as shown in Fig. 6(a). The figure shows that a higher $k_{\rm pd}$ leads to an unstable closed-loop system and this behavior is accurately captured by the DT model, which aligns with the relevant switch simulation shown in Fig. 6(c). Whereas, the CT SSM with delay in (4) fails to accurately predict the instability for higher gain, as shown in Fig. 6(b). Thus, the DT model can be used to design the digital

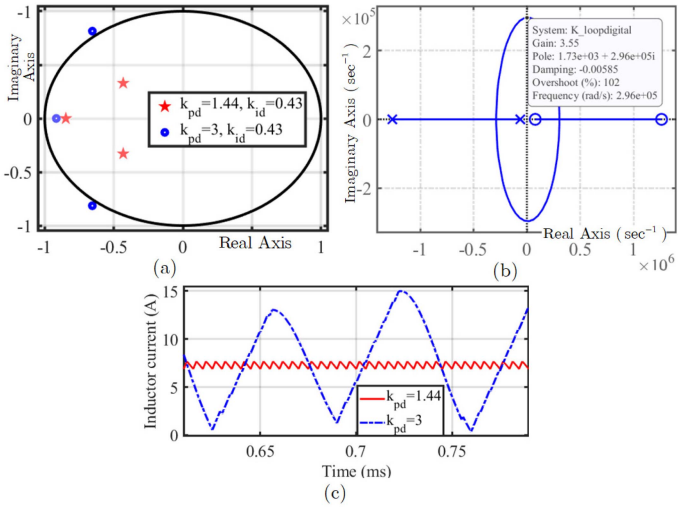


Fig. 6. (a) Eigenvalue plot of the overall closed-loop DT SSM for varying $k_{\rm pd}$. (b) Locus of the poles of $K_{\rm loop\_digital}(s)$ in (4). (c) Unstable time domain case study using a higher value of $k_{\rm pd}$ at $R = 1\Omega$.

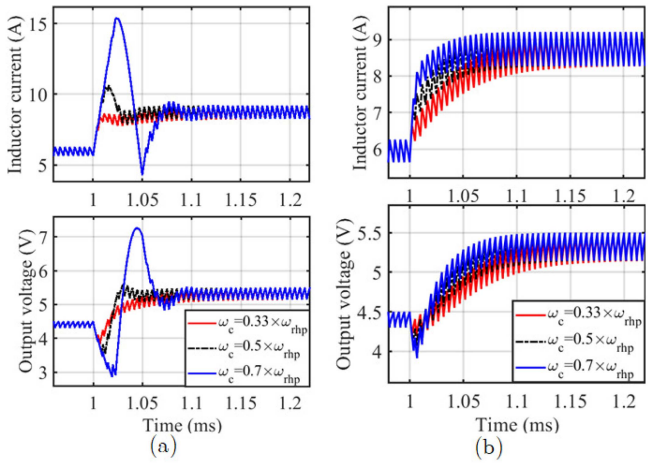


Fig. 7. Transient performance using (a) DTOF and (b) DTSF design approaches for a step change in $v_{\rm ref}$ from 4.5 to 5.5 V at $R = 1\Omega$ using different ω_c.

voltage controller directly in the digital domain and to accurately predict the stability boundary compared to that using the CT model.

E. DTOF Controller Design—Frequency Domain Approach

Fig. 3 shows the small-signal block diagram of a DCMC boost converter, where a PI controller in the form $G_c(s) = k_p + k_i/s$ is used. Primary loop shaping objectives in a DCMC boost converter are to 1) minimize the effect of the single pole of the plant by placing the controller zero ($\omega_{\rm cz} = k_i/k_p$) in coincidence with ω_{pl}, 2) achieve the desired gain crossover frequency $\omega_c = k_{\rm des}\,\omega_{\rm rhp}$ by setting the integral gain, 3) achieve zero steady-state error of $G_{\rm vc}(s)$, and 4) 60° PM. Thereafter, the backward difference method is used to obtain the digital PI controller gains as $k_{\rm pd} = k_p$ and $k_{\rm id} = k_i T_s$. Fig. 7(a) shows the reference transient performance of a boost converter driving

TABLE II
DESIGN SPECIFICATIONS OF SYNCHRONOUS BOOST CONVERTER

L	C	v_{in}	f_{sw}	r_{eq}	r_C	t_{sam}
6.8 μH	32.9 μF	3.3 V	200 kHz	4 mΩ	5 mΩ	250 ns

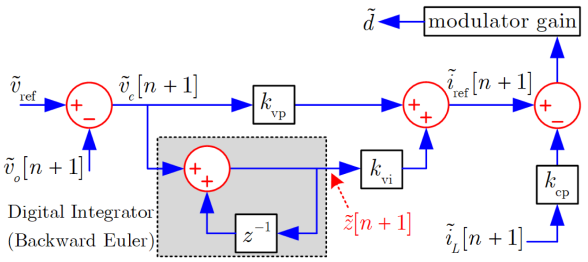


Fig. 8. State-feedback digital PI controller design approach in DCMC.

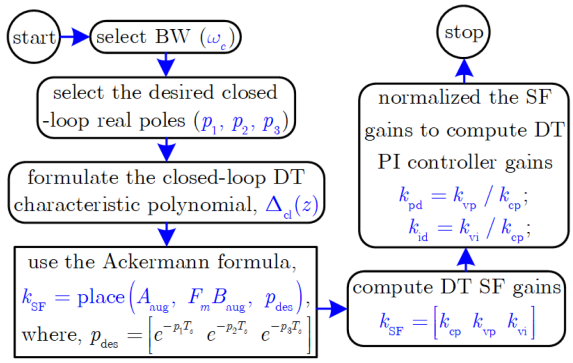


Fig. 9. Summary of the key steps in the proposed DTSF design approach.

a resistive load using the parameters specified in Table II. The figure shows that a higher ω_c results in larger voltage/current overshoot/undershoot, which is mainly because of decreasing PM for increasing ω_c. Hence, the practical tradeoff between achieving 60° PM and high closed-loop BW makes providing faster transient performance with reduced overshoot/undershoot challenging.

III. DESIGN OF DCMC USING SF APPROACH

A. Design Using Proposed DTSF Approach

The peak CMC with PI controller can be framed as an augmented SF system, which can be represented by a switching surface u_{sw}, and at the moment of switching in each cycle [4] as follows:

$$u_{\text{sw}} = k_{\text{p,SF}}\, v_e + k_{\text{i,SF}} \int v_e\, dt - k_{\text{c,SF}}\, i_L = 0$$
$$\Rightarrow \frac{k_{\text{p,SF}}}{k_{\text{c,SF}}} v_e + \frac{k_{\text{i,SF}}}{k_{\text{c,SF}}} \int v_e\, dt - i_L = 0 \tag{10}$$

where $v_e = (v_{\text{ref}} - v_o)$. The SF gain vector is defined as $k_{\text{SF}} = [k_{\text{c,SF}} \;\; k_{\text{p,SF}} \;\; k_{\text{i,SF}}]^T$; and the proportional and integral gains of the PI controller can be computed by normalizing the SF gains as $k_{\text{p,PI}} = k_{\text{p,SF}}/k_{\text{c,SF}}$, and $k_{\text{i,PI}} = k_{\text{i,SF}}/k_{\text{c,SF}}$ [4]. The DCMC with a digital PI control can be realized using a state feedback approach, as shown in Fig. 8, and the perturbed augmented DT SSM can be obtained as follows:

$$\begin{bmatrix} \tilde{x}_{n+1} \\ \tilde{z}_{n+1} \end{bmatrix} = \underbrace{\begin{bmatrix} A_{\text{eq}} & 0 \\ -C_{\text{eq}} A_{\text{eq}} & 1 \end{bmatrix}}_{A_{\text{aug}}} \begin{bmatrix} \tilde{x}_n \\ \tilde{z}_n \end{bmatrix} + \underbrace{\begin{bmatrix} B_{\text{eq}} \\ -C_{\text{eq}} B_{\text{eq}} \end{bmatrix}}_{B_{\text{aug}}} \tilde{d}_n \tag{11}$$

where, A_{eq}, B_{eq}, and C_{eq} are defined in (8). The closed-loop characteristic equation can be obtained using $\tilde{d}_n = F_m(\tilde{i}_{\text{ref}}[n] - \tilde{i}_{\text{L,n}})$ in (11), where $\tilde{i}_{\text{ref}}[n] = -k_{\text{pd}} C_{\text{eq}} \tilde{x}_n + k_{\text{id}} \tilde{z}_n$. The DT PI controller gains $k_{\text{pd}} = k_{\text{vp}}/k_{\text{cp}}$ and $k_{\text{id}} = k_{\text{vi}}/k_{\text{cp}}$ can be derived by using the normalization factors in (10). The key aspects of selecting the closed-loop eigenvalues include concern for the plant's open-loop pole location, gain-crossover frequency, and deliberate time-scale separation to ensure two different dynamics of the system, such as inductor current and output voltage. By integrating these considerations, in the proposed SF design approach, the desired closed-loop real poles are selected by considering 1) the zero of the PI controller as one of the poles, $p_1 = \omega_{pl}$, 2) the second pole p_2 is set at the gain crossover frequency $\omega_c = k_{\text{des}}\, \omega_{\text{rhp}}$, and 3) the third pole p_3 (linked with the inductor) is taken as 10 times faster than the second pole p_2. Using the Ackermann formula [37], the feedback controller gains can be computed by considering the desired closed-loop DT characteristic polynomial as follows:

$$\Delta_{\text{cl}}(z) = \left(z - e^{-p_1 T_s}\right)\left(z - e^{-p_2 T_s}\right)\left(z - e^{-p_3 T_s}\right). \tag{12}$$

The summary of the key steps in the proposed DTSF design approach is shown in Fig. 9. With the objective of achieving high control BW, a reference transient case study of a boost converter driving a resistive load using proposed DTSF design approach is presented in Fig. 7(b). In this case study, the digital PI controller's gains are determined by placing the closed-loop poles at $p_1 = 2/(R + 2r_C)C$, $p_2 = \omega_c = k_{\text{des}}\, \omega_{\text{rhp}}$ with $k_{\text{des}} \in \{0.33,\, 0.5,\, 0.7\}$, and $p_3 = 10\omega_c$. The figure highlights that the proposed design approach offers superior step-up reference transient performance without any overshoot/undershoot, even at higher ω_c. In addition, compared to the DTOF approach, which relies on an approximated first-order control-to-output TF to design the controller gains, the DTSF approach leverages the controllability property to directly control both i_L and v_o through pole-placement. This enables the proposed approach to offer greater flexibility in the placement of closed-loop poles, allowing for improved PM while maintaining the same control BW.

B. Controller Design Using DTSF for Fast Recovery Under CPL

A CPL with the nominal power P_{con} can be linearized close to its operating point as an incremental negative resistance (R_{CPL}), where $R_{\text{CPL}} = -V_o^2/P_{\text{con}}$, and reduces the damping of the overall system. The state-space model in (5) can be used for a boost converter driving a CPL by replacing $\alpha_{\text{DT}} = R_{\text{CPL}}/(R_{\text{CPL}} + r_C)$, and (11) can be used to derive the augmented DT SSM. The dominant pole of the generalized control-to-output TF of the boost converter driving CPL in (2)

TABLE III
SUMMARY OF DESIRED CLOSED-LOOP POLES EXPRESSIONS

Loads	Desired closed-loop poles
resistive	$p_1 = 2/(R + 2r_C)C,\ \ p_2 = \omega_c \in \boxed{0.5\,\omega_{\rm rhp},\ \omega_{\rm rhp}}\ ,\ \ p_3 = 10\omega_c$
CCL	$p_1 = \beta_{\rm CCL} - \sqrt{\beta_{\rm CCL}^2 - (D'/L)\gamma_{c2}},\ p_2 = \omega_c,\ p_3 = 10\omega_c$, where, $\beta_{\rm CCL} = F_{\rm mc}\alpha V_o/2L$ and $\gamma_{c2} = F_{\rm mc}I_{\rm con}/D'C$
CPL	$p_1 = \beta_{\rm CPL} - \sqrt{\beta_{\rm CPL}^2 - (D'^2/LC)},\ p_2 = \omega_c,\ p_3 = 10\omega_c$, where, $\beta_{\rm CPL} = \beta_{\rm CCL} - 2\gamma_{c2}L/D'^2T_s$

is considered to map the corresponding DT pole p_1 of the characteristic polynomial in (12), which is written as follows:

$$p_1 = \beta_{\rm CPL} - \sqrt{\beta_{\rm CPL}^2 - (D'^2/LC)} \tag{13}$$

where $\beta_{\rm CPL} = \beta_{\rm CCL} - 2\gamma_{c2}L/D'^2T_s$ and $\beta_{\rm CCL} = F_{\rm mc}\alpha V_o/2L$. With the objective of seeking to design the controller at higher BW, as DT SSM offers the opportunity to increase the BW further, the digital PI controller is designed by following the steps in Fig. 9 and placing the other two poles, p_2 at ω_c and p_3 at $10\,\omega_c$, where $\omega_c \in [0.5\,\omega_{\rm rhp},\ \omega_{\rm rhp}]$.

C. Design Steps of DTSF for Boost Converter Driving CCL

A CCL with the nominal value $I_{\rm con}$ can be represented by an equivalent internal resistance $R_{\rm CCL}$. The input and output matrices in (5) will be updated by substituting the variable $\alpha_{\rm DT}$ with $\alpha_{\rm CCL} = R_{\rm CCL}/(R_{\rm CCL} + r_C)$, when the boost converter is driving a CCL. The DT augmented SSM in (11) should be accordingly modified using the equivalent resistance $R_{\rm CCL}$. Thereafter, the steps mentioned in Fig. 9 are followed to design the DT PI controller by considering three poles $p_2 = \omega_c = 0.7\,\omega_{\rm rhp}$, $p_3 = 10 \times \omega_c$, and $p_1 = \beta_{\rm CCL} - \sqrt{\beta_{\rm CCL}^2 - (D'/L)\gamma_{c2}}$, where $\beta_{\rm CCL} = F_{\rm mc}\alpha V_o/2L$ and $\gamma_{c2} = F_{\rm mc}I_{\rm con}/D'C$.

The guidelines for choosing three poles p_1, p_2, and p_3 under different dc loads are summarized in Table III. This along with the flowchart in Fig. 9 can be used to design the digital PI controller gains using the proposed DTSF design approach in the DCMC boost converter driving different types of dc loads. In this process, (12) should be used in formulating the DT characteristic equation in the intermediate step.

IV. CLOSED-LOOP PERFORMANCE COMPARISON

A. Reference Transient Performance

Using the DTOF design, Fig. 10 shows that an attempt to achieve a higher closed-loop BW $\omega_c = 0.7\,\omega_{\rm rhp}$ results in the lower PM, which leads to larger overshoot/undershoot in the inductor current and output voltage. On the other hand, for a higher BW, the DTSF design offers superior step reference transient performance, with negligible overshoot/undershoot in both the output voltage and inductor current. Consequently, the proposed approach helps in reducing the RHP zero effect [shown in Fig. 10(a)], which allows one to further reduce the size of the output capacitor for achieving higher power density. The DTSF design retains the controllability and facilitates the pole placement for a better tradeoff between the BW and PM in a DCMC boost converter. This is difficult to achieve using the DTOF design approach, in which the full controllability may be lost using a frequency-domain loop-shaping technique.

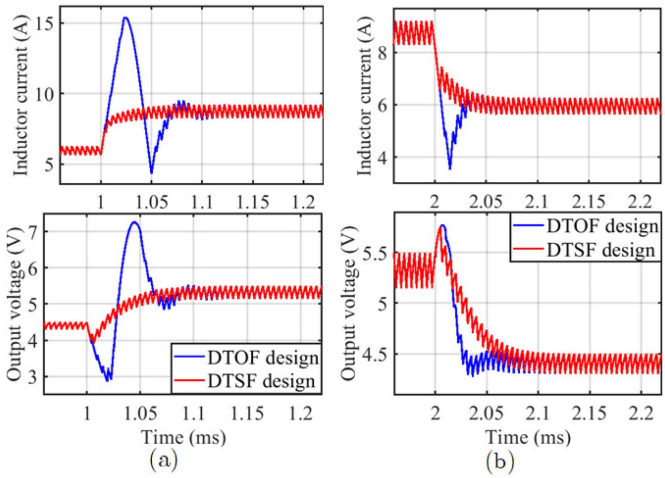


Fig. 10. Transient performance of the DCMC boost converter, using both the DTOF and DTSF design approaches, for a step change in $v_{\rm ref}$ from (a) 4.5 V to 5.5 V, and (b) back to 4.5 V at $R = 1\Omega$ using the BW $\omega_c = 0.7\,\omega_{\rm rhp}$.

Since the output voltage is sampled once per switching cycle in sync with the switching clock; the current reference remains constant throughout the switching cycle. As a result, the inner current loop stability of DCMC boost converter can be ensured for the operating duty ratio $D > 0.5$, if the compensating ramp is tuned as $m_c > 0.5\,(m_2 - m_1)$, where m_2 is the falling slope of i_L and m_c is the compensating ramp slope. The stability criterion is the same as for analog CMC with a fixed current reference; however, closed-loop stability criteria may differ. For the closed-loop system, if the quantized error voltage goes out of the zero-error bin [38], the fast-scale stability is primarily determined by the proportional gain, while the DT integral gain has an insignificant impact on the stability of a DCMC boost converter [39]. Using the DT framework, the ramp slope, m_c is chosen to ensure the stability. The simulation case study in Fig. 11 demonstrates that under DTOF design approach, for $m_c \leq 0.7\,(m_2 - m_1)$, the closed-loop poles move outside the unit circle when the output voltage is raised to 10 V, which results in undesirable high-periodic behavior with the duty ratio saturation. A higher compensating ramp with a slope of $m_c = 1.2\,(m_2 - m_1)$ can ensure fast-scale stability using the DTOF design approach; however, a higher slope tends to degrade the PM under CMC [21]. On the other hand, Fig. 11(a) shows that the proposed DTSF design approach can ensure stability using a smaller slope with $m_c = 0.7\,(m_2 - m_1)$, which results in fast transient along with a well-damped stable response.

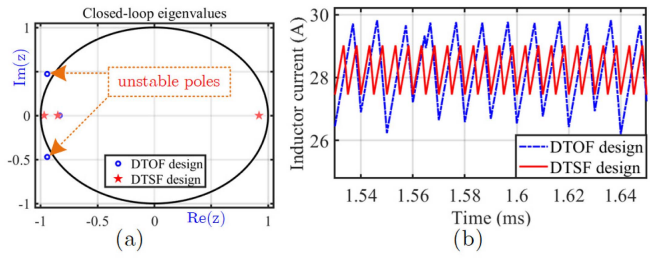


Fig. 11. (a) Locus of closed-loop poles in the z-plane under the DTOF and DTSF design approaches and (b) corresponding time domain traces to highlight cycle-by-cycle stability for a wide duty ratio operation.

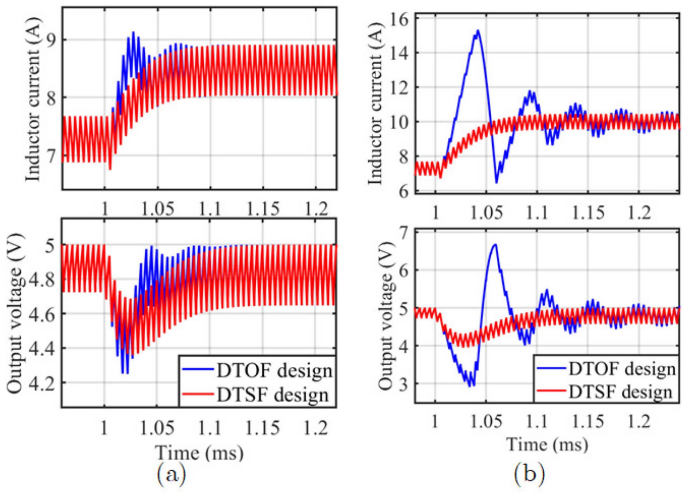


Fig. 12. Supply transient performance of the DCMC boost converter, using both the DTOF and DTSF design approaches, for a step change in $v_{\rm in}$ from (a) 3.3 V to 2.8 V, and (b) 3.3 V to 2.3 V using the BW $\omega_c = 0.7\,\omega_{\rm rhp}$.

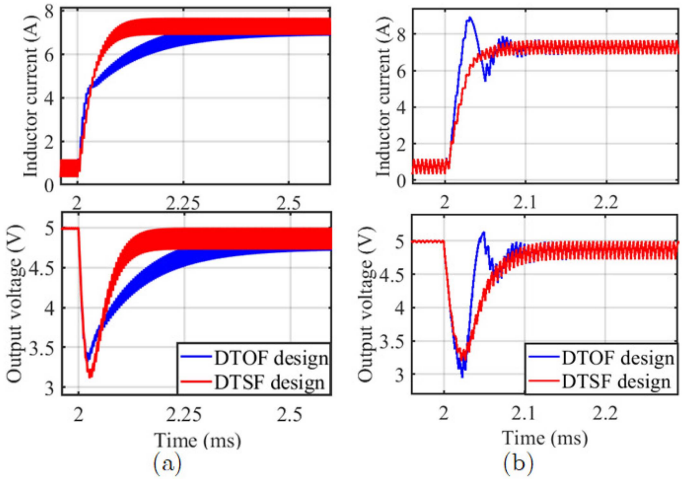


Fig. 13. Step-up load transient performance of the DCMC boost converter, using both the DTOF and DTSF design approaches, for a step change in R from 10Ω to 1Ω using the BW (a) $\omega_c = \omega_{\rm rhp}/2$, and (b) $\omega_c = \omega_{\rm rhp}$.

B. Supply Voltage Disturbance Rejection

The response of a boost converter driving a resistive load to a supply step transient using both the DTOF and DTSF design approaches is shown in Fig. 12. The DTSF approach provides inherent supply voltage compensation, resulting in excellent supply disturbance rejection, even during a 1 V variation in $v_{\rm in}$. The direct pole-placement flexibility in DTSF approach facilitates an improvement in the supply disturbance rejection performance over a wide input voltage range without considering any feedforward control or control with multiple degrees of freedom. Conversely, the DTOF causes a loss of such flexibility due to pole/zero cancellation; hence, the controller needs to set a current/voltage limit to prevent saturation.

C. Performance Comparison During Load Step Transient

An output impedance shaping technique is used to design the digital PI controller gains for improving load transient performance. Following the similar DTSF design method in Section III-A, the digital PI controller gains are computed to achieve the BW, $\omega_c \in [0.5\,\omega_{\rm rhp},\ \omega_{\rm rhp}]$. With a slightly higher (output) voltage undershoot during load step-up transient when $\omega_c = \omega_{\rm rhp}/2$, the DTSF approach can reduce the recovery time (0.16 ms) by fourfold in comparison with DTOF approach, as shown in Fig. 13(a). Since high load in a boost converter reduces the effective BW as $\omega_{\rm rhp}$ decreases, the substantial performance improvement is not obvious when BW increases to $\omega_c = \omega_{\rm rhp}$. However, the inadequate transient performance observed in DTOF approach, when $\omega_c \approx \omega_{\rm rhp}$, can be improved by considerably reducing the voltage/current overshoot/undershoot using the DTSF design approach, as shown in Fig. 13(b). Load current feedforward can be used to further improve performance and output impedance [4].

D. CPL Step Transient Performance

Fig. 14 shows the simulation result of a synchronous boost converter driving a CPL, which is obtained using the set of parameters in Table II for a step-change in the power $P_{\rm con}$ from 0.25 W to 5 W and back. The DTSF approach substantially enhances transient performance, achieving a recovery time of 0.1 ms for the same step-down load power transient using the same control BW $\omega_c = \omega_{\rm rhp}/2$, as shown in Fig. 14(b), which is approximately 17 times faster than DTOF. In addition, the voltage overshoot is reduced by 1.5 times as compared to the DTOF approach. Similarly, the step-up power transient performance can be significantly improved using the proposed DTSF design, as shown in Fig. 14(a) with 0.11 ms settling time and reduced voltage undershoot. The improvement of closed-loop performance under DTOF approach by increasing the BW to $\omega_c = 0.7\,\omega_{\rm rhp}$ results in subharmonic instability at the low output power levels, as observed in Fig. 15(a) and (b). Whereas, the proposed DTSF design technique offers fast power step-transient performance without affecting the converter's closed-loop stability requirements and improved closed-loop output impedance without load feedforward at higher BW, as demonstrated in Fig. 15(c).

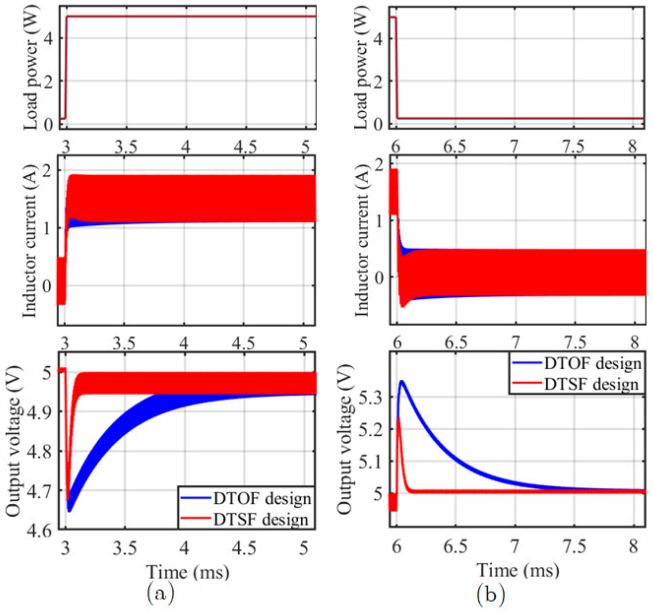


Fig. 14. Transient performance of the DCMC boost converter for a step change in CPL from (a) 0.25 W to 5 W, and (b) back to 0.25 W using $\omega_c = \omega_{\rm rhp}/2$.

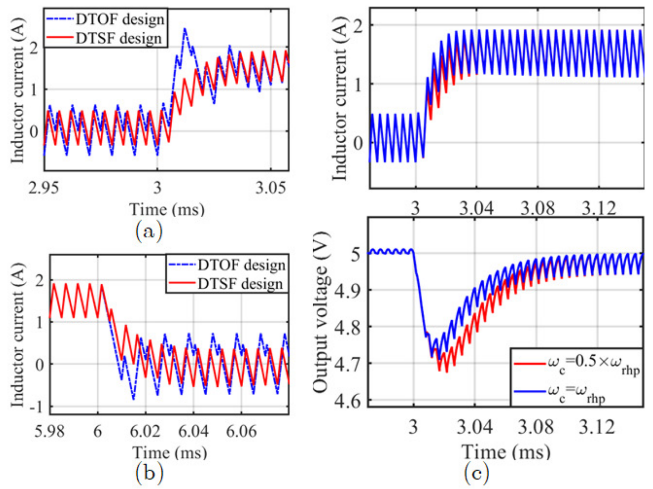


Fig. 15. Inductor current instability caused by high BW, $\omega_c = 0.7\,\omega_{\rm rhp}$, during step changes in CPL from (a) 0.25 W to 5 W, and (b) back; (c) Step-up power transient performance using DTSF approach with different ω_c.

E. Improved Reference Voltage Transient in CCL

Fig. 16 shows the step-reference transient performance of the DCMC boost converter driving a 5 A CCL, designed using both the DTOF and DTSF approaches, with the parameter set provided in Table II. Using the DTOF design approach, the digital PI controller gains are found to be $k_{\rm pd} = 2.05$ and $k_{\rm id} = 0.1967$ at higher BW $\omega_c = 0.7\,\omega_{\rm rhp}$. This results in 0.29 ms settling time with 0.67 V undershoot and 0.5 V overshoot in v_o during a step-up transient [in Fig. 16(a)], and 0.28 ms recovery time with 86 mV overshoot and 0.14 V undershoot in v_o during a step-down transient [in Fig. 16(b)]. On the other hand, using the same control BW, the DTSF design

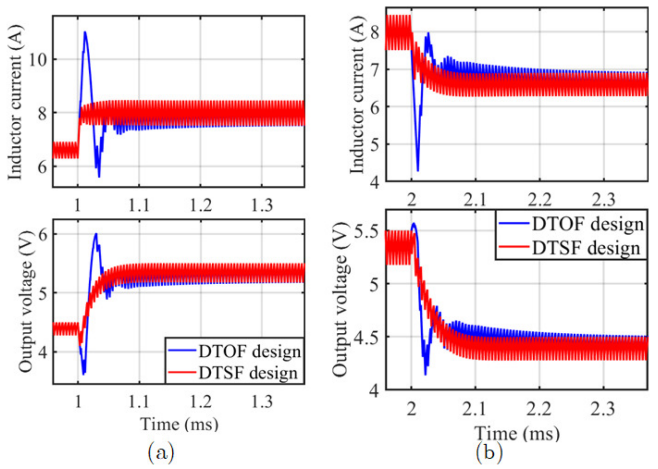


Fig. 16. Transient performance of the DCMC boost converter, using both the DTOF and DTSF design approaches, for a step change in $v_{\rm ref}$ from (a) 4.5 V to 5.5 V, and (b) back to 4.5 V using $\omega_c = 0.7\,\omega_{\rm rhp}$ under a CCL of 5 A.

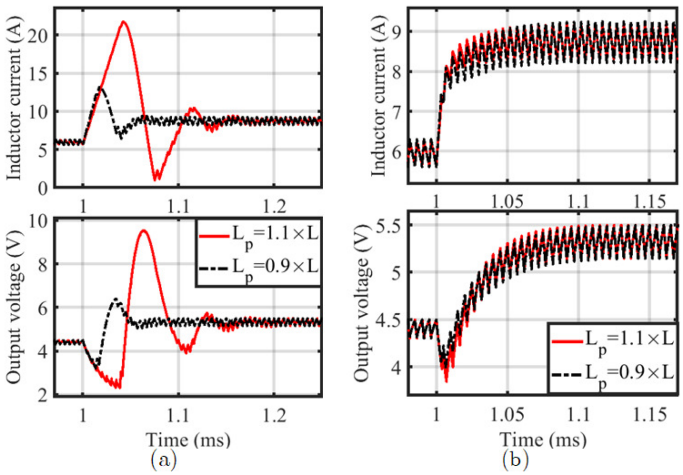


Fig. 17. Effect of inductor variations on the reference transient performance of the DCMC boost converter using (a) DTOF and (b) DTSF design approaches for step-up change in $v_{\rm ref}$ from 4.5 V to 5.5 V using $\omega_c = 0.7\,\omega_{\rm rhp}$.

technique offers superior transient performance with recovery times of 92 μs and 95 μs during step-up and step-down transients, respectively. During step-up, the voltage undershoot is reduced by four times without exhibiting any overshoot, and during step-down, there is no voltage overshoot/undershoot. It is important to highlight that using the proposed DTSF design, there is no overshoot/undershoot in the inductor current during step-up/down transients, which adequately optimizes the dynamic performance regardless of whether there are any limits on voltage/current overshoot/undershoot.

F. Robustness of DTSF Approach Against Parameter Variations

The proposed DTSF technique is designed using the nominal parameter set; however, it is important to analyze the effect of parameter variations on the transient performance. Fig. 17(b) shows that, under the DTSF design approach, $\pm 10\%$ variations

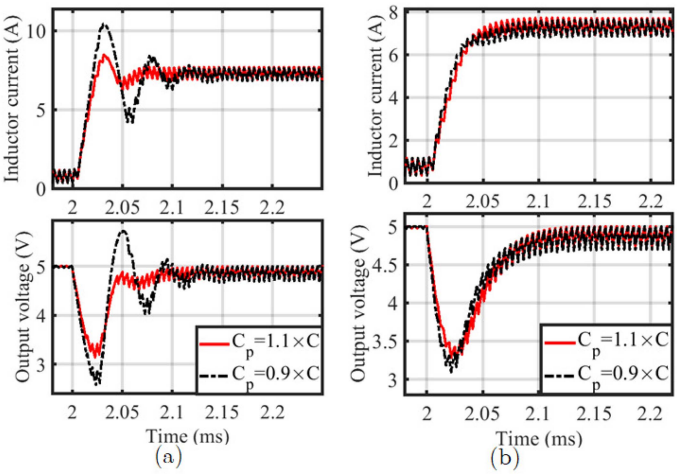


Fig. 18. Effect of capacitor variations on the load transient performance of the DCMC boost converter using (a) DTOF and (b) DTSF design approaches for a step change in load resistance from 10Ω to 1Ω using $\omega_c = \omega_{\rm rhp}$.

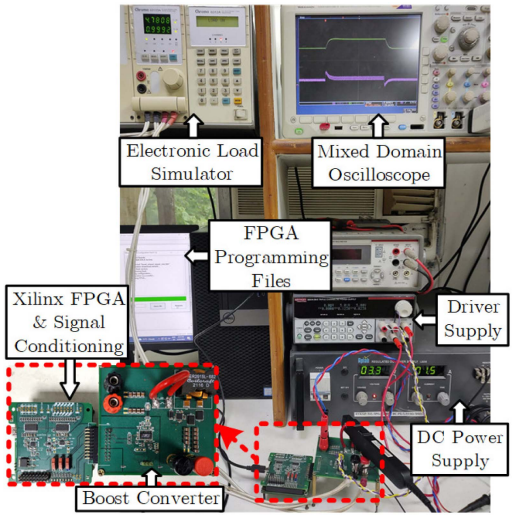


Fig. 19. Boost converter hardware prototype setup.

in the inductance (L_p), while keeping other parameters constant, have no significant impact on stability and transient performance for a step change in $v_{\rm ref}$ from 4.5 V to 5.5 V. Whereas the controlled reference signal generated by the DTOF approach is sensitive to parameter variations, resulting in nonrobust oscillatory behavior to the extent of closed-loop instability as shown in Fig. 17(a) and Fig. 18(a). Similarly, $\pm 10\%$ variations in the capacitance C_p have no substantial impact on the load (step-up) transient performance when the controller gains are computed using the DTSF approach, as shown in Fig. 18(b). Thus, the DTSF design approach retains significant performance improvement over the DTOF design method even under parameter variations.

V. Hardware Implementation and Performance Comparison Using Experimental Results

A. Hardware Implementation

A synchronous boost converter prototype is developed using the parameters in Table II, and the complete experimental setup is displayed in Fig. 19. The DCMC technique is implemented using a Xilinx Spartan-6 FPGA kit with a clock of 100 MHz. The digital PI controller parameters are designed following the steps described in Sections II and III. The inductor current is sensed using a 5 mΩ current sense resistor followed by a current sense amplifier with a gain of 10. A 10-bit ADC (AD9215) is used for sampling the output voltage v_o at the same rate as the switching frequency of 200 kHz.

B. Comparative Study of Reference Transient Performance

The experimental results in Fig. 20 show the reference transient performance of the DCMC boost converter using the DTOF design approach. The digital PI controller gains are found to be $k_{\rm pd} = 4.56$ and $k_{\rm id} = 0.56$, which result in 250 μs settling time and 0.8 V voltage overshoot during the step-up case. For the step-down case, the settling time and voltage undershoot are found to be 183 μs and 0.58 V, respectively.

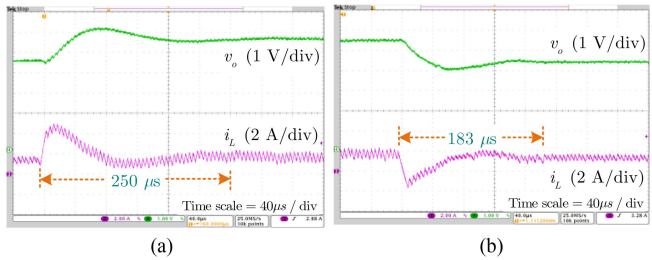


Fig. 20. Experimental transient performance using the DTOF design approach for a step change in $v_{\rm ref}$ from 4.5 V to 5.5 V, and back at $R = 5\Omega$. (a) Step-up reference transient. (b) Step-down reference transient.

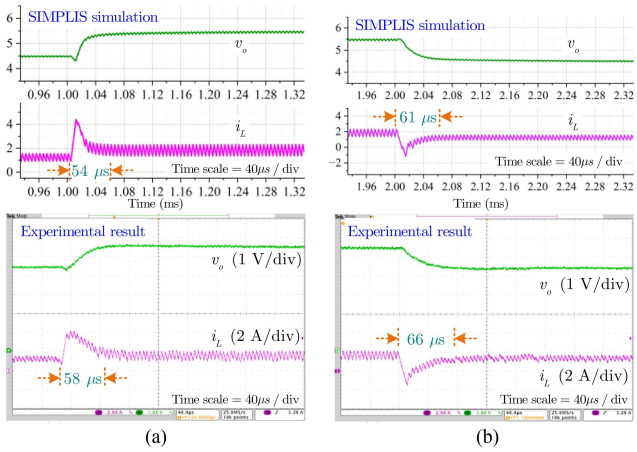
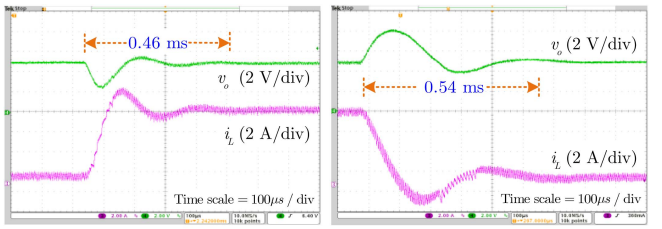


Fig. 21. Transient performance using the proposed DTSF approach for a step change in $v_{\rm ref}$ from (a) 4.5 V to 5.5 V, and (b) back to 4.5 V at $R = 5\Omega$: Verifying consistency using SIMPLIS simulation and experimental results. (a) Step-up reference transient. (b) Step-down reference transient.

Under the proposed DTSF design approach, the digital PI controller gains are found to be $k_{\rm pd} = 4.06$ and $k_{\rm id} = 0.176$. Fig. 21 demonstrates that the settling time is 58 μs during step-up and 66 μs during step-down transients, with no overshoot/undershoot in the output voltage. It is also important to

TABLE IV
COMPARATIVE ASSESSMENT OF PROPOSED DTSF DESIGN APPROACH

Step-down reference transient	Experimental result	Simulation result
Settling time (μs)	66	61
Current undershoot (A)	2	1.97
Step-down load transient	Experimental result	Simulation result
Settling time (ms)	0.28	0.278
Voltage overshoot (V)	2.23	2.2
Current undershoot (A)	0.7	0.62
Step-down transient under CCL	Experimental result	Simulation result
Settling time (μs)	82	73
Current undershoot (A)	1.65	1.61



(a) (b)

Fig. 22. Experimental transient performance using the DTOF design method for a step change in load current from 0.5 A to 5 A, and back to 0.5 A. (a) Step-up load transient. (b) Step-down load transient.

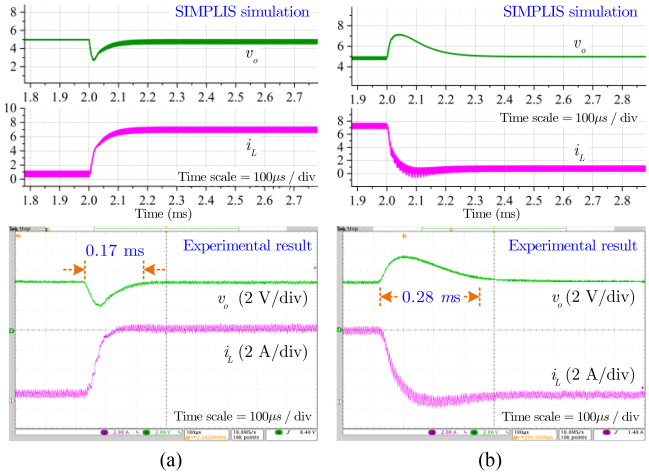
note that the SIMPLIS simulation and experimental results are in close agreement, as highlighted in Table IV. Slight deviations may be attributed to the unmodeled dynamics in the experimental prototype, which are not captured in the SIMPLIS simulation. Overall, the recovery time using the proposed DTSF design is improved by approximately fourfold compared to that obtained using the DTOF design.

C. Comparative Study of Load Transient Performance

Fig. 22 shows the experimental load transient performance using the DTOF technique for step changes in load current from 0.5 A to 5 A and back at 5 V constant output. Following the steps in Section III, the digital PI controller gains are obtained under the proposed DTSF design approach, and the step-up load transient performance comparison is summarized in Table V. The table shows that the recovery time using the proposed DTSF technique can be improved by nearly 2.7 times with no additional voltage and current overshoots compared to that obtained using the DTOF technique. A similar improvement is achieved during the step-down load transient, as shown in Fig. 23, where the proposed DTSF approach can reduce the settling time by twofold, and decrease the voltage overshoot and current undershoot by 0.7 V and 1.5 A, respectively.

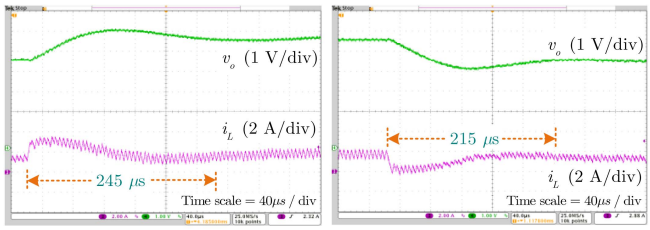
D. Step Reference Transient Under CCL—Comparative Study

A programmable dc electronic load (Chroma 6312 A) is used as a CCL of $I_{\rm con} = 1$ A for an experimental boost converter under the DCMC technique. For step changes in $v_{\rm ref}$ from 4.5 V to 5.5 V, and back, Fig. 24 shows that the DTOF design method results in recovery time of 245 μs during step-up and 215 μs during step-down. This can be improved by nearly three-fold (settling time of 75 μs during step-up and 82 μs during step-down),



(a) (b)

Fig. 23. Experimental transient performance using the DTSF design method for a step change in load current from 0.5 A to 5 A, and back to 0.5 A; Verifying consistency using SIMPLIS simulation and experimental results. (a) Step-up load transient. (b) Step-down load transient.



(a) (b)

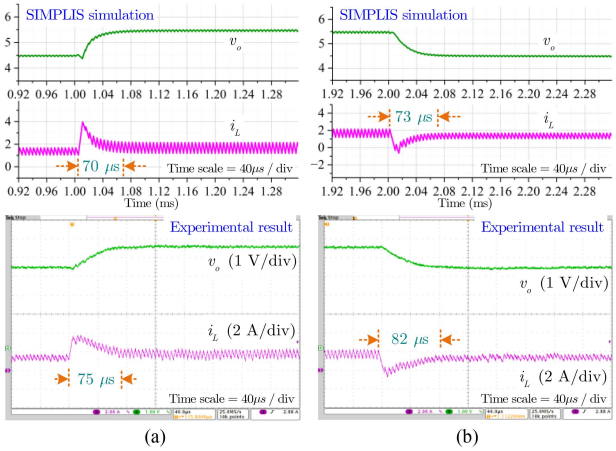
Fig. 24. Experimental reference transient response of the DCMC boost converter under the DTOF design approach for a step change in $v_{\rm ref}$ from 4.5 V to 5.5 V, and back with a constant load current of $I_{\rm con} = 1$ A. (a) Step-up reference transient. (b) Step-down reference transient.

along with the improved closed-loop damping, by enhancing the effective closed-loop BW using the DTSF design, as shown in Fig. 25. Also, the SIMPLIS simulation and experimental results are in relatively close agreement, as shown in Table IV.

In summary, the tradeoff between achieving the desired 60° PM and high closed-loop BW can be executed by implementing the proposed DTSF design technique, which can improve the transient performance and damping of a DCMC boost converter in comparison with its DTOF design counterpart. Also, the proposed technique allows the designers to realize advanced control techniques to optimize the converter's dynamic performance in the presence of constraints on voltage/current overshoot/undershoot even at higher BW, irrespective of the type of load, which is a similar perspective of designing the digital controller based on the linear quadratic regulator approach, Lyapunov approach, and so on. In addition, the proposed controller design algorithm additionally provides opportunities for real-time digital controller tuning, which will be the future perspective for designing the controller for an extensive spectrum of operating circumstances.

TABLE V
COMPARATIVE TRANSIENT PERFORMANCE: $\Delta v_{\rm ov}$, $\Delta v_{\rm un}$, AND Δi ARE THE VOLTAGE OVERSHOOT, VOLTAGE UNDERSHOOT, AND CURRENT OVERSHOOT

Design approaches	step-up reference transient performance comparison				step-up load transient performance comparison				
	Digital PI controller gains	settling time	$\Delta v_{\rm ov}$	Δi	Digital PI controller gains	settling time	$\Delta v_{\rm un}$	$\Delta v_{\rm ov}$	Δi
DTOF	$k_{\rm pd} = 4.56$, $k_{\rm id} = 0.56$	250 μs	0.58 V	3.2 A	$k_{\rm pd} = 1.96$, $k_{\rm id} = 0.438$	0.46 ms	2.4 V	0.6 V	2 A
DTSF	$k_{\rm pd} = 4.06$, $k_{\rm id} = 0.176$	58 μs	0 V	2.1 A	$k_{\rm pd} = 2.56$, $k_{\rm id} = 0.31$	0.17 ms	2 V	0 V	0 A



(a) (b)

Fig. 25. Transient performance using the proposed DTSF design method for a step change in $v_{\rm ref}$ from 4.5 V to 5.5 V, and back at 1 A CCL; Verifying consistency using SIMPLIS simulation and experimental results. (a) Step-up reference transient. (b) Step-down reference transient.

VI. CONCLUSION

In this article, a novel framework for designing the PI controller using a discrete-time state feedback (DTSF) approach in a DCMC boost converter was presented, and the design steps were summarized while the converter driving constant resistive load, CCL, and CPL. It was demonstrated analytically, as well as through simulation and experimental case studies under different types of dc loads that the DTSF design approach enables flexibility in the placement of closed-loop poles to achieve a superior PM for a higher control BW in comparison with its DTOF design counterpart. In addition, the proposed design approach provides additional freedom in improving the converter's dynamic performance in the presence of constraints on voltage/current overshoot/undershoot, even at higher BW. The effect of parameter variations and input voltage disturbances was found to be insignificant on the transient performances. The proposed controller design algorithm can be extended to other dc–dc converters in order to achieve high BW with improved dynamic performance.

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