Design of GaN Switching Power IC With Auto-Phase-Aligned EMI Adaptive Self-Cancellation and BER-Conscious Spread Spectrum Modulation

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***Abstract*—To address mounting electromagnetic interference (EMI) challenges in electric vehicle autonomous driving applications, this article develops an on-chip EMI adaptive self-cancellation (ASC) technique, which stays effective in varying operation conditions. It incorporates an auto-phase-aligned control mechanism to significantly enhance the effectiveness of the ASC technique. Meanwhile, to improve high-frequency EMI suppression, a spread-spectrum modulation (SSM) technique works harmoniously with the ASC to modulate the switching frequency f_{SW}, adaptive to operation conditions. The maximum spread range Δf_{SW} of the SSM is actively regulated to strictly limit the bit error rate (BER) in the communication system for safety and security. To validate the effectiveness of this article, a switching power converter IC prototype was implemented on a 180-nm BCD process, with a chip area of 1.3 mm^2. The converter is purposely designed using GaN power switches and operating at a nominal f_{SW} of 2.2 MHz, imposing more severe *di/dt* and *dv/dt* challenges than classic kilohertz-level silicon counterparts. Experimental results prove that the on-chip ASC technique achieves adaptive ripple self-cancellation in response to 150% input and 200% output dynamic voltage changes from the respective nominal levels. The ASC technique alone achieves a maximum EMI reduction of 9.5 dB. In collaboration with the BER-conscious SSM technique, a total EMI reduction of 16.5 dB is achieved at the nominal f_{SW}, satisfying stringent automotive CISPR 25 Class 5 standard.**

***Index Terms*—Adaptive self-cancellation (ASC), electromagnetic interference (EMI), gallium nitride (GaN) switching power converter, spread-spectrum modulation (SSM).**

I. Introduction

Today automotive industry is experiencing a significant paradigm shift towards autonomous driving in electrically powered and connected vehicles, demanding an ever-increasing number of sophisticated electronic components and modules within limited vehicle space. With unprecedentedly heightened levels of system integration and complexity, automotive manufacturers face severe electromagnetic interference (EMI) reliability challenges [1], [2], [3]. Excessive EMI noise generated within modern vehicles could compromise signal integrity, leading to potentially catastrophic system failures and malfunctions. In particular, autonomous driving systems require intricate communication between sensors and control units. For example, in popular power over coaxial (PoC) applications shown in Fig. 1, the coax cable is used for both power delivery and data communication [4]. EMI coupled into communication channels presents a significant threat to communication safety [5], [6]. Furthermore, considering vehicle space limitation, power delivery circuits must have high power density to comply with spatial constraints. This necessitates operating these circuits at higher frequencies, facilitating the miniaturization of bulky power passive components. Unfortunately, the resulting fast switching actions elevate the slew rates of *dv/dt* and *di/dt* significantly, further deteriorating system reliability [7], [8].

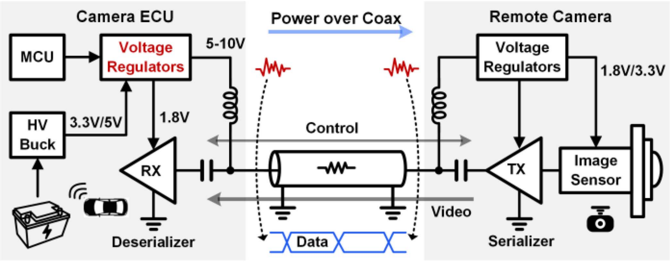

Fig. 1. Block diagram of autonomous driving power management unit using power over coaxial (PoC) cable.

Historically, passive EMI filters have been adopted to suppress EMI. However, their usually bulky power passives demand considerable system volume, thereby compromising power density significantly. To minimize the footprint of passive EMI filters, active EMI filters (AEFs) such as [9], [10], [11], are also reported. Such an AEF often incorporates a sensing mechanism to monitor the input noise ripple, then employs an operational amplifier to inject counteracting signals to cancel out the EMI noise accordingly [11]. However, to suppress EMI noise effectively, the amplifier must output adequate power, leading to sizable efficiency degradation. In addition, sophisticated compensation networks must be designed to maintain loop stability. Very often,

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finite bandwidths of the noise detection circuit and the amplifier limit the EMI suppression ability at high frequency range. This limitation becomes particularly pronounced in today's wide bandgap power circuits, where high frequency is a distinct merit to retain high power density and low cost. To overcome such, a switched AEF was reported [12], which brilliantly introduces an auxiliary converter to inject an ac current, neutralizing the input supply current ripple ($\Delta I_{\mathrm{SUPPLY}}$). This auxiliary converter shares the control signal with the main power converter, thereby eliminating the need for loop compensation. However, it lacks active control mechanism between the switched filter and the main power converter, potentially leading to imprecise ripple cancellation due to operation condition changes, which could deteriorate drastically at high f_{SW}. Alternative ripple cancellation techniques [13], [14] employ a coupled inductor and eliminate the need for active control circuit. However, their effectiveness of EMI suppression is largely limited by leakage inductance of the coupled inductor. On the other hand, instead of focusing on power passives, a mixed-signal ripple canceller [15] reduces the output ripples using an on-chip triangular waveform generator. However, power efficiency can be compromised significantly.

In addition to hardware-based EMI filter solutions, software-based spread spectrum modulation (SSM) techniques have also been employed for EMI reduction [11], [16], [17]. Because a technique as such does not require additional passive components, it is highly appealing in high power density applications. An effective SSM technique spreads noise into a broader frequency range Δf_{SW} to lower the spurious EMI peaks. Hence, its effectiveness highly depends on the Δf_{SW} [16]. A Δf^3 SSM approach [18] dynamically adjusts the Δf_{SW} based on operation conditions, thereby optimizing EMI performance. However, studies found that large Δf_{SW} will increase the bit error rate (BER) in communication systems [6], [19], [20], thus could potentially reduce signal integrity. Therefore, Δf_{SW} should be strategically constrained within a limited range to balance effective EMI mitigation and reliable communication.

In addition, active gate driving techniques are also widely applied to reduce EMI by adjusting *dv/dt* and *di/dt* [21], [22]. While such method is effective in addressing high-frequency EMI, their efficacy at the fundamental switching frequency remains constrained. Moreover, the overall EMI performance, particularly radiated EMI, is strongly influenced by the PCB layout. Minimizing parasitic inductance in both the power and gate drive loops is essential for reducing voltage and current ringing, thereby suppressing radiated EMI [23].

To address the aforementioned challenges, this article introduces an EMI adaptive self-cancellation (ASC) technique and a BER-conscious SSM approach. To improve power density and accommodate varying conditions in power converters, the on-chip EMI ASC technique facilitates adaptive EMI suppression, with an integrated autophase-aligned control mechanism for precise ripple cancellation. On the other hand, a BER-conscious SSM is employed to work cohesively with the ASC to achieve EMI attenuation across a wide frequency range. Particularly, the spread range Δf_{SW} is actively controlled within a specific range for communication safety.

The rest of this article is organized as follows. Section II introduces the system architecture and operation principle of the ASC EMI control and the BER-conscious SSM. Section III presents corresponding circuit implementation methods. To validate our design approaches, experimental verification is presented in Section IV. Finally, Section V concludes this article.

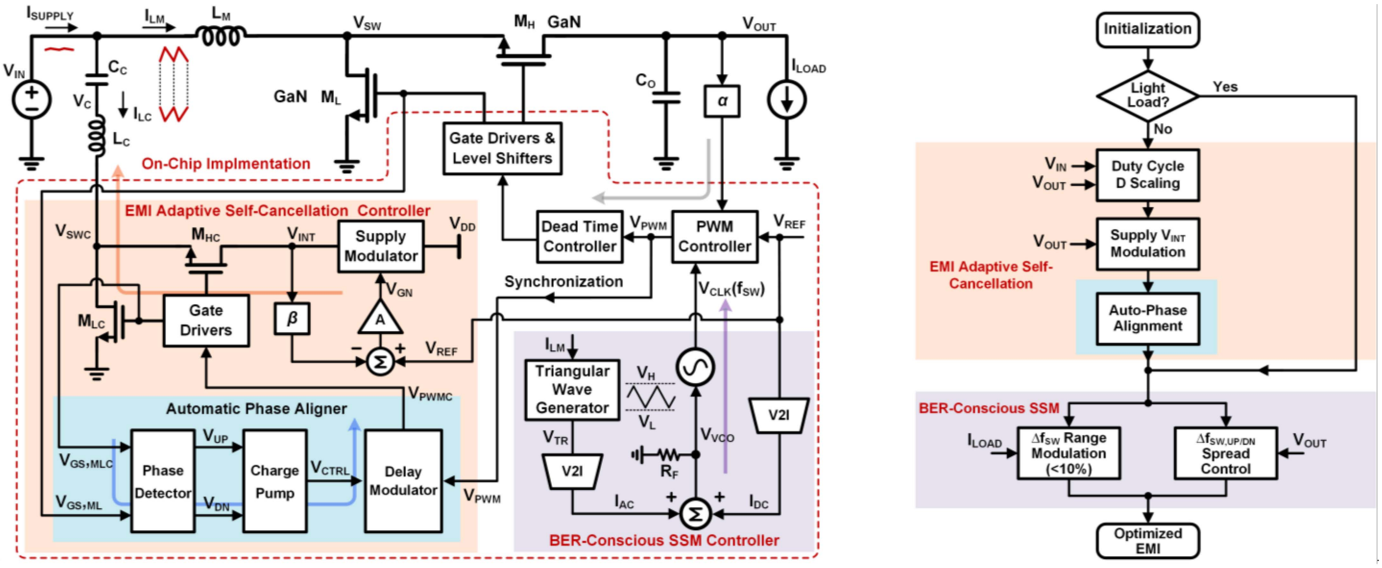
II. SYSTEM ARCHITECTURE AND CONTROL SCHEMES

A. System Overview

In order to demonstrate the proposed EMI ASC control and the BER-conscious SSM technique, a GaN-based boost switching power converter is presented in Fig. 2. Compared to silicon counterparts, GaN-based power circuits face heightened EMI challenges due to significantly more drastic *di/dt* and *dv/dt* switching transients. Hence, the GaN-based implementation of this article offers more stringent test on the effectiveness of the proposed techniques. As illustrated in Fig. 2(a), the converter primarily consists of four key modules, in addition to the power stage, namely a PWM feedback controller, an EMI ASC controller, an automatic phase aligner, and a BER-conscious SSM controller. The PWM feedback controller fulfills the conventional closed-loop voltage regulation. To achieve the ASC, a secondary power stage is built [12], including on-chip silicon power switches M_{LC} and M_{HC}. In conjunction with an inductor L_C, the stage generates an ac current I_{LC} to the input of the main power stage via a capacitor C_C. By properly switching M_{LC} and M_{HC} and adjusting V_{INT}, the current ripple in I_{LC} can be made in anti-phase with that in I_{LM} while maintaining the same magnitude. Critically, to reinforce accurate ripple cancellation, the automatic phase aligner ensures precise synchronization of switching actions between the main boost converter and the ASC stage. Meanwhile, to further reduce EMI especially at high frequency and address communication safety, the BER-conscious SSM module optimizes the f_{SW} modulation to execute EMI suppression, while avoiding BER-degradation.

Fig. 2(b) illustrates the operation flow chart in response to operation condition changes. As V_{IN} or V_{OUT} varies, the duty cycle of the ASC stage is synchronized with the main converter. Additionally, changes in V_{OUT} modulate the input voltage V_{INT} of the ASC stage. Furthermore, the autophase alignment is performed to enhance the ASC against process variation. These corresponding adjustments ensure adaptive ripple cancellation across various operation conditions. To mitigate the efficiency penalty, the ASC module is disabled at light load. On the other hand, the proposed BER-conscious SSM technique can also respond to condition changes. The frequency spread direction $\Delta f_{\mathrm{SW,UP/DN}}$ and spread range Δf_{SW} are adjusted based on I_{LOAD} and V_{OUT}. Δf_{SW} is continuously monitored and restricted within 10% of the fundamental switching frequency f_{sw0} to prevent any adverse impact on BER for communication safety. This article allows the EMI ASC control and SSM control work seamlessly and jointly for EMI reduction across a wide range of operation conditions and frequencies.

In the following sections, details of the proposed operation techniques are explained in due course.



(a) (b)

Fig. 2. Proposed GaN power converter with EMI ASC control and BER-conscious SSM: (a) block diagram, and (b) system-level operation flow chart.

B. EMI Adaptive Self-Cancellation

Conducted EMI in power circuits arises from the frequent switching actions, resulting in voltage and current ripples at the input side [24]. For a boost converter, the input current is the continuous inductor current I_{LM}. Therefore, the input supply current ripple $\Delta I_{\mathrm{SUPPLY}}$ equals the current ripple of I_{LM}, which can be expressed as

$$\Delta\, I_{LM} = \frac{D\,(1-D)\,V_{\mathrm{OUT}}}{L_M f_{SW}} \tag{1}$$

where D is the duty ratio of the switch M_L. To suppress the conducted EMI, it is imperative to generate a counteractive current that cancels the current ripple ΔI_{LM}. Consequently, the implementation of a complementary switching mechanism is adopted to induce an inverse current slope, facilitating the ripple cancellation.

As shown in Fig. 2(a), a half-bridge power stage comprising M_{LC} and M_{HC} is connected to the input of the boost converter via L_M and C_C, which builds an auxiliary buck converter with an input voltage V_{INT}. By synchronizing the control signal of this auxiliary converter to the PWM signal of the boost converter, complementary switching can be achieved [12]. As shown in Fig. 3(a), when M_L turns on, I_{LM} in the boost converter ramps up at a slope of V_{IN}/L_M. To cancel out the positive inductor current slope, I_{LC} in the auxiliary converter must have a negative slope. Hence, during the on-time of M_L, M_{HC} turns ON while M_{LC} is OFF. The compensated current I_{LC} ramps down with a slope of $(V_C - V_{\mathrm{INT}})/L_C$, which will cancel out the ripple value of ΔI_{LM}. V_C is the node voltage between L_C and C_C. Note that the positive direction of I_{LC} is defined from the input towards the switching node V_{SWC}. Similarly, during the on-time of M_H, M_{LC} turns on to generate the counteracting current slope. Due to the complementary switching operation, the duty cycle D of M_L in the boost converter is copied to M_{HC} in the auxiliary converter. Consequently, V_C is computed as DV_{INT} and the current ripple of L_C is described as

$$\Delta\, I_{LC} = \frac{D\,(1-D)\,V_{\mathrm{INT}}}{L_C f_{\mathrm{SW}}}\,. \tag{2}$$

Note that there is no dc current in I_{LC}. For effective ripple self-cancellation, ΔI_{LC} should be equivalent to ΔI_{LM}. Therefore, solving (1) and (2) will result in

$$\frac{V_{\mathrm{INT}}}{V_{\mathrm{OUT}}} = \frac{L_C}{L_M}\,. \tag{3}$$

By properly adjusting V_{INT} and the inductance ratio between L_C and L_M, the input ripple-free condition can be realized theoretically.

Note that the self-cancellation condition remains unaffected by V_{IN} of the boost converter, offering a notable advantage, especially considering the potential fluctuations in automotive battery input voltage due to load dumps and cold cranks [2]. For example, if V_{IN} increases during a load dump, D will be reduced by the feedback controller to maintain output regulation and thus ΔI_{LM} decreases, as shown in Fig. 3(a). Due to the synchronized operation between the auxiliary converter and the boost converter, ΔI_{LC} is reduced to match ΔI_{LM} by adjusting D proportionally, resulting in ripple self-cancellation.

On the other hand, the condition described in (3) is dependent on V_{OUT}, limiting the effectiveness of self-cancellation under V_{OUT} change. The remote cameras in automotive applications are powered over coaxial cables, which might need adjustable V_{OUT} in boost converters [4]. Additionally, LED drivers demand output current regulation rather than voltage, leading to a wide range of V_{OUT} [2]. As indicated in (3), to maintain a ripple-free input current under V_{OUT} change, V_{INT} must be scaled based on V_{OUT}. Consequently, a supply voltage modulator is proposed to adjust V_{INT} based on V_{OUT}. This modulator is powered directly by the input source V_{DD} of gate drivers, thus obviating

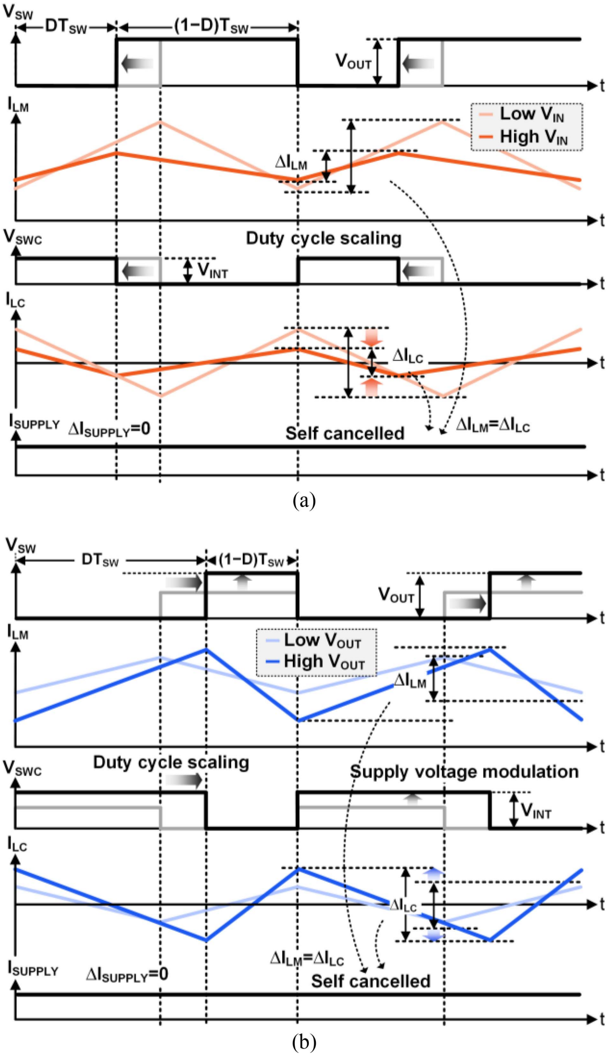


Fig. 3. Operation waveforms of proposed EMI ASC technique under (a) V_{IN} change, and (b) V_{OUT} change.

the requirement for an auxiliary power supply. As depicted in Fig. 2(a), the reference voltage V_{REF} in the PWM controller is fed into the supply modulator. V_{INT} is then scaled down and compared with V_{REF} to generate the control voltage V_{GN}, which further adjusts the resistance of the supply modulator for V_{INT} regulation. As shown in Fig. 3(b), an increase in V_{OUT} results in a corresponding increase in ΔI_{LM}. To counteract the ripple change, V_{INT} is elevated by the supply modulator proportionally. With the coordination of the duty ratio scaling and the supply voltage modulation, ΔI_{LC} is adjusted to match the magnitude of ΔI_{LM}, achieving ripple self-cancellation for EMI suppression.

Given that α and β are the scaling in the feedback networks of the converter and the supply modulator, respectively, the relationship between V_{INT} and V_{OUT} can be expressed as

$$\frac{V_{\mathrm{INT}}}{V_{\mathrm{OUT}}} = \frac{\alpha}{\beta}\,. \tag{4}$$

Combining (3) and (4), the condition for achieving the ASC can be updated as

$$\frac{L_C}{L_M} = \frac{\alpha}{\beta}\,. \tag{5}$$

Therefore, by carefully choosing the appropriate inductance and the feedback networks, the current ripple of the converter can be eliminated theoretically, regardless of different V_{IN} and V_{OUT} conditions. Furthermore, the voltage scaling ratios α and β offer considerable design flexibility in choosing L_C and L_M. The α and β are achieved by resistor dividers on circuit level, which are detailed in Section III-A. Furthermore, although the inductance mismatch between L_C and L_M can lead to imperfect cancellation, the impact can be minimized by calibrating the feedback factor β in the resistor divider of the ASC stage.

It should be noted that, since the ASC technique requires the use of an inductive ac current to cancel the input inductor current ripple, it can be directly applied to the topologies where an inductor is employed at the input, such as boost converters, SEPIC converters [13] and Kappa buck converters [24].

C. Autophase-Aligned Control

The switching actions between the auxiliary converter and the primary power stage must be synchronized to ensure accurate ripple cancellation. However, directly feeding the PWM signal to the ASC stage without delay compensation can lead to delay mismatch that undermines the effectiveness of ripple self-cancellation. As shown in Fig. 2(a), the power switches M_L and M_H are subjected to significantly higher voltage and current stresses compared to M_{LC} and M_{HC}, necessitating larger transistor size and consequently larger gate capacitance. The gate drivers for M_L and M_H must be designed to have strong peak current driving capability, which introduces longer propagation delays. Moreover, level shifters are required to provide high voltage isolation and voltage level conversion, which contributes additional propagation delay. As a result, the signal path from V_{PWM} to $V_{\mathrm{GS,ML}}$ experiences more delay compared to that from V_{PWM} to $V_{\mathrm{GS,MLC}}$, resulting in misaligned switching operation, as depicted in Fig. 4. Furthermore, the propagation delays of gate drivers and level shifters are sensitive to both process and temperature variations. The delay mismatches caused by these factors can further degrade the phase alignment between the primary power stage and the ASC stage, jeopardizing the effectiveness of ripple self-cancellation.

To overcome this challenge, an automatic phase alignment mechanism is proposed, as shown in Fig. 2(a). A delay modulator is introduced between V_{PWM} and the gate drivers of M_{LC} and M_{HC}, providing delay compensation to synchronize the switching actions precisely. The mechanism involves a phase detector that measures the delay discrepancy between $V_{\mathrm{GS,ML}}$ and $V_{\mathrm{GS,MLC}}$. Consequently, the difference in pulse width between the phase detector's output signal V_{UP} and V_{DN} indicates the delay error that needs to be compensated. Applying the pulse signals to a charge pump, a control voltage V_{CTRL} can be generated, which further determines the adjustable delay time in the delay modulator. Therefore, the propagation delay from

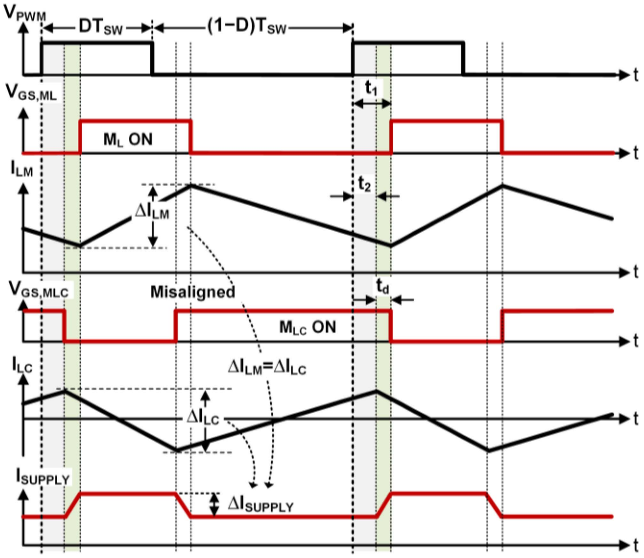
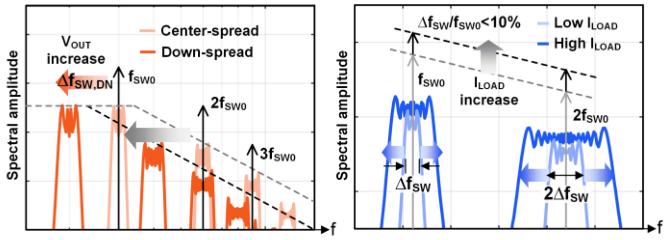


Fig. 4. Challenges of ripple self-cancellation technique due to delay mismatch.



(a) (b)

Fig. 5. Frequency domain illustration of (a) $\Delta f_{\mathrm{SW,UP/DN}}$ spread control, and (b) Δf_{SW} range modulation of proposed BER-conscious SSM.

V_{PWM} to $V_{\mathrm{PWM}\,C}$ can be modulated adaptively until the precise alignment between $V_{\mathrm{GS,ML}}$ and $V_{\mathrm{GS,MLC}}$ is achieved.

D. BER-Conscious SSM

Due to the parasitic effects of passive components, the effectiveness of ripple self-cancellation is limited [12]. Consequently, the proposed EMI ASC technique becomes less effective against high-frequency EMI. To mitigate this, an SSM control is employed to accomplish EMI reduction across a wide frequency range. The triangular modulation profile is chosen for the SSM due to its low design overhead and effective EMI suppression capabilitiy. While the Hershey-Kiss modulation profile provides maximum EMI reduction compared to sinusoidal and triangular profiles [16], it requires highly complex circuitry for system implementation, leading to higher cost and power consumption.

As EMI originates from the discontinuous switches' voltage (V_{DS}) and current (I_{DS}), variations in V_{OUT} and I_{LOAD} in a boost converter can greatly influence the EMI performance [18]. To accommodate V_{OUT} change, a $\Delta f_{\mathrm{SW,UP/DN}}$ spread control scheme is proposed to adjust the frequency spreading direction. As shown in Fig. 5(a), when V_{OUT} increases, f_{SW} is modulated downward, shifting EMI into lower frequency range.

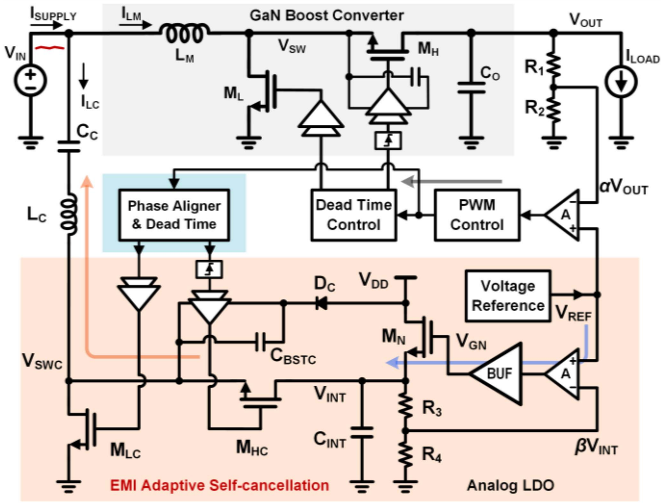


Fig. 6. Circuit schematic of proposed EMI ASC controller.

Furthermore, a Δf_{SW} range control scheme is proposed to modulate Δf_{SW} in response to variations in the load current. When I_{LOAD} increases, EMI noise level increases at fixed f_{SW} and its harmonics. To compensate for such, frequency modulation range Δf_{SW} can be widened to spread EMI energy over a broader spectrum for further reduced peak EMI [see Fig. 5(b)]. However, a large Δf_{SW} can potentially increase BER [6]. Particularly, study shows that BER rises notably when the spreading ratio between the spread frequency range Δf_{SW} and the center switching frequency f_{SW0} exceeds 15% [19]. Therefore, the proposed SSM actively limits the envelope of triangular profile ensure that $\Delta f_{\mathrm{SW}}/f_{\mathrm{SW0}}$ remains less than 10% for communication safety. Moreover, a modulation frequency f_M envelope tracking scheme is proposed to monitor the frequency of triangular profile and adjust its slew rate accordingly, regulating modulation frequency at 20 kHz to maximize EMI reduction, while preventing audible noise [18].

III. CIRCUIT IMPLEMENTATION

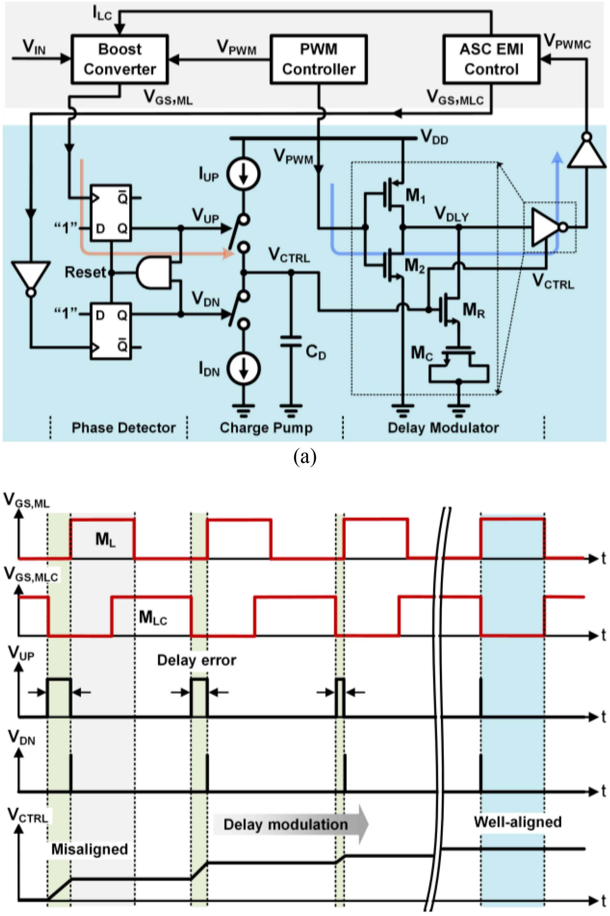
A. EMI Adaptive Self-Cancellation Controller

Fig. 6 shows the circuit implementation of the proposed EMI ASC control scheme. For the power switch selections, the maximum voltage stress of M_{LC} and M_{HC} is the supply voltage V_{DD} of the gate drivers. Therefore, M_{LC} and M_{HC} are designed using on-chip low-voltage N-type power transistors for high power density and low switching loss. Note that both switches can be achieved with zero-voltage switching due to the bidirectional inductor current I_{LC}. To effectively drive the high-side transistor M_{HC}, a bootstrap circuit is powered by V_{DD} via a Schottky diode D_C to charge the capacitor C_{BSTZ}, providing a floating supply rail for the high-side gate driver. Furthermore, an N-type low-voltage transistor M_N is placed between V_{DD} and V_{INT}, serving as the power transistor of a low dropout (LDO) voltage regulator for V_{INT} regulation. Specifically, if V_{OUT} rises due to the elevated V_{REF}, the difference between V_{REF} and the feedback voltage $\beta V_{\rm INT}$ increases. This discrepancy is further amplified by the error amplifier and is then passed through a voltage buffer, resulting in a higher gate voltage V_{GN} to drive M_N. Consequently, the ON-resistance of M_N decreases, allowing more current to flow from V_{DD} to charge the capacitor $C_{\rm INT}$. As a result, $V_{\rm INT}$ increases following the rise of $V_{\rm OUT}$. Such a negative feedback loop ensures that $V_{\rm INT}$ is regulated at $V_{\rm REF}/\beta$, where β equals $R_4/(R_3+R_4)$. Similarly, the scaling factor α for V_{OUT} is determined by $R_2/(R_1+R_2)$.

In selecting passive components, the absence of a dc current in I_{LC} allows for the use of a chip-scale inductor, contributing to improved power density. By appropriately determining the inductance values and scaling factors to meet the condition described in (5), ripple self-cancellation can be realized automatically. And a multilayer ceramic chip capacitor is chosen for C_C. The small footprint of L_C and C_C, combined with on-chip power switches M_{LC} and M_{HC}, ensures that the proposed ASC control exhibits little overhead on power density. Moreover, the ASC stage shares the same power source V_{DD} (5 V in this article) with the gate drivers of the boost converter, eliminating the need for an additional designated power supply. In the event of V_{DD} transient, the analog LDO regulates $V_{\rm INT}$, ensuring that ripple cancellation remains unaffected.

B. Automatic Phase Aligner

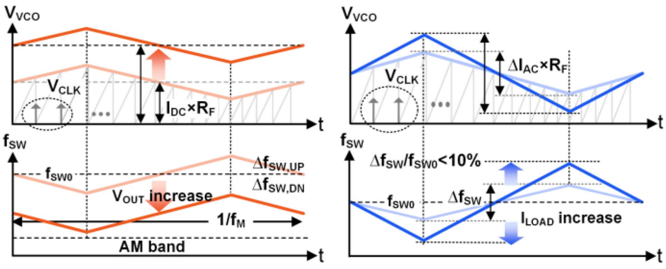
Fig. 7(a) shows the circuit schematic of the proposed delay-locked loop-based automatic phase aligner. To monitor the phase alignment of switching actions between the boost converter and the auxiliary converter, $V_{\rm GS,ML}$ and $V_{\rm GS,MLC}$ are analyzed by a phase detector formed by D flip-flops. Due to the complementary logic between these two signals, $V_{\rm GS,MLC}$ is fed into the phase detector after an inverter. Note that the phase detector should avoid using V_{GS} of the high-side switch as feedback signal, since it requires level shifting to the logic circuits, introducing extra delay. If the falling edge of $V_{\rm GS,MLC}$ precedes the rising edge of $V_{\rm GS,ML}$, as shown in Fig. 7(b), the delay error is translated into the pulse width of $V_{\rm UP}$, which charges the capacitor C_D. As a result, the control voltage $V_{\rm CTRL}$ increases and extends the delay from $V_{\rm PMM}$ to $V_{{\rm PWM}C}$ by adjusting the time constant in the delay modulator. Therefore, the phase difference between $V_{\rm GS,ML}$ and $V_{\rm GS,MLC}$ can be reduced. After several switching cycles, precise alignment of the switching actions can be achieved. A delay chain is implemented to compensate for the worst-case propagation delay mismatch. As $V_{\rm CTRL}$ gets refreshed in each switching cycle, the impact of the transistors' leakage current at high temperature is negligible.



(a)

(b)

Fig. 7. Proposed automatic phase aligner: (a) circuit schematic, and (b) operation timing diagram.



(a)

(b)

Fig. 8. Operation waveforms of (a) $\Delta f_{\rm SW,UP/DN}$ spread control, and (b) $\Delta f_{\rm SW}$ range modulation.

C. BER-Conscious SSM Controller

Fig. 8 shows the operation waveforms of BER-conscious adaptive SSM control. The detailed circuit implementation can be found in [18]. As shown in Fig. 2(a), the voltage-controller oscillator (VCO) is employed to dynamically adjust the switching frequency $f_{\rm SW}$ of the boost converter. The clock frequency of VCO is designed to be inversely proportional to the input voltage $V_{\rm VCO}$. The spread direction $\Delta f_{\rm SW,UP/DN}$ and spread range $\Delta f_{\rm SW}$ are determined by a dc current $I_{\rm DC}$ and an ac current $I_{\rm AC}$, respectively. In response to $V_{\rm OUT}$ change, $I_{\rm DC}$ goes up to raise the dc level of $V_{\rm VCO}$. Consequently, the ramp signal required longer time to reach $V_{\rm VCO}$ before being reset, as illustrated in Fig. 8(a). This results in a downward spread modulation of $f_{\rm SW}$ into lower frequency spectrum. On the other hand, when $I_{\rm LOAD}$ increases, the triangular waveform generator produces a wider envelop, which is converted to an ac current into the resistor R_F, as shown in Fig. 8(b). Therefore, a wider envelope on $V_{\rm VCO}$ can be achieved for larger $\Delta f_{\rm SW}$ spread range.

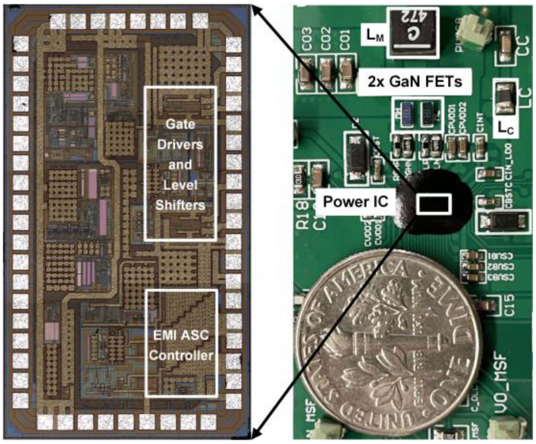
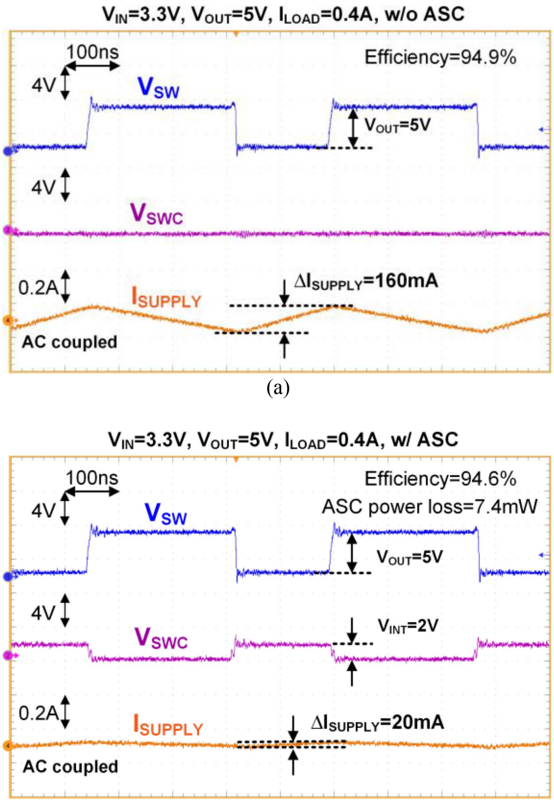


Fig. 9. Photographs of IC die and test PCB.



(a)

(b)

Fig. 10. Measured switching node and input current at $V_{\rm IN}$ = 3.3 V, $V_{\rm OUT}$ = 5 V, and $I_{\rm LOAD}$ = 0.4 A: (a) without EMI ASC control, and (b) with EMI ASC control.

Meanwhile, to address the potential BER degradation, the maximum envelope is constrained within the triangular waveform generator to ensure that $\Delta f_{\rm SW}/f_{\rm SW0}$ does not exceed 10%. To prevent the modulation frequency f_M from entering audible noise band, an f_M envelope tracking circuit is also implemented to adjust the slew rate in triangular profile in order to regulate f_M at 20 kHz [18]. This enables optimum EMI suppression while simultaneously preventing audible noise.

IV. EXPERIMENTAL VERIFICATION

An IC prototype of this design was fabricated in a 180-nm BCD process [25], with a die area of 1.3 mm^2, as shown in Fig. 9. Enhancement mode GaN transistors are utilized for power switches for M_L and M_H in the boost converter, while M_{LC} and M_{HC} are implemented by on-chip low-voltage transistors. Both on-chip 5V power switches are designed with an on-resistance of 140 mΩ, occupying a die area of 0.1 mm^2. The total silicon area of the ASC technique implementation is 0.16 mm^2, accounting for 12.3% of the total chip area. The boost converter power stage is capable of delivering an output voltage ranging from 5 to 24 V with a maximum output power of 5 W. Targeting at autonomous driving PoC applications, the prototype accommodates an input voltage of 3.3 to 5 V and an output voltage of 5 to 10 V [2], [4]. The inductors L_M and L_C are chosen as 3.3 and 1.2 μH, respectively.

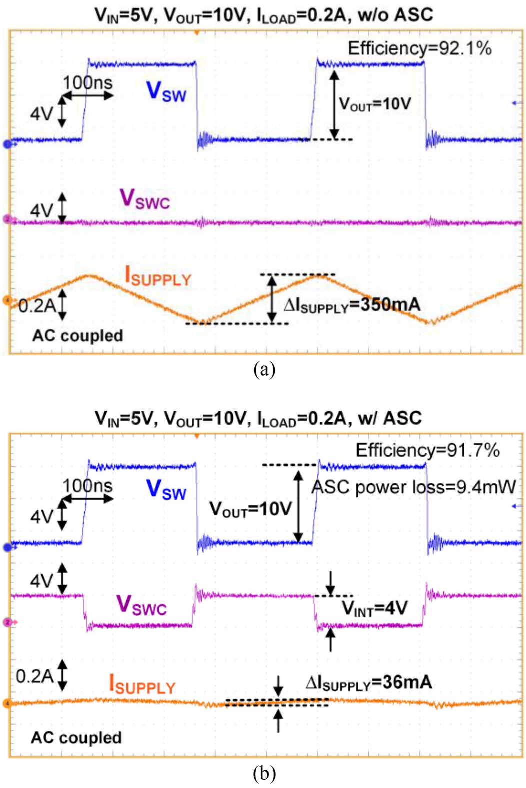
To validate the ripple self-cancellation technique, Fig. 10 shows the comparison waveforms of the switching node voltage and input current. As shown in Fig. 10(a), the input current ripple is 160 mA at a $f_{\rm SW}$ of 2.2 MHz without self-cancellation. Thanks to the ASC technique, the input current ripples are reduced by eight times in Fig. 10(b), from 160 to 20 mA. The power comsumption by the ASC is 7.4 mW, accouting for a 0.3% power efficiency penalty at an output power of 2 W.

As $V_{\rm IN}$ increases by 1.5 times and $V_{\rm OUT}$ doubles in Fig. 11(a), $\Delta I_{\rm SUPPLY}$ significantly increases to 350 mA. To accommodate such condition changes, the proposed ASC technique adjusts the duty ratio and the supply voltage $V_{\rm INT}$ correspondingly, as depicted in Fig. 11(b). Specifically, in response to the two times $V_{\rm OUT}$ change, $V_{\rm INT}$ is scaled from 2 to 4 V to generate the counteracting signal, resulting in an input ripple of 36 mA. Due to the larger current ripple required for self-cancellation, the power loss of the ASC increases from 7.4 to 9.4 mW at the same output power level of 2 W, leading to an efficiency penalty of 0.4%.

To verify the effectiveness of the proposed autophase aligned control, Fig. 12(a) shows the ripple cancellation waveforms without this technique. A delay mismatch of 20 ns between the switching actions results in a $\Delta I_{\rm SUPPLY}$ of 56 mA, despite I_{LM} and I_{LC} having an equal magnitude of current ripple. In comparison, $\Delta I_{\rm SUPPLY}$ can be reduced to 20 mA thanks to the automatic phase alignment, improving the ripple cancellation by 2.8 times, as shown in Fig. 12(b).

To validate the integration of the ASC and SSM techniques, Fig. 13 shows the measured $V_{\rm SW}$ and $I_{\rm SUPPLY}$ waveforms with fast requisition mode enabled in the oscilloscope. With the continuous variation of $f_{\rm SW}$, the ripple cancellation technique still achieves a $\Delta I_{\rm SUPPLY}$ of 30 mA, verifying that ASC and SSM can work seamlessly.

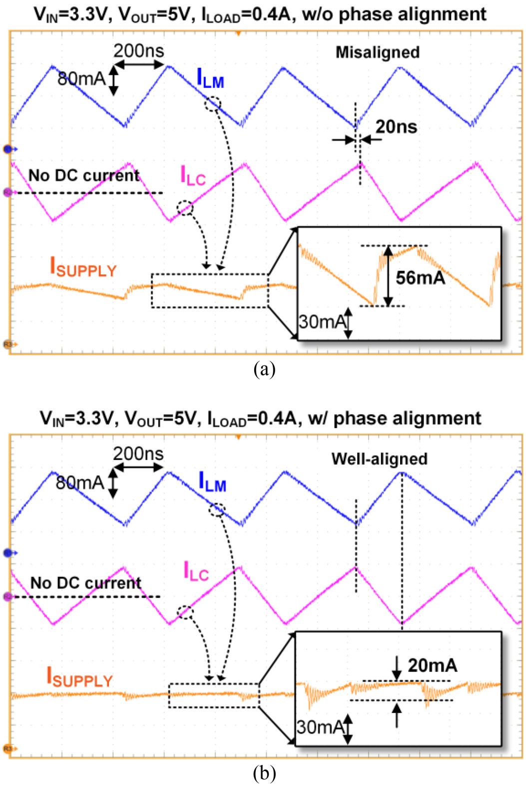
The conducted EMI performance is also measured to validate the EMI reduction resulting from ripple self-cancellation. A line impedance stabilization network is inserted between the input power source and the boost converter, providing a 50 Ω impedance for the spectrum analyzer. Fig. 14 depicts the measured EMI performance from 1 to 30 MHz with a resolution



(a)

(b)

Fig. 11. Measured switching node and input current at $V_{\rm IN}=5$ V, $V_{\rm OUT}=10$ V, and $I_{\rm LOAD}=0.2$ A: (a) without EMI ASC control, and (b) with EMI ASC control.



(a)

(b)

Fig. 12. Measured ripple cancellation waveforms: (a) without delay compensation, and (b) with autophase-aligned control.

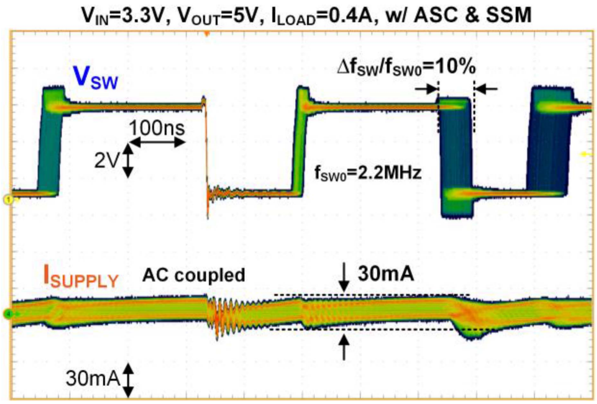


Fig. 13. Measured $V_{\rm SW}$ and $I_{\rm SUPPLY}$ under both the ASC and the SSM techniques.

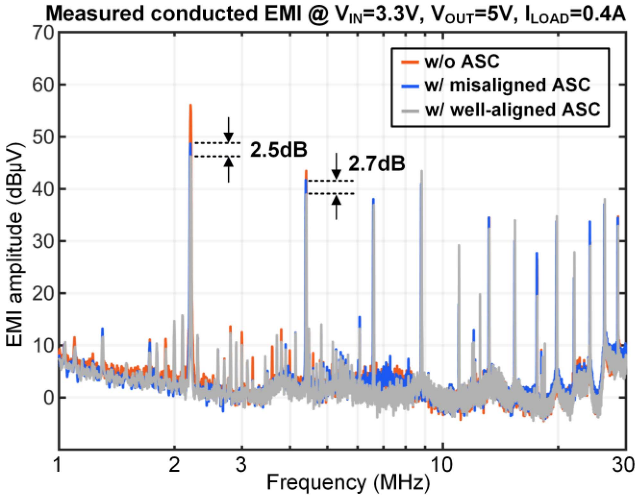


Fig. 14. Measured conducted EMI with/without proposed ASC and autophase alignment being presented.

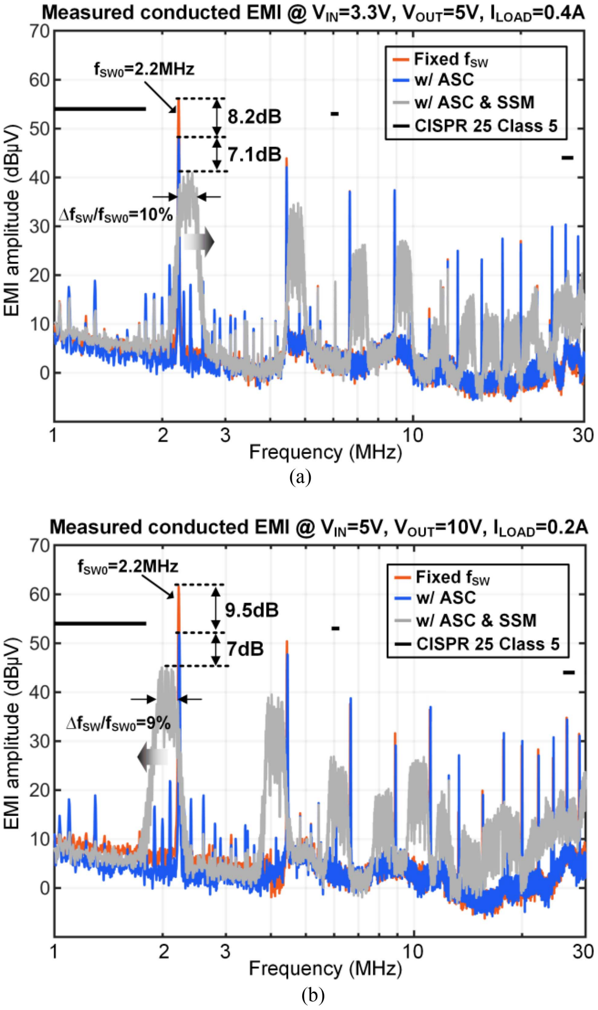
bandwidth of 9 kHz. The proposed EMI ASC control with auto-phase alignment reduces EMI by 2.5 dB at the switching frequency of 2.2 MHz. Note that the ASC control exhibits no EMI reduction beyond the third frequency harmonics due to the parasitic effects of inductors and capacitors. Therefore, high-frequency EMI suppression must be addressed by the SSM technique.

Fig. 15(a) shows the measured EMI spectrum with both the ASC and the SSM enabled at 3.3 to 5 V conversion. The adoption of ASC control contributes to an EMI reduction of 8.2 dB at 2.2 MHz, while SSM further improves EMI by 7.1 dB with a spread ratio of 10%. Moreover, the high-frequency EMI can be reduced by 10 dB at 30 MHz. As $V_{\rm OUT}$ increases, SSM only performs down spread of $f_{\rm SW}$, as shown in Fig. 15(b), shifting EMI into a lower frequency range for further EMI reduction. Meanwhile, the ratio of $f_{\rm SW}/f_{\rm SW0}$ is confined within 10% to minimize its impact on BER. Overall, in response to a 1.5 times input voltage and 2 times output voltage changes, the proposed techniques achieve a total EMI reduction of 16.5 dB at 2.2 MHz for a 5 to 10 V conversion. Furthermore, the conducted EMI performance successfully meets the peak EMI limits defined in CISPR 25 Class 5 standard.

TABLE I
PERFORMANCE COMPARISON WITH PRIOR WORKS

Design		APEC 2024 [13]	TPEL 2020 [15]	APEC 2020 [24]	TVLSI 2014 [26]	This article
Topology		SEPIC	Buck	Buck	Boost	Boost
Input voltage V_{IN}		4.5–40 V	5 V	12, 48 V	2.7–4.2 V	3–12 V
Output voltage V_{O}		12 V	0.8 V	5 V	3.3–5 V	5–24 V
Switching frequency f_{SW}		400 kHz	1 MHz	400 kHz	1 MHz	2.2 MHz
EMI suppression method		Coupled L + LC tank	Mixed-signal canceller	Kappa (L + C)	SSM	ASC + SSM
Max EMI/ripple reduction	At f_{SW}	17.3 dB	24 dB	16 dB	14 dB	16.5 dB
	At 30 MHz	3 dB*	10 dB @10 MHz*	2 dB*	Not reported	10 dB
Adaptive to operation condition?		Yes	Yes	No	No	Yes
Efficiency penalty		1.3%	35%*	Not reported	0.2%*	0.3% @ 4W 0.5% @ 2W

* Estimated from measured data.



(a)

(b)

Fig. 15. Measured conducted EMI spectrum comparison at (a) $V_{\mathrm{IN}} = 3.3$ V, $V_{\mathrm{OUT}} = 5$ V, and $I_{\mathrm{LOAD}} = 0.4$ A, and (b) $V_{\mathrm{IN}} = 5$ V, $V_{\mathrm{OUT}} = 10$ V, and $I_{\mathrm{LOAD}} = 0.2$ A.

Finally, Table I compares this article with prior arts. SEPIC converter in [13] utilizes a coupled inductor and resonant LC tank to realize ripple cancellation without any active control circuitry. However, it suffers from limited high frequency EMI suppression due to parasitic effects and process variations in inductors. Joshi et al. [15] employ a mixed-signal approach to cancel the triangular output current ripple without applying additional inductor, improving the power density significantly. However, it employs many transconductance amplification stages to generate the triangular waveform, leading to great efficiency overhead. An improved buck topology in [24] achieves continuous input and output currents for EMI reduction. Unfortunately, the additional power inductor required significantly compromises power density. Liou et al. [26] apply conventional SSM to suppress EMI with negligible impact on efficiency. However, as the operation voltage increases, conventional SSM technique may become inadequate for meeting the stringent automotive EMI requirement. In comparison, this article operates at a much higher switching frequency of 2.2 MHz while achieving a total EMI reduction of 16.5 dB at f_{SW}. And it maintains a 10 dB EMI suppression at 30 MHz. The additional LC components are implemented in a chip-scale package due to low RMS current, minimizing the impact on power density. The proposed ASC and BER-conscious SSM result in a power efficiency overhead of 0.3% at an output power of 4 W and 0.5% at 2 W.

V. CONCLUSION

This article presents a design work of a GaN power converter IC using EMI ASC and BER-conscious SSM controls for autonomous driving applications. An ASC control is proposed to achieve adaptive EMI suppression across varying converter's operation conditions. Moreover, an auto-phase-aligned control mechanism is developed to accomplish precise ripple self-cancellation. Furthermore, a BER-conscious adaptive SSM technique is implemented to work with ASC seamlessly to reduce EMI across wide frequency spectrum while limiting the frequency spreading ratio for enhanced communication safety. The experimental results successfully validate the proposed design.

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