Design and Reliability Analysis of a New Non-Isolated DC–DC Converter Without Coupled Inductors

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***Abstract*—This article proposes a new non-isolated dc–dc converter without coupled inductors to attain a higher voltage gain at a low duty ratio, less voltage stress across the switch, and improved reliability. The operation of the proposed converter is examined through the steady-state mathematical equations in continuous conduction mode and discontinuous conduction mode. The boundary condition mode of the proposed topology is also discussed. Reliability analysis is performed using the MIL-HDBK-217F standard to predict the failure rate of the individual components. A laboratory-based prototype is developed and tested with 250 W to validate the operation of the proposed converter. Also, the proposed converter is tested with steady-state and dynamic conditions by changing the duty ratio and load values. The efficiency and power density of the proposed converter are 91.8% and 37.71 W/in^3 (2.3 kW/L).**

***Index Terms*—Converter, high gain, power density, reliability.**

I. Introduction

THE increase in global warming, pollution, and energy consumption has pawed the path for researchers to focus on adopting renewable energy sources [1]. Renewable energy sources require a power electronic converter interface to connect it to the appropriate load, where the dc–dc converter is one of the crucial converters [2], [3]. DC–Dc converters are broadly classified as isolated and non-isolated converters. The non-isolated converters have been preferred in many applications to avoid core loss, weight, space, and cost [4]. Several attempts have been made in non-isolated converter configurations by considering distinct features, such as the number of semiconductor devices, input and output ports, passive components, size, efficiency, power density, and cost [5], [6]. A quadratic boost converter (QBC) is one of the non-isolated converters categories, providing higher voltage gain for all duty ratio than conventional converters. The different QBC topologies have been developed in the literature with three categories: combining different conventional converters, incorporating the voltage multiplier cells (VMC) with conventional converters, and adding the passive components to the existing converters.

The converter in [7] has been developed by combining the modified quadratic converter with the SEPIC to attain a higher voltage gain. However, the converter has been demonstrated at an extreme duty cycle ($D > 70\%$), which increases the overall power loss of the converter. The quadratic-based buck–boost converter has been developed in [8] that utilizes two semiconductor switches, which may increase the switching losses of the converter. Also, the converter developed in [7], [8], and [9] utilizes three inductors, which increases the size of the converter and thereby reduces the power density.

In [10], the converter has been designed by combining the switched inductors with a QBC. The converter utilizes two semiconductor switches, operating at a switching frequency of 100 kHz, which increases the switching loss, capacitance loss, and body diode loss of the switch. The converter in [11] and [12] has been developed by combining a QBC with VMC. In [11], the voltage stress of the switches, capacitors, and diodes suffers due to high voltage stress that increases the failure rate of the components and thereby reduces the reliability of the converter. The converter developed in [12] has been demonstrated to obtain an efficiency of 88% and achieves a lower voltage gain to component count ratio. The converter in [13] and [14] has been designed by integrating the QBC with a switched inductor and VMC, respectively. These topologies suffer from higher voltage stress due to the placement of the semiconductor switch near the load side of the converter, which leads to an increase in the failure rate of the switch. The topologies developed in [15] and [16] utilize two semiconductor switches that increase the overall size and control complexity. In [17], the basic QBC has been altered by adding one additional capacitor. The less voltage gain of the converter has been obtained, and reliability analysis has been examined using FIDES. The converter developed in [18] has three inductors and two semiconductor switches that reduce the power density of the converter. It has been demonstrated to attain an efficiency of 83.52% . The developed converter in [19] and [20] utilizes more component

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count to attain a higher voltage gain, increasing the size and its cost also decreasing the power density. The developed converter in [21] and [22] utilizes a two-semiconductor switch, which increases the power loss of the converter. Therefore, an attempt is made to develop a unique non-isolated dc–dc converter in this article to overcome the drawbacks mentioned above.

The aspect of innovation of this article is given as follows.

1) A new non-isolated dc–dc converter is developed with a few advantages, such as higher voltage gain at less duty ratio, low voltage stress on the semiconductor switch, and high lifetime of individual components.
2) The voltage stress across the switch is less than half of the output voltage. Therefore, the lifetime of the switch is increased.
3) Failure rate of the individual components is determined by using the military handbook for the lifetime prediction.

II. Operating Principle of the Proposed Converter

Fig. 1(a) shows the configuration of a proposed converter. It consists of a single semiconductor switch (M_1), two inductors $(L_1$ and $L_2)$, four capacitors $(C_1, C_2, C_3$, and $C_0)$, and five diodes $(D_1, D_2, D_3, D_4$, and $D_5)$ to attain a higher voltage gain with less duty ratio and less voltage stress across the switch. The proposed converter operation is examined in continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Fig. 1(b)–(d) shows the analytical voltage and current waveform of inductors and switch, diodes, and capacitors, respectively. The operation of a proposed converter in CCM has two different modes, which are discussed as follows.

A. Continuous Conduction Mode

Mode I$(t_0 < t < t_1)$: During this period, the switch M_1 is turned ON and the diodes D_2 and D_4 are in forward biased condition. Fig. 2(a) shows the current traversal path of the proposed converter in Mode I operation. The inductors L_1 and L_2 are magnetized by the source V_i and the capacitor C_1, respectively. The capacitors C_1, C_3, and C_0 are discharged, and the capacitor C_2 is charged

$$V_{L1} = V_i \tag{1}$$

$$V_{L2} = V_{C1} = (V_{C2} - V_{C3}). \tag{2}$$

Mode II$(t_1 < t < t_2)$: During this period, the switch M_1 is turned OFF and the diodes D_2 and D_4 are in reverse biased condition. Fig. 2(b) shows the current traversal path of the proposed converter. The inductors L_1 and L_2 are demagnetized. The capacitor C_2 is discharged, and the capacitors C_1, C_3, and C_0 are charged

$$V_{L1} = V_i - V_{C1} = V_i + V_{C2} + V_{C3} - V_0 \tag{3}$$

$$V_{L2} = -V_{C3} = V_{C1} + V_{C2} - V_0. \tag{4}$$

Applying the volt-sec balance principle to the inductors L_1 and L_2, then the voltage across capacitors and voltage gain

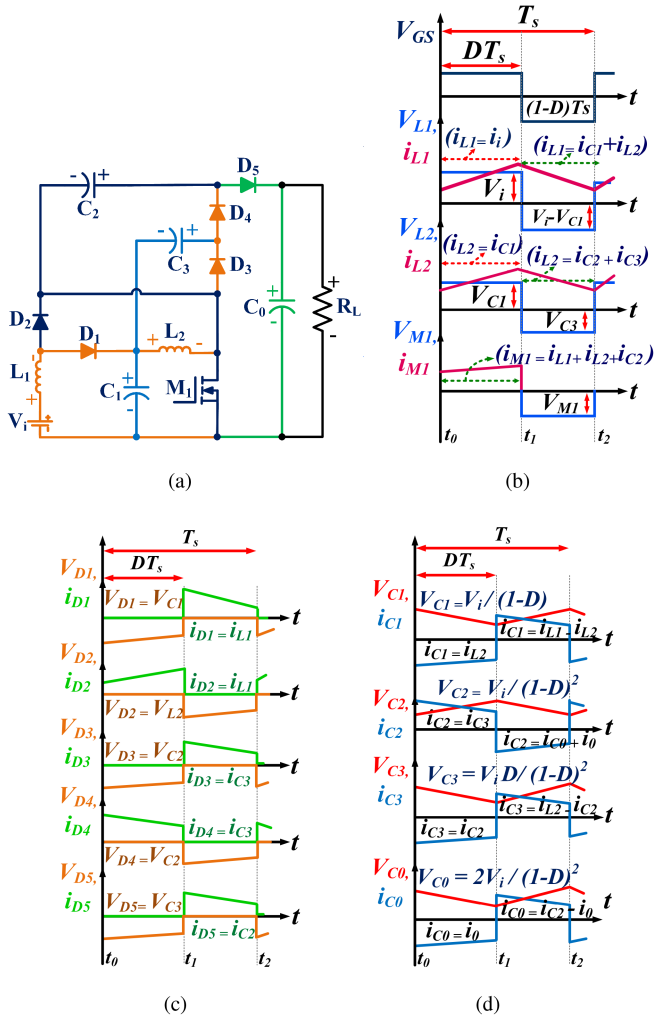


Fig. 1. (a) Configuration of a proposed converter, analytical waveforms in CCM. (b) Inductors (L_1 and L_2) and switch (M_1). (c) Diodes (D_1, D_2, D_3, D_4, and D_5). (d) Capacitors (C_1, C_2, C_3, and C_0).

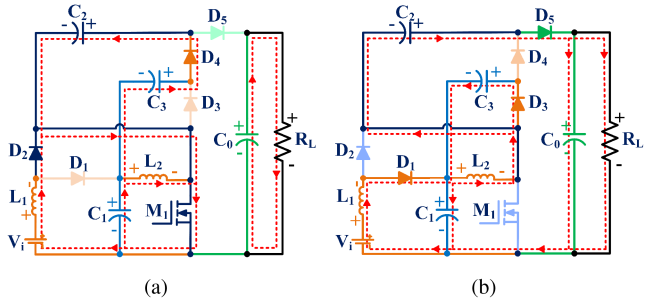


Fig. 2. CCM operation. (a) Mode I. (b) Mode II.

equations are obtained

$$V_{C1} = \frac{V_i}{(1-D)}; V_{C2} = \frac{V_i}{(1-D)^2}; V_{C3} = \frac{V_i D}{(1-D)^2}. \tag{5}$$

The voltage gain of the proposed converter under CCM is

$$G_{CCM} = \frac{V_0}{V_i} = \frac{2}{(1-D)^2}. \tag{6}$$

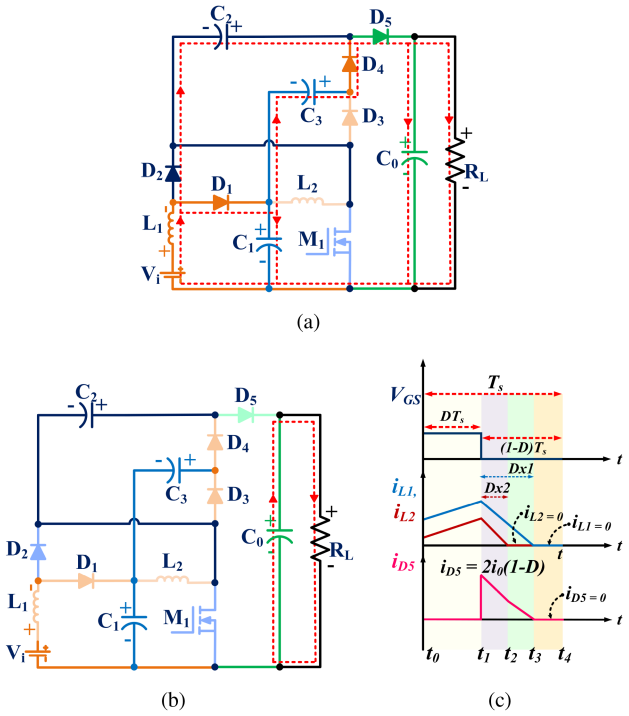


Fig. 3. DCM operation: (a) Mode III; (b) Mode IV; (c) analytical waveform.

B. Discontinuous Conduction Mode I

Four different modes of operation are found in DCM operation. The operation of Mode I is similar to CCM. In Mode II $(t_1 < t < t_2)$, both inductors current i_{L1} and i_{L2} start to decay. The inductor current i_{L2} decays to zero in Mode III $(t_2 < t < t_3)$, as shown in Fig. 3(a), but still inductor current i_{L1} supplies the load through diode D_5. In Mode IV, $(t_3 < t < t_4)$, the inductor current i_{L1} decays to zero, as shown in Fig. 3(b), and therefore the diode D_5 is in blocking condition. During this mode, the energy present in the capacitor C_0 supplies to the load. Fig. 3(c) shows the analytical waveform of the DCM.

Mode I $(t_0 < t < t_1)$*:* During this period $(t_0 < t < t_1)$, the semiconductor switch M_1 is turned ON at the instant t_0. The inductors L_1 and L_2 are magnetized in the same way as the Mode I operation of CCM. The peak current of inductors L_1 and L_2 are identified as follows:

$$i_{L1P} = \frac{V_i D T_S}{L_1} \tag{7}$$

$$i_{L2P} = \frac{V_i D T_S}{(1-D)L_2}. \tag{8}$$

Mode II $(t_1 < t < t_2)$*:* During this period, the semiconductor switch M_1 is turned OFF. At instant t_1, the inductors L_1 and L_2 start to decay, and it is noted that the inductor L_2 decays faster than the inductor L_1 and it reaches to zero at the instant t_2. D_{x2} is the decaying period of an inductor current L_2. In this mode, the inductor L_1 continues to decay and does not reach zero. The peak current of inductor L_2 in Mode II is as follows:

$$i_{L2P} = \left[\frac{2V_i(1-D) - V_0(1-D)^2}{L_2(1-D)^2}\right] D_{x2} T_S. \tag{9}$$

Mode III $(t_2 < t < t_3)$*:* During this period, the semiconductor switch M_1 is turned OFF. At instant t_2, the current of the inductor L_2 is zero, so the diode D_2 gets forward bias. This allows the current of the inductor L_1 to discharge its stored energy to supply the capacitor C_0 through the diode D_2 and C_2. Also, it supplies to load through diode D_5. It should be noted that the inductor L_1 reaches zero at the instant t_3. The current of the inductor L_1 is calculated for the period $(t_1 < t < t_3)$ is as follows, and "D_{x1}" is the decaying period of inductor current L_1:

$$i_{L2P} = 0 \tag{10}$$

$$i_{L1P} = \left[\frac{V_i(D^2 - D + 2) - V_0(1-D)^2}{L_1(1-D)^2}\right] D_{x1} T_S. \tag{11}$$

Mode IV $(t_3 < t < t_4)$*:* During this period, the semiconductor switch M_1 is turned OFF. At instant t_3, no current flows through the diode D_5 and the diode enters into blocking state. The parameter "D_{x1}" can be determined by equating (7) and (11)

$$D_{x1} = \left[\frac{V_i D(1-D)^2}{V_i(D^2 - D + 2) - V_0(1-D)^2}\right]. \tag{12}$$

The average current of the capacitor C_0 can be expressed as follows:

$$i_{C0} = \frac{1}{2} D_{x1} i_{L1P} - i_0. \tag{13}$$

By substituting (11) and (12) in (13), the capacitor current i_{C0} can be expressed as follows:

$$i_{C0} = \left[\frac{V_i D^2(1-D)^2}{2L_1 f_s(D^2 - D + 2) - \frac{V_0}{V_i}(1-D)^2}\right] - \frac{V_0}{R}. \tag{14}$$

By further simplification, the dc voltage gain (G_{DCM}) in DCM is determined as follows:

$$G_{\text{DCM}} = \frac{D}{2(D-1)} \pm \frac{1}{2}\sqrt{D\left[\frac{D+8}{(D-1)^2} - \frac{2D}{K_{L1}}\right]} \tag{15}$$

where

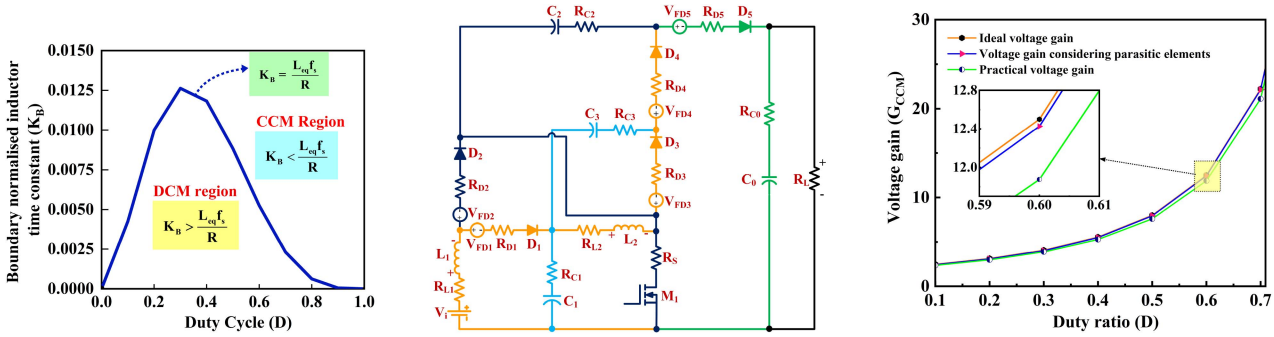
$$K_{L1} = \frac{L_1 f_s}{R}. \tag{16}$$

C. Boundary Condition Mode (BCM)

When the proposed converter is operated at the boundary of CCM and DCM, then the voltage gain of CCM is equal to DCM. The boundary normalized inductor time constant (K_B) is obtained as follows:

$$K_B = \frac{D^2(1-D)^4}{\sqrt{2}\,(1 + D - D^2)}. \tag{17}$$

Fig. 4(a) depicts the plot of the boundary normalized inductor time constant (K_B) versus duty cycle (D). If $K_L > K_B$, then



(a) (b) (c)

Fig. 4. (a) "K_B" versus duty cycle. (b) Equivalent circuit of the proposed converter considering parasitic elements. (c) Comparison of voltage gain considering parasitic and non-parasitic elements.

the proposed converter is operated under the CCM region. Otherwise, it enters into the DCM operation.

D. Effect of Parasitic Elements on Voltage Gain

The equivalent circuit of the proposed converter considering the parasitic elements is shown in Fig. 4(b). The voltage gain of the proposed converter considering parasitic elements can be determined using the equation of inductor L_2 in the two modes of operation under CCM. The voltage equation of the inductor L_2 in Mode I operation

$$V_{L2} = V_{C1} - i_{C1}R_{C1} - i_{L2}R_{L2} - i_S R_S. \tag{18}$$

The voltage equation of the inductor L_2 in Mode II operation

$$V_{L2} = V_{C1} - i_{L1}(R_{L1} + R_{D1}) + V_{C2} - i_{L2}R_{L2} - V_{\text{FD1}} - V_{\text{FD5}} - i_{C2}(R_{C2} + R_{C0} + R_{D5}) + i_0 R_{C0} - V_0. \tag{19}$$

The voltage gain of the proposed converter considering parasitic elements is derived as follows:

$$\left.\begin{aligned} &\frac{2V_i}{(1-D)^2} - (V_{\text{FD1}} + V_{\text{FD5}}) - \frac{(i_{C1}R_{C1} + i_S R_S)D}{(1-D)} + \\ &\frac{i_{L1}(R_{L1}+R_{D1})D}{(1-D)} - i_{C2}(R_{C2} + R_{D5} + R_{C0}) + i_0 R_{C0} \end{aligned}\right\} = V_0 \tag{20}$$

where V_{FD1}, V_{FD2}, V_{FD3}, V_{FD4}, and V_{FD5} and R_{D1}, R_{D2}, R_{D3}, R_{D4}, and R_{D5} are the cut-in voltages and internal resistances of the diodes D_1, D_2, D_3, D_4, and D_5, respectively. R_{L1} and R_{L2}, and R_{C1}, R_{C2}, R_{C3}, and R_{C0} are the internal resistance of the inductors and capacitors, respectively. Fig. 4(c) shows the different voltage gain of the proposed converter considering without parasitic elements, with parasitic elements, and its practical voltage gain. It is noted that the voltage gain with parasitic elements and practical voltage gain differs from the theoretical voltage gain. The output voltage of the proposed converter considering the parasitic elements, without parasitic elements, and experimental voltage for a duty ratio of 0.6 is 300 V, 296 V, and 283 V, respectively.

III. Design Consideration

A. Calculation of Currents

The capacitor current equation for the turn ON period of the switch M_1 is as follows:

$$C_1\frac{dV_{C1}}{dt} = -i_{L2}; C_2\frac{dV_{C2}}{dt} = C_3\frac{dV_{C3}}{dt}; C_0\frac{dV_{C0}}{dt} = -i_0. \tag{21}$$

The capacitor current equation for the turn OFF period of the switch M_1 is as follows:

$$C_1\frac{dV_{C1}}{dt} = i_{L1} - i_{L2}; C_2\frac{dV_{C2}}{dt} = -i_0 - i_{C0} \tag{22}$$

$$C_3\frac{dV_{C3}}{dt} = i_{L2} - i_{C2}; C_0\frac{dV_{C0}}{dt} = i_{C2} - i_0. \tag{23}$$

Applying the amp-sec balance principle with the (21)–(23), the following current equations are obtained:

$$i_{L1} = \frac{i_0}{(1-D)^3}; i_{L2} = \frac{i_0}{(1-D)^2}; i_{C2} = \frac{i_0}{(1-D)}. \tag{24}$$

B. Current Ripple of the Inductors

The current ripple of the inductors L_1 and L_2 are obtained from the Mode I as follows:

$$\Delta i_{L1} = \frac{V_i D}{L_1 f_s}; \Delta i_{L2} = \frac{V_i D}{L_2(1-D)f_s}. \tag{25}$$

C. Voltage Ripple of the Capacitor

The voltage ripple of the capacitors is obtained as follows:

$$\Delta V_{C1} = \frac{V_0 D}{R(1-D)^2 C_1 f_s}; \Delta V_{C2} = \frac{2V_0(1-D)}{RC_2 f_s} \tag{26}$$

$$\Delta V_{C3} = \frac{V_0 D}{R(1-D)C_3 f_s}; \Delta V_{C0} = \frac{V_0 D}{RC_0 f_s}. \tag{27}$$

D. Voltage Stress of the Switch and Diodes

The voltage stress of the switch and diodes are calculated during their respective nonconduction period

$$V_{M1} = \frac{V_i}{(1-D)^2}; V_{D1} = \frac{V_i}{(1-D)}; V_{D2} = \frac{V_i D}{(1-D)^2} \tag{28}$$

$$V_{D3} = V_{D4} = V_{D5} = \frac{V_i}{(1-D)^2}. \tag{29}$$

It is found that the voltage stress across the switch and diodes is less than 50% of the output voltage. The voltage stress of the components may significantly affect the reliability of the converter.

E. Current Stress of Switch and Diodes

The current stress of the switch and diodes are calculated during their respective conduction period

$$i_{M1(\text{AVG})} = i_0 D\left[\frac{(2-D)+(1-D)^2}{(1-D)^3}\right] \tag{30}$$

$$i_{D1(\text{AVG})} = \frac{i_0}{(1-D)^2}; i_{D2(\text{AVG})} = \frac{i_0 D}{(1-D)^3} \tag{31}$$

$$i_{D3,D4(\text{AVG})} = \frac{i_0 D}{(1-D)}; i_{D5(\text{AVG})} = 2i_0(1-D). \tag{32}$$

IV. Efficiency Analysis

The efficiency of the proposed converter is determined by calculating the power loss of inductors, capacitors, diodes, and switch. The power loss of the inductors L_1 and L_2 is calculated as follows:

$$P_{L1} = r_{L1}\frac{i_0^2}{(1-D)^6}; P_{L2} = r_{L2}\frac{i_0^2}{(1-D)^4} \tag{33}$$

where r_{L1} and r_{L2} are the equivalent series resistance of the inductors L_1 and L_2, respectively. The power loss of the capacitors C_1, C_2, C_3, and C_0 are determined by using the following expression:

$$P_{C1} = r_{C1}\frac{i_0^2}{(1-D)^2}; P_{C2} = r_{C2}\frac{i_0^2}{(1-D)^2} \tag{34}$$

$$P_{C3} = r_{C3}\frac{i_0^2}{(1-D)^2}; P_{C0} = r_{C0} i_0^2 \tag{35}$$

where r_{C1}, r_{C2}, r_{C3}, and r_{C0} are the equivalent series resistance of the capacitors C_1, C_2, C_3, and C_0, respectively.

The total power loss of the diodes is calculated by adding the forward resistance loss, forward voltage loss, and reverse recovery loss. Forward resistance loss (P_{RFD}) of individual diodes is given as follows:

$$\begin{aligned}
P_{\text{RFD1}} &= R_{\text{FD1}} i_{D1_RMS}^2 = R_{\text{FD1}}\tfrac{{i_0}^2}{(1-D)^5} \\
P_{\text{RFD2}} &= R_{\text{FD2}} i_{D2_RMS}^2 = R_{\text{FD2}}\tfrac{{i_0}^2 D}{(1-D)^6} \\
P_{\text{RFD3}} &= R_{\text{FD3}} i_{D3_RMS}^2 = R_{\text{FD3}}\tfrac{{i_0}^2}{(1-D)} \\
P_{\text{RFD4}} &= R_{\text{FD4}} i_{D4_RMS}^2 = R_{\text{FD4}}\tfrac{{i_0}^2 D}{(1-D)^2} \\
P_{\text{RFD5}} &= R_{\text{FD5}} i_{D5_RMS}^2 = 4R_{\text{FD5}}{i_0}^2(1-D)
\end{aligned} \tag{36}$$

where i_D is the current flowing through the diode and R_{FD} is the forward resistance of the diode.

Forward voltage loss (P_{VFD}) of individual diodes is given as follows:

$$\begin{aligned}
P_{\text{VFD1}} &= V_{\text{FD1}} i_{D1_avg} = V_{\text{FD1}}\tfrac{i_0}{(1-D)^2} \\
P_{\text{VFD2}} &= V_{\text{FD2}} i_{D2_avg} = V_{\text{FD2}}\tfrac{i_0 D}{(1-D)^3} \\
P_{\text{VFD3}} &= V_{\text{FD3}} i_{D3_avg} = V_{\text{FD3}} i_0 \\
P_{\text{VFD4}} &= V_{\text{FD4}} i_{D4_avg} = V_{\text{FD4}}\tfrac{i_0 D}{(1-D)} \\
P_{\text{VFD5}} &= V_{\text{FD5}} i_{D5_avg} = 2V_{\text{FD5}} i_0(1-D)
\end{aligned} \tag{37}$$

where V_{FD} is the cut-in voltage of the diode.

Reverse recovery losses (P_{RRL})

$$\sum_{i=1}^{5} P_{(\text{RRL},i)} = \sum_{i=1}^{5} V_{(\text{RRM},i)} i_{(\text{RRM},i)} t_b f_s. \tag{38}$$

where V_{RRM} is the peak reverse voltage, I_{RRM} is the peak reverse current, and t_b is the time from peak I_{RRM} to the instant where 25% of I_{RRM} is reached. The forward resistance loss (P_{RFD}), forward voltage loss (P_{VFD}), and reverse recovery loss of the diodes (P_{RRL}) are added to determine the overall loss of the diodes.

The power loss of the switch (M_1) is calculated by adding the conduction loss (P_{RDS}), switching loss (P_{SW}), output capacitance loss (P_{Coss}), and reverse recovery loss of the body diodes (P_{BD}) of the switch. The power loss of the semiconductor switch (M_1) is obtained as follows:

$$P_{\text{Loss\_switch}} = P_{\text{RDS}} + P_{\text{SW}} + P_{\text{Coss}} + P_{\text{BD}} \tag{39}$$

$$P_{\text{RDS}} = \left[{i_0}^2 D\left[\frac{(2-D)+(1-D)^2}{(1-D)^3}\right]^2\right] R_{DS} \tag{40}$$

$$P_{\text{SW}} = \frac{1}{2} f_s V_m I_m (t_{\text{on}} + t_{\text{off}}) \tag{41}$$

$$P_{\text{Coss}} = f_s C_s \frac{V_i^2}{2(1-D)^4} \tag{42}$$

where R_{DS} is the on-state resistance, V_m and I_m are the maximum voltage and current of the switch, respectively, f_s is the switching frequency, t_{on} is the turn ON time that combines the delay time and rising time, and t_{off} is the turn OFFtime that combines the delay time and fall time.

Fig. 5(a) shows the efficiency of the proposed converter for various ranges of output power. Fig. 5(b) shows the efficiency against various duty cycles for a constant load of 250 W. From Fig. 5(a), it is noted that the maximum efficiency of the proposed converter is 91.8% . The intrinsic body diode losses are significant only when the converter operates at higher switching frequencies ($\geq$100 kHz). Therefore, the reverse recovery loss of the body diode (P_{BD}) is not considered in the power loss calculation. Fig. 5(c) clearly depicts the loss breakdown of individual components.

V. Experimental Results

The prototype of the proposed converter is developed and verified with 250 W under CCM operation. The operation of

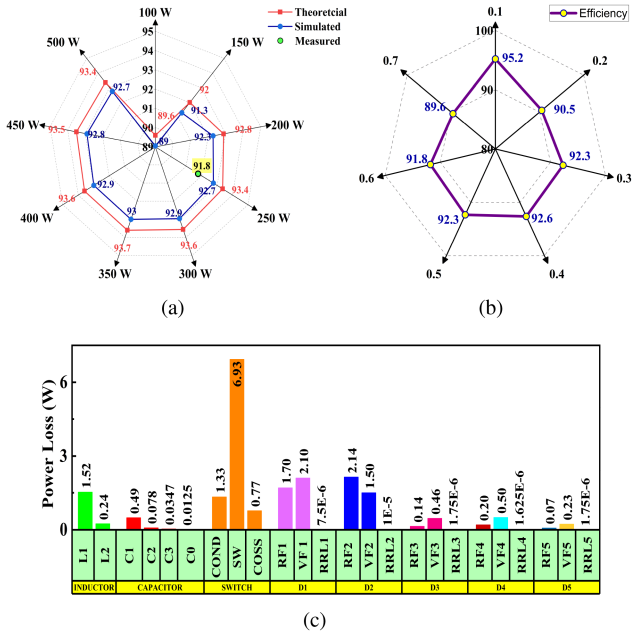


Fig. 5. (a) Efficiency versus different output power. (b) Efficiency versus different duty cycle. (c) Power loss distribution for each component.

TABLE I
SPECIFICATIONS OF PROPOSED CONVERTER

Parameters	Values	Dimension
Switch	IXFH120N30X3	0.62"(L) x 0.19"(B)
L_1	1 mH	1.70"(L) x 1.20"(B)
L_2	1.2 mH	1.30"(L) x 0.90"(B)
D_1	SRA 2090	0.41"(L) x 0.17"(B)
D_2	STPS30120C	0.39"(L) x 0.17"(B)
D_3, D_4,and D_5	STPS60SM200C	0.60"(L) x 0.19"(B)
C_1	ESY156M100AE3	0.43"(L) x 0.25"(D)
C_2	ECA2DHG3R3	0.44"(L) x 0.24"(D)
C_3	ULD2C5R6MED	0.43"(L) x 0.24"(D)
C_0	ULD2G2R2MPD	0.45"(L) x 0.31"(D)

L- Length, B- Breadth, D- Diameter, L_1,L_2-Inductors,C_1,C_2, C_3, and C_0-Capacitors, D_1,D_2,D_3,D_4,and D_5-Diodes

the proposed converter is analyzed with a 60% duty ratio at a switching frequency of 50 kHz for an input voltage of 24 V. The parameters utilized for developing the prototype are given in Table I. The maximum height of the prototype is 1.65 in, and the total area is 4.02 in^2. The power density of the proposed converter is 37.71 W/in^3 (2.3 kW/L).

Fig. 6(a) shows the experimental waveform of the input and output voltage of the proposed converter. The output voltage (V_0) achieved across the converter terminal for a 250 W load is 283 V, and it is noted that the ripple voltage is 4 V, which is 1.4% of the output voltage. Fig. 6(b) shows the experimental waveform of the input and output current waveform. The input and output current of the proposed converter is 10.2 A and 0.8 A, respectively. Fig. 6(c) represents the current waveform of the inductors L_1 and L_2.The average value of the inductor currents of L_1 and L_2 is approximately 11 A and 4.6 A, respectively. The maximum voltage stress of diodes D_1 and D_2, D_3 and D_4, and D_5 and switch M_1 are shown in Fig. 6(d)–(f), respectively. The peak voltage across the diodes of D_1 and D_2, D_3 and D_4, and D_5 are 60 V and 86 V, 144.5 V and 139 V, and 140.6 V, respectively. The maximum voltage stress across the switch M_1 is 144.5 V. The maximum voltage drop across the capacitors C_1 and C_2 and C_3 and C_0 is shown in Fig. 6(g) and (h), respectively. The voltage stress across the capacitors C_1 and C_2 and C_3 and C_0 is 60 V and 137 V and 86 V and 258 V, respectively. Also, it is noted that the voltage stress of the diodes and capacitors closely matches the theoretical values. To corroborate the performance of the proposed converter under dynamic conditions, it is tested with varying duty ratio values and load values separately. The proposed converter is tested with varying duty cycles (i.e., D = 0.4, D = 0.5, and D = 0.6) for a constant load of 360 Ω, which is shown in Fig. 6(a). Also, it is tested with a constant duty cycle of 60% by the varying load of 600 Ω, 450 Ω, and 360 Ω, which is shown in Fig. 6(j). It is noted that the behavior of the proposed converter responds well during the sudden change in duty ratio value and load value. Fig. 6(k) shows the laboratory-based experimental setup and the size of the converter. The experimental results confirmed that the proposed converter can provide a higher voltage gain with reduced voltage stress across switch (M_1).

VI. COMPARATIVE ANALYSIS WITH OTHER TOPOLOGIES IN THE LITERATURE

The proposed converter is compared with existing QBC topologies developed in[7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], and [30]. Table II represents a detailed comparison of a proposed converter based on different features, such as component utilization, voltage gain (G_{CCM}), voltage stress, duty ratio to attain 12.5 voltage gain, operating duty ratio, and its' switching frequency with recently developed quadratic boost topologies. Fig. 7(a) shows the voltage gain comparison of the proposed converter with existing QBC topologies. It is worth mentioning that the proposed converter's voltage gain is high among all existing QBCs in [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], and [28]. The converter in [29] and [30] has higher voltage gain but the total component count is found to be high as compared with the proposed converter. Due to higher number of diodes, the power loss of the diodes are higher than the proposed converter. Fig. 7(b) shows the ratio of voltage gain to total component count (G_{CCM}/TCC) and a ratio of the voltage stress of a switch to the voltage gain (V_{SW}/G_{CCM}) of the existing QBCs and proposed converter. It is highlighted that the proposed converter has a higher voltage gain to TCC ratio than the existing QBCs. This ratio exhibits how effectively the components are utilized to attain the desired voltage gain. The ratio of the voltage stress on the switch to the voltage gain of the proposed converter is low except for the converters developed in [12] and [18] because it has the same ratio as aligned with the proposed converter. Fig. 7(c) illustrates the operating duty cycle and switching frequency of the existing QBCs. The converter developed in [7], [12], and [24] are operated at a higher duty cycle ($D \geq 0.7$), this may increase the conduction loss of the switch and thereby decrease the efficiency of the converter. Also, the converters found in [10], [11], [13], [18], [24], and [30] are

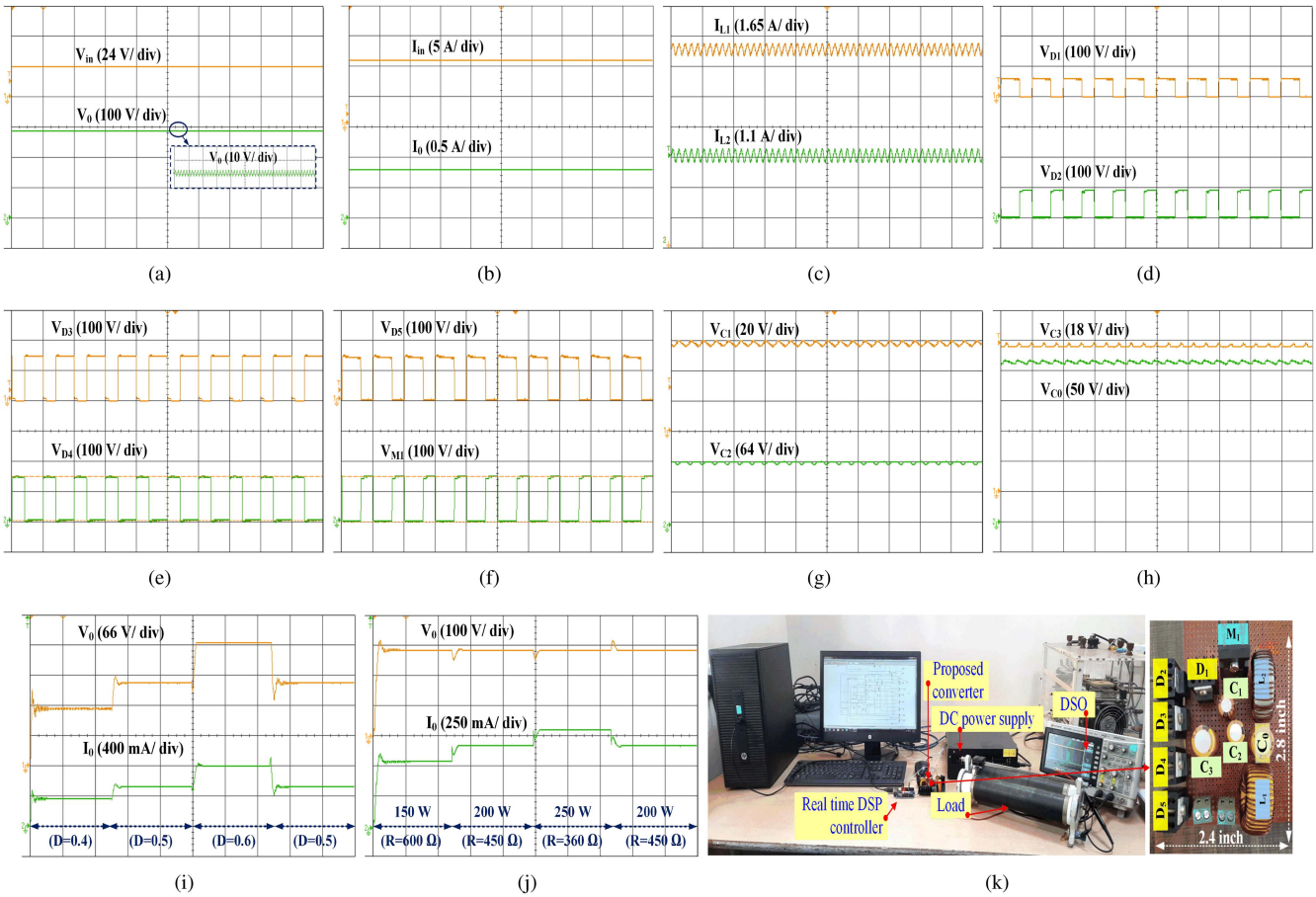


Fig. 6. Experimental waveforms for the proposed converter: (a) V_0 and V_{in}, (b) I_{in} and I_0, (c) i_{L1} and i_{L1}, (d) V_{D1} and V_{D2}, (e) V_{D3} and V_{D4}, (f) V_{D5} and V_{M1}, (g) V_{C1} and V_{C2}, (h) V_{C3} and V_{C0}, (i) V_0 and I_0 for various duty cycle with constant load, and (h) V_0 and I_0 for various load condition with constant duty cycle. (k) Experimental setup.

TABLE II
COMPARISON OF PROPOSED CONVERTER WITH EXISTING QBC TOPOLOGIES

Reference	Components [S/L/C/D]	Voltage gain (G_{CCM})	Voltage stress ($\frac{V_{sw}}{V_i}$)	Duty ratio to attain $G_{CCM} = 12.5$	Operating duty ratio	Frequency (kHz)
Proposed	**1/2/4/5**	$\frac{2}{(1-D)^2}$	$S_1 = \frac{1}{(1-D)^2}$	**0.6**	**0.6**	**50**
[7]	1/3/4/4	$\frac{1+D}{(1-D)^2}$	$S_1 = \frac{1}{(1-D)^2}$	0.64	0.70	50
[8]	2/3/3/2	$(\frac{D}{1-D})^2$	$S_1 = \frac{1}{(1-D)^2}; S_2 = \frac{(D)}{(1-D)^2}$	0.78	0.414	60
[9]	1/3/4/4	$\frac{1+D}{(1-D)^2}$	$S_1 = \frac{1+D}{(1-D)^2}$	0.64	0.64	20
[10]	2/2/3/3	$\frac{1-D+D^2}{(1-D)^2}$	–	0.74	0.55	100
[11]	1/3/2/5	$\frac{1+D}{(1-D)^2}$	$S_1 = \frac{1}{(1-D)^2}$	0.64	0.594	10
[12]	1/3/4/5	$\frac{2}{(1-D)^2}$	$S_1 = \frac{1}{(1-D)^2}$	0.6	0.70	60
[13]	1/3/3/5	$\frac{2}{(1-D)^2}$	$S_1 = \frac{2}{(1-D)^2}$	0.60	0.60	100
[14]	1/3/2/6	$\frac{1+D}{(1-D)^2}$	$S_1 = \frac{1+D}{(1-D)^2}$	0.64	0.558	60
[15]	2/2/2/2	$\frac{1}{(1-D)^2}$	$S_1 = \frac{1}{1-D}; S_2 = \frac{(1)}{(1-D)^2}$	0.72	0.465	50
[16]	2/2/2/2	$\frac{1}{(1-D)^2}$	$S_1 = \frac{1}{(1-D)^2}$	0.72	0.653	50
[17]	1/2/3/2	$\frac{1-D^2}{(1-D)^2}$	$S_1 = \frac{1}{(1-D)}$	0.85	0.40	60
[18]	2/3/3/4	$\frac{2}{(1-D)^2}$	$S_1 = \frac{1}{(1-D)^2}$	0.60	0.60	100
[19]	1/2/4/5	$\frac{2-D}{(1-D)^2}$	$S_1 = \frac{1}{(1-D)^2}$	0.675	0.50	50
[20]	1/3/6/6	$\frac{3-D}{(1-D)^2}$	$S_1 = \frac{1}{(1-D)^2}$	0.56	0.50	-
[21]	2/2/3/3	$\frac{1+D}{(1-D)^2}$	$S_1 = \frac{1}{1-D}; S_2 = \frac{(1+D)}{(1-D)^2}$	0.64	0.50	50
[22]	2/2/4/4	$\frac{3-D}{(1-D)^2}$	$S_1 = \frac{1}{1-D}; S_2 = \frac{(2-D)}{(1-D)^2}$	0.56	0.40	10
[23]	1/3/4/4	$\frac{1+D}{(1-D)^2}$	$S_1 = \frac{1}{(1-D)^2}$	0.64	0.50	50
[24]	2/2/3/3	$\frac{3-2D}{(1-D)^2}$	$S_1 = (1-D); S_2 = \frac{(1-2D(1-D)^2)}{(1-D)^2}$	0.625	0.70	200
[25]	1/4/6/5	$\frac{1+2D-2D^2}{(1-D)^2}$	$S_1 = \frac{1}{(1-D)^2}$	0.66	0.60	50
[26]	1/2/2/3	$\frac{1}{(1-D)^2}$	$S_1 = \frac{1}{(1-D)^2}$	0.72	0.47	20
[27]	1/3/4/4	$\frac{1+D}{(1-D)^2}$	$S_1 = \frac{1}{(1-D)^2}$	0.64	0.60	50
[28]	1/3/4/3	$\frac{1+D}{(1-D)^2}$	$S_1 = \frac{1}{(1-D)^2}$	0.64	0.50	10
[29]	1/2/5/6	$\frac{4-3D}{(1-D)^2}$	$S_1 = \frac{1}{(1-D)^2}$	0.57	0.50	10
[30]	1/2/6/7	$\frac{3}{(1-D)^2}$	$S_1 = \frac{3}{(1-D)^2}$	0.51	0.60	200

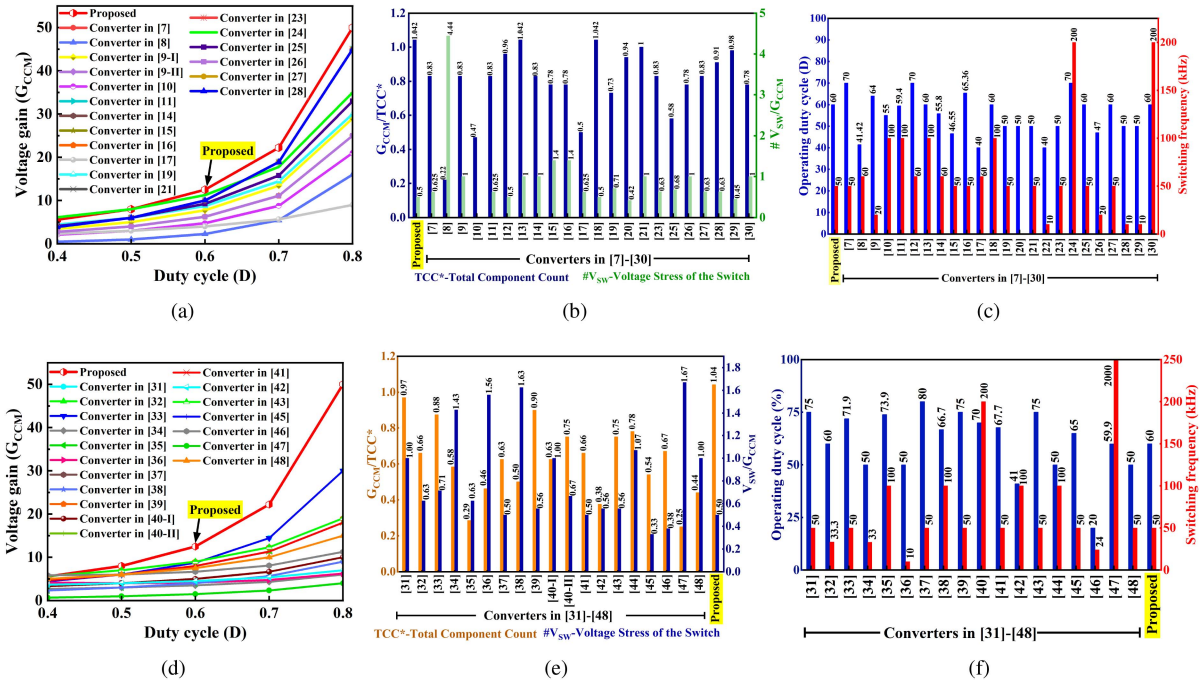


Fig. 7. Comparison of the proposed converter with Quadratic based topologies. a) Voltage gain versus duty cycle. b) Ratio of G_{CCM}/TCC and V_{SW}/G_{CCM}. c) Operating duty cycle and switching frequency (kHz); other non-isolated topologies. d) Voltage gain versus duty cycle. e) Ratio of G_{CCM}/TCC and V_{SW}/G_{CCM}. f) Operating duty cycle and switching frequency (kHz).

operated at high switching frequency (≥100 kHz) this could increase the switching loss, output capacitance loss of the switch, and reverse recovery loss of diodes, which may result in reducing the overall efficiency of the converter. In addition, the uniqueness of the proposed converter is portrayed by comparing the same features of the proposed converter with other recently developed non-isolated based converters [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48]. Fig. 7(d) indicates the voltage gain comparison, where the proposed converter provides higher voltage gain. The voltage gain and G_{CCM}/TCC and V_{SW}/G_{CCM} of the proposed converter is compared with other recently developed non-isolated based converters, as illustrated in Fig. 7(d). It is found that the proposed converter has higher voltage gain and high G_{CCM}/TCC than the developed converters in [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], and [48]. From Fig. 7(e), it is noted that the ratio of V_{SW}/G_{CCM} proposed converter is low except for the converters developed in [45] and [46]. From Fig. 7(f), it is seen that the converters found in [31], [33], [35], [37], [39], [40], and [43] are operated at a higher duty cycle (i.e., $D \geq 0.7$) and the converters in [35], [37], [38], [40], [41], [42], [44], and [47] utilize higher switching frequency, which shall increase the overall power loss of the developed converters. Fig. 8(a) shows the component stress factor (CSF) of the proposed converter for varying duty cycles. From Fig. 8(b), it is noted that the CSF of the proposed converter is high for extreme duty cycle (i.e., $D \geq 0.7$). Therefore, operating the proposed converter at D = 0.6 is preferable, where the total CSF is 50. Fig. 8(b) shows the switch device power (SDP) rating for different voltage gain. The SDP rating

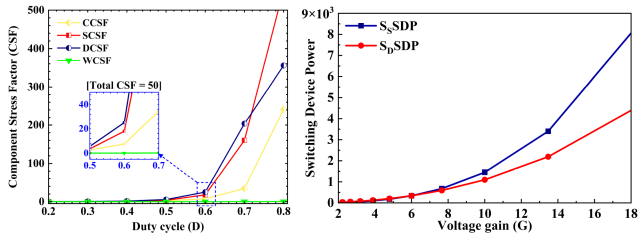


Fig. 8. (a) CSF versus duty Cycle and (b) SDP versus G_{CCM}.

considers the voltage and current stress of the semiconductor devices (switch and diodes) and provides a quantifiable value that indicates the power-handling capability of the devices. In addition, it aids in cost estimation, selecting the appropriate switching devices, and effective thermal management methods. These comparisons show that the proposed converter has superior features to the recently developed non-isolated converters and existing QBCs.

VII. Reliability Analysis for the Proposed Converter

The reliability of the converter depends mainly on the failure rate of each component. This analysis could help to predict the occurrence of failure so that sudden discontinuity of service, mainly in critical applications, such as aerospace and medical devices, can be avoided. The literature shows that the power semiconductor devices and capacitors were more prone to failure than other components in a power electronic

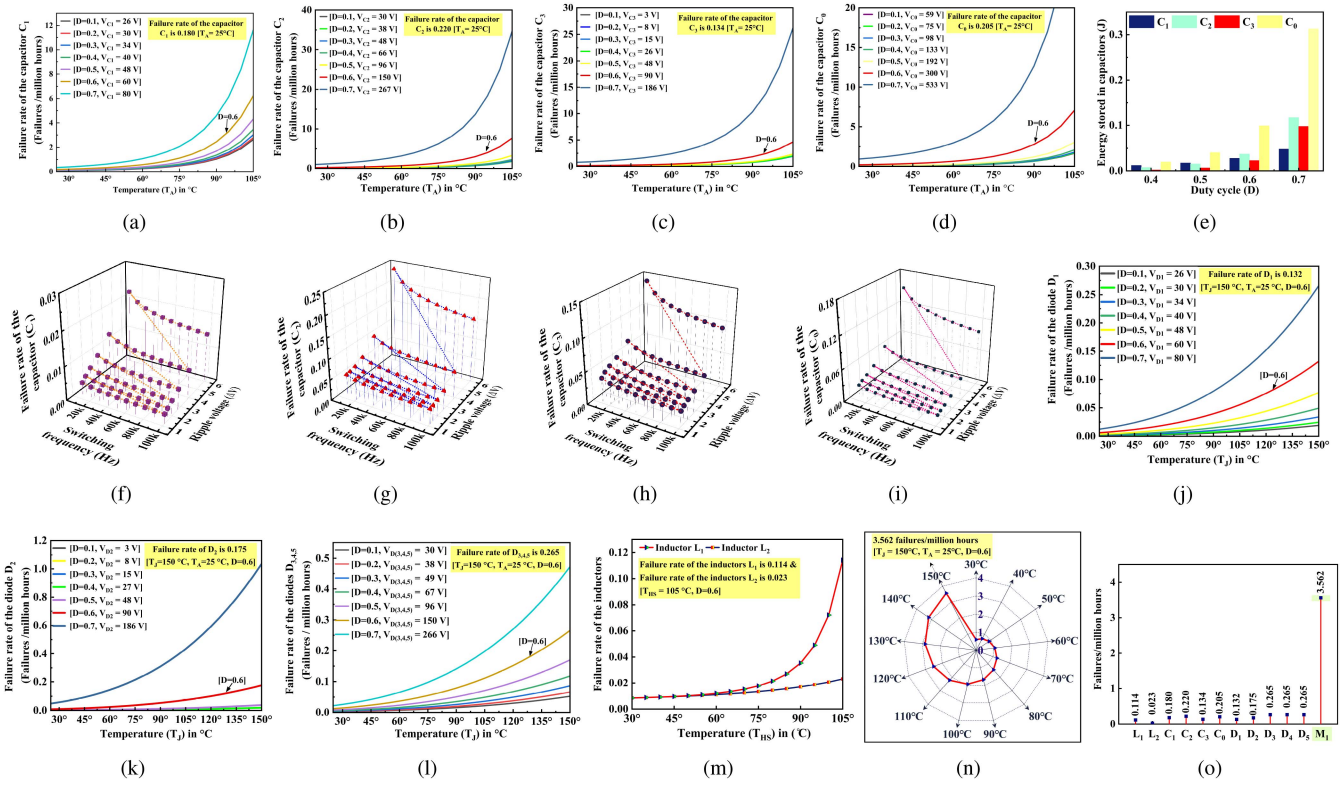


Fig. 9. Failure rate of capacitors (a) C_1, (b) C_2, (c) C_3, and (d) C_4. (e) Energy stored in capacitors; Impact of switching frequency and ripple voltage of capacitors: (f) C_1, (g) C_2, (h) C_3, and (i) C_4. Failure rate of diodes: (j) D_1, (k) D_2, and (l) $D_{3,4,5}$. (m) Failure of inductors: (L_1 and L_2). (n) Failure rate of the switch (M_1). (o) Failure rate per million hours for all components (T_A is the ambient temperature, T_J is the junction temperature, T_{HS} is the hot-spot temperature).

converter. The failure rate calculation can be estimated using different standards, such as MIL-HDBK-217F, Telcordia SR-322, Siemens SN 29500, FIDES, IEC-TR-62380, PRISM and 217 Plus, and China 299B/C [49]. Each standard has its own merits and demerits. In power electronic converters, the voltage stress of the semiconductor device and the rise-in-temperature in the component are the two essential features that determine the exact failure rate of the individual components. Perhaps the PRISM and 217 plus standard describes multiple environmental factors, but it does not account for the temperature rise in the component [49]. FIDES is a newer standard (2000 s), but it lacks the long-term historical validation of MIL-HDBK-217F and the calculation method is complex [49]. On the other hand, the MIL-HDBK-217F standard includes all electrical and electronic components with 14 different operational environments and temperature rise in components, which is one of the unique features. MIL-HDBK-217F uses component operating conditions, such as electrical stresses, thermal stresses, and environmental stresses [50], [51]. Therefore, MIL-HDBK-217F is simpler to determine the failure rate than the other standards available in the literature. The standard was re-reviewed and validated on 2 June 2022, which indicates that it is to be used for reliability of the equipment being designed. Therefore, component failure analysis is done for the proposed converter using the military handbook (MIL-HDBK-217F). The following values are considered to determine the failure rate of each component in the proposed converter. Ambient temperature is 25 °C, hot-spot temperature of inductor is 105 °C, and junction temperature of switch and diodes is 150 °C.

A. Capacitor

The failure rate of the capacitor directly depends on the voltage stress and ambient temperature (T_A). The failure rate of the capacitor can be obtained using the following expression:

$$\lambda_{\text{capacitor}} = \lambda_{b,n}\pi_{CV,n}\pi_Q\pi_E \tag{43}$$

where π_{CV} is the capacitance factor, π_Q is the quality factor, π_E is the environment factor, and λ_b is the base failure rate. The base failure rate of the capacitor varies with respect to the change in ambient temperature (T_A) and the voltage stress across the capacitors. Also, the capacitance factor (π_{CV}) depends on the value of capacitance used. The base failure rate of the capacitor can be obtained using (44):

$$\lambda_{b,n} = 0.00254\left[\left(\frac{S_n}{0.5}\right)^3 + 1\right]\exp\left(5.09\left(\frac{T_A + 273}{378}\right)^5\right). \tag{44}$$

The capacitance factor can be determined as follows:

$$\pi_{CV,n} = 0.34{C_n}^{0.18} \tag{45}$$

where n = 0,1,2,3. The value of π_Q and π_E is taken as 1. Fig. 9(a)–(d) shows the failure rate analysis of the capacitor plotted against the voltage stress and ambient temperature. From

Fig. 9(a)–(d), it is inferred that an increase of ambient temperature and voltage stress causes higher chances of failures/million hours. Based on the considered values, the failure rate of each capacitor is identified, and the values of C_1, C_2, C_3, and C_0 are 0.18, 0.22, 0.13, and 0.21 failures/million hours, respectively. Compared with other capacitors, the failure rate of the capacitors C_2 and C_0 is higher due to the higher voltage stress across C_2 and C_0 in the proposed converter.

1) Energy Stored in a Capacitor: The energy stored in a capacitor is proportional to the capacitance value and the voltage stress across the capacitor. The duty cycle selection and placement of the capacitor are two significant factors in deciding the voltage stress across the capacitor. The increase in voltage stress could directly increase the energy stored in the capacitor. The energy stored in the capacitors can be determined using (46):

$$E_{\text{cap},n} = \frac{1}{2} C_n V_{Cn}^2 \tag{46}$$

where n=0,1,2,3. Increased voltage stress and energy stored in the capacitor could simultaneously increase the power loss and create voltage spikes. Fig. 9(e) shows the energy stored in the individual capacitors.

2) Impact of Ripple Voltage and Switching Frequency: The failure rate of the capacitors depends on the selection of the capacitors. The selection of capacitors depends on the ripple voltage and switching frequency. Therefore, it is essential to discuss the impact caused by the switching frequency and voltage ripple of the capacitor. The failure rate of the individual capacitors can be determined using the following:

$$\lambda_{b,C1} = 0.0008636 \left[\left(\frac{S_1}{0.5}\right)^3 + 1\right] \exp\left(5.09\left(\frac{T_A+273}{378}\right)^5\right) \times \left[\frac{V_0 D}{R(1-D)^2 \Delta V_{C1} f_s}\right]^{0.18} \tag{47}$$

$$\lambda_{b,C2} = 0.0008636 \left[\left(\frac{S_2}{0.5}\right)^3 + 1\right] \exp\left(5.09\left(\frac{T_A+273}{378}\right)^5\right) \times \left[\frac{2V_0(1-D)}{R\Delta V_{C2} f_s}\right]^{0.18} \tag{48}$$

$$\lambda_{b,C3} = 0.0008636 \left[\left(\frac{S_3}{0.5}\right)^3 + 1\right] \exp\left(5.09\left(\frac{T_A+273}{378}\right)^5\right) \left[\frac{V_0 D}{R(1-D)\Delta V_{C3} f_s}\right]^{0.18} \tag{49}$$

$$\lambda_{b,C0} = 0.0008636 \left[\left(\frac{S_0}{0.5}\right)^3 + 1\right] \exp\left(5.09\left(\frac{T_A+273}{378}\right)^5\right) \times \left[\frac{V_0 D}{R\Delta V_{C0} f_s}\right]^{0.18}. \tag{50}$$

Using the above equations, the graph is plotted for different switching frequencies (f_s) and ripple voltages (ΔV_C). Fig. 9(f)–(i) shows the failure rate of the capacitor for various values of switching frequency and ripple voltage for C_1, C_2, C_3, and C_0, respectively. From Fig. 9(f)–(i), it is evident that the impact of voltage ripple with respect to failure rate is less when compared to the failure rate with respect to switching frequency. It is also noted that the failure rate of the capacitor increases for a lower switching frequency.

B. Diode

The failure rate of the diode depends on the junction temperature and voltage stress of the diode. The failure rate of the diode can be determined using the following expression:

$$\lambda_{\text{diode}} = \lambda_b \pi_T \pi_{S,n} \pi_C \pi_Q \pi_E. \tag{51}$$

where π_C is the contact construction factor, π_T is the temperature factor, and π_S is the electrical stress factor. The electrical stress factor (π_S) can be calculated based on the following expression:

$$\pi_{S,n} = 0.54(V_S \le 0.3), V_S^{2.43}(0.3 < V_S \le 1) \tag{52}$$

where n = 1,2,3,4,5. Also, the temperature factor (π_T) can be determined using the following expression:

$$\pi_T = \exp\left(-3091\left[\frac{1}{T_J+273} - \frac{1}{298}\right]\right) \tag{53}$$

where V_S is the voltage stress ratio and T_J is the junction temperature of the diode, the values of λ_b, π_C, π_Q, and π_E are 0.003, 1, 5.5, and 1, respectively. Fig. 9(j)–(l) shows the failure rate of the diodes D_1, D_2, and $D_{(3,4,5)}$, respectively. From Fig. 9(j)–(l), it is seen that the increase in voltage stress and temperature may increase the chances of failures/million hours. Based on the considered values, the failure rate of each capacitor is identified, and the values of D_1, D_2, and$D_{(3,4,5)}$ are 0.13, 0.18, and 0.27 failures/million hours, respectively.

C. Inductor

The failure rate of the inductor depends on the insulation class and hot-spot temperature (T_{HS}). The failure rate of the inductor can be calculated using the following expression:

$$\lambda_{\text{inductor}} = \lambda_b \pi_C \pi_Q \pi_E. \tag{54}$$

The base failure rate of the inductors L_1 and L_2 can be found using the (55) and (56)

$$\lambda_{b,1} = 0.000379 \exp\left(\frac{T_{\text{HS}}+273}{352}\right)^{14} \tag{55}$$

$$\lambda_{b,2} = 0.000319 \exp\left(\frac{T_{\text{HS}}+273}{364}\right)^{6.7}. \tag{56}$$

The values of π_C, π_Q, and π_E are taken as 1, 20, and 1, respectively. Based on the considered values, the failure rate of each inductor L_1 and L_2 are found to be 0.11 and 0.02 failures/million hours, respectively. Fig. 9(m) shows the failure rate of the inductors. An increase in hot-spot temperature increases the chances of failure.

D. Switch

The failure rate of the switch (M_1) is calculated using the following equation:

$$\lambda_{\text{MOSFET}} = \lambda_b \pi_T \pi_A \pi_Q \pi_E \tag{57}$$

where π_T is the temperature factor, π_A is the application factor, π_E is the environmental factor, and π_Q is the quality factor. The temperature factor π_T can be determined using the following expression:

$$\pi_T = \exp\left(-1925\left[\frac{1}{T_J + 273} - \frac{1}{298}\right]\right). \tag{58}$$

The values of π_A, π_E, π_Q, and λ_b are taken as 8, 1, 5.5, and 0.012, respectively. Based on the considered values, the failure rate of the switch (M_1) is calculated as 3.56 failures/ million hours. Fig. 9(n) shows the failure rate with respect to changes in the junction temperature of the switch. It is evident that the increase in junction temperature increases the chance of failure/million hours. The failure rate of each component is shown in Fig. 9(o). It is noted that the semiconductor switch (M_1) has a higher failure rate than other components in the proposed topology.

VIII. Conclusion

A new non-isolated quadratic-based converter topology with a single semiconductor switch has been proposed. The proposed converter is operated at a 60% duty cycle with a switching frequency of 50 kHz. The voltage gain of the proposed converter is 12.5 under CCM. The DCM and BCM of the proposed converter are explained. The mathematical expression for voltage stress and the current of the switch and diode are derived. The semiconductor switch and the output capacitors have low voltage stress compared to many other non-isolated topologies. The detailed comparison of different parameters, such as voltage gain and voltage stress of switch and capacitor, are analyzed with quadratic-based converters and other non-isolated converters. The experimental results for all the components of the proposed converter under CCM are portrayed. The efficiency and power density of the proposed converter is 91.8% and 37.71 W/in^3. The failure rate of each component has been determined using reliability analysis. Due to high voltage gain, less voltage stress, and high reliability, it is well-situated for photovoltaic and fuel cells.

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