Active Gate Driver With Auxiliary Branch for Current Sharing of Paralleled SiC MOSFETs

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***Abstract*—In high-power applications, paralleling silicon carbide MOSFETs is commonly adopted to overcome the current limitation of a single device and achieve higher current capability. However, imbalanced dynamic currents during the switching process can lead to uneven power and thermal distribution, negatively affecting the overall stability of the system. This article presents an active gate driver (AGD) that features an auxiliary driving branch designed to improve current sharing among the MOSFETs. The proposed AGD only requires a single switch to achieve the conversion of driving modes, reducing the complexity of the control program. Moreover, the proposed AGD enables multilevel driving resistance adjustment by controlling the activation time of the auxiliary branch. Experimental validation confirms the efficacy of the proposed AGD. Test results indicate that the presented AGD enhances current sharing performance across diverse load conditions while improving current sharing in dc–ac conversion scenarios. In addition, in experiments involving multiple parallel devices, the proposed AGD demonstrates exceptional current sharing performance.**

***Index Terms*—Active gate driver (AGD), auxiliary driving, parallel current sharing, silicon carbide (SiC) MOSFET.**

I. Introduction

In COMPARISON to silicon (Si) material, silicon carbide (SiC) presents several advantages, including ultra-low conduction losses, exceptional switching frequencies, superior thermal conductivity, and enhanced voltage withstand capabilities [1]. These characteristics render SiC metal oxide semiconductor field effect transistor (MOSFET) a compelling alternative to silicon-insulated gate bipolar transistors in high-voltage applications. In high-power scenarios, multiple devices are frequently employed in parallel to increase the current capacity of the power module, given the limitations of individual chip performance [2], [3]. However, the imbalance of current distribution in these parallel configurations poses a considerable challenge to the stability of power electronic systems [4], [5].

The imbalanced current in the parallel device arises from inconsistent device parameters and circuit characteristics. The inconsistent device parameters are mainly caused by the limitation of manufacturing process. In fact, SiC MOSFETs exhibit greater parameter dispersion than Si MOSFETs, adversely affecting current sharing [6], [7]. The effect of various device parameters on dynamic current sharing has been reviewed in [8]. As shown in [8], the dynamic parallel current is mainly affected by the threshold voltage (V_{th}) and the input capacitance (C_{iss}). In contrast, the static parallel current is mainly affected by the on resistance ($R_{\mathrm{ds\_on}}$). Unlike Si MOSFETs, the $R_{\mathrm{ds\_on}}$ of SiC MOSFETs varies with the drain-source voltage [7]. When the drain-source voltage of SiC MOSFETs is below 650 V, $R_{\mathrm{ds\_on}}$ shows positive temperature coefficient characteristics; however, when the voltage exceeds 3.5 kV, $R_{\mathrm{ds\_on}}$ changes to a negative temperature coefficient, which worsens the static current sharing.

The inconsistent circuit parameters are mainly caused by the asymmetric circuit structure. When there are multiple parallel devices in the circuit, the inherent limitation of PCB layout poses a significant challenge to achieving complete symmetry of each branch [8], resulting in parasitic impedance inconsistency among parallel branches. The dynamic currents are mainly affected by the source parasitic inductance (L_s) inconsistency, while the drain parasitic inductance (L_d) and gate parasitic inductance (L_g) inconsistencies have a relatively small effect [9]. However, when the drain current varies continuously during conduction, L_d and L_s can affect the static current sharing [10]. Therefore, the effect of L_d, L_s on static current sharing deserves careful consideration. Furthermore, due to the inherent delay in the gate driver chip, the time it takes for the signal to reach each SiC MOSFET can vary, exacerbating the current sharing problem [11], [12]. In addition, inconsistent driving resistances and driving voltages can also adversely affect current sharing [13].

Building on the previous analysis, addressing the current sharing issue is critical to improve the suitability of SiC MOSFETs for high-power applications. Currently, there are passive and active methods for current sharing. However, each method has inherent limitations.

The most straight passive current balancing approach is device screening [14], [15], [16]. [17] proposes a curve matching method for device screening. However, this method exhibits two major limitations: high implementation costs due to device parameter variations, and inability to compensate for circuit parasitic parameter mismatches. Another type of passive methods is to add passive components. Mao et al. [25] and Miao

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et al. [26] employ negative coupled inductors at the source terminals to compensate for parasitic inductance mismatches in parallel paths. However, these approaches lead to excessively bulky circuit configurations when scaling to multiple parallel devices. In addition, symmetrical circuit layouts can also improve parallel current sharing [18], [19], [20], [21], [22]. Specifically, Wang et al. [8] implement a Cu clip-bonding structure to balance source parasitic inductances among parallel devices, while He et al. [23] and Qu et al. [24] utilize decoupling capacitors to enforce identical current paths during switching transients. However, when the number of parallel devices is more than two devices, symmetrical layout is difficult to achieve. Also, it is required to redesign the power circuit. Furthermore, it is unable to compensate for the current imbalance caused by intrinsic device parameter variations.

Besides the above-mentioned passive methods, the active methods realize the current sharing by dynamically adjusting the parameters of the driving circuit to control the device current [27], [28], [29], [30]. Xue et al. [31] and Bortis et al. [32] control the driving signal delay to synchronize the parallel current edge. However, the current edge synchronization cannot eliminate the imbalance of the parallel current slope, which will cause the parallel SiC MOSFETs to withstand inconsistent current peaks and switching losses. In [33], the following SiC MOSFET gate voltage tracks the reference SiC MOSFET gate voltage. However, a consistent gate voltage cannot guarantee a consistent parallel current if the threshold voltages are different. Sasaki et al. [34] used a variable gate resistance to improve the parallel Si IGBT current sharing. While the switching speed of SiC MOSFET is faster than Si IGBT, the response speed of the proposed active gate driver (AGD) may not meet the requirements of SiC MOSFET. In addition, this method does not allow for multiple levels adjustment of the driving resistance, resulting in low accuracy adjustment of the driving resistances. He et al. [35] introduce a voltage-controlled current source to adjust the driving current dynamically during the switching process and changes the SiC MOSFETs switching trajectory to achieve current balancing. However, this method introduces additional source inductance in the power circuit, which may cause circuit current oscillation. Du et al. [36] and Wen et al. [37] propose dynamic gate voltage adjustment during switching transients to achieve current sharing in parallel devices. However, these methods require multiple switching actions with stringent timing coordination to avoid malfunctions. Moreover, Du et al. [36] relies on numerous integrated circuits (ICs) for current sensing, significantly increasing system complexity.

In summary, due to manufacturing process limitations of SiC MOSFETs, their device parameters exhibit considerable dispersion, leading to severe current imbalance problems [14]. In addition, current AGD methods still face challenges in structural and control complexity. To address these, this article proposes an AGD scheme that incorporates an auxiliary driving branch to dynamically adjust gate resistance, thereby compensating for current imbalance in parallel operation caused by device parameter mismatches. Compared with previous methods, the proposed AGD offers three main advantages.

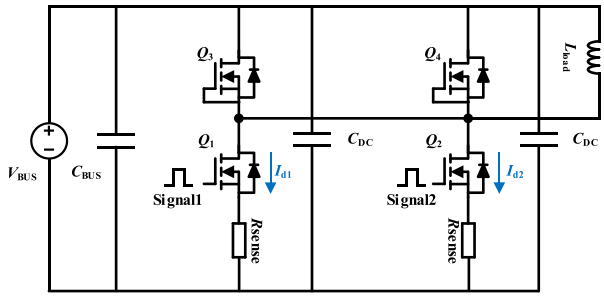

Fig. 1. Typical parallel circuit topology.

Simple control strategy: Only a single switch action is required for gate resistance adjustment, relaxing timing design constraints.

Simple circuit structure: Compared with existing methods, the proposed AGD reduces the number of IC chips.

Furthermore, unlike conventional variable gate resistance AGD methods, the proposed AGD introduces an additional control variable (auxiliary branch activation time), thereby enhancing flexibility in gate resistance tuning.

The rest of this article is organized as follows: Section II introduces the principle of the proposed AGD and current sharing. Section III presents the implementation of the proposed AGD. In Section IV, experimental results are provided to verify the effectiveness of the proposed AGD. Finally, Section V summarizes this article.

II. Principle of Proposed AGD and Current Sharing

This section examines the mechanism of parallel imbalanced current, proposing an AGD to improve current sharing among parallel devices. The principle of the AGD is described in detail within this section. The proposed AGD for current sharing is illustrated by a test circuit, as shown in Fig. 1. For convenience, two parallel branches are used as an example to demonstrate the principle of AGD. Q_1 and Q_2 are paralleled SiC MOSFETs. Q_1 is selected as the controlled device, Q_2 is selected as the reference device, Q_3 and Q_4 are freewheeling diodes, C_{DC} serves as the decoupling capacitor to provide a dynamic current path during the switching transient, R_{sense} is the Shunt resistor, C_{BUS} is the bus capacitor, V_{BUS} is the bus voltage source, and L_{load} serves as inductive load. I_{d1} and I_{d2} are the currents flowing through Q_1 and $Q_{2,}$ respectively.

A. Analysis of Imbalance Parallel Current

Fig. 2 illustrates the typical curves of imbalanced parallel current during the switching transient. Stage I to Stage VIII are defined by the state of Q_1.

As depicted in Fig. 2, the imbalanced parallel currents are characterized by inconsistent turn ON/OFF delay and inconsistent rising/falling current slopes.

1) Turn-on Transient: Fig. 2(a) shows the waveforms of the turn-ON transient. In Stage I, when the driving signal changes from negative to positive at t_1, the positive driving voltage starts

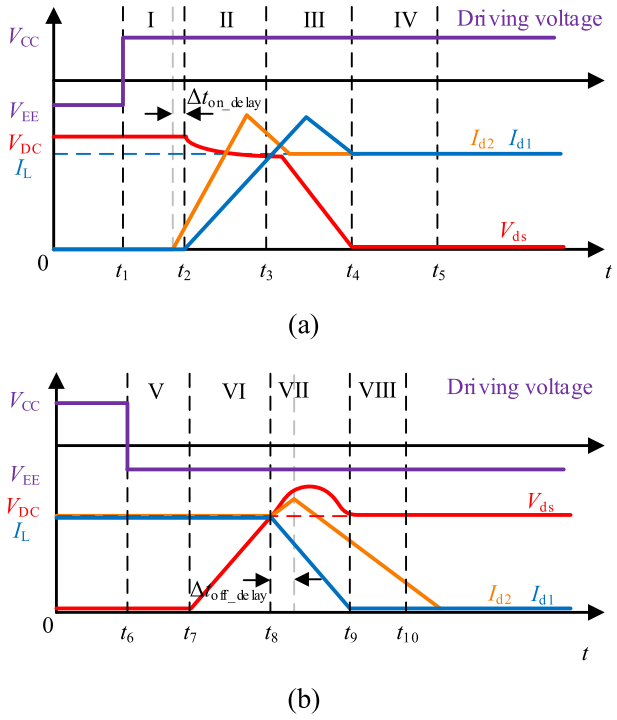

Fig. 2. Typical curves of imbalance parallel currents. (a) Turn-ON transient. (b) Turn-OFF transient.

to charge C_{iss} (C_{gs}+C_{gd}) of SiC MOSFET through the driving resistance R_{g_on}. This process can be equivalent to the first-order RC charging circuit. The duration of this stage can be calculated as

$$t_{\text{on\_delay}} = R_{\text{g\_on}} \cdot C_{\text{iss}} \cdot \ln\left(\frac{V_{\text{CC}} - V_{\text{EE}}}{V_{\text{CC}} - V_{\text{th}}}\right) \tag{1}$$

where V_{th} is the threshold voltage of SiC MOSFET. According to (1), the turn-ON delay difference of the parallel current can be calculated as

$$\begin{aligned}\Delta t_{\text{on\_delay}} &= t_{\text{on\_delay2}} - t_{\text{on\_delay1}} \\ &= (R_{\text{g\_on}} + \Delta R_{\text{g\_on}}) \cdot (C_{\text{iss}} + \Delta C_{\text{iss}}) \\ &\quad \cdot \ln\left(\frac{V_{\text{CC}} - V_{\text{EE}}}{V_{\text{CC}} - (V_{\text{th}} + \Delta V_{\text{th}})}\right) \\ &\quad - R_{\text{g\_on}} \cdot C_{\text{iss}} \cdot \ln\left(\frac{V_{\text{CC}} - V_{\text{EE}}}{V_{\text{CC}} - V_{\text{th}}}\right)\end{aligned} \tag{2}$$

where ΔR_{g_on}, ΔC_{iss}, and ΔV_{th} represent the variation of parameters between two parallel devices.

During Stage II, when the gate-source voltage V_{gs} exceeds V_{th}, the device current begins to rise. During this stage, the gate current satisfies

$$\begin{aligned}V_{\text{cc}} &= V_{\text{gs}} + L_s \frac{dI_{\text{don}}}{dt} + I_g \cdot R_g \\ I_g &= C_{\text{iss}} \cdot \frac{dV_{\text{gs}}}{dt}.\end{aligned} \tag{3}$$

The current flowing through the device can be calculated as

$$I_{\text{don}} = g_m \cdot (V_{\text{gs}} - V_{\text{th}}). \tag{4}$$

Combined (3) and (4), the current rising slope can be expressed as

$$\frac{dI_{\text{don}}}{dt} = g_m \frac{dV_{\text{gs}}}{dt} = \frac{g_m(V_{\text{CC}} - V_{\text{th}}) - I_{\text{don}}}{R_{g\_\text{on}} C_{\text{iss}} + L_S g_m} \tag{5}$$

where L_S is the source parasitic inductance, and g_m is the transconductance, representing the ratio of variation of I_d and V_{gs}. During this stage, the device current slope remains unchanged. Therefore, the current slope of the whole current rising process can be equivalent to the current slope when I_{don} reaches load current I_L [38]. The current slope satisfies

$$\frac{dI_{\text{don}}}{dt} = \frac{g_m(V_{\text{CC}} - V_{\text{th}}) - I_L}{R_{g\_\text{on}} C_{\text{iss}} + L_S g_m}. \tag{6}$$

Similarly, the parallel rising current slope difference satisfies

$$\begin{aligned}\Delta k_{\text{on}} &= \left|\frac{dI_{d2\text{on}}}{dt}\right| - \left|\frac{dI_{d1\text{on}}}{dt}\right| \\ &= \frac{(g_m + \Delta g_m) \cdot (V_{\text{CC}} - (V_{\text{th}} + \Delta V_{\text{th}})) - I_L}{(R_{g\_\text{on}} + \Delta R_{g\_\text{on}}) \cdot (C_{\text{iss}} + \Delta C_{\text{iss}}) + L_S \cdot (g_m + \Delta g_m)} \\ &\quad - \frac{g_m \cdot (V_{\text{CC}} - V_{\text{th}}) - I_L}{R_{g\_\text{on}} \cdot C_{\text{iss}} + L_S \cdot g_m}\end{aligned} \tag{7}$$

where Δg_m represents the transconductance variation of the parallel devices.

2) Turn-off Transient: As illustrated in Fig. 2(b), it is assumed that Q_1 has a faster turn-OFF speed than Q_2. Consequently, when Q_1 begins to turn OFF, Q_2 continues to conduct. This means that the total current flowing through both Q_1 and Q_2 remains constant, leading to a slight increase in I_{d2}. As Q_2 starts to turn OFF, I_{d2} begins to decrease, and the load current begins to switch to the freewheeling diode. From the analysis above, the turn-OFF delay difference between Q_1 and Q_2 ($\Delta t_{\text{off\_delay}}$) is shown in Fig. 2(b). Since the turn-OFF transient is like the turn-ON transient, the theoretical analysis is not repeated here. Consequently, the turn-OFF delay difference and current slope difference between the parallel devices satisfy

$$\begin{aligned}\Delta t_{\text{off\_delay}} &= R_{g\_\text{off}} \cdot C_{\text{iss}} \cdot \ln\left(1 - \frac{\Delta V_{\text{mil}}}{V_{\text{EE}} - V_{\text{mil}}}\right) \\ &\quad + \Delta R_{g\_\text{off}} \cdot C_{\text{iss}} \cdot \ln\left(\frac{V_{\text{EE}} - V_{\text{CC}}}{V_{\text{EE}} - V_{\text{mil}} - \Delta V_{\text{mil}}}\right)\end{aligned} \tag{8}$$

and

$$\begin{aligned}\Delta k_{\text{off}} &= \left|\frac{dI_{d2\text{off}}}{dt}\right| - \left|\frac{dI_{d1\text{off}}}{dt}\right| \\ &= -\frac{(I_L - g_m \cdot (V_{\text{EE}} - V_{\text{th}})) \cdot C_{\text{iss}}}{(R_{g\_\text{off}} C_{\text{iss}} + L_S g_m) \cdot ((R_{g\_\text{off}} - \Delta R_{g\_\text{off}}) C_{\text{iss}} x + L_S g_m)} \\ &\quad \cdot \Delta R_{g\_\text{off}} \cdot \\ &\quad + \frac{g_m}{(R_{g\_\text{off}} - \Delta R_{g\_\text{off}}) \cdot C_{\text{iss}} + L_S g_m} \cdot \Delta V_{\text{th}}\end{aligned} \tag{9}$$

where V_{mil} is Miller voltage. By combining (2), (7), (8), and (9), it is possible to offset the current imbalances by modifying the driving resistance. This article introduces a main-auxiliary

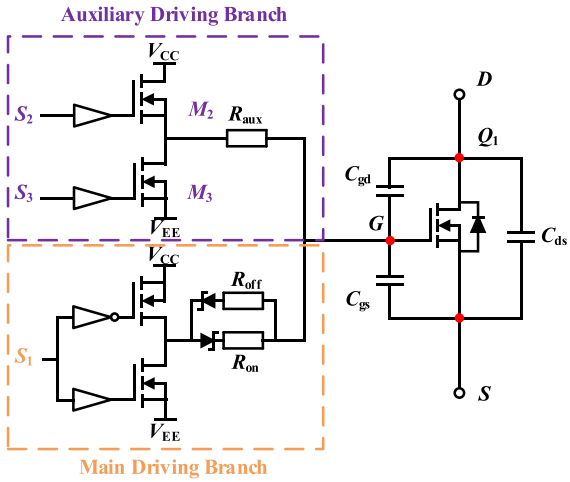

Fig. 3. Proposed MADC.

TABLE I
DRIVING MODE DEFINITION

	S_3	S_2	S_1
Mode I	0	0	1
Mode II	0	0	0
Mode III	0	1	1
Mode IV	1	0	0

driving circuit (MADC) that dynamically adjusts the driving resistance throughout the switching process. The working principle of this circuit will be discussed in the following section.

B. Variable Driving Resistance Principle

Fig. 3 shows the proposed MADC. As depicted in Fig. 3, the main driving branch consists of a push-pull circuit and driving resistances $R_{\rm on}$, $R_{\rm off}$. On the other hand, the auxiliary driving branch consists of a push-pull circuit and connected to the gate of the controlled device through $R_{\rm aux}$. $C_{\rm gd}$, $C_{\rm gs}$, and $C_{\rm ds}$ are the junction capacitances of the SiC MOSFET.

S_1 serves as the main driving signal, which controls the turn-ON/OFF of Q_1. S_2 and S_3 are auxiliary driving signals that adjust the driving resistance dynamically during the turn ON/OFF transient.

The proposed AGD has four working modes, which depend on the logical states of S_1, S_2, and S_3. Accordingly, the definition of the specific drive mode is given in Table I. Modes I and III are used in the turn-ON transient, and Modes II and IV are used in the turn-OFF transient. In each model, the driving resistance satisfies

$$R_g = \begin{cases} R_{\rm on} & \text{Mode I} \\ R_{\rm off} & \text{Mode II} \\ R_{\rm on}//R_{\rm aux} & \text{Mode III} \\ R_{\rm off}//R_{\rm aux} & \text{Mode IV} \end{cases}. \tag{10}$$

For simplicity, Stage I can be used as a reference to illustrate the principle of variable driving resistance. During this stage, the positive driving power supply $V_{\rm CC}$ charges the $C_{\rm iss}$ of the device through the driving resistance. The gate-source voltage

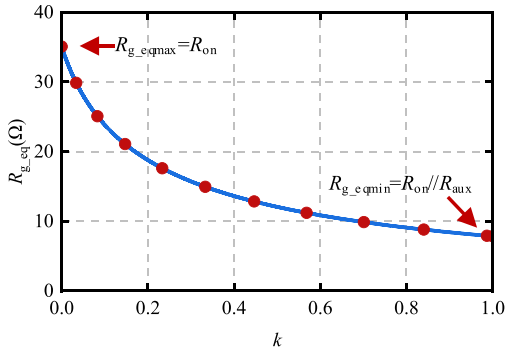

Fig. 4. Relationship between R_{g_eq} and k.

$V_{\rm gs}$ satisfies

$$V_{\rm gs} = V_{\rm CC} + (V_{\rm EE} - V_{\rm CC}){\rm e}^{-\frac{t}{R_g C_{\rm iss}}} \tag{11}$$

where $V_{\rm CC}$ is the positive driving voltage, and $V_{\rm EE}$ is the negative driving voltage. The charge of the $C_{\rm iss}$ can be calculated as

$$\begin{aligned} Q_g &= C_{\rm iss}\int_0^{t_{\rm stage1}} \frac{{\rm d}V_{\rm gs\_eq}}{{\rm d}t}{\rm d}t \\ &= C_{\rm iss}\int_0^{t_{s21}} \frac{{\rm d}V_{\rm gs(1)}}{{\rm d}t}{\rm d}t + C_{\rm iss}\int_{t_{s21}}^{t_{\rm stage1}} \frac{{\rm d}V_{\rm gs(3)}}{{\rm d}t}{\rm d}t \end{aligned} \tag{12}$$

where Q_g is the charge of $C_{\rm iss}$ in Stage I, $t_{\rm stage1}$ represents duration of stage I, t_{s21} represents the action time of Mode III during Stage I, and $t_{s21} \in [0, t_{\rm stage1}]$, ${\rm d}V_{\rm gs}(1)/{\rm d}t$ and ${\rm d}V_{\rm gs}(3)/{\rm d}t$ are the gate-source voltage slope under Mode I and Mode III, respectively. ${\rm d}V_{\rm gs\_eq}/{\rm d}t$ is the equivalent gate-source voltage slope during Stage I. Differentiating (11) and substituting into (12) yields

$${\rm e}^{-\frac{t_{\rm stage1}}{R_{g\_eq}C_{\rm iss}}} = {\rm e}^{-\frac{t_{s22}}{R_{\rm on}//R_{\rm aux}C_{\rm iss}}} + {\rm e}^{-\frac{t_{\rm stage1}}{R_{\rm on}C_{\rm iss}}} - {\rm e}^{-\frac{t_{s22}}{R_{\rm on}C_{\rm iss}}}. \tag{13}$$

In order to facilitate the description of the relationship between R_{g_eq} and t_{s21}, t_{s21} is redefined as

$$t_{s21} = k\, t_{\rm stage1} \tag{14}$$

where $k \in [0, 1]$. Combining with (13) and (14), the relationship between R_{g_eq} and k is shown in Fig. 4, which illustrates that R_{g_eq} can be controlled by adjusting t_{s21}. According to Fig. 4, the adjustment range of R_{g_eq} satisfies

$$R_{g\_eq} \in [R_{\rm on}//R_{\rm aux}, R_{\rm on}]. \tag{15}$$

In other stages, the equivalent driving resistance can be adjusted by modifying the on-time of S_2 and S_3, similar to Stage I.

C. Synchronization of Imbalance Parallel Current

The proposed AGD illustrated in Fig. 5 is used to achieve synchronization of imbalance parallel currents, which mainly consists of four parts.

1) *Main-Auxiliary driving unit:* As depicted in Fig. 5(b), the orange part is the main driving branch, which is controlled

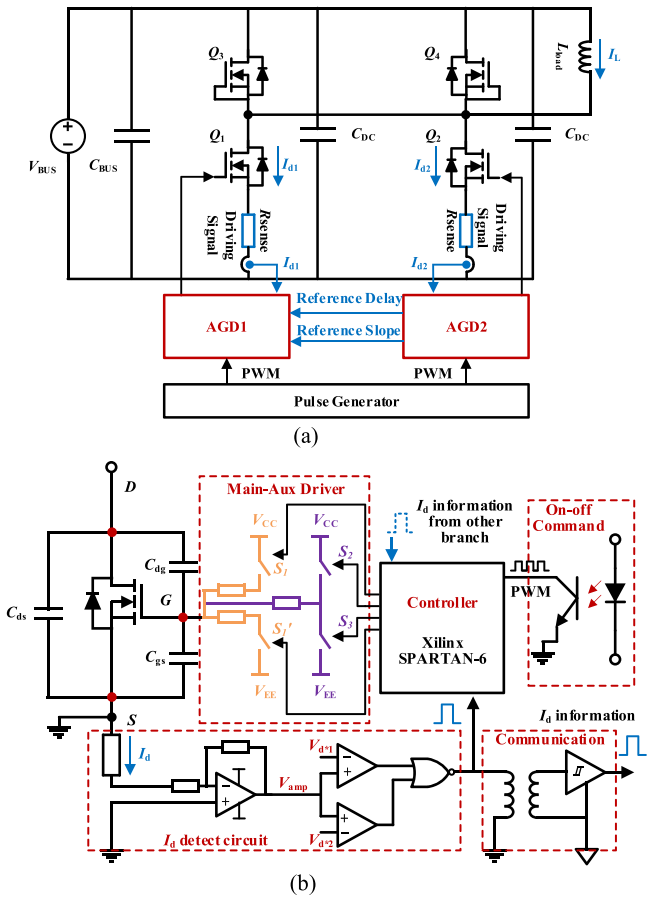

Fig. 5. Parallel current synchronization principle. (a) Overall circuit structure. (b) Proposed AGD.

by S_1, and the purple part is the auxiliary driving branch, which is controlled by S_2 and S_3.

2) *I_d detection unit:* It detects the current flowing through the SiC MOSFET I_d and transforms the information into a digital signal.

3) *Controller unit:* It generates the control signal according to the current information.

4) *Communication unit:* It transmits the current information between the reference branch and the controlled branch.

Fig. 6 shows the process of imbalance parallel current synchronization. The synchronization process consists of switching delay and current slope synchronization. This section will discuss the synchronization process in detail.

1) Synchronization of Switching Delay: As shown in Fig. 6(a) and (b), there exist time delay errors and current slew rate errors between parallel-connected currents.

First, the turn ON/OFF delay errors between parallel currents need to be synchronized. One current path is selected as the reference (e.g., I_{d2} is taken as the reference). Based on the time delay error between the regulated current (I_{d2}) and the reference current in the present cycle, the operating time of the auxiliary branch in the next cycle is adjusted. The adjustment time should satisfy

$$t_{s21}[N+1] = t_{s21}[N] + \Delta t_{s21} \tag{16}$$

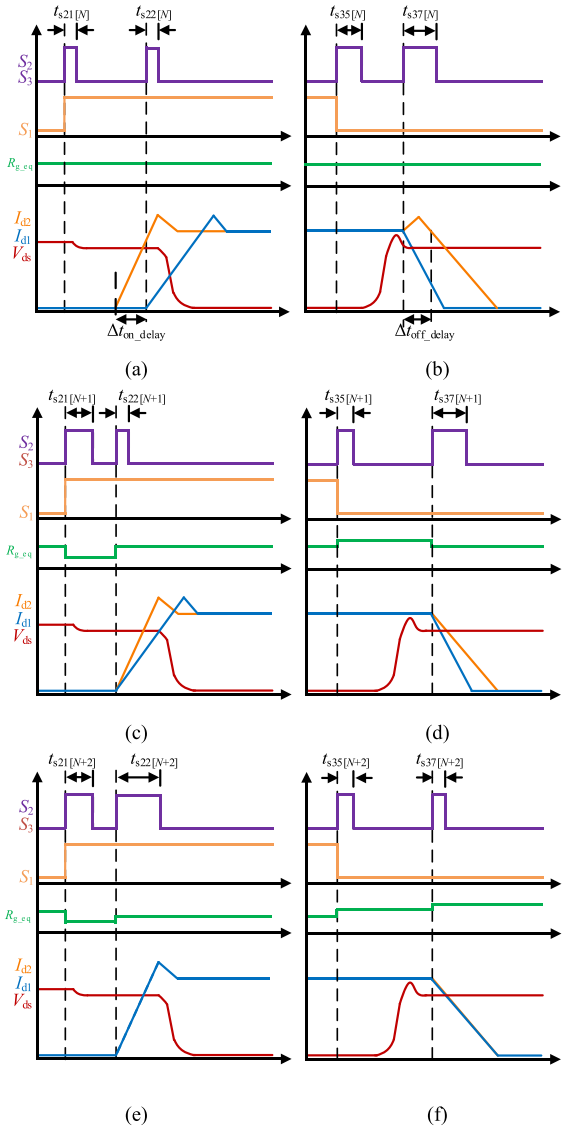

Fig. 6. Process of imbalance parallel current synchronization. (a) Imbalance turn-ON parallel current. (b) Imbalance turn-OFF parallel current. (c) Turn-ON delay synchronization. (d) Turn-OFF delay synchronization. (e) Turn-ON current slope synchronization. (f) Turn-OFF current slope synchronization.

$$t_{s35}[N+1] = t_{s35}[N] + \Delta t_{s35} \tag{17}$$

where N is an integer greater than 0, representing the number of switching cycles. Δt_{s21} is the increased action time of Mode III in the next switching cycle during Stage I, and Δt_{s35} is the increased action time of Mode IV in the next switching cycle during Stage V.

2) Synchronization of Parallel Current Slopes: After synchronizing the turn ON/OFF delay, the proposed AGD starts to synchronize the parallel current slopes.

Similar to the turn ON/OFF delay synchronization, the parallel current slopes synchronization is achieved by adjusting the action time (t_{s22} and t_{s37}) of Mode III and Mode IV during Stage II and Stage VII, as shown in Fig. 7. Therefore, during these stages, the action time of Mode III and Mode IV in the

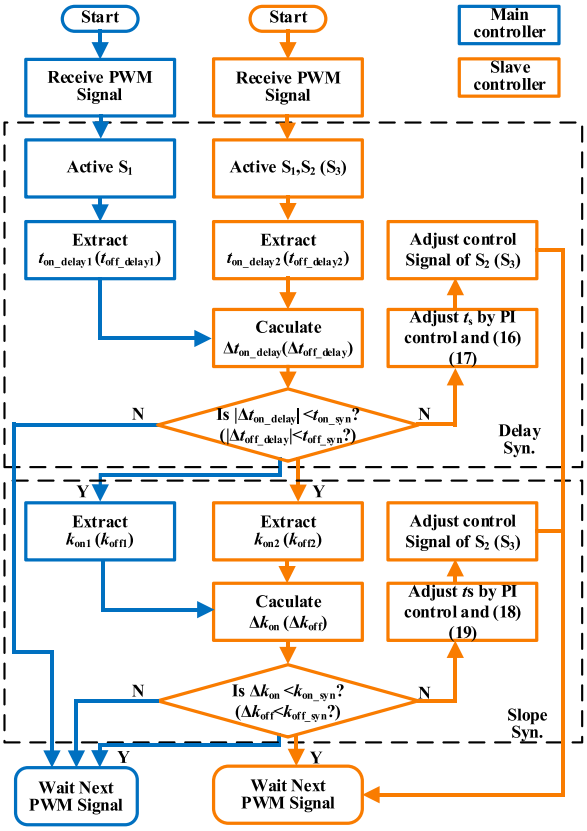

Fig. 7. Synchronization algorithms schematic.

TABLE II
ON-TIME ADJUSTMENT OF S_2 AND S_3

	t_{s21}	t_{s22}	t_{s35}	t_{s37}
$\Delta t_{on\_delay}>0$ (<0)	↓ (↑)	–	–	–
$\Delta t_{off\_delay}>0$ (<0)	–	–	↓ (↑)	–
$\Delta k_{on}>0$ (<0)	–	↑ (↓)	–	–
$\Delta k_{off}>0$ (<0)	–	–	–	↑ (↓)

next switching cycle can be calculated as

$$t_{s22}[N+1] = t_{s22}[N]+\Delta t_{s22} \tag{18}$$

$$t_{s37}[N+1] = t_{s37}[N]+\Delta t_{s37} \tag{19}$$

where Δt_{s22} is the increased action time of Mode III in the next switching cycle during Stage II and Δt_{s37} is the increased action time of Mode IV in the next switching cycle during Stage VII.

Combined with the definition of ΔR_g and Fig. 4, the action time of Mode III and Mode IV is inversely related to ΔR_g. Table II presents the on-time adjustment trend of Mode III and Mode IV under different turn ON/OFF delay differences and parallel current slope differences. In addition, the method of adjusting the on-time of S_2 and S_3 at various stages will be discussed in the next section.

$I_{d(1)}$	$I_{d(2)}$	...	$I_{d(n-1)}$	$I_{d(n)}$
PI_1	PI_2	...	PI_{n-1}	PI_n

Fig. 8. Establish lookup table.

D. Parallel Current Synchronization Algorithm

Based on the analysis in Section II-C, the control algorithm is divided into two parts: Turn ON/OFF delay synchronization and current slope synchronization, as illustrated in Fig. 7. In addition, the proposed AGD achieves multiple parallel devices current sharing through reference-following control, which will also be introduced in this section.

1) Design of the Synchronization Algorithm: As depicted in Fig. 7, the synchronization algorithm consists of two sequential stages: delay synchronization and slope synchronization. The slope synchronization stage is activated only after the delay synchronization condition is satisfied $|\Delta t_{\text{on\_delay}}| < t_{\text{on\_syn}}$ or $|\Delta t_{\text{off\_delay}}| < t_{\text{off\_syn}}$. Subsequently, the current slope is continuously regulated until the slope synchronization criteria are met ($|\Delta k_{\text{on}}| < k_{\text{on\_syn}}$ or $|\Delta k_{\text{off}}| < k_{\text{off\_syn}}$). To mitigate potential oscillations induced by the PI controller, both $t_{\text{on\_syn}}$ ($t_{\text{off\_syn}}$) and $k_{\text{on\_syn}}$ ($k_{\text{off\_syn}}$) are set to a value slightly larger than zero. Furthermore, to address the control performance degradation caused by fixed PI parameters under varying switching current magnitudes, this article adopts a look-up table method to achieve adaptive adjustment of PI parameters. As shown in Fig. 8, the optimal PI parameters for different current levels are determined empirically and stored in a parameter table. In the process of current sharing, the corresponding PI parameters are obtained by referencing the table based on the switching current magnitudes, thereby enabling dynamic adjustment of PI parameters and enhancing the control performance of the proposed AGD under varying switching current magnitudes.

In addition, as shown in Fig. 6(a) and (b), the initial value of the action time of the auxiliary branch should be carefully designed so that the driving resistance of the parallel branch is consistent in the initial state.

2) Design of Multiple Parallel Devices Control Algorithm: To achieve higher power capacity and larger current, it is common to use more than two SiC MOSFETs in parallel. The commonly adopted methods for controlling multiple parallel SiC MOSFETs include daisy chain control, average value control, and reference-following control. Compared with the other methods, reference-following control has faster dynamic control speed [37]. Therefore, it is utilized to ensure current sharing among the multiple parallel devices in the proposed AGD. As illustrated in Fig. 9, the main branch current information is transmitted to the local controller of the following branch through the communication circuit. The local controller calculates the $\Delta t_{\text{on\_delay}}$ ($\Delta t_{\text{off\_delay}}$) and Δk_{on} (Δk_{off}) and takes them as the PI control input. By adjusting the auxiliary branch action time t_s through the PI controller, the Δt_{delay} and Δk are tracked to the expected value 0, which means the reference-following branch current synchronization is realized.

TABLE III
EXPRESSION OF ΔR_{g_ON} AND ΔR_{g_OFF}

Condition	Expression of ΔR_{g_on} and ΔR_{g_off}	ΔR_{g_on} and ΔR_{g_off} min	max
Turn_on delay Syn.	$\Delta R_{g\_on} = \frac{R_{g\_on} \cdot C_{iss} \cdot \ln\left(\frac{V_{CC}-V_{EE}}{V_{CC}-V_{th}}\right)}{(C_{iss}+\Delta C_{iss}) \cdot \ln\left(\frac{V_{CC}-V_{EE}}{V_{CC}-(V_{th}+\Delta V_{th})}\right)} - R_{g\_on}$	−3.3 Ω	4.3 Ω
Rising current slope Syn.	$\Delta R_{g\_on} = \frac{((g_m+\Delta g_m)\cdot(V_{CC}-(V_{th}+\Delta V_{th}))-I_L)\cdot(R_{g\_on}\cdot C_{iss}+L_S\cdot g_m)}{(g_m\cdot(V_{CC}-V_{th})-I_L)\cdot(C_{iss}+\Delta C_{iss})} - \frac{L_S\cdot(g_m+\Delta g_m)}{(C_{iss}+\Delta C_{iss})} - R_{g\_on}$	−10.2 Ω	7.9 Ω
Turn_off delay Syn.	$\Delta R_{g\_off} = \frac{R_{g\_off} \cdot C_{iss} \cdot \ln\left(\frac{V_{EE}-V_{CC}}{V_{EE}-V_{mil}}\right)}{(C_{iss}+\Delta C_{iss}) \cdot \ln\left(\frac{V_{EE}-V_{CC}}{V_{EE}-(V_{mil}+\Delta V_{mil})}\right)} - R_{g\_off}$	−3.1 Ω	3.9 Ω
Falling current slope Syn.	$\Delta R_{g\_off} = \frac{(I_L-(g_m+\Delta g_m)\cdot(V_{EE}-(V_{th}+\Delta V_{th})))\cdot(R_{g\_off}\cdot C_{iss}+L_S\cdot g_m)}{(I_L-g_m\cdot(V_{EE}-V_{th}))\cdot(C_{iss}+\Delta C_{iss})} - \frac{L_S\cdot(g_m+\Delta g_m)}{(C_{iss}+\Delta C_{iss})} - R_{g\_off}$	−7.1 Ω	8.0 Ω

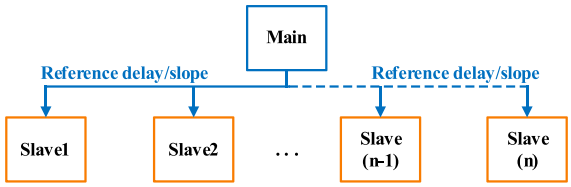

Fig. 9. reference-following control topology.

III. IMPLEMENTATION OF THE AGD

According to Fig. 4, the proposed AGD consists of four parts: MADC, I_d detection unit, control unit, and communication unit. This section introduces the design process and working principle of each part in detail.

A. Implementation of the MADC

Determination of the adjustment range of the driving resistance: The design of the driving resistance is crucial for successfully implementing the proposed AGD. The current regulation ability of the proposed AGD depends on the adjustable range of the driving resistance. When current balancing is achieved among parallel devices, both the switching timing error and current slew rate error between parallel devices become zero. The corresponding gate resistance adjustment values, derived from (2), (7), (8), and (9), are summarized in Table III. According to Table III, the selection of gate resistance values depends on both the parameter variations of the devices and the magnitude of I_L. In this work, it assumes that C_{iss} and g_m fluctuate within ±5% of their nominal values, while V_{th} varies within ±20% of its nominal value [14]. The current ranges from zero to the maximum continuous current rating of the device. All device parameters are obtained from the official datasheet of C3M0032120K. The extremum values of gate resistance within the constrained range are determined using the quasi-Newton method, with the results presented in Table III. When designing the gate resistance values, the variation range should satisfy the following conditions.

During turn ON transient:

$$\begin{aligned} R_{g\_eq}\min &= R_{on}//R_{aux} < 20\,\Omega - 10.2\,\Omega = 9.8\,\Omega \\ R_{g\_eq}\max &= R_{on} > 20\,\Omega + 7.9\,\Omega = 27.9\,\Omega. \end{aligned} \tag{20}$$

During turn off transient:

$$\begin{aligned} R_{g\_eq}\min &= R_{off}//R_{aux} < 20\,\Omega - 7.1\,\Omega = 12.9\,\Omega \\ R_{g\_eq}\max &= R_{off} > 20\,\Omega + 8.0\,\Omega = 28\,\Omega. \end{aligned} \tag{21}$$

Based on the above-mentioned analysis and considering a 30% design margin, the final selected values are determined as

$$R_{on} = 35\,\Omega, R_{off} = 35\,\Omega, R_{aux} = 10\,\Omega. \tag{22}$$

B. Implementation of the I_d Detection Unit

In general, the I_d is measured by assessing the voltage across both ends of the Kelvin inductor during the current conversion process [39]. This approach necessitates careful design of the parameters within the *RC* integral detection circuit. In this AGD, to simplify design, a low-resistance sensing resistor (R_{sense}) is connected in series with the device to measure its current. During switching transients (turn-ON and turn-OFF), the voltage across R_{sense} is amplified to exact the device current I_d. Furthermore, to minimize the adverse effects of parasitic inductance (which can lead to dynamic current oscillations) and reduce the impact of R_{sense} variations on current-sharing performance [40], the

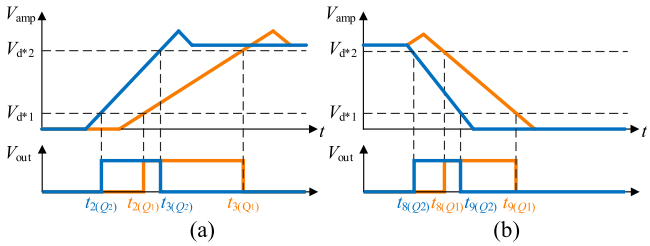

Fig. 10. Relationship between V_{out} and V_d. (a) Turn-ON transient. (b) Turn-OFF transient.

proposed AGD utilizes a low-resistance (1 mΩ), low-inductance (<2 nH), and high-precision (±1%) shunt resistor as R_{sense}. In practice, the bandwidth of the amplifier should be greater than the equivalent bandwidth of the current rising/falling edges of SiC MOSFETs, such as 5–10 times higher [35]. The equivalent bandwidth satisfies

$$\text{BW} = \frac{0.35}{t_r} \tag{23}$$

where t_r represents the current rising time. In this experiment, t_r is about 100 ns. The operational amplifier is selected as OPA847 from TI, whose bandwidth is much higher than the equivalent bandwidth of SiC MOSFET. In addition, using a window comparator (WCP) to capture the device current information. The WCP consists of TLV3502, whose propagation delay is about 7 ns.

To illustrate the detection working process, Fig. 10 shows the typical waveform of the I_d detection unit. During turn-ON process, as soon as the I_d starts to rise, the output of the amplifier will increase with the rising current. Once the amplifier output voltage V_{amp} exceeds V_{d*1}, the output voltage of WCP changes from negative to positive. When the V_{amp} continues to rise beyond V_{d*2}, WCP generates a negative voltage. Meanwhile, the output of WCP is transmitted not only to its control unit but also to the control unit of other branches. The $\Delta t_{\text{on\_delay}}$ can be calculated as

$$\Delta t_{\text{on\_delay}} = t_2(Q_2) - t_2(Q_1). \tag{24}$$

In addition, the current rises approximately at a constant slope, which satisfies

$$\frac{\mathrm{d}I_{\text{don}}}{\mathrm{d}t} = k\frac{V_{d*2} - V_{d*1}}{t_3(Q_i) - t_2(Q_i)} (i = 1, 2) \tag{25}$$

where k is the ratio of V_{amp} and I_d. i represents the ith branch. According to (25), The Δk_{on} can be equivalent to

$$\Delta k_{\text{on}} \Leftrightarrow (t_3(Q_2) - t_2(Q_2)) - (t_3(Q_1) - t_2(Q_1)). \tag{26}$$

During the turn-OFF process, when the I_d starts to fall, the V_{amp} will decrease with the falling current. Once the V_{amp} is lower than V_{d*2}, the output of WCP changes from negative to positive.

When the V_{amp} continues to fall beyond V_{d*1}, WCP generates a negative voltage. Similar to the turn-ON process, the $\Delta t_{\text{off\_delay}}$, and Δk_{off} can be equivalent as

$$\Delta t_{\text{off\_delay}} = t_8(Q_2) - t_8(Q_1) \tag{27}$$

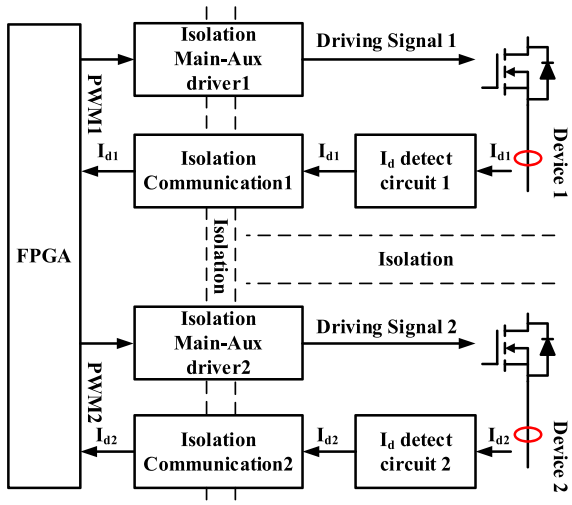

Fig. 11. Alternative scheme of signal FPGA.

$$\Delta k_{\text{off}} \Leftrightarrow (t_9(Q_2) - t_8(Q_2)) - (t_9(Q_1) - t_8(Q_1)). \tag{28}$$

Similarly, the output of WCP is not only transmitted to its own control unit, but also to the control unit of other branches.

C. Implementation of the Control Unit

This article employs an FPGA as the control unit, with clock frequency and internal resources being the key considerations during device selection. From (24) to (28), the proposed AGD calculates the switching delay and current slope based on the clock of the controller. A higher clock frequency improves time resolution, thereby enhancing the system's control accuracy. Although a higher clock frequency enhances control accuracy, it also raises system costs. Thus, FPGA selection requires a careful tradeoff between control accuracy and cost. In addition, to ensure the control accuracy, the clock frequency should be more than 200 MHz when an FPGA is used as the active gate drive controller to realize multibranch parallel current sharing [37]. Considering comprehensively, this article selects the Spartan-6 from Xilinx as the control chip. This chip has a maximum clock frequency of 360 MHz, and the calculation error is less than 3 ns, which meets the control accuracy requirements.

The proposed control architecture employs a dedicated FPGA configuration for each individual branch circuit. In practical engineering applications, for multibranch parallel structures, the control architecture shown in Fig. 11 can be adopted to enhance the integration level of AGD and reduce its cost. Taking two parallel branches as an example, where Device 1 serves as the reference branch and Device 2 acts as the controlled branch, the current information from each branch is isolated and transmitted to the FPGA for processing. The FPGA then generates driving signals based on the current information to achieve current sharing between parallel branches. It should be noted that when the FPGA executes the current-sharing program for two parallel branches, its internal resource utilization reaches 20%. Each additional parallel branch increases resource utilization by approximately 20%. Therefore, when employing

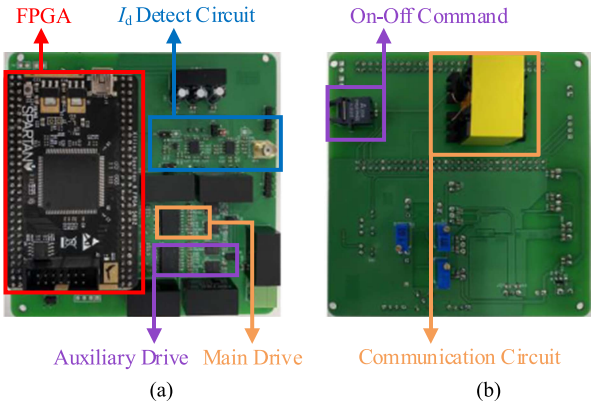

Fig. 12. Prototype of the proposed AGD. (a) Front side. (b) Back side.

the control architecture shown in Fig. 11, attention must be paid to the FPGA's internal resource usage.

D. Implementation of the Communication Unit

The isolated signal transformer serves as the communication unit for transmitting signals between branches. The magnetic core material of the transformer is PC50, and the turns of the primary and secondary windings are both 20 turns. It should be noted that the design of the control program takes into account the impact of the communication unit on switching delay errors, which is approximately a fixed time of 10 ns. Using an isolation transformer to transmit the signal has the advantages of a simple structure and low cost.

IV. Experimental Verification

This section describes the proposed AGD prototype and test platform. In addition, current sharing experiments under different load conditions and multidevice current sharing experiments are carried out to verify the effectiveness of the proposed AGD.

A. Test and Measurement Setup

A prototype is carried out to evaluate the effectiveness of the proposed AGD, as shown in Fig. 12.

The experimental platform is shown in Fig. 13. The selected SiC MOSFET is C3MM0032120K from Wolf-speed, and its recommended driving voltage is 15 and -5 V.

The detailed parameters of the power circuit, the proposed AGD circuit, and the measurements are listed in Table IV. Using scope MDO3024 from Tektronix records the details of the waveform; its wideband is 200 MHz, and its sampling rate is 2.5 G.

B. Experimental Results

The experiments were conducted at 400 V and 40 A to verify the effectiveness of the proposed AGD. The results of the experiments are illustrated in Figs. 14 and 15. The experimental results demonstrate that the proposed AGD during the switching process effectively enhances current sharing. The dynamic current difference is significantly reduced from 3.63 to 1.1 A

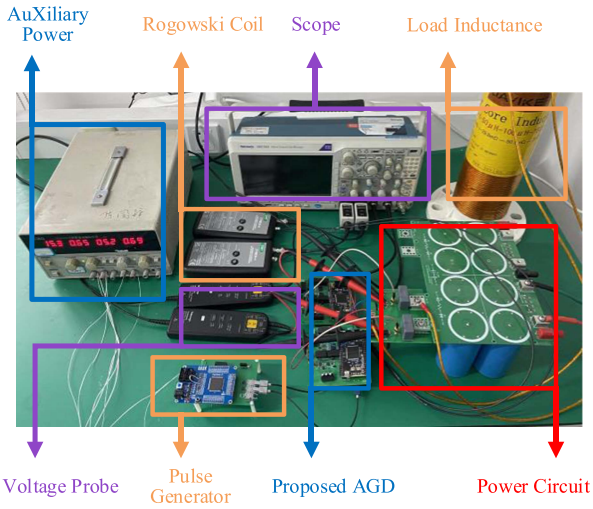

Fig. 13. Experimental platform.

TABLE IV
Information of Test Circuit and Measurement Equipment

Item		Information
Power Circuit	SiC MOSFET	C3M0032120K
	C_{BUS}	200 μF
	C_{DC}	10 μF
	L_{load}	200 μH
AGD Circuit	Drive Chip	UCC21520
	R_{on}/R_{off}	35 Ω
	R_{aux}	10 Ω
	Isolated power	QA151M
	Amplifier	OPA847
	Comparator	TLV3502
FPGA	Control Chip	Xilinx SPARTAN-6
Measurement	Voltage Probe	Tektronix THDP90200
	Rogowski Coil	PEM CWT Ultra-mini
	Oscilloscope	Tektronix MDO3024

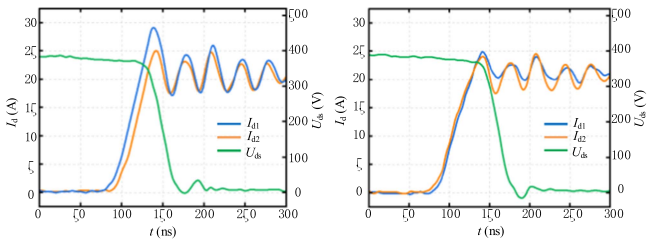

Fig. 14. Experimental waveform of two paralleled devices during the turn-ON process. (a) Without AGD. (b) With AGD.

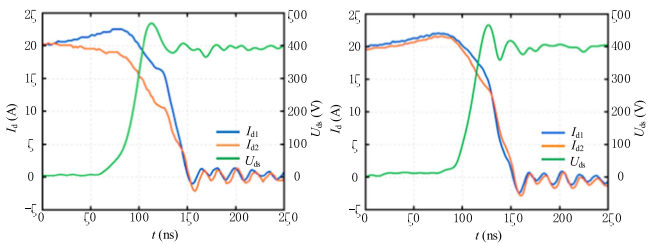

Fig. 15. Experimental waveform of two paralleled devices during the turn-OFF process. (a) Without AGD. (b) With AGD.

TABLE V
EXPERIMENTAL RESULTS OF 400 V AND 40 A

		E_{loss1} (μJ)	E_{loss2} (μJ)	ΔE_{loss} (μJ)	λ
Turn-on	w/o AGD	207.8	257.1	49.3	21.2%
	with AGD	248.8	239.8	9.0	3.6%
Turn-off	w/o AGD	196.0	139.4	56.6	33.7%
	with AGD	184.4	170.1	14.3	7.9%

TABLE VI
EXPERIMENTAL RESULTS OF DIFFERENT CURRENT LEVEL

	Condition	400 V 20 A	400 V 40 A	400 V 60 A
Turn-on	w/o AGD	19.3%	21.2%	24.1%
	with AGD	4.3%	3.6%	5.5%
Turn-off	w/o AGD	32.3%	33.7%	29.5%
	with AGD	6.4%	7.9%	8.1%

during turn-ON transient and from 3.6 to 1.4 A during turn-OFF transient.

Tables V and VI present the switching loss comparison across different current levels. To better illustrate the effectiveness of the proposed AGD, a current sharing factor is introduced and is defined as follows:

$$\lambda = \frac{\Delta E}{E_{\text{loss\_avg}}} \tag{29}$$

where ΔE and E_{avg} satisfy

$$\Delta E = E_{\text{loss},i\_\max} - E_{\text{loss},i\_\min} \tag{30}$$

$$E_{\text{loss\_avg}} = \frac{\sum_{i=1}^{n} E_{\text{loss},i}}{n} \tag{31}$$

where n represents the total number of parallel branches, and $E_{\text{loss},i}$ indicates the switching loss of the i_{th} branch.

In addition, the smaller λ means better current sharing. As shown in Table V, the proposed AGD effectively balances switching losses among parallel devices, reducing the risk of premature failure caused by excessive stress on individual devices and ultimately enhancing overall system reliability.

To verify the effectiveness of the proposed AGD under various operating conditions, experiments under 400 V, 20 A and 400 V, 60 A were added. The experimental results are presented in Table VI. With AGD implementation, the turn-ON/turn-OFF loss imbalances are reduced by: 15%/25.9% at 20 A, 17.6%/25.8% at 40 A, and 18.6%/21.4% at 60 A load current. Experimental results demonstrate that the proposed AGD effectively achieves parallel current sharing across varying load current levels.

In addition, the proposed AGD can be extended for multidevice current sharing, as discussed in Section III. This article verifies the effectiveness of the proposed AGD using three parallel devices. Fig. 16 illustrates the experimental waveform of the turn-ON transient, while Fig. 17 shows the waveform of the

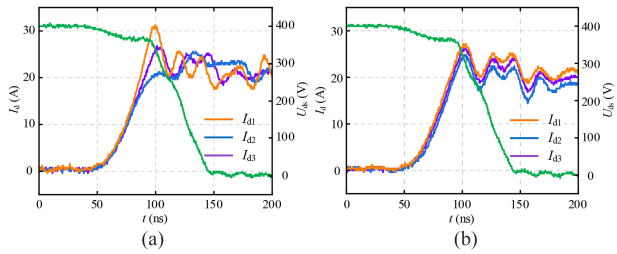

Fig. 16. Experimental waveform of multiple paralleled devices during the turn-ON process. (a) Without AGD. (b) With AGD.

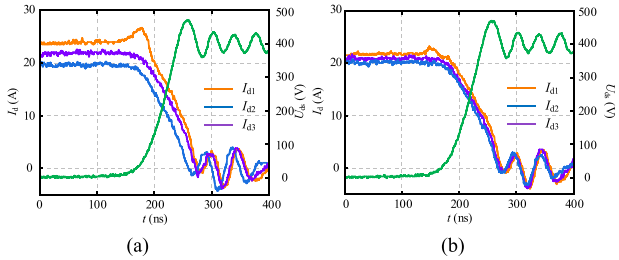

Fig. 17. Experimental waveform of multiple paralleled devices during the turn-OFF process. (a) Without AGD. (b) With AGD.

TABLE VII
EXPERIMENTAL RESULTS OF MULTIPLE PARALLELED DEVICES

		E_{loss1} (μJ)	E_{loss2} (μJ)	E_{loss3} (μJ)	λ
Turn-on	w/o AGD	216.8	196.7	180.9	18.1%
	with AGD	191.1	179.1	179.8	6.5%
Turn-off	w/o AGD	141.2	87.5	117.1	46.6%
	with AGD	128.3	120.1	116.5	9.7%

turn-OFF transient. The switching losses of the parallel devices are shown in Table VII.

As shown in Table VII, the maximum turn-ON loss difference decreases from 28.9 to 12.0 μJ, representing an 11.6% reduction in imbalance. Similarly, the maximum turn-OFF loss difference reduces from 53.7 to 11.8 μJ, corresponding to a 36.9% imbalance improvement. These results demonstrate the proposed AGD's effectiveness in mitigating switching loss imbalance among parallel devices. Furthermore, by balancing switching losses, the thermal distribution among parallel devices is improved, effectively enhancing the overall system reliability.

In addition, a full-bridge test platform is built to verify the effectiveness of the proposed AGD in dc–ac applications. Fig. 18(a) and (b) shows the comparative experimental waveforms of the traditional driving scheme and the proposed AGD. At the peak current of 20 A, the maximum difference of parallel current is reduced from 16.5 to 4.5 A, and the parallel current imbalance is suppressed. The experimental results show that the proposed AGD maintains excellent current sharing performance under variable load conditions, which confirms the effectiveness of the control method.

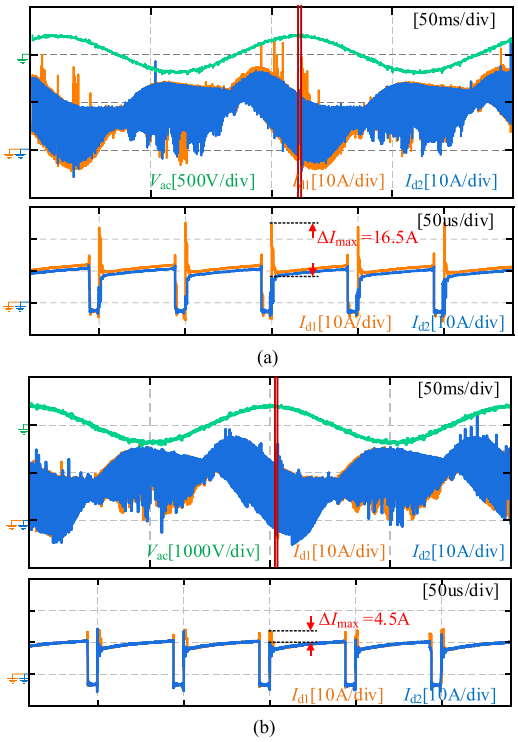

Fig. 18. Waveforms of inverter. (a) Without AGD. (b) With AGD.

V. Conclusion

This article presents an AGD with an auxiliary driving branch to achieve current sharing by synchronizing both the turn-ON/turn-OFF delays and current slew rates of parallel-connected devices. The proposed AGD employs two push-pull circuit structures, which enable driving mode adjustment with only a single switch, thereby simplifying the switching timing design. Moreover, the AGD can dynamically adjust the activation duration of the auxiliary path through an internal closed-loop controller based on the turn-ON/OFF delay and slew rate discrepancies among paralleled devices, ensuring current balancing under various load conditions. Experimental results validate the effectiveness of the proposed AGD. Furthermore, the presented AGD can be readily extended to support multiple paralleled devices, making it particularly attractive for high-power converter applications.

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