A Simplified Time-Domain Model-Based Maximum Efficiency Tracking-Aided Synchronous Rectification Strategy for *CLLC* Chargers

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***Abstract*—Synchronous rectification (SR), achieved by replacing secondary-side diodes with active MOSFET channels, is crucial for reducing conduction losses in *CLLC* converters. Traditional SR methods, however, either entail costly and bulky hardware or rely on complex mathematical models. This article introduces a simplified time-domain model (STDM) that utilizes mathematical principles and detailed operational assumptions to provide initial duty cycles and gate signal phases for SR under various frequencies and load conditions. However, the STDM's overall accuracy is compromised by parasitic parameters and parameter tolerance of the resonant tank. Directly employing the STDM-based SR method may lead to hard-switching of MOSFETs or increased circulating current, reducing system efficiency. To mitigate this issue, a maximum efficiency tracking (MET)-aided SR signal adjustment method is proposed, which further modifies the duty cycle and phase shift to minimize the current passing through the diodes. This STDM-MET-SR approach does not necessitate high-bandwidth sensors or complex control algorithms while offering immunity to parasitic parameters and system parameter variations. Experimental results demonstrate that the STDM-MET generated SR signals contain negligible errors compared to the required SR signals, and the efficiency of the *CLLC* converter with STDM-MET-SR implemented is significantly improved compared to those of diode rectification. Overall, the proposed STDM-MET-SR approach offers a cost-effective and efficient solution to reduce conduction losses in *CLLC* converters.**

***Index Terms*—*CLLC* converter, maximum efficiency tracking (MET), parasitic parameter, simplified time-domain model (STDM), synchronous rectification (SR).**

I. Introduction

IN THE field of power electronics, bidirectional dc–dc converters play a pivotal role in various applications, ranging from renewable energy systems (RESs) to electric vehicles [1], [2], [3]. Among the bidirectional dc–dc converters, the *CLLC* converter is a popular structure due to its high efficiency, full range of soft-switching, bidirectional identical-gain transferring characteristics [4], and effective EMI behaviors [5]. However, the efficiency and the performance of *CLLC* converters are limited by the body diode rectification (BDR). The high voltage drop of the SiC MOSFET body diode significantly increases the conduction loss of the switches, reducing system efficiency and requiring redundant cooling systems. To address the issue, synchronous rectification (SR) was employed by replacing body diodes with efficient MOSFETs' channels [6].

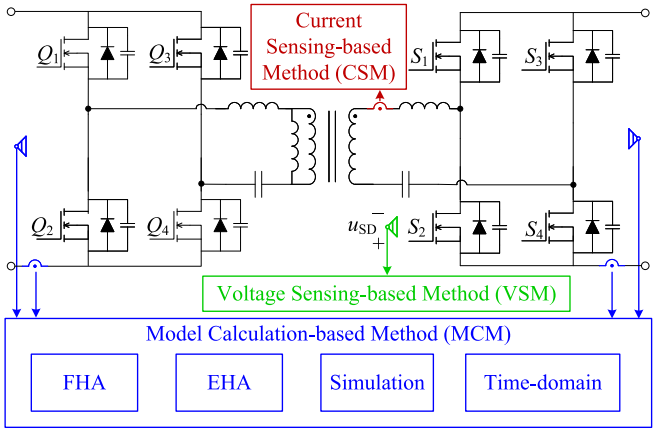

Fig. 1. Commonly used SR methods in previous papers.

Typically, there are three main methods to realize SR in resonant converters, which are illustrated in Fig. 1. The main methods are 1) voltage sensing-based method (VSM), 2) current sensing-based method (CSM), and 3) model calculation-based method (MCM).

VSM enables the determination of SR switching time based on the voltage across the device (the voltage from source to drain u_{SD}). When the body diode is conducting, u_{SD} corresponds to the voltage drop across the diodes, indicating the need to activate SR [7]. And when u_{SD} passes through zero, it signifies that the current flowing through the device has also passed through zero, indicating the need to deactivate SR. Subsequently, the value of u_{SD} becomes the output voltage, and the corresponding switches remain off. During this process, however, u_{SD} often becomes extremely low (body diode forward voltage) after SR is enabled,

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making it vulnerable to parasitic effects such as the leakage inductance resulting from MOSFET packaging and the on-board inductance arising from the driver to the gate of the MOSFET [8]. These inductive effects cause the detected zero crossing point of u_{SD} to occur earlier than the actual zero crossing point of the current, resulting in premature deactivation of SR, which adversely affects the efficiency of the converter [9]. One solution is employing resistance–capacitance (*RC*) delay circuit, which can be used to compensate for the advanced turn-OFFtime [7], [10]. However, the choice of the time constant for the *RC* circuit needs to be selected with precision to align with the impedance ratio of the leakage inductance and the MOSFET ON-state resistance, which is challenging to match since the parameters vary with the manufacturing tolerances and operation conditions [11]. Therefore, considering the uncertainty of parasitic inductance, VSM-based adaptive SR methods were proposed to mitigate SR errors by detecting the body diode conduction state first and then adjusting the SR conduction time in the subsequent switching cycle based on this detection [12], [13]. For instance, an adaptive SR method with a primary closed-loop controller was introduced in [12], utilizing ripple detection to adjust the SR on-time according to the detection of body diode conduction. Nonetheless, since these adaptive SR strategies depend on the measurement of u_{SD}, achieving a noise-tolerant solution still poses a significant challenge.

Another commonly used SR method is CSM, which is due to its generation of SR signals via detecting the polarity of the secondary-side current i_s: when $i_s > 0$, S_1 and S_4 turn ON; when $i_s < 0$, S_2 and S_3 turn ON; and when $i_s = 0$, all secondary-side switches are deactivated [14]. Similar to VSM, however, during the discontinuous state, the current i_s may not remain at zero because the parasitic capacitance oscillates with the resonant inductance. If a conventional CSM is employed, false triggering may occur due to the parasitic oscillation during this period [4]. Besides, the secondary-side current is measured by a current transformer (CT) in practice, and the volume and weight of CTs and their complicated signal processing circuit are relatively large, which decreases the converter's power density [15], [16]. In addition, conventional CTs also bring extra power losses in the converter. Despite a lossless SR method is proposed in [17], using a Rogowski coil, to increase the system efficiency, the problem of cost and size still remains. Thus, Chen et al. [18] proposed an SR scheme based on resonant inductor voltage sensing. In this method, the direction of the resonant current is derived indirectly from the inductor voltage; thus, eliminating the requirement for current sensors.

Regardless of utilizing VSM or CSM, extra high-bandwidth sensing and conditioning circuits are always required, which would increase the system cost, size, power loss, and control complexity. To eliminate these risks, therefore, the MCM-based SR becomes increasingly popular. The principle of MCM lies in the determination of the conduction time of secondary switches based on mathematical models, eliminating the necessity for high-bandwidth sensors. However, establishing an accurate yet simplified mathematical model that provides precise conduction time of secondary-side switches for the *CLLC* converters remains challenging. The current mathematical models can be classified into two main approaches: the first harmonic approximation (FHA) model and the time-domain model (TDM).

The popularity of the FHA model lies in its simplicity and suitability for engineering calculations. By using the Fourier decomposition, the square voltage/current waves are broken down into fundamental and high-order harmonics. Then the fundamental harmonic is analyzed while the high-order components are neglected [19]. As an example, Li et al. [20] proposed an SR method of calculating SR conduction time using the FHA model. However, this approximation in the FHA model causes the findings to be inaccurate, especially when the switching frequency is far from the resonant frequency [21], [22]. This difference can cause inaccurate SR signals, leading to circulating current that reduces efficiency. Attempting to enhance the accuracy of the FHA model, Sankar et al. [23] proposed the extended harmonics approximation (EHA) model, which considers high odd-order harmonics. However, neither FHA nor EHA is suitable for analyzing the discontinuous mode when the operation frequency is less than the resonant frequency [24].

TDM, on the other hand, is proposed to boost the model's accuracy. The main idea of TDM is to list all the time-domain expressions and try to solve those using boundary conditions. In [6], [25], and[26], accurate TDMs are developed to generate SR signals. However, deriving exact closed-form solutions is challenging due to the presence of nonlinear trigonometric terms; nevertheless, mathematical approximations can be utilized to facilitate the practical implementation of SR. In [25], a lookup table is employed to solve the problems of complex mathematical models in real-time controllers. In [6] and [26], based on the complicated TDM, polynomial fitting methods are applied to generate the SR signals. Although the mathematical approximations can alleviate the computation burden of the real-time controller, the TDM per se is still complex, leading to a heavy workload for engineers. To further simplify the TDM, Cao et al. [27] utilized the superposition principle for the *CLLC* converters, which provides a possibility to solve the mathematical model. In [28], a simplified model that properly approximates the operation waveforms is proposed; however, when the switching frequency exceeds the resonant frequency, the switching time of MOSFETs on the rectification side cannot be obtained solely based on assumptions. Besides, the artificial intelligence-based method [29] also gained considerable interest for its capability to capture the complex nonlinear relationships in *CLLC* converters; however, this approach requires a costly neural network accelerator during the training process. As a result, despite previous research efforts to generate SR signals using mathematical models, balancing simplicity and accuracy in the production of SR signals remains a challenging task.

Moreover, all TDMs discussed in [6], [25], [26], [27], [28], and [29] overlook the impact of parasitic components in the circuits, such as stray capacitances and winding resistances in isolation transformers, and parasitic capacitances of the power devices, which are critical in real-world scenarios. These components significantly dampen the accuracy of SR, and the inaccuracy further diminishes the benefits of SR. Since TDM per se is inherently complex, incorporating additional parasitic parameters further complicates the model. Hence, introducing

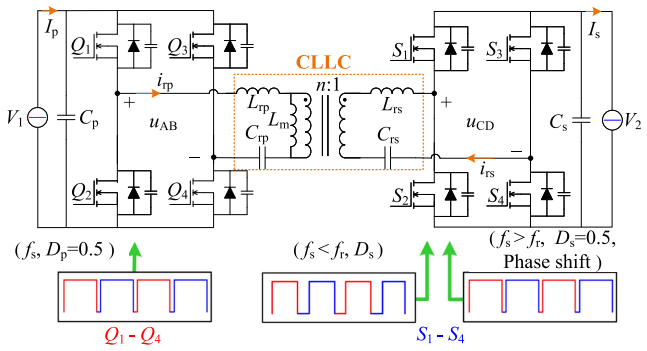

Fig. 2. System structure of the *CLLC* converter with SR.

an additional control freedom to compensate for the accuracy of simplified mathematical models may be preferable for parasitic-inclusive *CLLC* converters.

Consequently, this article presents a simple yet accurate SR strategy for the *CLLC* converter. To realize this goal while considering simplicity and accuracy, a simplified time-domain model (STDM) is proposed based on the mathematical and operational assumptions, which is fundamental to realizing SR in *CLLC* converters. In addition, to mitigate the impact of the parasitics, a maximum efficiency tracking (MET)-aided SR signal adjustment method is proposed, which further modifies the duty cycle and phase shift to minimize the current passing through the diodes. This approach utilizes different duty cycles and phase shifts in various frequency regions to optimize a *CLLC*'s performance, resulting in improved efficiency and reliability. The rest of this article is organized as follows. Section II presents the system modeling and STDM derivation. Section III introduces the STDM-MET-SR realization. Section IV validates the proposed SR strategy via experiments. Finally, Section V concludes this article.

II. System Configuration and Modeling

A. System Configuration

The *CLLC* converter configuration is shown in Fig. 2, where the input and output voltages are V_1 and V_2, respectively. C_1 is the dc-link capacitor, and C_2 is the capacitive filter. The turn ratio of the transformer is n, and the transformer magnetizing inductance is $L_{\rm m}$. $L_{\rm rp}$, $L_{\rm rs}$, $C_{\rm rp}$, and $C_{\rm rs}$ are the series inductors and the capacitors of the primary and the secondary sides.

When designing resonant parameters, two intermediate parameters are always employed: inductance ratio k ($k \gg 1$) and characteristic impedance Z_0, which are respectively expressed as

$$k = \frac{L_{\rm m}}{L_{\rm rp}} = \frac{L_{\rm m}}{n^2 L_{\rm rs}}, Z_0 = \sqrt{\frac{L_{\rm rp}}{C_{\rm rp}}} = n^2\sqrt{\frac{L_{\rm rs}}{C_{\rm rs}}}. \tag{1}$$

A *CLLC* charger typically regulates the output voltage using the pulse frequency modulation method, where all switches operate at the frequency of $f_{\rm s}$, and the resonant tank has a

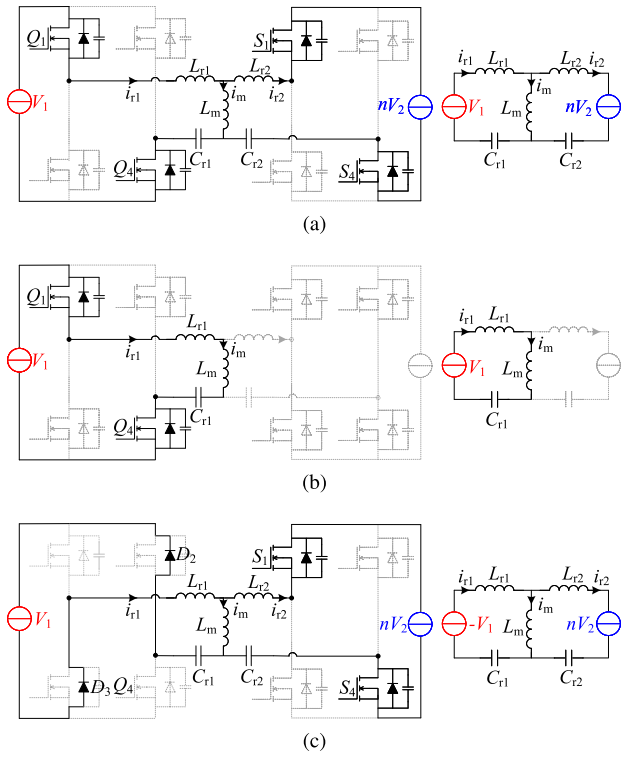

Fig. 3. System operation stages. (a) P stage. (b) O stage. (c) N stage.

resonant frequency of $f_{\rm r}$ that satisfies

$$f_{\rm r} = \frac{1}{2\pi\sqrt{L_{\rm rp}C_{\rm rp}}} = \frac{1}{2\pi\sqrt{L_{\rm rs}C_{\rm rs}}}. \tag{2}$$

The resonant period and the switching period are defined as $T_{\rm r}$ and $T_{\rm s}$, respectively.

To simplify the analysis, the resonant parameters are designed symmetrically, which can be derived as

$$\begin{cases} L_{\rm r1} = L_{\rm r2} = L_{\rm rp} = n^2 L_{\rm rs} \\ C_{\rm r1} = C_{\rm r2} = C_{\rm rp} = C_{\rm rs}/n^2. \end{cases} \tag{3}$$

In the TDM, a *CLLC* converter can operate in three stages: P, N, and O stages, as shown in Fig. 3. In Fig. 3, the voltages and currents are reflected to the primary-side. The relationship between the switching state of MOSFETs and the stages in half switching period can be illustrated as follows:

1) *P stage:* The switches Q_1, Q_4, S_1, and S_4 conduct, and the input and output voltages share the same polarity. In this stage, series inductance and capacitance are resonant, while the sinusoidal current is generated in the resonant tank. Due to the leakage inductance $L_{\rm m}$ is greater than the series inductance, $L_{\rm m}$ ceases to participate in the resonance, and the magnetizing current increases linearly.
2) *O stage:* The switches Q_1 and Q_4 turn ON, and the secondary-side current remains zero. In this stage, the inductance $(L_{\rm m} + L_{\rm r1})$ and the capacitance $C_{\rm r1}$ are resonance, and the resonant frequency $f_{\rm r}'$ satisfies

$$f_{\rm r}' = \frac{1}{2\pi\sqrt{(L_{\rm r1}+L_{\rm m})C_{\rm r1}}} = \frac{1}{2\pi\sqrt{(k+1)L_{\rm r1}C_{\rm r1}}}. \tag{4}$$

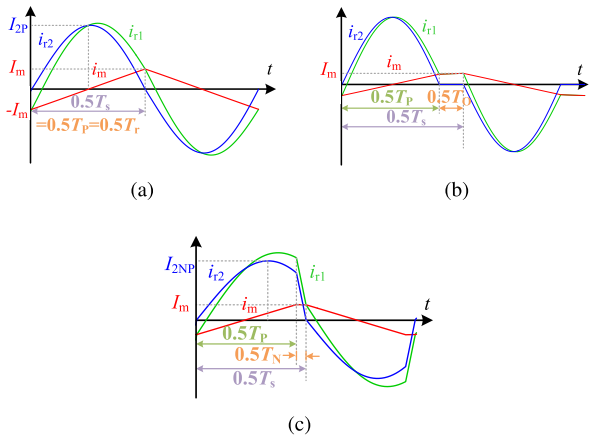

Fig. 4. Current waveforms. (a) $f_s = f_r$. (b) $f_s < f_r$. (c) $f_s > f_r$.

Since k is far greater than 1, $f_r' \ll f_r$ is typically satisfied, and the currents in the *O* stage can be seen as constants.

3) *N stage:* The switches D_2, D_3, S_1, and S_4 conduct, and the input and output voltages are of the opposite polarity.

By combining the three operation stages, the *CLLC* converter can operate in several modes depending on the switching frequencies and loads. When $f_s = f_r$, the *CLLC* stays in the P mode regardless of load variations. However, when $f_s < f_r$, the *CLLC* can operate in PN/PON/PO modes, among which the PO mode is preferred due to its soft-switching characteristics and monotonic voltage gain with decreasing frequency. In contrast, the PN and PON modes are not suitable, as they may result in the loss of soft-switching and nonmonotonic gain. On the other hand, when $f_s > f_r$, the *CLLC* typically operates in the NP mode.

B. Modeling When $f_s = f_r$

Based on the above-mentioned analyses, a *CLLC* converter operates in the P mode when $f_s = f_r$. Hence, the duration of the P stage satisfies

$$T_P = T_s = T_r. \tag{5}$$

According to Fig. 4(a), the secondary-side current i_{r2} takes the form of sinusoidal waveforms; thus, by assuming I_{2P} is the amplitude of i_{r2}, i_{r2} can be expressed as

$$i_{r2}(t) = I_{2P}\sin(\omega_r t) \tag{6}$$

where $\omega_r = 2\pi f_r$ is the resonant angular frequency, and I_{2P} is the coefficient.

According to Fig. 3(a) and Kirchhoff's law, the relationship between the primary- and secondary-side currents satisfies

$$i_{r1}(t) = i_{r2}(t) + i_m(t) \tag{7}$$

where $i_m = -\frac{V_1 T_r}{4L_m} + \frac{V_1}{L_m}t$ is the magnetizing current.

C. Modeling When $f_s < f_r$

When $f_s < f_r$, the *CLLC* converter is expected to work in the PO mode due to the realization of zero-voltage switching and the acquisition of a monotonic gain curve. In the PO mode, the durations of the P and O stages satisfy

$$0.5T_P + 0.5T_O = 0.5T_s \tag{8}$$

where T_P and T_O are durations of P and O stages, respectively.

In the P stage, the primary- and secondary-side currents [28] can be simply expressed as

$$\begin{cases} i_{r1}(t) = & I_{2PO}\sin(\omega_r t) + I_m \sin\left(\sqrt{\frac{1}{2k+1}}\omega_r t + \phi\right) \\ i_{r2}(t) = & I_{2PO}\sin(\omega_r t) \end{cases} \tag{9}$$

where I_{2PO}, I_m, and ϕ are the undetermined coefficients.

Based on the above-mentioned analyses, in the O stage, L_m participates the resonance with L_{r1} and C_{r1}, and the currents i_{r1} and i_m can be assumed to remain constant. In other words, during the O stage, i_{r1} is equal to i_m, while i_{r2} remains at zero. Then, based on the half-wave symmetry and continuity principles, the current satisfies

$$\begin{cases} i_{r1}(0) + i_{r1}(0.5T_s) = 0 \\ i_{r2}(0) = i_{r2}(0.5T_P) = 0. \end{cases} \tag{10}$$

Substituting (10) into (9), the equivalence between the duration of the P stage and the resonant period can be acquired, i.e.,

$$0.5T_P = 0.5T_r. \tag{11}$$

Therefore, in the PO mode, the duration of the P stage equals the resonant period. That is, the conduction time of the secondary-side MOSFETs should be equivalent to that of the P stage in this mode, which is fundamental to realizing SR when $f_s < f_r$.

D. Modeling When $f_s > f_r$

When $f_s > f_r$, the *CLLC* converter operates in the NP mode (P stage + N stage), in which the operation period satisfies

$$0.5T_P + 0.5T_N = 0.5T_s. \tag{12}$$

Based on the previous analyses, the NP mode in half a period T_s can be divided into two stages. During $(0, 0.5T_P)$, the *CLLC* converter operates in the P stage, and during $(0.5T_P, 0.5T_s)$, it functions in the N stage, where the input and output voltages have opposite polarities. To simplify the analysis, the N stage can be equivalently divided using the superposition principle [27], comprising two substages: the P′ stage and the N′ stage, as illustrated in Fig. 5. As a result, the equivalent circuit of NP mode can be summarized as follows: the P′ stage lasts over the whole period T_s, and the N′ stage operates during $(0.5T_P, 0.5T_s)$. Then, the output current of the *CLLC* converter can be analyzed separately.

In the P′ stage, the operation principles are similar to the circuit when $f_s = f_r$. Hence, the current $i_{r21}(t)$ during $(0, 0.5T_s)$ can be described as

$$i_{r21}(t) = I_{2NP}\sin(\omega_r t) \tag{13}$$

where I_{2NP} is the undetermined coefficient.

In the N′ stage, based on the equivalent circuit and under the assumption that $i_m(t)$ remains constant during this stage,

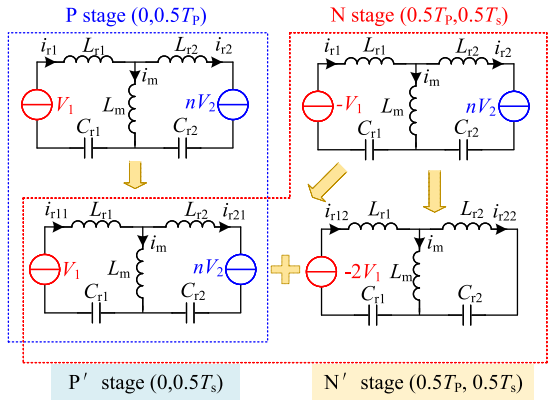

Fig. 5. Equivalent circuit in the NP mode using the superposition principle.

the current $i_{r22}(t)$ can be determined by solving the differential equations, which is

$$i_{r22}(t) = \frac{-2V_1}{2Z_0}\sin(\omega_r(t-0.5T_P)). \tag{14}$$

Then, according to the superposition principle, the secondary side current in the NP mode can be expressed as

$$i_{r2}(t) = i_{r21}(t) + i_{r22}(t)H(t-0.5T_P) \tag{15}$$

where $H(t-0.5T_P)$ is the unit step function, which returns 0 when $t \in (0, 0.5T_P)$ and 1 when $t \in (0.5T_P, 0.5T_s)$.

Hence, the output current can be expressed as

$$\begin{aligned} I_2 &= \frac{2n}{T_s}\int_0^{0.5T_s} i_{r2}(t)\mathrm{d}t \\ &= \frac{2n}{T_s}\left[\int_0^{0.5T_s} i_{r21}(t)\mathrm{d}t + \int_{0.5T_P}^{0.5T_s} i_{r22}(t)\mathrm{d}t\right] \\ &= \frac{2nI_{2NP}}{T_s}\int_0^{\frac{T_s}{2}} \sin\omega_r t\mathrm{d}t - \frac{2nV_1}{Z_0T_s}\int_{\frac{T_P}{2}}^{\frac{T_s}{2}} \sin\omega_r(t-0.5T_P)\mathrm{d}t. \end{aligned} \tag{16}$$

In (16), it is evident that the undetermined parameter I_{2NP} remains, except for the system operation and resonant parameters. Thus, (17) is introduced to obtain the value of I_{2NP}

$$i_{r2}(0.5T_s) = 0. \tag{17}$$

Substituting (17) into (15), the I_{2NP} can be calculated as

$$I_{2NP} = \frac{V_1\sin(\pi f_r(T_s - T_P))}{Z_0\sin(\pi f_r T_s)}. \tag{18}$$

And by substituting (18) into (16), the relationship among the duration of the N stage, the operation frequency f_s, the input voltage V_1, and the output current I_2 can be expressed by

$$\begin{aligned} T_N &= f(f_s, V_1, I_2) \\ &= \frac{\sin^{-1}\left(\frac{\pi I_2 Z_0 f_r + 2nV_1 f_s}{nV_1 f_s\sqrt{\tan^2\left(\frac{\pi f_r}{2f_s}\right)+4}}\right) - \tan^{-1}\left(\frac{2}{\tan\left(\frac{\pi f_r}{2f_s}\right)}\right)}{\pi f_r}. \end{aligned} \tag{19}$$

TABLE I
P/O/N STAGE DURATIONS

Operation frequency	T_P	T_O	T_N
$f_s < f_r$	T_r	$T_s - T_r$	0
$f_s = f_r$	$T_s = T_r$	0	0
$f_s > f_r$	$f(f_s, V_1, I_2)$	0	$T_s - f(f_s, V_1, I_2)$

Similarly, the duration of the N stage in the discharging mode is $T_N = f(f_s, V_2, I_1)$. In conclusion, the P/O/N stage durations in different switching frequency regions can be summarized, as shown in Table I. Then, the durations can be employed to determine the switching duty cycle and phase shift of the rectification-side MOSFETs.

III. SR Implementation

A. Generation of Initial SR Signals Based on STDM

SR is essential for *CLLC* chargers, which significantly reduces the conduction loss that is due to the high ON-state voltage drop of the body diodes. Based on the above-mentioned analyses, the required SR signals in different frequency regions can be depicted, which is shown in Fig. 6. When the switching frequency is smaller than the resonant frequency, the secondary-side SR signals are synchronized with the primary-side driving signals, and the duty cycle D_s is concomitantly reduced with the switching frequency. According to (11) and Fig. 4(b), the secondary-side MOSFETs should be turned on in the P stage, which allows the duty cycle D_s to be derived as

$$D_s = \frac{f_s}{2f_r}. \tag{20}$$

Therefore, the realization of SR in the $f_s < f_r$ region is achieved when the secondary side switches apply the assigned duty cycle using (20).

When the switching frequency is the same as the resonant frequency, the *CLLC* converter operates in a complete resonant state; thus, the SR signals of the secondary-side MOSFETs should be identical to the signals of the primary side.

When the switching frequency is larger than the resonant frequency, the duty cycle of SR signals D_s is to be equal to 0.5 according to (17), and a phase shift α is to be applied

$$\alpha = 2\pi\frac{0.5T_N}{T_s} = g(f_s, V_1, I_2). \tag{21}$$

Contrary to the simple duty cycle variations [based on (20)] when $f_s \le f_r$, it is difficult to directly calculate the accurate phase shift α in a low-cost real-time controller using (19) and (21) due to the nonlinear components. Hence, a polynomial fitting method, similar to those used in [6] and [26], can be employed to simplify the complex computation process. First of all, based on (21), the phase shifts with different operation conditions can be calculated, and the derived phase shifts can form a 4-D mapping table (α-f_s, V_1, I_2). Then, numerical fitting tools such as the MATLAB fit function can be employed to fit the calculated phase shifts using a multiple-order polynomial. Based on the above-mentioned calculation, the initial SR signals can be generated.

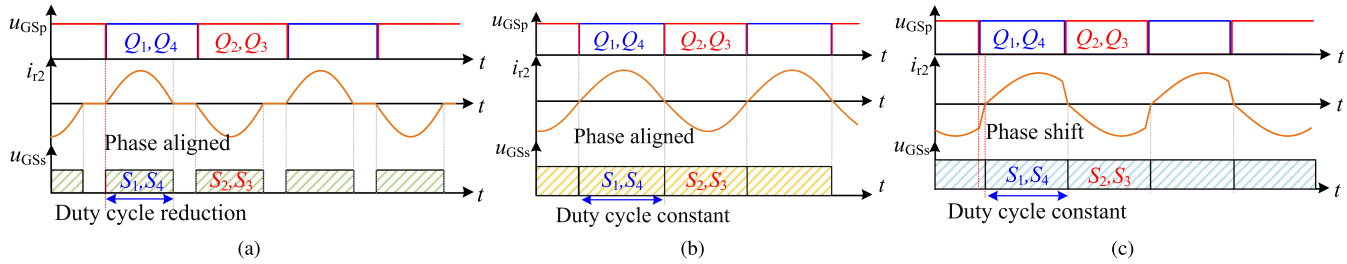

Fig. 6. Typical operation waveforms and required SR signal when (a) $f_s < f_r$, (b) $f_s = f_r$, and (c) $f_s > f_r$.

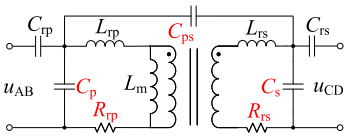

Fig. 7. Equivalent circuit of resonant tank with parasitic components.

B. Effects of Parasitics and Tolerances on Accuracy of STDM-Based SR Signals

The derived duty cycle and phase shift are based on an ideal STDM, which is impractical in real-world scenarios. For instance, a realistic isolation high-frequency transformer model [30], [31], which accounts for parasitic elements, is illustrated in Fig. 7. In this figure, R_{rp} and R_{rs} represent the effective winding resistances of the transformer. C_p and C_s correspond to the intrawinding capacitances of the primary and secondary windings, respectively, while C_{ps} denotes the interwinding capacitance between the two windings. These parasitic elements change the current waveforms in the resonant tank. In addition, the output capacitance of the MOSFET C_{oss} further widens the discrepancy between the ideal and the real-world systems. Furthermore, previous analyses assumed symmetrical inductances and capacitances without any tolerances, which is also unrealistic. Variations in these parameters can occur due to temperature fluctuations, manufacturing tolerances, and aging effects, making it unlikely that the ideally derived duty cycle and phase shift will be directly applicable to practical *CLLC* converters.

As a consequence, such an assumption for idealism will weaken the accuracy of SR calculations, and inaccurate SR MOSFET turn-ON and turn-OFF timings will further affect the system's efficiency. For instance, if the secondary-side SR MOSFETs turn OFF after i_{rs} crosses zero, the current in the SR will decrease to a negative value, resulting in a reverse current through the SR MOSFETs. Conversely, if the secondary-side SR MOSFETs turn OFF too early or turn ON too late, a portion of i_{rs} will flow through the body diode of the SR MOSFETs. And if the MOSFETs turn ON too early, hard-switching will occur. All these issues lead to considerable power losses, and in combination with the SR signals initially generated based on the STDM, a duty cycle and phase shift adjustment strategy is required for parasitic-inclusive *CLLC* chargers.

C. MET-Aided SR Strategy

As previously discussed, the inadequate accuracy of SR signals based on the STDM leads to a decrease in system efficiency due to the influence of parasitics and parameter variation. To address this issue, a MET-aided SR strategy is proposed. The fundamental principle is that the initial SR signals can be calculated based on the STDM under different operation conditions in real-time controllers. To improve the accuracy of SR signals, the STDM-derived values are further refined by dynamically adjusting the duty cycle or phase shift to maximize MOSFET conduction and reduce diode losses. This is achieved through a dynamic-search-based MET (DS-MET) process, which requires no high-bandwidth sensors and remains robust to parasitic effects and parameter uncertainties. Given the rapid searching process, constant input voltage and output power are assumed, and efficiency optimization is realized by minimizing the input current I_p. In essence, the optimal SR control point corresponds to the condition where I_p reaches its minimum $I_{p,min}$.

In this article, the utilized DS-MET is similar to the well-known maximum power point tracking (MPPT) technique in photovoltaic systems [32], [33]. Unlike MPPT, however, the purpose of the tracking here is to maximize the overall system efficiency by changing the duty cycle and phase shift. Fig. 8 depicts the flowchart of a DS-MET. Utilizing the *CLLC* converter that operates in the $f_s < f_r$ region as an example, it indicates that the duty cycle D_s of the secondary-side MOSFETs should be altered according to their operation conditions. The core process can be described as follows.

The DS-MET algorithm starts by initializing the duty cycle $D_s(0)$, which is initially calculated based on the STDM. The input current $I_p(0)$ is measured (low-bandwidth signal derived from multiple measurements via a digital moving average filter) and stored in the real-time controller as a reference point for subsequent iterations. At each update step σ, executed at an interval of T_{sa}, the duty cycle is adjusted by a small increment ΔD_s, and the filtered input current $I_p(\sigma)$ is compared with the previous value to determine whether the adjustment improves system efficiency. If $I_p(\sigma+1) < I_p(\sigma)$, the current step is deemed beneficial, and the duty cycle is further adjusted in the same direction. Otherwise, the direction is reversed.

This iterative process continues until a minimum input current $I_{p,min}$ is found, corresponding to the optimal duty cycle D_s. Once found, this value is saved and used for continued operation.

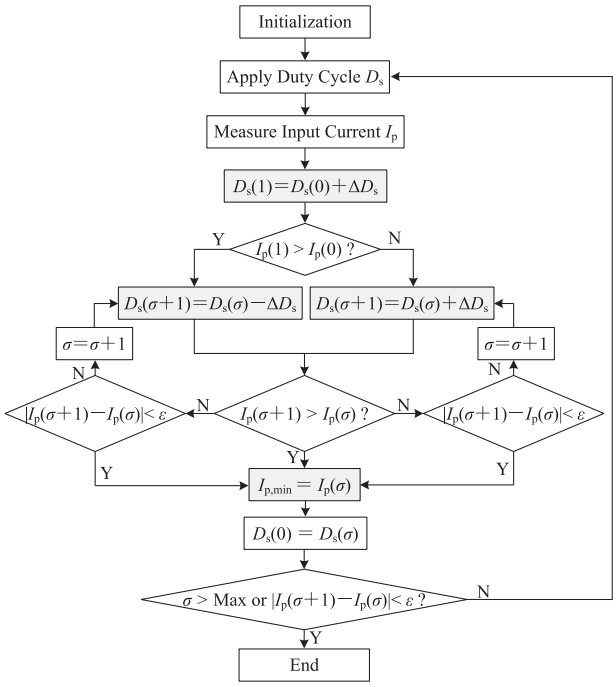

Fig. 8. Flowchart of the DS-MET algorithm.

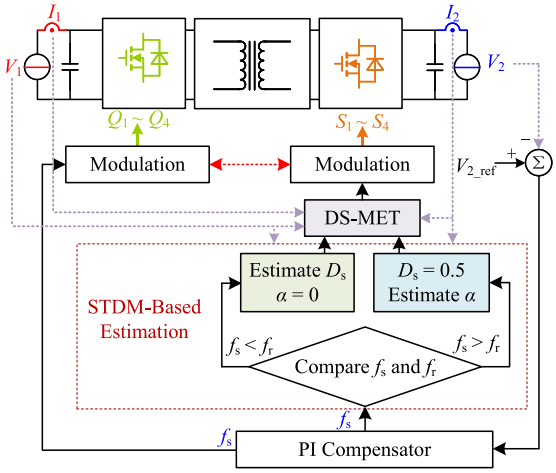

Fig. 9. Process of generating SR signals based on a close-loop STDM-MET-SR.

This iterative process helps *CLLC* converters operate at the most efficient point by continuously searching for the optimal duty cycle that minimizes power losses.

In addition, a local threshold and global termination check are introduced in Fig. 8. A threshold ε is applied in both branches (increasing and decreasing the duty cycle) to evaluate the current change. If the change is smaller than ε, the iteration stops early, enabling more efficient convergence to the optimal value. At the final stage, a global termination condition is added, halting the algorithm either when the maximum iteration limit (max in Fig. 8) is reached or when the current change falls below the predefined threshold. This design balances iteration limits with the threshold condition, ensuring efficiency by terminating the process as it approaches the optimal point. The inclusion of parasitic effects and possible variations in parameters means that real-time control and adjustments are required to maintain optimal performance. The DS-MET approach ensures that the system can operate at maximum efficiency without the need for additional sensors, relying instead on feedback from the input current to dynamically tune the duty cycle.

Based on the DS-MET, the proposed STDM and DS-MET combined SR strategy (STDM-MET-SR) can be summarized as Fig. 9, which can be divided into two parts: $f_s \leq f_r$ and $f_s > f_r$. When $f_s \leq f_r$, the secondary-side switches would maintain the aligned phase with switches in the primary side and reduce their initial duty cycles D_s based on (20); when $f_s > f_r$, the duty cycle remains at 0.5, but the initial phase shift α determined by operation condition V_1, I_2, and f_s, should be applied to the switches based on (21). Subsequently, the calculated duty cycle D_s or phase shift α should be optimized based on the DS-MET strategy. In the proposed SR strategy, the STDM provides relatively accurate calculations, which not only speed up the adjustment process but also reduce the risk of the MET falling into a local optimum, thereby preventing a decrease in system efficiency. In addition, since the dc voltage and current sensors are commonly employed in the closed-loop voltage/current regulation and system monitoring, no extra high-bandwidth sensors are applied to the system. Besides, due to the DS-MET is similar to the MPPT method, the proposed STDM-MET-SR method can be easily implemented in entry-performance controllers.

Moreover, a basic soft-start mechanism is implemented in the real-time controller to ensure safe initialization. A state machine is employed to realize the soft-start procedure and manage the activation of SR. Without a controlled startup, excessive inrush current may flow through the bridges and transformer, imposing high stress on the components that can be potentially destructive. To prevent this, the system initially limits energy transfer into the resonant tank while keeping the SR disabled. During this phase, the *CLLC* converter operates in body diode conduction mode, ensuring unidirectional current flow and avoiding the risk of reverse conduction or shoot-through due to incomplete transformer magnetization [12]. Once the output voltage reaches its target, the state machine transitions to steady-state operation mode and progressively enables SR control to avoid sudden current surges during the transition. This staged activation ensures that the proposed SR algorithm is only applied under steady-state conditions, reducing the risk of instability during startup.

IV. Experiments

A. Prototype Implementation

An 1 kW experimental platform for the *CLLC* charger is established to verify the proposed SR strategy, as illustrated in Fig. 10. The real-time controller and sensors are provided by Imperix. For the *CLLC* converter, SiC MOSFETs are utilized as the main switches, while SiC Schottky diodes are used for comparison to evaluate the impact of SR, as they have a lower forward voltage compared to the body diodes of the SiC MOSFETs. A dc electronic load bank is connected with the *CLLC* converter as a variable load. The system specifications, including the asymmetrically

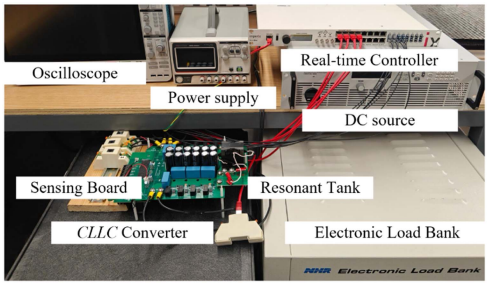

Fig. 10. Experiment setup.

TABLE II
EXPERIMENTAL SPECIFICATIONS

Parameters	Symbol	Value
Input voltage (rated)	V_1	160–200 V (180 V)
Output voltage	V_2	180 V
Turns ratio	n	1
Series inductances	$L_{\rm rp}$, $L_{\rm rs}$	25.1 µH, 25.7 μH
Magnetizing inductance	$L_{\rm m}$	211 μH
Series capacitances	$C_{\rm rp}$, $C_{\rm rs}$	167.1 nF, 169.3 nF
Parasitic capacitances	$C_{\rm p}$, $C_{\rm s}$, $C_{\rm ps}$	687 pF, 643 pF, 51.5 pF
Frequency	$f_{\rm r}$, $f_{\rm s}$	100 kHz, 50–200 kHz
SiC MOSFETs	$Q_{\rm i}$, $S_{\rm i}$	Cree C3M0065100K
SiC Schottky diodes	$D_{\rm i}$	ROHM SCS220AE

implemented resonant parameters and the measured parasitic parameters, are listed in Table II. The asymmetry in the resonant parameters is introduced to account for real-world variations, as manufacturing tolerances and aging effects can cause deviations from the ideal values.

B. SR Strategy Verification

To validate the effectiveness and the accuracy of the proposed STDM-MET-SR strategy, the steady-state waveforms of the *CLLC* converter under different operating frequencies and load conditions are measured, as shown in Fig. 11. In this experimental setup, the input voltage is maintained constant at 180 V, while the output voltage varies according to different operating frequencies and load conditions. The output load is adjusted from full load (100%), to half load (50%), then to light load (25%). Besides, the resonant frequency of the resonant tank utilized in this experiment is approximately 100 kHz.

When $f_{\rm s} < f_{\rm r}$, the *CLLC* charger operates in PO mode. In this condition, reduced duty cycles are applied to the secondary-side MOSFETs. Fig. 11(a) to (f) shows the waveforms when the system is operating at 60 and 80 kHz. Under full load, half load, and light load, the required SR signals are consistently aligned with the previous analyses, where the SR error is significantly below $0.5T_{\rm s}$, confirming the effectiveness of the proposed SR strategy when $f_{\rm s} < f_{\rm r}$. Besides, from Fig. 11(a) and (d), it is evident that the duty cycle and operation frequency increase concomitantly, which is in agreement with the theoretical analysis. According to Fig. 11(a)–(c) or 11(d)–(f), the required secondary-side duty cycles and output power also decrease concomitantly. In addition, due to the resonance between parasitic capacitance and series inductance, the secondary-side current [see Fig. 11(a)–(f)] is unable to remain at zero during O stage; therefore, applying the conventional CSM approach in this scenario may generate false SR signals. However, these false signals are eliminated when the proposed model-based SR method is utilized.

When $f_{\rm s} > f_{\rm r}$, the *CLLC* charger operates in NP mode, requiring a phase shift between the primary-side MOSFETs and the secondary-side MOSFETs. Fig. 11(g)–(l) shows the waveforms when the system is operating at 120 and 140 kHz. According to the experimental results, the phase shifts as the load becomes lighter and increases as operating frequencies amplify under the same load conditions, which aligns with (19). In Fig. 11(i), the system operates in NP mode under light load, where the phase shift is reduced to approximately zero.

In P mode, the operating frequency is approximately 100 kHz. The SR phase shift of the secondary-side MOSFETs remains at zero, and the duty cycle remains at 0.5 (with the dead time being negligible). The experimental waveforms, shown in Fig. 12, exhibit sinusoidal currents, which correspond well with the theoretical waveforms.

Fig. 13 presents the steady-state waveforms prior to and following the load changes. In Fig. 13(a), the converter operates under $f_{\rm s} < f_{\rm r}$. As the load changes from half load to full load, the switching frequency increases from approximately 70 to 78 kHz, with the duty cycle adjusting accordingly. Fig. 13(b) shows the converter behavior when $f_{\rm s} > f_{\rm r}$; in this case, the switching frequency decreases from approximately 184 to 141 kHz as the load increases from half load to 75%, while the phase shift adapts to the load variation and the duty cycle remains fixed at 0.5 (neglecting dead time). These experimental results are in strong agreement with the theoretical analysis.

As illustrated in Figs. 11–13, by employing the proposed SR method, the duty cycle/phase of the secondary-side MOSFETs in the parasitic-inclusive *CLLC* converter can be adjusted based on the input voltage, operating frequency, and output power, regardless of whether the *CLLC* resonant converter operates in the P mode, PO mode, or NP mode.

In addition, the transient behavior of the *CLLC* resonant converter during startup and load changes is experimentally measured using the proposed SR strategy. During the soft-start process, SR is initially disabled to prevent shoot-through and ensure safe operation before the transformer core is fully magnetized. As shown in Fig. 14(a), the secondary side operates in body diode conduction mode, allowing unidirectional current flow while avoiding premature SR activation. Once the output voltage stabilizes and predefined criteria are met, SR is progressively enabled. In this transition phase [see Fig. 14(b)], conduction gradually shifts from the body diodes to the MOSFET channels, minimizing conduction losses and ensuring a smooth transition to normal operation. The $u_{\rm DS}$ waveform demonstrates this shift by showing a decreased voltage drop across the device after SR activation. A slight increase in resonant current is also observed due to the sudden reduction in conduction impedance, which is an expected outcome of transitioning from diode to channel conduction. This staged activation sequence demonstrates the robustness of the proposed control logic during startup.

A similar level of robustness is also observed during dynamic load transitions, as detailed in Fig. 15 for the case of $f_{\rm s} < f_{\rm r}$ and

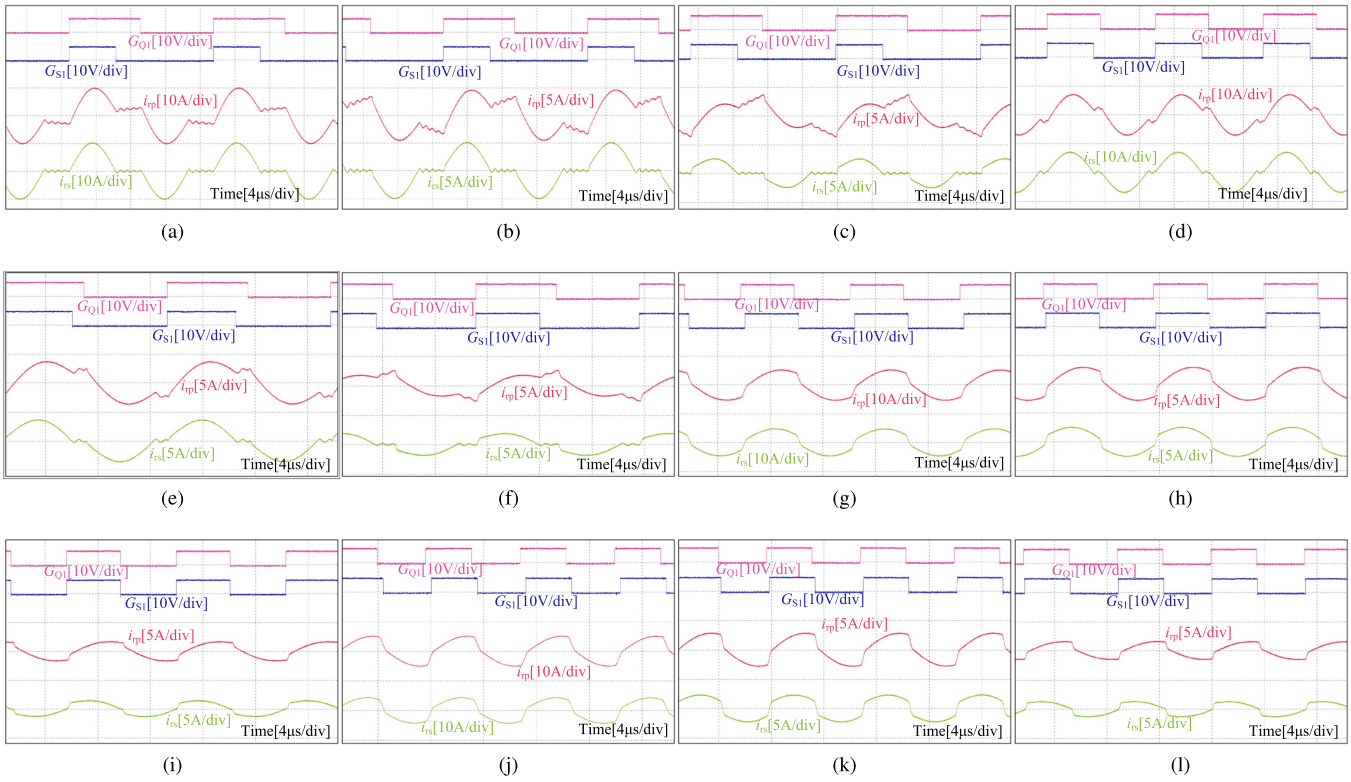

Fig. 11. Detailed waveforms with different frequencies and loads. (a) 60 kHz, full load. (b) 60 kHz, half load. (c) 60 kHz, light load. (d) 80 kHz, full load. (e) 80 kHz, half load. (f) 80 kHz, light load. (g) 120 kHz, full load. (h) 120 kHz, half load. (i) 120 kHz, light load. (j) 140 kHz, full load. (k) 140 kHz, half load. (l) 140 kHz, light load.

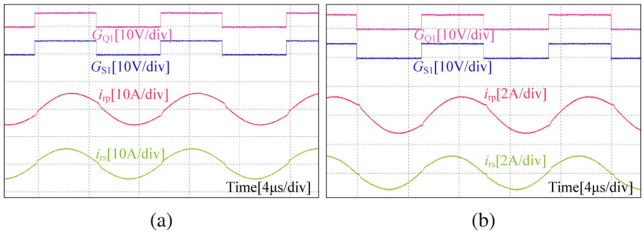

Fig. 12. Detailed waveforms in the P mode with (a) full load and (b) light load.

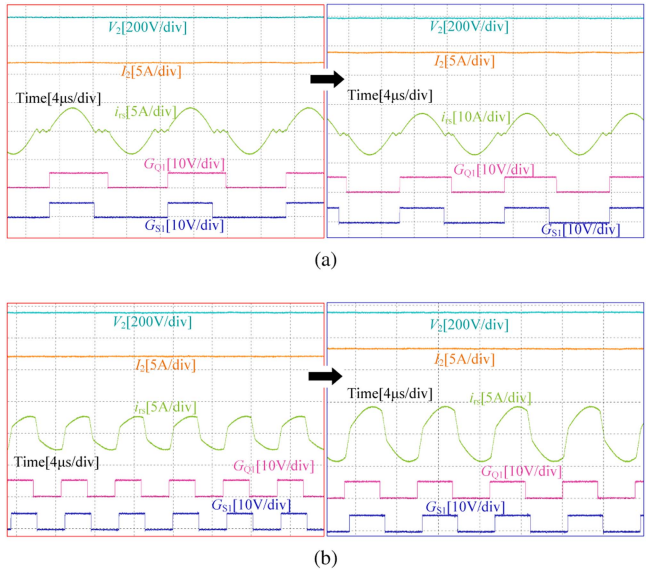

Fig. 13. Steady-state waveforms prior to and following load transitions. (a) Case with $f_s < f_r$. (b) Case with $f_s > f_r$.

in Fig. 16 for $f_s > f_r$. In both scenarios, the system maintains stable operation during load steps up and down. A short period of body diode conduction is observed following the load step, which is expected, as the SR controller intentionally avoids reacting to transient disturbances. The u_{DS} waveforms confirm that SR resumes normal switching shortly afterward without overshoot or erratic behavior.

C. Efficiency and Loss Breakdown

Ultimately, the system efficiency with the proposed SR method is measured using the YOKOGAWA WT5000 power analyzer and compared with VSM-SR, as well as BDR and SiC Schottky diode rectification (SSDR), under various loads and frequencies, as shown in Fig. 17. Fig. 17(a) presents the efficiency with different input voltages at full load, while Fig. 17(b) shows the efficiency with different loads at the nominal frequency.

Fig. 17(a) indicates that the proposed SR strategy significantly improves overall efficiency across a wide input voltage range

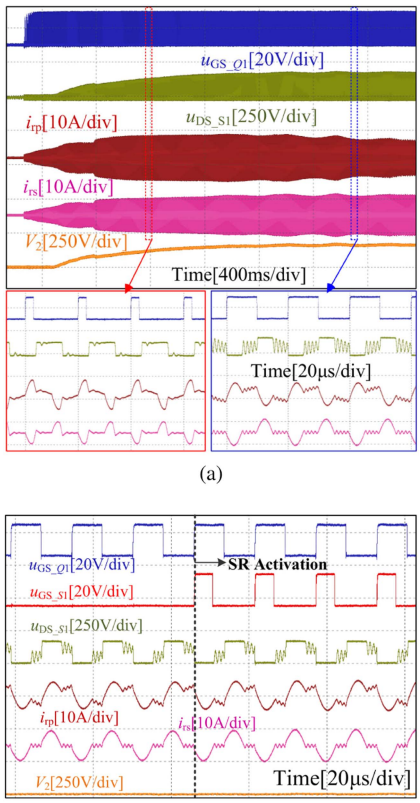

Fig. 14. System behavior during soft-start sequence. (a) Initial phase with SR disabled. (b) Transition phase as SR is activated and conduction shifts from body diode to channel.

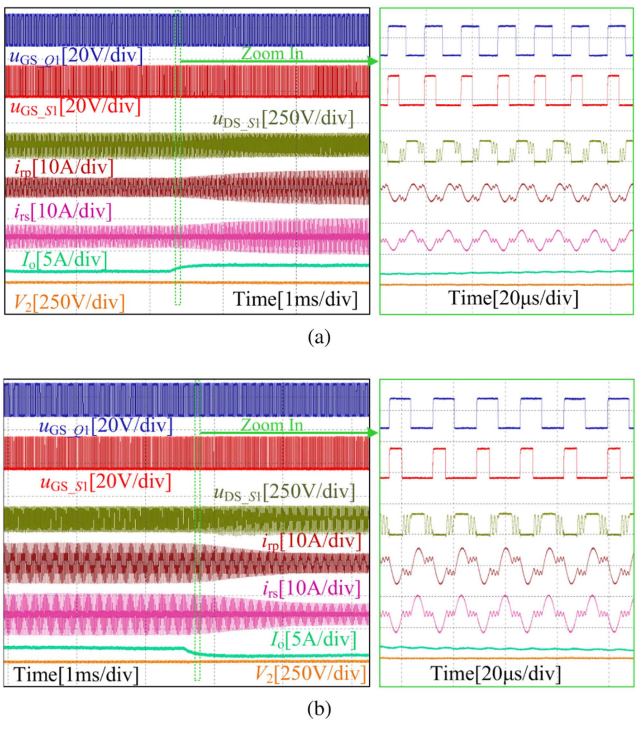

Fig. 15. Proposed SR performance during dynamic load transitions when $f_s < f_r$. (a) Load step-up. (b) Load step-down.

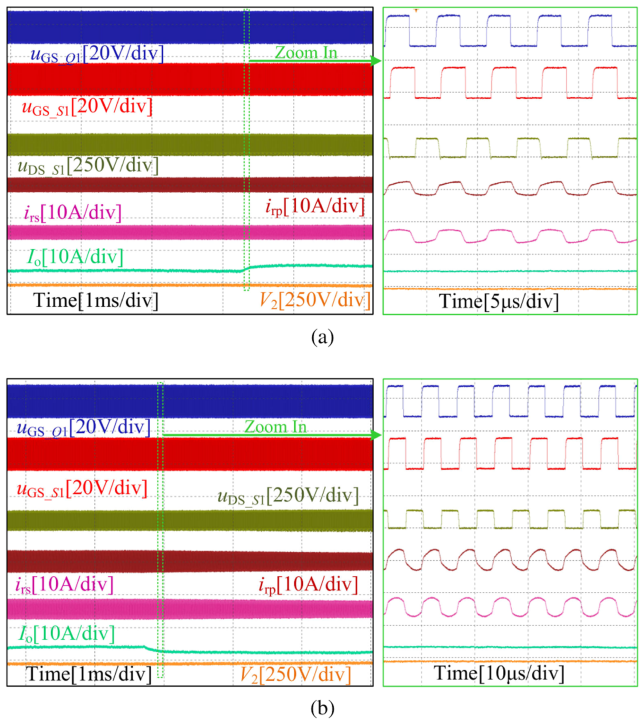

Fig. 16. Proposed SR performance during dynamic load transitions when $f_s > f_r$. (a) Load step-up. (b) Load step-down.

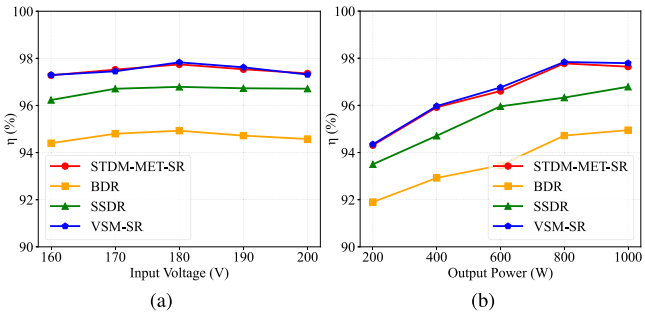

Fig. 17. Efficiency comparison of SR with different input voltages and loads. a) Different Input Voltage (b) Different Loads.

compared to the BDR. Besides, system efficiency is improved when applying unidirectional SSDR compared to BDR, due to the significantly lower forward voltage drop of the Schottky diode, which reduces conduction losses. When employing the VSM-SR, the full-load efficiency of the *CLLC* converter is comparable to the proposed method. Fig. 17(b) reinforces the effectiveness of the proposed SR method at varying output power levels. Fig. 18 presents the loss breakdown comparison between the proposed method and BDR at nominal condition, highlighting that STDM-MET-SR exhibits notably lower device loss than BDR, with minimal differences in other loss categories. These experimental results verify that the power device loss can be significantly reduced by replacing the body diodes with active MOSFET channels. In conclusion, the results demonstrate that the proposed SR approach can significantly enhance system efficiency without requiring additional components or complex control methods.

TABLE III
COMPARISON WITH EXISTING SR METHODS

References	[7]	[12]	[17]	[20]	[23]	[6]	[25]	This work
Type	VSM	VSM	CSM	MCM	MCM	MCM	MCM	MCM
Model	–	–	–	FHA	EHA	TDM	TDM	STDM
Closed-form expression acquired	–	–	–	No	No	No	No	Yes
Extra high-bandwidth sensors required	Yes	Yes	Yes	No	No	No	No	No
Signal sensitivity	Sensitive	Sensitive	Sensitive	Insensitive	Insensitive	Insensitive	Insensitive	Insensitive
Accuracy	High	High	High	Low	Medium	High	High	High
Calculation complexity	Low	Low	Low	Medium	High	High	High	Medium
Implementation complexity	High	Medium	High	Medium	High	High	Medium	Medium
Output power (kW)	1	1	2	3.3	3.3	1.2	3	1
Peak efficiency (%)	95.9	>95	98.3	–	97.2	97.2	97.1	97.8

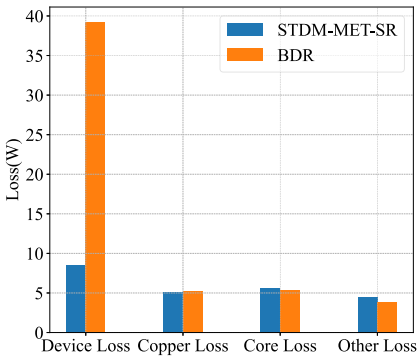

Fig. 18. Loss breakdown comparison with proposed SR and BDR.

Finally, Table III presents a comparative analysis of the proposed SR driving scheme's performance against previously published works. The results demonstrate that the proposed SR driving scheme achieves a more optimal balance between complexity and accuracy compared to the existing SR strategies.

V. CONCLUSION

This article proposes a novel STDM-MET-SR strategy for *CLLC* chargers, providing a straightforward and accurate method for estimating the required gate signals of SR without necessitating costly and bulky hardware or intricate mathematical models. Moreover, the proposed strategy is highly immune to parasitic parameters and system parameter variations, which makes it suitable for practical applications. Experimental results demonstrate that converters with STDM-MET-SR achieve significantly improved efficiency compared to diode rectification. Ultimately, the proposed strategy is proven to be a promising solution that reduces conduction losses and improves the efficiency of *CLLC* converters.

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