# ZVS Implementation Analysis and Optimization Design of *LLC* Converter Based on TDM-DC

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***Abstract*—To improve the operational efficiency of *LLC* converters and ensure zero-voltage switching (ZVS) across the entire operating range, this article proposes an optimized design method based on the time-domain analysis. Existing methods typically ignore the current drop during dead time and the influence of parasitic capacitance, resulting in overly optimistic ZVS estimations. To address this issue, a time-domain model with dead time and capacitance consideration (TDM-DC) is derived. Potential operating trajectories are analyzed, and a solver is established. Based on TDM-DC, key factors affecting ZVS implementation are investigated, and a TDM-DC-based design methodology for *LLC* converters is proposed. Compared with the existing methods, the proposed approach verifies higher accuracy and lower computational complexity, enabling its industrial applicability. A 3-kW prototype achieves 97.0% (500 W) peak efficiency through optimized parameters. The maximum efficiency improvement after optimization is 4.8%. Experimental results under various conditions match theoretical analysis, demonstrating that the *LLC* converter achieves the required output voltage range while maintaining full-range soft switching.**

***Index Terms*—Dead time, *LLC* converter, optimal design, parasitic capacitor, time-domain analysis.**

## I. Introduction

LLC resonant converters are widely used in server power supplies [1], [2], LED lighting [3], [4], onboard battery chargers [5], [6], and renewable energy applications [7], [8] due to their advantages of wide voltage gain, high power density, zero-voltage switching (ZVS), and a narrow variation range of switching frequency. Therefore, optimizing the design of *LLC* converters to improve efficiency is of great significance.

Design approaches based on frequency-domain analysis can result in significant errors under off-resonance conditions, causing excessive converter gain [9], [10], [11], [12], [13], [14]. Compared with time-domain analyses, these approaches often select a smaller excitation inductance $L_m$, thereby increasing circulating currents and associated losses. Prevalent design methods that apply inequality constraints to the inductance ratio $k$ and quality factor $Q$ tend to involve subjective parameter selection, causing substantial deviations from optimal performance.

In wide voltage-range applications, time-domain analysis offers advantages, owing to its precise calculation of resonant waveforms. The prevailing optimization objectives focus on minimizing losses; the authors in [10] and [11] optimize efficiency through loss models; Menke et al. [12] use a weighted sum of efficiencies at different power points as the optimization target; Fang et al. [13] propose a time-weighted average efficiency for battery charging profiles; Wei et al. [14] minimize inductor rms current to indirectly curb losses; and Wei and Mantooth [15] employ weighted averages of primary and secondary currents as optimization objectives.

Optimizing $L_m$ serves as an alternative approach. $L_m$ directly influences the inductor current magnitude required for achieving ZVS in *LLC* converters, conduction losses, and primary-side turn-OFF losses. Lu et al. [9] reduce total conduction losses by identifying the maximum $L_m$ that satisfies voltage gain requirements. The authors in [16] and [17] design converters to operate at peak gain points to maximize $L_m$. Jiao et al. [18] establish the discontinuous current mode (DCM) operational constraints for *LLC*-DC transformer (DCX) converters and derive the maximum $L_m$ under these constraints.

However, an increased $L_m$ diminishes the magnetizing current available for soft switching, necessitating rigorous analysis of switch output capacitance $C_{oss}$ dynamics during the dead time. Conventional methods treat $L_m$ as a constant-current source that charges $C_{oss}$ and derive the ZVS constraint $L_m < t_d / (16 C_{oss} f_r)$, where $t_d$ and $f_r$ represent the dead time and resonant frequency, respectively [19], [20], [21], [22], [23]. However, these approaches assume a constant inductor current during dead time while neglecting its decay, which leads to an overestimation of the ZVS probability.

Furthermore, the implementation of ZVS in primary switches is critically affected by parasitic capacitances present in secondary-side switches and transformers. Studies reveal that even when the constraints in [19], [20], [21], [22], and [23] are met, high-power *LLC* converters may lose ZVS capability due to premature $L_m$ clamping occurring after complete discharge of secondary-side switch capacitance [21], [22]. To address parasitic capacitance in medium-boost transformers, Jiang et al. [24] increase the resonant inductance to ensure that the capacitance is charged before the dead time, thereby enabling reliable ZVS.

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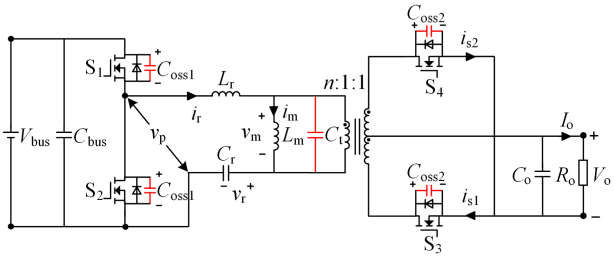


Fig. 1. Topology of the half-bridge *LLC* considering parasitic capacitances.

Sun et al. [25] achieve ZVS by considering the nonlinear switch capacitance and load effects during the design of $L_m$. However, [24] and [25] are limited to DCX applications, necessitating extension to wide voltage-range scenarios. Although Xiao et al. [26] develop a piecewise time-domain model incorporating parasitic capacitances, it relies on idealized models for initial state variables and neglects the effects of capacitance on voltage gain. The advanced state-space analysis in [27] enables precise waveform computation by accounting for both primary and secondary parasitic capacitances, but it suffers from high computational complexity.

The contributions of this work can be summarized as follows.

1) A deadtime-incorporated time-domain model (TDM-DC) is proposed for *LLC* converters, which captures current decay during dead time intervals and accounts for parasitic capacitance effects, thereby preventing the overestimation of ZVS achievement.
2) A TDM-DC-based design methodology is developed to eliminate complex ZVS constraints while guaranteeing full-range ZVS operation. This methodology achieves simpler operations and faster computation due to the superior performance of the TDM-DC.

The rest of this article is organized as follows. Section II derives the TDM-DC for *LLC* converters, taking into account the effects of parasitic capacitance. Section III analyzes the achievement of ZVS under current decay, parasitic effects, and load variations, and validates TDM-DCs accuracy. Section IV proposes a parameter optimization methodology based on TDM-DC and provides detailed design procedures tailored to specific design requirements. Section V presents the experimental verification of the theoretical analysis, along with comprehensive comparative evaluations. Finally, Section VI concludes this article.

## II. Time-Domain Model of *LLC* Converter Considering Dead Time and Parasitic Capacitance (TDM-DC)

The topology of the half-bridge *LLC* resonant converter is shown in Fig. 1. The converter consists of primary-side switches $S_1$ and $S_2$, secondary-side switches $S_3$ and $S_4$, an input capacitor $C_{\text{bus}}$, an output capacitor $C_o$, a transformer $T$ with a turns ratio of $n$:1:1, and a resonant tank. The resonant tank includes the resonant inductor $L_r$, the resonant capacitor $C_r$, and the magnetizing inductance $L_m$. Here, $C_p = 2C_{oss1}$ and $C_s = C_t + 2C_{oss2}/n^2$ are defined.

Transformers have parasitic capacitance due to their electromagnetic coupling. The three-capacitance equivalent model

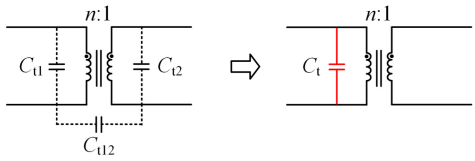


Fig. 2. Transformer parasitic capacitance equivalent model.

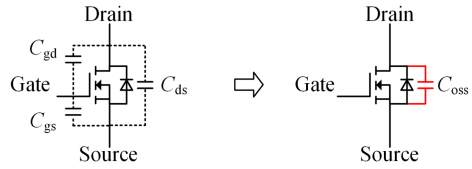


Fig. 3. MOSFET parasitic capacitance equivalent modeling.

is commonly used for dynamic circuit modeling, as shown in Fig. 2. If the line voltage drop is neglected, the three stray capacitances can be represented by a single equivalent capacitance $C_t$ on the primary side [28], as illustrated in Fig. 1.

Due to its physical structure and manufacturing process, a MOSFET has parasitic capacitances between its terminals, as shown in Fig. 3. Since $C_{gs}$ is much larger than $C_{gd}$, the output capacitance ($C_{oss}$) can be considered as $C_{gd}$ and $C_{ds}$ in parallel.

To ensure that the time-domain analysis results are applicable to various primary-side topologies, this article removes the dc component during the analysis. The resonant tank input voltage $v_p$ is defined as the ac component of the drain–source voltage of $S_2$, with an amplitude of $V_{\text{in}} = V_{\text{bus}}/2$. The voltage $v_r$ represents the ac component across $C_r$. For generalized analysis, normalized variables are employed: the voltage base $V_{\text{base}} = V_{\text{in}}$ and the current base $I_{\text{base}} = V_{\text{base}}/\sqrt{L_r/C_r}$. The *LLC* converter adopts a frequency modulation control strategy with a switching frequency $f_s$. Given the symmetry of the waveforms between positive and negative half cycles, this section focuses solely on the half cycle from $S_2$ turn-OFF to $S_1$ turn-ON.

### A. Operating Modes and Time-Domain Expressions of LLC Converter

This article divides the *LLC* converter's operation into dead time phases and conduction phases. During the dead time phases, three subphases are defined based on the states of the secondary-side switch: $P_d$ mode [$S_3$-ON, Fig. 4(a)], $N_d$ mode [$S_4$-ON, Fig. 4(c)], and $O_d$ mode [both OFF, Fig. 4(e)].

The normalized state variables $i_{rn}$, $i_{mn}$, $v_{rn}$, and $v_{pn}$ during the $P_d$ mode are expressed in the time domain as follows:

$$\begin{cases} i_{rn\_pd}(\theta) = \frac{V_u}{u}\sin(u\theta) + I_{rn}\cos(u\theta) \\ i_{mn\_pd}(\theta) = I_{mn} + M\theta/k \\ v_{rn\_pd}(\theta) = \frac{I_{rn}}{u}\sin(u\theta) + \frac{V_u}{u^2} - \frac{V_u}{u^2}\cos(u\theta) + V_{rn} \\ v_{pn\_pd}(\theta) = -\frac{I_{rn}}{up}\sin(u\theta) - \frac{V_u}{u^2p} + \frac{V_u}{u^2p}\cos(u\theta) + V_{pn}. \end{cases} \tag{1}$$

The normalized values $I_{rn}$, $I_{mn}$, $V_{rn}$, and $V_{pn}$ represent the initial states of $i_{rn}$, $i_{mn}$, $v_{rn}$, and $v_{pn}$ at $t = 0$. The normalized time is given by $\theta = -t/\sqrt{L_rC_r}$. Key dimensionless parameters include the voltage gain $M = nV_o/V_{\text{in}}$, the inductance ratio

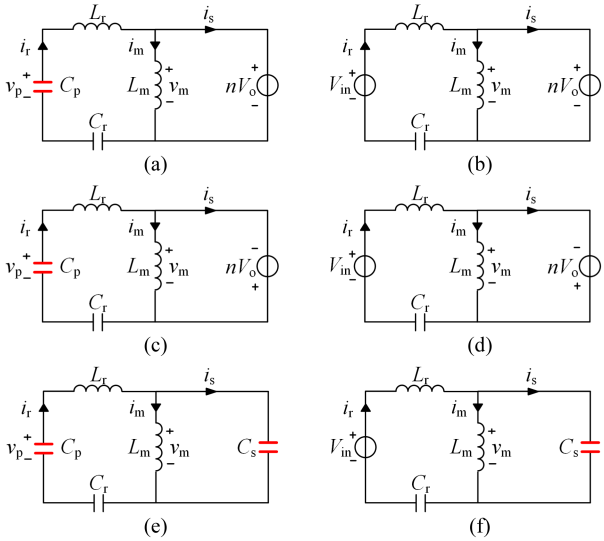


Fig. 4. Equivalent circuit of *LLC* converter in each operating mode. (a) $P_d$ mode. (b) $P$ mode. (c) $N_d$ mode. (d) $N$ mode. (e) $O_d$ mode. (f) $O_s$ mode.

$k = L_m/L_r$, the primary capacitance ratio $p = C_p/C_r$, the auxiliary variable $Vu = Vpn - Vrn - M$, and the auxiliary parameter $u = \sqrt{(p+1)/p}$.

The $N_d$ and $P_d$ modes differ as $v_m$ is clamped by the $-V_o$. Replacing $M$ with $-M$ in (1) yields the time-domain expressions for all state variables in the $N_d$ mode.

Due to minimal $i_m$ variation in the $O_d$ mode, $L_m$ is treated as a constant-current source for solving $i_{rn}$, $v_{rn}$, $v_{pn}$, and $v_{mn}$, while $i_{mn}$ derived from (2). All state variables are expressed in (3)

$$i_{mn\_od} = \int_0^{\theta} v_{mn\_od} d\theta + I_{mn} \tag{2}$$

$$\begin{cases} i_{rn\_od}(\theta) = -\frac{V_v}{v}\sin(v\theta) + gI_{rn}\cos(v\theta) + \frac{1}{qv^2}I_{rn} \\ i_{mn\_od}(\theta) = \frac{V_v}{kqv^3}\sin(v\theta) - \frac{g}{kqv^2}I_{rn}\cos(v\theta) \\ \quad +\frac{1}{k}(V_{mn} - \frac{V_v}{qv^2})\theta - \frac{g}{2kq}I_{rn}\theta^2 + I_{rn} \\ \quad +\frac{g}{kqv^2}I_{rn} \\ v_{rn\_od}(\theta) = V_{rn} - \frac{V_v}{v^2} + \frac{g}{v}I_{rn}\sin(v\theta) + \frac{V_v}{v^2}\cos(v\theta) \\ \quad +\frac{I_{rn}}{qv^2}\theta \\ v_{pn\_od}(\theta) = V_{pn} + \frac{V_v}{pv^2} - \frac{g}{pv}I_{rn}\sin(v\theta) - \frac{V_v}{pv^2}\cos(v\theta) \\ \quad -\frac{I_{rn}}{pqv^2}\theta \\ v_{mn\_od}(\theta) = V_{mn} - \frac{V_v}{qv^2} + \frac{g}{qv}I_{rn}\sin(v\theta) + \frac{V_v}{qv^2}\cos(v\theta) \\ \quad -\frac{gI_{rn}}{q}\theta. \end{cases} \tag{3}$$

The normalized values $V_{mn}$ represent the initial states of $v_{mn}$ at $t = 0$. Key dimensionless parameters include the parasitic capacitance ratio $q = C_s/C_r$, the auxiliary variable $v = \sqrt{(pq+p+q)/pq}$, $g = (pq+q)/(pq+p+q)$, and $V_x = V_m - V_{pn} + V_{mn}$.

During the dead time, $C_p$ is charged until $v_p$ reaches $V_{\text{in}}$, triggering $S_1$ activation. This action disengages $C_p$ from resonance and initiates the conduction phase, during which the equivalent circuits in Fig. 4(a), (c), and (e) simplify to the $P$, $N$, and $O_s$ modes, as shown in Fig. 4(b), (d), and (f), respectively. The time-domain expressions for the state variables during $P$ mode

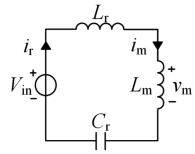

Fig. 5. Operating mode ignoring parasitic capacitance ($S_3$ and $S_4$ OFF).

are given as follows [17]:

$$\begin{cases} i_{rn\_p}(\theta) = -(M + V_{rn} - 1)\sin(\theta) + I_{rn}\cos(\theta) \\ i_{mn\_p}(\theta) = I_{mn} + M\theta/k \\ v_{rn\_p}(\theta) = I_{rn}\sin(\theta) + (M + V_{rn} - 1)\cos(\theta) + 1 - M. \end{cases} \tag{4}$$

By substituting $M$ with $-M$ in (4), the time-domain expressions of the state variables in $N$ mode can be derived.

Given the minimal $v_r$ variation in the $O_s$ mode, $C_r$ is treated as a constant-voltage source for solving $i_{rn}$, $i_{mn}$, and $v_{mn}$, while $v_{rn}$ derived from (5). All state variables are provided in (6)

$$v_{rn\_os} = \int_0^{\theta} i_{rn\_os} d\theta + V_{rn} \tag{5}$$

$$\begin{cases} i_{rn\_os}(\theta) = -\frac{V_w}{w}\sin(w\theta) - I_w\cos(w\theta) - (V_w - V_{mn})\theta \\ \quad +I_w + I_{rn} \\ i_{mn\_os}(\theta) = \frac{V_w}{w}\sin(w\theta) + I_w\cos(w\theta) - (V_w - V_{mn})\theta \\ \quad +I_w + I_{rn} \\ v_{rn\_os}(\theta) = \frac{I_w}{w}\sin(w\theta) + \frac{V_w}{w^2}\cos(w\theta) \\ \quad -\frac{V_{rn}-1}{2k+2}\theta^2 + (I_w + I_{rn})\theta + V_{rn} - \frac{V_w}{w^2} \\ v_{mn\_os}(\theta) = V_w\cos(w\theta) - V_w + V_{mn} \\ \quad +(I_{rn} - I_{mn})\sin(w\theta) \end{cases} \tag{6}$$

where the auxiliary variable $V_w = k(V_{rn} - 1)/(k+1) + V_{mn}$, $I_w = k(I_{mn} - I_{mn})/(k+1)$, and $w = \sqrt{(k+1)/kq}$.

Neglecting the parasitic capacitance $C_s$, the $O_s$ mode circuit reduces to the $O$ mode configuration, as shown in Fig. 5.

The normalized state variables during the $O$ mode are expressed in the time domain as follows [17]:

$$\begin{cases} i_{rn\_o}(\theta) = -h(V_{rn} - 1)\sin(h\theta) + I_{rn}\cos(h\theta) \\ v_{rn\_o}(\theta) = \frac{I_{rn}}{h}\sin(h\theta) + (V_{rn} - 1)\cos(h\theta) + 1 \\ v_{mn\_o}(\theta) = -\frac{kI_{rn}}{h}\sin(h\theta) - \frac{k(V_{rn}-1)}{h^2}\cos(h\theta) \end{cases} \tag{7}$$

where the auxiliary variable $h = \sqrt{1/(k+1)}$. The $O$ mode applications are detailed in Section II-B.

### B. Operating Trajectory and Solver Establishment

The previously proposed operating modes constitute all possible trajectories of the *LLC* converter within half a switching cycle. However, the presence of $C_s$ causes variations in the number of operating modes within the trajectory during subresonant operation, thereby complicating the solver formulation. As shown in Fig. 6(a), the $[t_1, t_2]$ interval features alternating $O_s$ and $N$ modes, resulting in eight modes per half cycle. This study simplifies the analysis by replacing these alternating modes with a single $O$ mode that disregards parasitic effects. The modified trajectory, as shown in Fig. 6(b), contains only the $O_d$, $P_d$, $P$,

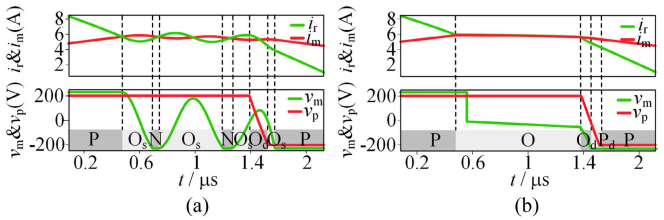


Fig. 6. *LLC* converter operating trajectory diagram. (a) Actual operating trajectory. (b) Simplified operating trajectory.

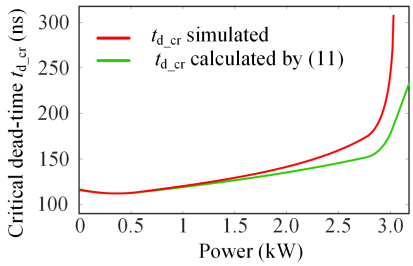


Fig. 7. $t_{d\_cr}$ versus load curves [simulation and calculation by (11), $f_s = 85$ kHz].

TABLE I
TRAJECTORIES AND CONVERSION CONDITIONS OF *LLC* CONVERTER WITH DEAD TIME AND PARASITIC CAPACITANCE

| Operating Trajectories | Transition Conditions | | |
|---|---|---|---|
| $P_dPO_sN/P_dPON$ | $v_{cpn}$=1 | $i_{rn}$=$i_{mn}$ | $v_{mn}$=−$M$ |
| $O_dP_dPO$ | $v_{mn}$=$M$ | $v_{cpn}$=1 | $i_{rn}$=$i_{mn}$ |
| $O_dO_sPO$ | $v_{cpn}$=1 | $v_{mn}$=$M$ | $i_{rn}$=$i_{mn}$ |
| $N_dO_dO_sP$ | $i_{rn}$=$i_{mn}$ | $v_{cpn}$=1 | $v_{mn}$=$M$ |
| $N_dO_dP_dP$ | $i_{rn}$=$i_{mn}$ | $v_{mn}$=$M$ | $v_{cpn}$=1 |
| $N_dNO_sP$ | $v_{cpn}$=1 | $i_{rn}$=$i_{mn}$ | $v_{mn}$=$M$ |

TABLE II
CIRCUIT PARAMETERS OF *LLC* RESONANT CONVERTER

| Items | Values |
|---|---|
| Input voltage $V_{bus}$ | 400 V |
| Turn ratio of transformer $n$ | 14:3:3 |
| Resonant Inductor $L_r$ | 31.66 μH |
| Resonant Capacitance $C_r$ | 80 nF |
| Excitation Inductor $L_m$ | 100 μH |
| Parasitic capacitance of the primary switch $C_p$ | 1.8 nF |
| Total referred parasitic capacitance $C_s$ | 275 pF |

and *O* modes. Table I summarizes all simplified trajectories and their transition conditions.

To determine the variables ($I_{rn}$, $I_{mn}$, $V_{rn}$, $V_{mn}$, $M$) and the mode transition instants ($\theta_1$, $\theta_2$, $\theta_3$), it is necessary to establish boundary conditions for the solver, including continuity conditions, symmetry conditions, conversion conditions (as specified in Table I), and charge conservation constraints.

*1) Continuity Conditions:* If $X$ and $Y$ denote two distinct adjacent phases, with $\theta_{\text{start}}$ and $\theta_{\text{end}}$ representing the initial and final instants of each mode, respectively, the continuity conditions are satisfied

$$\begin{aligned} i_X(\theta_{\text{end}}) &= i_Y(\theta_{\text{start}}) \\ v_X(\theta_{\text{end}}) &= v_Y(\theta_{\text{start}}). \end{aligned} \tag{8}$$

*2) Symmetry Conditions:* If $X$ represents the initial mode of the trajectory and $Y$ denotes the final mode, the symmetry conditions become

$$\begin{aligned} i_X(\theta_{\text{start}}) + i_Y(\theta_{\text{end}}) &= 0 \\ v_X(\theta_{\text{start}}) + v_Y(\theta_{\text{end}}) &= 0. \end{aligned} \tag{9}$$

*3) Charge Conservation Constraints:* The charge conservation constraints require

$$\int_0^{\theta_4} (i_{rn}(\theta) - i_{mn}(\theta))d\theta = P_{on}\theta_4/M \tag{10}$$

where $P_{on}$ denotes the normalized value of the transmitted power. The parameter $\theta_4 = 1/(2f_s\sqrt{L_rC_r})$.

For various operating trajectories, all unknowns can be determined by applying all boundary conditions, which defines them as an operating trajectory solver.

## III. ANALYSIS OF ZVS IMPLEMENTATION BASED ON TDM-DC

In Section II, solvers for all operating trajectories were established. When the switching frequency and power are known, the termination instants of each operating mode can be calculated. The transition time from the dead time phase to the conduction phase marks the complete discharge of $C_{oss}$, which is defined as the critical dead time $t_{d\_cr}$. A shorter $t_{d\_cr}$ indicates an easier realization of ZVS, and this parameter will be used to evaluate the difficulty of ZVS implementation in subsequent analysis. The simulation results in this section are obtained using PLECS version 4.7.3.

### A. Impact of Dead Time Current Decay on ZVS Implementation

The conventional dead time calculation method, as shown in (11), assumes constant current during dead time [18]. Fig. 7 compares the $C_s$-neglected simulated $t_{d\_cr}$ with values derived from (11), while Table II lists the *LLC* converter parameters

$$I_{\text{off}}t_{d\_cr} = 2V_{\text{in}}C_p \tag{11}$$

where $I_{\text{off}}$ is the switch-OFF current.

Fig. 7 reveals that the $t_{d\_cr}$ calculated by (11) is lower than the simulated values, and this discrepancy grows with increasing power, leading to optimistic ZVS estimates.

The waveforms in Fig. 8(a) show a significant reduction in $i_r$ during the dead time, deviating from the assumed constant current $I_{\text{off}}$ (yellow). The actual $v_{DS2}$ waveform (green) takes longer to reach zero than the theoretical prediction (yellow) from (11). At higher power levels [see Fig. 8(b)], $i_r$ reverses during dead time, resulting in the complete loss of ZVS, even though (11) indicates that ZVS can be maintained. This exposes limitations in constant-current-based ZVS estimation and highlights

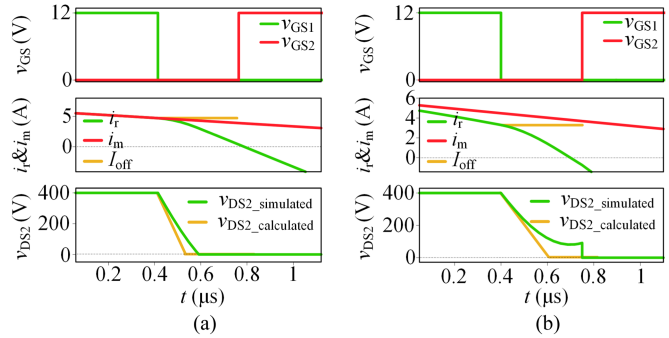


Fig. 8. *LLC* converter waveforms [simulation and calculation by (11), $f_s = 85$ kHz]. (a) 2.8 kW waveform. (b) 3.1 kW waveform.

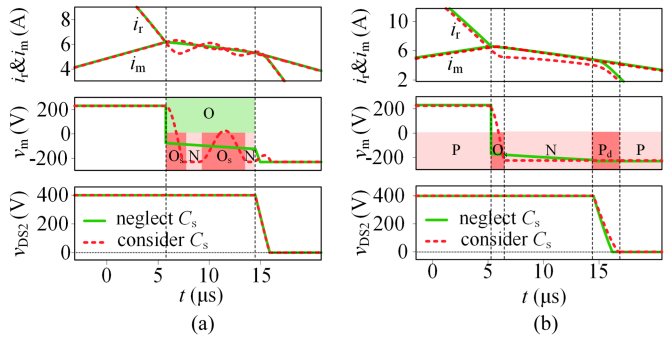


Fig. 10. *LLC* converter waveforms ($C_s$-considered and $C_s$-neglected, $f_s = 85$ kHz). (a) 2 kW waveform. (b) 2.7 kW waveform.

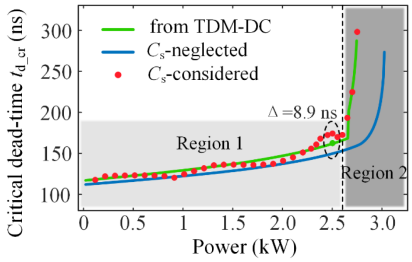


Fig. 9. $t_{d\_cr}$ versus load curves (simulation and TDM-DC derived, $f_s = 85$ kHz).

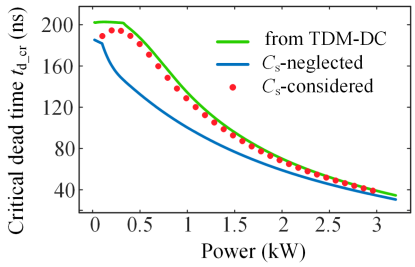


Fig. 11. $t_{d\_cr}$ versus load curves (simulation and TDM-DC derived, $f_s = 110$ kHz).

the necessity of considering dead time for the accurate ZVS evaluation.

### B. *Impact of Parasitic Capacitance* $C_s$ *on ZVS Implementation*

The previous analysis examined that how current decay during dead time negatively affects the attainment of ZVS. When incorporating parasitic effects, the ZVS conditions of *LLC* converter deteriorate further. The initial investigation focuses on the influence of $C_s$ during subresonant operation, with Fig. 9 comparing the $t_{d\_cr}$ derived from TDM-DC with simulated results, both with and without $C_s$.

Fig. 9 shows that TDM-DC calculation results exhibit an error of less than 8.9 ns (5.5% of the dead time) compared with $C_s$-considered simulations. The TDM-DC calculation results are slightly different from the $C_s$-ignored simulations in region 1, but significantly higher than the results in region 2. This discrepancy arises from $C_s$-induced changes in the operating trajectory, as analyzed in the following text.

The simulation waveforms, as shown in Fig. 10(a), correspond to the operating conditions of region 1 in Fig. 9. When considering $C_s$, the $i_r$ and $i_m$ waveforms exhibit oscillations after their intersection, rather than overlapping as observed when $C_s$ is neglected. The oscillation centers of these currents remain close to the waveforms obtained without $C_s$ consideration. This proximity ensures that the $i_r$ magnitudes at the start of the dead time, as well as the current decay rates during dead time, remain similar, ultimately resulting in equivalent $t_{d\_cr}$. The analysis confirms that the effects of parasitic capacitance diminish significantly when multiple crossings between $i_r$ and $i_m$ occur within

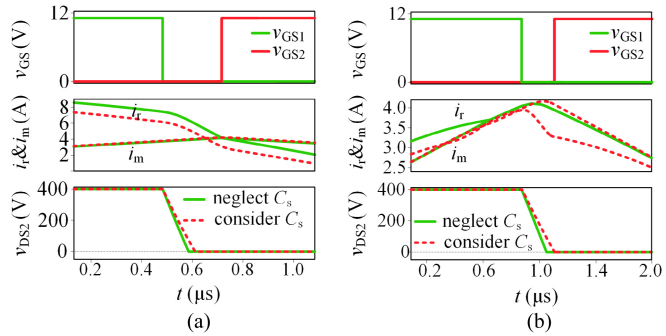


Fig. 12. *LLC* converter waveforms ($C_s$-considered and $C_s$-neglected, $f_s = 110$ kHz). (a) 1 kW waveform. (b) 50 W waveform.

half a switching cycle. Therefore, employing the *O* mode for trajectory simplification does not introduce significant errors.

Unlike region 1 of Fig. 9, under heavier loads, $i_r$ maintains a nearly parallel declining trajectory after its initial intersection with $i_m$, causing a much lower $i_r$ at dead time entry and a longer $t_{d\_cr}$, as shown in Fig. 10(b). This phenomenon occurs when the converter operates along the $P_dPO_sN$ trajectory, with substantially degraded ZVS conditions. The green curve in Fig. 9 verifies that the TDM-DC accurately captures this behavior.

Under over-resonant operation, significant differences in $t_{d\_cr}$ are observed between simulations with and without $C_s$ consideration at light-load conditions (see Fig. 11). This is because the minimal turn-OFF current at light loads makes $t_{d\_cr}$ highly sensitive—small reductions in current can dramatically extend $t_{d\_cr}$. Fig. 12(a) illustrates that the inclusion of $C_s$ reduces the

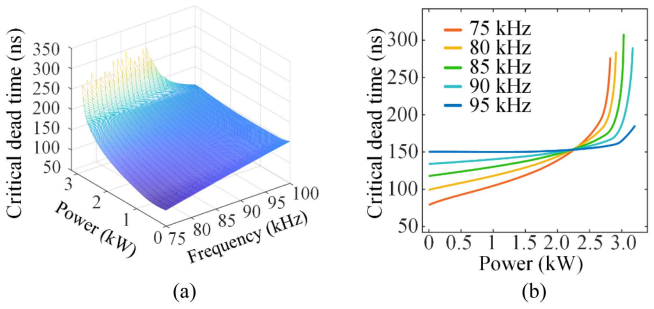


Fig. 13. $t_{d\_cr}$ versus load and frequency (subresonant). (a) $t_{d\_cr}$ versus load and frequency. (b) $t_{d\_cr}$ versus load.

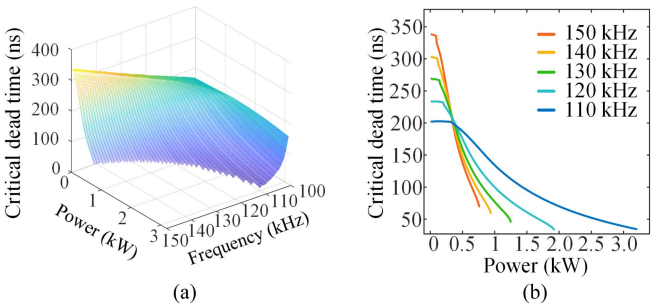


Fig. 14. $t_{d\_cr}$ versus load and frequency (over-resonant). (a) $t_{d\_cr}$ versus load and frequency. (b) $t_{d\_cr}$ versus power.

turn-OFF current, thereby prolonging $t_{d\_cr}$. Fig. 12(b) demonstrates that $C_s$ accelerates current decay during the dead time, which also contributes to the extension of $t_{d\_cr}$.

Therefore, TDM-DC calculations are consistent with the full-frequency simulations with $C_s$, confirming that the TDM-DC method accurately reflects the criteria for achieving ZVS.

### C. Impact of Load Conditions on ZVS Implementation

Fig. 13(a) shows the TDM-DC-calculated $t_{d\_cr}$ as a function of load in subresonant mode. In high-power regions, $t_{d\_cr}$ is significantly higher than in low-power regions, indicating that achieving ZVS becomes more challenging at higher power levels.

The curves in Fig. 13(b) demonstrate that the most stringent ZVS condition occurs during maximum power operation. This is because heavier loads reduce the slope of $i_r$ during the $O_{(s/d)}$ mode and decrease the turn-OFF current, thereby prolonging $t_{d\_cr}$.

Fig. 14(a) illustrates the relationship between $t_{d\_cr}$ and load in the over-resonant mode, as obtained using TDM-DC. Fig. 14(b) shows that the maximum $t_{d\_cr}$ occurs at the maximum switching frequency and minimum power. This is because, during low-power operation, the $O_dO_sPO$ trajectory is followed, in which the turn-OFF current ($I_{\text{off}} \approx i_m$) becomes minimal compared with other trajectories. With negligible variation in the $i_m$ slope at low power, the equation $I_{\text{off}} = nV_o/(4L_mf_s)$ indicates that increasing the switching frequency reduces the turn-OFF current, thereby worsening the ZVS conditions.

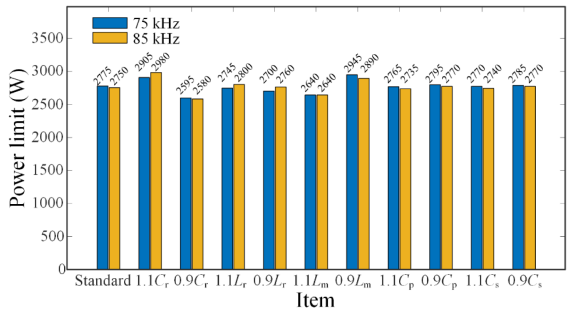


Fig. 15. Sensitivity analysis of the ZVS realization range.

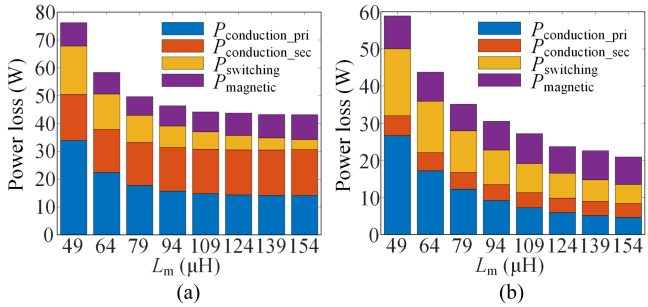


Fig. 16. Power loss versus $L_m$ ($f_r = 100$ kHz, $f_s = 70$ kHz, $V_{\text{bus}} = 400$ V, $V_o = 58$ V, and $n = 14{:}3$). (a) $P = 1500$ W. (b) $P = 750$ W.

### D. Sensitivity Analysis of the ZVS Realization Range

Fig. 15 shows the effect of ±10% tolerances in $C_r$, $L_r$, $L_m$, $C_p$, and $C_s$ on the ZVS power range. A ±10% change in $C_r$ causes up to an 8.36% variation in the ZVS range. For $L_r$ and $L_m$, the maximum changes are 2.7% and 6.13%, respectively. $C_p$ and $C_s$ have minimal impact, with changes within 1%. Thus, tolerances in $C_r$, $L_r$, and $L_m$ moderately affect the ZVS range. In practice, designing for 5%–10% additional power margin can help ensure ZVS operation.

## IV. Parameter Optimization Design Based on TDM-DC

The TDM-DC method effectively captures *LLC* resonant converters' ZVS characteristics, serving as the foundation for the proposed parameter optimization method. This approach directly assesses ZVS feasibility by checking for the existence of solutions in numerical solvers and optimizes parameters by maximizing $L_m$ to reduce power losses. Thus, the relationship between power loss and $L_m$ should be analyzed first.

### A. Relationship Between Power Loss and $L_m$

Fig. 16 illustrates power losses versus $L_m$ in 70-kHz/58-V *LLC* converters, using the calculation method described in [10]. Fig. 16(a) shows that increasing $L_m$ reduces primary-side conduction losses, thereby decreasing total losses. This occurs because a larger $L_m$ decreases $i_m$, reducing primary-side rms current.

At full-load output of 1500 W, when $L_m$ increases from 49 to 109 $\mu$H (+122%), the loss decreases by 32 W, resulting in a 2.1% increase in efficiency. At 50% rated load, increasing $L_m$

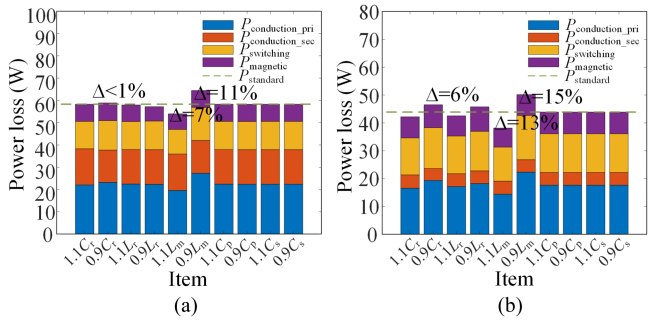


Fig. 17. Sensitivity analysis of the power loss. (a) $P = 750$ W. (b) $P = 1500$ W.

from 49 to 109 $\mu$H reduces the loss by 31.6 W, corresponding to a 4.2% efficiency improvement. As $L_m$ increases further, the loss reduction at full load becomes marginal, while at half load, the total loss decreases by an additional 6.28 W, with a corresponding 0.8% efficiency gain. Therefore, increasing $L_m$ is more effective for efficiency improvement under light-load conditions.

### B. Sensitivity Analysis of the Power Loss

To assess the impact of component tolerances, the sensitivity of total loss to $C_r$, $L_r$, $C_p$, and $C_s$ is analyzed. The design with $L_m = 64$ $\mu$H ($C_r = 174$ nF, $L_r = 14.56$ $\mu$H, $C_p = 1.8$ nF, and $C_s = 275$ pF, as shown in Fig. 16) is used. Total loss is calculated at output powers of 1500 and 750 W, with each parameter varied by $\pm 10\%$. Results are shown in Fig. 17.

The green dashed line in the figure shows the baseline loss without parameter tolerances. At 750-W output, $L_r$ and $C_r$ tolerances cause up to a 6% change in loss, but only a 0.34% change in efficiency, showing weak sensitivity. $L_m$ tolerance causes up to a 15% change in loss, confirming its strong effect. At 1500-W output, tolerances of parameters other than $L_m$ change the loss by less than 1%, indicating reduced sensitivity at higher power. Tolerances of $C_p$ and $C_s$ mainly affect dead time dynamics and have a negligible impact on efficiency.

### C. TDM-DC-Based Parameter Optimization Methodology

The steps of the parameter optimization method are shown in Fig. 18. This section details the parameter optimization process through a design case, following these steps.

*Step 1*: Basic parameters are determined based on circuit design requirements. The basic parameters of the design case are presented in Table III.

The parasitic capacitance $C_t$ can be estimated during transformer design using the method in [29] or extracted from the impedance characteristics after fabrication as in [30].

The transformer's open-circuit impedance peaks at the first parallel resonance frequency $f_1$. Using an impedance analyzer to find $f_1$, $C_t$ can be calculated with the following equation:

$$f_1 = \frac{1}{2\pi\sqrt{L_m C_t}}. \tag{12}$$

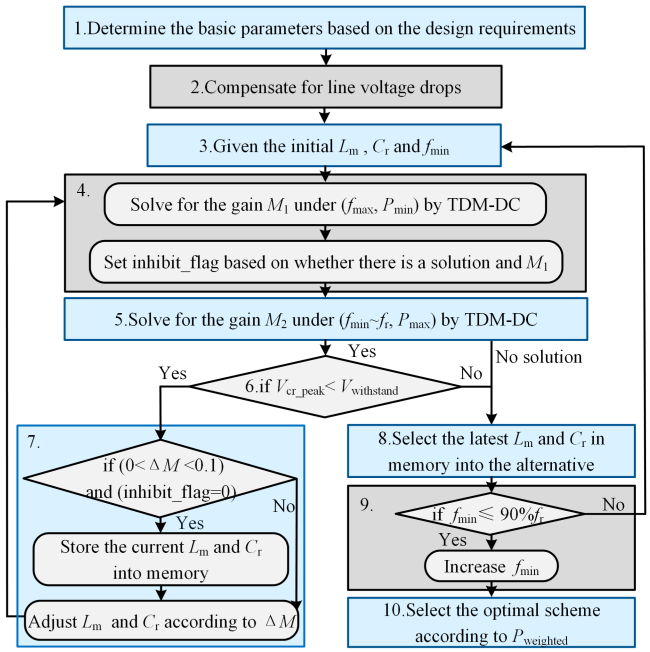


Fig. 18. Flowchart of the parameter optimization method based on TDM-DC.

TABLE III
BASIC PARAMETERS OF PROTOTYPE

| Items | Values |
|---|---|
| Resonant frequency $f_r$ | 100 kHz |
| Maximum operating frequency $f_{max}$ | 150 kHz |
| Turn ratio of transformer $n$ | 14:3:3 |
| Input voltage $V_{bus}$ | 400 V |
| Parasitic capacitance of the primary switch $C_p$ | 925 pF×2 |
| Total referred parasitic capacitance $C_s$ | 255 pF |
| Maximum output power $P_{max}$ | 3000 W |
| Maximum output voltage $V_{o\_max}$ | 58 V |
| Minimum output voltage $V_{o\_min}$ | 36 V |

If $f_1$ is too high for the instrument, connect an auxiliary capacitor $C_{aux}$ in parallel with the primary side and subtract its effect from the result. The transformer of the prototype in this article was measured to have $C_t = 85.3$ pF.

Due to the nonlinearity of $C_{oss}$, the time-equivalent capacitance $C_{o(tr)}$ or the charge-equivalent capacitance $C_{Q,\mathrm{eq}}$ is used for modeling. $C_{o(tr)}$ is given in the datasheet, while $C_{Q,\mathrm{eq}}$ can be calculated using the following equation [31]:

$$C_{Q,\mathrm{eq}}(V_{DS}) = \frac{Q_{oss}(V_{DS})}{V_{DS}} = \frac{\int_0^{V_{DS}} C_{oss}(v)dv}{V_{DS}}. \tag{13}$$

In the prototype of this article, $C_{oss1} = 925$ pF and $C_{oss2} = 1848$ pF.

*Step 2*: Compensate line voltage drop. The equivalent input voltage $V_{\mathrm{in\_eq}}$ is reduced according to (14) in order to simulate the line voltage drop effects

$$V_{\mathrm{in\_eq}} = V_{\mathrm{in}} - \frac{P_{\mathrm{max}}}{\eta V_{\mathrm{in}}} R_{\mathrm{con1\_est}}$$
$$R_{\mathrm{con1\_est}} = R_{ds(\mathrm{on})1} + R_{Cr} + R_{Lr} + R_{Tp} \tag{14}$$

where the efficiency $\eta$ is estimated at 92%. The total primary-side conduction resistance $R_{\mathrm{con1\_est}}$ includes the switch ON-resistance $R_{ds(\mathrm{on})1}$, resonant capacitor resistance $R_{Cr}$, resonant inductor ac resistance $R_{Lr}$, and transformer primary ac resistance $R_{Tp}$. $R_{ds(\mathrm{on})1}$ and $R_{Cr}$ derive from datasheets, while $R_{Lr}$ and $R_{Tp}$ are estimated via [32]. With $R_{\mathrm{con1\_est}}$ set to 0.2 Ω, $V_{\mathrm{in\_eq}}$ becomes 196 V. To offset secondary-side voltage drops, the target maximum output voltage $V_{\mathrm{target\_max}}$ is set to 60 V.

*Step 3*: Given the initial $L_m$, $C_r$, and $f_{\min}$. The initial minimum operating frequency $f_{\min}$ is set to 70% of $f_r$.

*Step 4*: The TDM-DC solver computes gain $M_1$ under ($f_{\max}$, $P_{\min}$) conditions. The minimum output power $P_{\min}$ is set to 1% of $P_{\max}$. If either no solution exists (indicating ZVS loss) or $M_1$ exceeds $M_{\mathrm{target\_min}}$ (defined as $nV_{o\_\min}/V_{\mathrm{in}}$), the inhibit_flag should be set to 1 to prevent potential storage behavior in Step 7. Otherwise, the flag should be cleared.

*Step 5*: The TDM-DC solver verifies solution existence across the ($f_{\min}$ to $f_{\max}$, $P_{\max}$) operating region. Any unsolved frequency indicates ZVS loss, which initiates Step 8. The gain under ($f_{\min}$, $P_{\max}$) conditions is $M_2$.

*Step 6*: Maintain the peak voltage of $C_r$ under conditions ($f_{\min}$, $P_{\max}$) below its rated withstand voltage (850 V), or the procedure will proceed to Step 8.

*Step 7*: Adjust $L_m$ and $C_r$ according to $\Delta M.\Delta M = M_2 - M_{\mathrm{target\ max}}$, where $M_2$ is the gain from Step 5, and $M_{\mathrm{target\_max}} = nV_{\mathrm{target\_max}}/V_{\mathrm{in\_eq}}$. Current $L_m$ and $C_r$ values must be stored before adjustment when $0 < \Delta M < 0.1$ and inhibit flag $= 0$.

The adjustment strategy follows these rules: reducing $L_m$ to boost gain when $\Delta M \leq -0.1$; increasing $C_r$ to suppress gain when $\Delta M \geq 0.1$; elevating $L_m$ to optimize efficiency, when $0 < \Delta M < 0.1$; and decreasing $C_r$ to enhance gain when $-0.1 < \Delta M \leq 0$. The adjustment step sizes for $L_m$ and $C_r$ are 1 $\mu$H and 1 nF, respectively. Operation returns to step 4 after adjustment.

*Step 8*: Store the latest $L_m$ and $C_r$ parameters from Step 7 as candidates, achieving maximum $L_m$ at minimum operating frequency with minimal primary-side conduction losses.

*Step 9*: Increase the minimum operating frequency $f_{\min}$. This adjustment narrows the frequency variation range in the design. After increasing $f_{\min}$, return to Step 3. When $f_{\min}$ exceeds 90% of $f_r$, execute Step 10.

*Step 10*: Determine the optimal solution through comprehensive loss $P_{\mathrm{weighted}}$. Since $L_m$ exerts greater influence on primary-side conduction loss in low-power operation, a comprehensive power loss calculation formula that integrates weighted full-load and half-load losses is developed, enabling systematic efficiency optimization across varying operating conditions

$$P_{\mathbf{weighted}} = \beta_{\mathrm{half}} P_{\mathrm{loss\_half}} + \beta_{\mathrm{full}} P_{\mathrm{loss\_full}}. \tag{15}$$

In this case, $\beta_{\mathrm{half}}$ and $\beta_{\mathrm{full}}$ are both 0.5. Following Yu et al.'s study [10], power losses of all candidate solutions under ($f_{\min}$, $P_{\max/\mathrm{half}}$) conditions were computed. Fig. 19 shows $P_{\mathrm{weighted}}$ for different designs. The $f_{\min} = 75$ kHz configuration ($L_m = 75$ $\mu$H, $C_r = 88$ nF, and $L_r = 28.784$ $\mu$H) was ultimately selected, as designs with $f_{\min}$ between 74 and 77 kHz exhibited comparable $P_{\mathrm{weighted}}$.

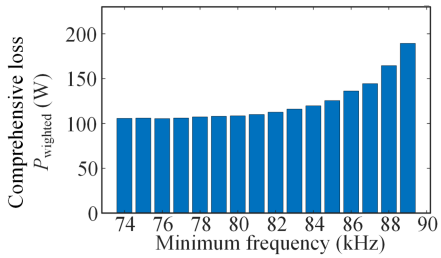


Fig. 19. Comprehensive conduction loss of each design solution.

### D. Measures to Safeguard Numerical Accuracy and Stability

The parameter design process is implemented in MATLAB R2021a. To improve the numerical stability and accuracy of the computational process, the following measures are taken.

1) Use the int() function to solve the integral term with higher precision.
2) Use the *f*solve() function to solve nonlinear equations. Its accuracy can be improved by setting the values of the options FunctionTolerance, StepTolerance, and OptimalityTolerance, e.g., all to $10^{-9}$.
3) The condition number $\kappa(J)$ is monitored during the *f*solve() function solution process. When $\kappa(J)$ fails to converge or persistent oscillations occur, the initial value needs to be adjusted to resolve the problem.
4) Using the calculation results of similar parameters as the initial point improves the convergence speed and avoids *f*solve() from falling into the local optimal solution.

### E. Simplified Methods for Engineers

Engineers can optimize *LLC* converter parameters through simulation as follows.

1) After initial resonant parameter selection, create a simulation model. Add parallel capacitors to the primary and secondary switches to represent $C_p$ and $C_s$, with values obtained from datasheets. Use a 1.5 times margin to include transformer parasitic capacitance.
2) Simulate at 110% rated load and minimum operating frequency. If output voltage requirements are met, increase $L_m$ to improve efficiency. If not, decrease $C_r$ and increase $L_r$, keeping the resonant frequency unchanged.
3) Repeat step 2 until ZVS is lost in the primary switches or the voltage of $C_r$ exceeds the rated withstand voltage. The $L_m$ at this point is the upper ZVS limit. For margin, select 80% of this $L_m$ for the final design.

## V. Simulation and Experimental Verification

An *LLC* resonant converter prototype (see Fig. 20) was constructed according to the design methodology described in Section IV, with key parameters, as listed in Table IV.

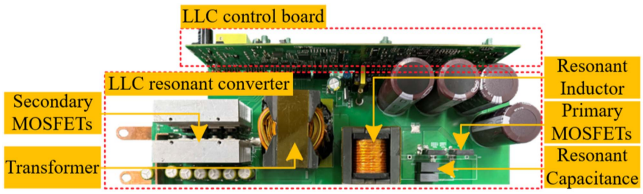


Fig. 20. *LLC* resonant converter prototype.

TABLE IV
PARAMETERS OF THE PROTOTYPE *LLC* CONVERTER

| Key Component | Parameters |
|---|---|
| $S_1$-$S_2$ | IPW60R060P7 |
| $S_3$-$S_4$ | 4 IRFB4332PbF in parallel |
| Transformer | PQ6565, PC95, $L_m = 74.56$ µH |
| Resonant inductance | PQ5050, PC95, $L_r = 28.524$ µH |
| Resonant capacitors | MMKP82, 1000Vdc, $C_r$ =33+56 nF |

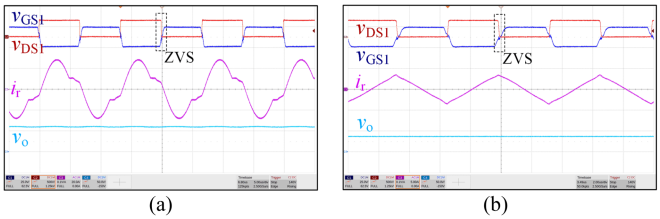


Fig. 21. *LLC* converter waveforms for output voltage-range compliance. (a) $V_{\rm bus} = 400$ V, $P = 3000$ W, and $f_s = 75$ kHz. (b) $V_{\rm bus} = 400$ V, $P = 30$ W, and $f_s = 150$ kHz.

The parameters of actual components exhibit virtually negligible deviations from their theoretical values, primarily due to manufacturing processes and commercial specifications.

### A. Verification of Design Requirements

Fig. 21(a) shows the full-load experimental waveforms, achieving a 58.6 V output at $f_{\rm min}$, which meets the 58 V requirement. Fig. 21(b) illustrates the minimum-power operation, delivering a 35.6 V output at $f_{\rm max}$, satisfying the 36 V specification. ZVS operation is verified in both conditions.

### B. Verification of Waveforms

This section shows the agreement between the experimental and computed waveforms using operational trajectory examples, proving TDM-DCs reliability in ZVS estimation.

Fig. 22 presents the experimental and calculated waveforms of the converter during $P_dPO_sN$ operation, using consistent color schemes and coordinate scales. Fig. 22(a) shows that $v_{DS3}$ reaches $2v_o$ without discharge, which confirms the $P_dPO_sN$ trajectory in which $i_r$ and $i_m$ no longer intersect.

Fig. 23 presents the experimental and calculated waveforms of the converter's $O_dO_sPO$ operation. As seen in Fig. 23(b) and (d), TDM-DC employs the $O$ mode instead of an $O_sPO_s$ segment. In this case, the simplified calculations accurately reflect the linear trends of $i_r$ and the resonance of $v_{DS3}$, showing good agreement between the experimental results and theoretical calculations.

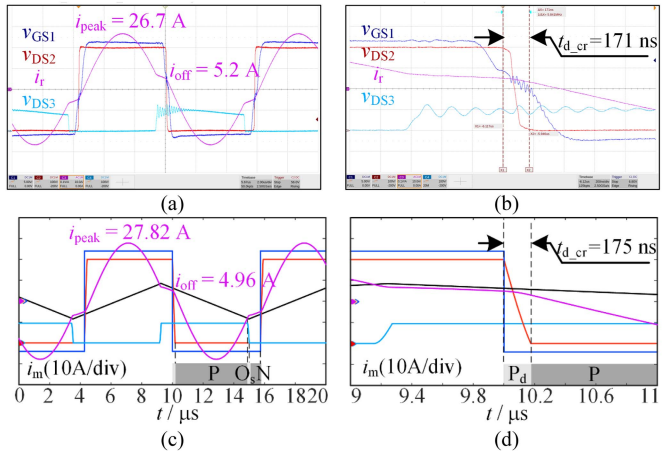


Fig. 22. *LLC* converter key waveforms ($P = 3000$ W, $f_s = 87$ kHz, $P_dPO_sN$). (a) Experimental waveforms. (b) Experimental turning OFF waveforms. (c) Calculated waveforms. (d) Calculated turning OFF waveforms.

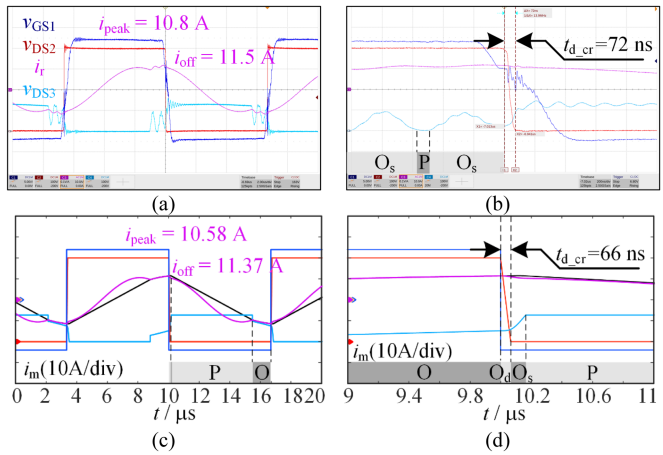


Fig. 23. *LLC* converter key waveforms ($P = 650$ W, $f_s = 75$ kHz, $O_dO_sPO$). (a) Experimental waveforms. (b) Experimental turning OFF waveforms. (c) Calculated waveforms. (d) Calculated turning OFF waveforms.

Fig. 24 shows the experimental and calculated waveforms of the converter operating in $N_dO_dO_sP$ trajectory. The rise in $v_{DS3}$ voltage during the dead time, as shown in Fig. 24(b) and (d), indicates that $C_s$ partially shunts $i_r$, thereby accelerating its decay. This trend worsens the ZVS conditions by reducing the available discharging current.

### C. Comparison of Critical Dead Time

Fig. 25 shows the $t_{d\_cr}$ variations under full-load conditions across operating frequencies. The blue curve represents theoretical predictions calculated during the design process, where conservative efficiency estimates and larger parasitic parameters were used to ensure a safety margin. These values exceed experimental measurements, indicating the converter's tolerance for demanding ZVS conditions. Meanwhile, $t_{d\_cr}$ calculations using actual efficiency and parasitic parameters closely match experimental results (deviation $< 9.4\%$), confirming the accuracy of the TDM-DC time-domain model.

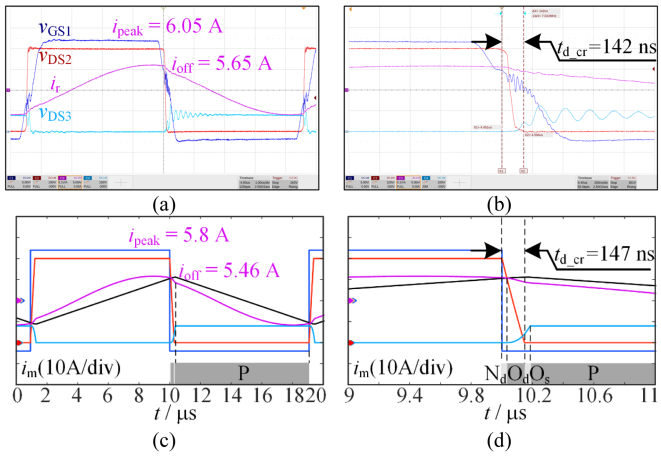


Fig. 24. *LLC* converter key waveforms ($P = 400$ W, $f_s = 110$ kHz, $N_dO_dO_sP$). (a) Experimental waveforms. (b) Experimental turning OFF waveforms. (c) Calculated waveforms. (d) Calculated turning OFF waveforms.

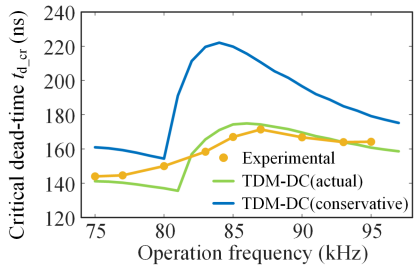


Fig. 25. $t_{d\_cr}$ versus frequency ($V_{bus} = 400$ V and $P = 3000$ W).

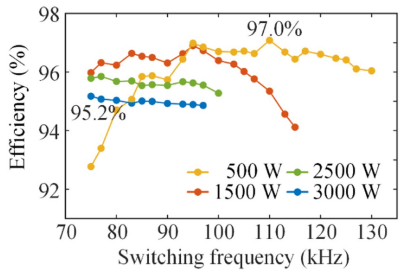


Fig. 26. Efficiency curves at various switching frequencies.

## D. Efficiency

Fig. 26 presents the efficiency characteristics of the proposed converter under varying switching frequencies. Efficiency data at 2500 and 3000 W were unrecorded due to derating operation in over-resonant state caused by current limitations. The converter achieves 95.2% peak efficiency at rated load with a 97.0% peak at 500 W, demonstrating the role of the proposed design methodology in efficiency optimization.

Fig. 27 compares the converter efficiency before and after optimization. The resonant parameters of the *LLC* converter before optimization are: $L_m = 52.65$ $\mu$H, $C_r = 82$ nF, and $L_r = 30.891$ $\mu$H. Solid circles represent the efficiency data after optimization, while hollow circles represent the data before optimization. For each power level (denoted by color), efficiency was measured at multiple load currents due to the variable output

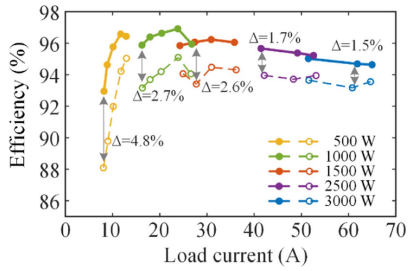


Fig. 27. Comparison of efficiency before and after optimization.

TABLE V
COMPARISONS OF DIFFERENT DESIGN METHODS

| Ref. | Model used | Optimization goal | ZVS constraint | Parasitic capacitance | Compute speed |
|---|---|---|---|---|---|
| [11] | Ideal | Minimal loss | (16) | Ignore | 14.655 s |
| [14] | Ideal | Minimal $i_{p\ RMS}$ | (17) | Consider | 255.88 s |
| [16] | Ideal | Maximal $L_m$ | Simulation verification | Ignore | slow |
| [24] | Piecewise approx. | Maximal $L_m/L_r$ | $v_{ds}(t)$ for MOSFET | Consider | slow |
| Proposed | TDM-DC | Minimal $P_{weighted}$ | TDM-DC equations | Consider | 22.18 s |

voltage of the *LLC* converter. After optimization, the full-load efficiency improved by up to 1.5%, with a maximum gain of 4.8% at 500 W. The improvement gradually decreases as the output power increases, indicating that increasing $L_m$ has a more significant effect on efficiency under light-load conditions.

## E. Comparison of Design Methods

Table V compares the proposed method with other time-domain approaches. The TDM-DC model demonstrates higher accuracy than the idealized models in [11], [14], and [16], and matches the accuracy of the piecewise approximation model.

The proposed method directly optimizes power losses, offering more direct and accurate optimization than [14], [16], and [24]. It considers both full-load and half-load converter losses, avoiding additional losses during partial-load operation that occur with single-point optimization. By maximizing $L_m$ across varying $f_{min}$ values, the approach reduces the number of iterations compared with exhaustive searches, thereby improving computational efficiency.

Regarding ZVS constraints, the ZVS conditions in [11] and [14] shown as (16) and (17) assume constant $i_r$ during the dead time, which leads to the optimistic estimations of ZVS achievement. The method in [24] requires first solving an ideal model to obtain initial states, and then solving $v_{ds}(t) = 0$ to determine ZVS realization, introducing additional steps. Moreover, variations in the operational trajectory can introduce errors in the initial values obtained from the ideal model, thereby adversely affecting the estimation of ZVS realization. The proposed method directly determines the feasibility of ZVS based on the existence of solver solutions, thereby improving computational efficiency

$$I_{off} t_d \geq 2 V_{bus} C_{oss1} \tag{16}$$

$$I_{off} t_d \geq a V_{in} C_{oss1} + b V_o C_{oss2} + (C_{stray} + C_t) V_{in} \tag{17}$$

where $C_{\text{stray}}$ denotes the stray capacitance inherent in the printed circuit board, while coefficients $a$ and $b$ are determined by the converter topology.

## VI. Conclusion

This article presents an optimized design method for *LLC* converters to achieve high-efficiency and full-range ZVS based on the time-domain analysis. By developing a TDM-DC that accounts for dead time and parasitic capacitance, this work introduces a high-precision ZVS condition solver.

The proposed method analyzes key ZVS factors, revealing that current decay during dead time and trajectory changes induced by parasitic capacitance worsen ZVS conditions. The proposed *LLC* converter design method guarantees ZVS realization throughout the complete operating range while maintaining superior computational precision and efficiency. A 3-kW prototype with optimized parameters achieves 97.0% peak efficiency and 95.2% efficiency at rated power, validating the method's effectiveness.

Despite the results of this study, the following limitations remain.

1) For GaN devices with lower $C_{oss}$, current changes during dead time are less important, making TDM-DC less significant.
2) In *LLC* converters above 1 MHz, printed circuit board (PCB) and transformer parasitic inductance increasingly affect model accuracy.
3) For soft-saturation inductors, large inductance variation with current limits the method's applicability.
4) TDM-DC applies only to pulse frequency modulation.

In summary, the proposed approach presents new solutions for efficient *LLC* converter design and ZVS implementation, with both theoretical significance and engineering value.

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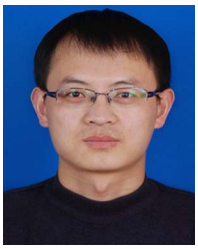

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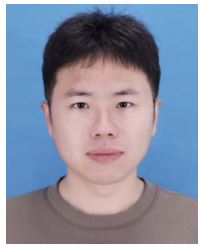

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