The Harmonically Partitioned Power Converter Architecture: Single-Stage Single-Phase ac/dc Power Conversion Using Bidirectional Switches

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***Abstract*—This article proposes a novel single-stage single-phase ac/dc power conversion architecture called a harmonically partitioned power converter (HPPC). The HPPC leverages bidirectional switches (BDSs) to directly modulate the ac line voltage and enforces a harmonically partitioned loading network, resulting in automatic unity power factor, complete power pulsation decoupling, continuous gain variation, and galvanic isolation within a single conversion stage. This architecture provides a substantial opportunity for miniaturization and performance advances to all single-phase ac/dc power converters with power factor requirements on the ac port. The HPPC enables miniaturization by relegating all magnetic components to a high frequency ac tank and by operating the buffer capacitor at a port with no dc voltage regulation requirements. Further, the conversion is achieved in a single stage, eliminating the efficiency penalty traditionally suffered by single-phase ac/dc converters which achieve these functionalities via individual conversion stages processing the entire power throughput sequentially. The article introduces the principle of operation of the HPPC, derives the high level governing equations of the architecture, and presents design equations for a simple "single-branch" implementation of the general architecture. An experimental prototype utilizing anti-series connected GaN HEMTs to emulate monolithic BDS devices is presented and validates the operating principles and modeling for a single-branch implementation with the following specifications: $\mathbf{V_{in} = 120\,V_{rms}}$, $\mathbf{f_g = 60\,Hz}$, $\mathbf{V_o = 250\,V_{dc}}$, $\mathbf{P_o = 250\,W}$, and $\mathbf{f_{HF} = 210\,kHz}$.**

***Index Terms*—Monolithic bidirectional switch (MBDS), power pulsation decoupling, single-phase ac/dc power converters, single-stage power conversion.**

I. Introduction

SINGLE-PHASE ac/dc power electronic converters with power factor requirements (e.g., via IEC61000-3-2 current emission standards [1]) are ubiquitous in the modern electrical landscape. Fig. 1 illustrates a block diagram overview for a typical single-phase ac/dc power converter employed today. This converter contains the following.

1) A diode bridge to rectify the input ac line voltage.
2) An EMI filter used to prevent high frequency switching content from propagating into the ac port.
3) A front-end power factor correction (PFC) converter, which regulates the input current to be sinusoidal and in-phase with the ac input voltage (for unity power factor).
4) A dc link energy buffer capacitor, which decouples the front-end converter and the isolated dc/dc converter. The front-end converter, typically a boost converter, regulates this voltage around some nominal value. This buffer sinks the instantaneous second line-frequency harmonic power being pulled from the input source (e.g., by sinking a line-harmonic current) and is sized to minimize voltage ripple and be nominally dc.
5) An isolated dc/dc converter which regulates the dc output voltage and provides requisite galvanic isolation.

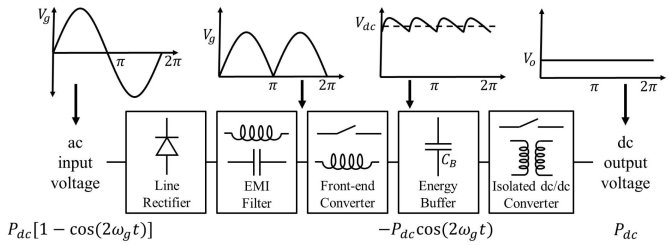

Fig. 1. Block diagram overview of a typical single-phase ac/dc power converter illustrating standard voltage and power progressions for unity power factor operation.

There are two fundamental issues which limit the performance and miniaturization of these converters today.

1) Multiple power conversion stages are necessary to achieve the required input PFC, output voltage regulation, and system isolation.

Since each of the conversion stages process the entire power throughput sequentially, the efficiency of the converter is multiplicative and incurs a substantial penalty. This often inhibits very high overall conversion efficiencies [2]. For example, if the diode rectifier, front-end converter, and dc/dc converter have extremely high efficiencies of $\eta_{rect} = 99.5\%$, $\eta_{pfc} = \eta_{dc} = 98.5\%$, respectively, the overall conversion efficiency is $\eta = \eta_{rect}\eta_{pfc}\eta_{dc} \approx 96.5\%$. There are many PFC converters in use today [3] and it has become commonplace to employ "bridgeless" PFCs, which combine the diode rectifier and PFC converter into a single stage [4]. Here, the inductor is placed on the ac side

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of the bridge and two rectifier devices are typically replaced with controllable switches (e.g., MOSFETs). This integration enables fewer switching devices to be used which can improve efficiency and cost, but still incurs the multiplicative efficiency penalty associated with the dc/dc conversion stage, which is not integrated into the bridgeless PFC. While single-stage single-phase switched-mode ac/dc converters have gained significant interest in recent decades [5], [6], [7] (see Sections III-B and III-C for a more comprehensive discussion), these solutions generally require complex control and increased device stresses while still imposing constraints on energy buffer miniaturization.

2) The energy buffer capacitor linking the PFC and isolated dc/dc converter stages is oversized owing to the conflicting requirements of buffering twice-line harmonic power and minimizing the voltage ripple experienced by the dc/dc stage.

For an ac/dc converter operating with unity power factor at the ac port, the instantaneous power flow is

$$p_{\text{ac}}(t) = v_{\text{ac}}(t) \cdot i_{\text{ac}}(t) = P_{dc}[1 - \cos(2\omega_g t)] \tag{1}$$

where $P_{dc} = V_g^2/2R_{ac}$, V_g is the amplitude of the sinusoidal voltage, R_{ac} is the effective resistance loading the ac port, and $\omega_g = 2\pi f_g$ is the ac angular frequency. Thus, dc and second line-harmonic power is drawn. The peak swing in second line-harmonic stored energy E_{C_B} is found by integrating (1) as $E_{C_B} = P_{dc}/\omega_g$, where the subscript denotes the assumption of a capacitor C_B buffering this time-varying power component. The capacitor C_B is also tasked with maintaining a nominally dc voltage to avoid over-stressing and to ensure high efficiency in the following dc/dc conversion stage [8]. As a first-order approximation, the required buffer capacitance to meet an allowable ripple ratio on the dc link $\mathcal{R} = v_{pk}/V_{dc}$ [4] is

$$C_B \approx \frac{2P_{dc}}{\mathcal{R}\omega_g V_{dc}^2} = \frac{2E_{C_B,\text{ripple}}}{V_{dc}^2} \tag{2}$$

where V_{dc} is the nominal dc bus voltage and $E_{C_B,\text{ripple}}$ is the peak energy stored by this capacitor which is sized for the ripple requirement. Note that this value is $1/\mathcal{R}$ times larger than the energy buffering requirement E_{C_B}, where $\mathcal{R} \ll 1$. Thus, the dc link capacitor is massively oversized to meet the voltage ripple requirement compared to what is needed to achieve unity power factor (which we call its "true minimum" energy storage requirement). For example, assuming a standard bus voltage of $V_{dc} = 400\,V$, and for the operating specifications experimentally validated in this article, $P_{dc} = 250\,W$, $\mathcal{R} = 5.67\%$, $\omega_g = 2\pi \cdot 60$, the minimum capacitance to meet the ripple requirement would be $C_B = 146.2\mu$F. A substantial opportunity for miniaturization of this capacitor is to move it to a port with no dc voltage regulation requirements [9], where for the same specifications and $\mathcal{R} = 100\%$ the required buffer capacitance is $C_B = 46\mu$F.

There has been a considerable amount of work in the literature to miniaturize the buffer capacitor through power pulsation decoupling [10], [11], [12]. Active energy buffers (AEB) [13], [14], [15], [16], [17], [18] reduce buffer capacitance by separating the energy storage and voltage regulation functions through placement of the capacitor at a port which can sustain wider voltage swings (i.e., increasing the allowable ripple ratio $\mathcal{R}$). The reduction in buffer capacitance for these solutions typically comes with an increase in component voltage stress, complexity, or a net efficiency penalty. The stacked switched capacitor (SSC) buffer [19], [20], [21], a type of AEB, has shown impressive power density but suffers from discrete gain operation and the requirement of a large number of capacitors and switches whose auxiliary circuitry can undermine the goal of miniaturization. Another interesting method to reduce the size of the energy buffer capacitor is the harmonic injection technique, which purposely draws line harmonic currents and reduces the power factor [22], [23], [24]. This decreases the required twice-line frequency energy buffering but is fundamentally limited by the allowable input current harmonics specified by, e.g., IEC61000-3-2. Research and development has largely revolved around the general conversion architecture shown in Fig. 1, where multiple conversion stages are necessary and the energy buffer capacitor performs some degree of voltage regulation. An ideal architecture for miniaturization of these converters while maintaining high efficiencies would instead be a single-stage power converter which fully decouples the energy buffer capacitor from any port with dc voltage regulation requirements and which can achieve unity power factor, galvanic isolation, and dc voltage conversion within this single conversion stage.

This work proposes a novel single-stage power conversion architecture, called a harmonically partitioned power converter (HPPC), which overcomes the bottlenecks to miniaturization described in this section. The proposed architecture fully leverages emerging (and soon to be commercially available) monolithic wide bandgap bidirectional switches (BDSs). These devices are four-quadrant switches: they block bipolar voltage when OFF and can sustain bidirectional current when ON. Their monolithic integration in GaN enables for the first time a means of implementing BDSs in a fast-switching, scalable, and relatively low-cost form factor [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38]. Our HPPC architecture leverages this capability to achieve automatic unity power factor, true minimum energy storage buffering, and gain variation with energy exchanged in a high frequency ac tank instead of through a dc link. This removes the requirement for a front-end PFC converter or a dc/dc stage, realizing single-stage power conversion and permitting maximum miniaturization of the energy storage buffer capacitor. Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) of the BDS devices is also achievable in certain realizations of the architecture. This article focuses on a specific implementation of the HPPC, called the "single-branch" implementation, to verify the theory of operation. This is selected due to its relative simplicity and its structural similarity to converters the reader may already be familiar with, such as the LLC converter. The described single-branch implementation requires variable passive components or a variable turns ratio transformer [39], [40], [41], which represents a unique but tractable design challenge for this implementation. However, we emphasize that this need for variable components is not fundamental to the general HPPC architecture itself.

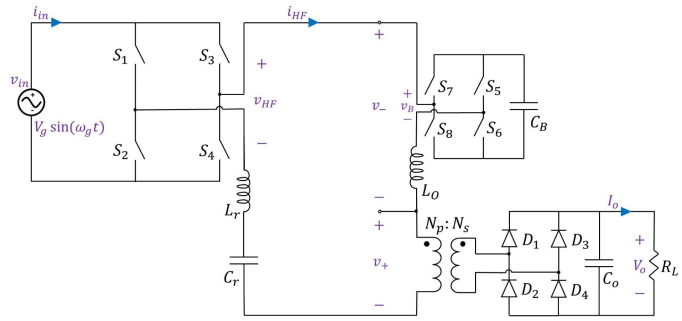

Fig. 2. Single-branch HPPC implementation using a full-bridge BDS inverter, BDS inverter active capacitive energy buffer with inductive cancellation, and a high frequency transformer diode rectifier combination.

The rest of this article is organized as follows. Section II describes in detail a specific "single-branch" implementation of the architecture and is a relatively simple to implement realization that aids in communicating our HPPCs idea but which is also only modestly performing. Section III describes an experimental prototype of this single-branch realization which uses anti-series unipolar GaN HEMTs to realize the BDSs. This prototype validates the operating theory of our architecture and this section also includes a comparison between our work and other single-stage single-phase ac/dc converters proposed in the literature. Section IV introduces the general HPPC architecture, focusing on its high-level governing equations and the general principles of its operation to achieve unity PFC, gain control, isolation, and true-minimum energy buffering. Section V discusses several practical considerations of the HPPC and Section VI covers future improvements and innovations. Finally, Section VII concludes this article.

II. A Single-Branch HPPC Implementation

In this section, we describe one example implementation of the HPPC which has a relatively simple practical realization and is particularly beneficial in conveying the operating characteristics of the architecture. This realization, shown in Fig. 2[1] and referred to as an example of the "single-branch" architecture, demonstrates the salient benefits of automatic unity power factor, true minimum energy storage, continuous gain variation, and galvanic isolation. The primary disadvantage of this implementation is that the BDS devices S_1–S_4 only achieve soft switching throughout half of the line cycle. It will be shown in Section IV that by adding an additional branch in parallel, which we call the "dual-branch" variation, the BDS devices can achieve ZVS throughout the entire line cycle. The sections that follow provide a mathematical derivation of the HPPC design equations, making use of several trigonometric identities which are listed in Table I.

[1]The reader may recognize a similarity between this implementation and the popular LLC or Dual Active Bridge (DAB) converters. This is intentional, building on the popularity and high performance of these topologies, but it is emphasized that this is only one implementation of the single-branch HPPC and of the larger general HPPC architecture described in Section IV.

TABLE I
List of Trigonometric Identities

ID	Trigonometric Identity
#1	$\sin(A)\sin(B) = \frac{1}{2}[\cos(A-B) - \cos(A+B)]$
#2	$\cos(A)\cos(B) = \frac{1}{2}[\cos(A+B) + \cos(A-B)]$
#3	$\cos^2(A) = \frac{1}{2}[1 + \cos(2A)]$
#4	$\cos(A)\sin(B) = \frac{1}{2}[\sin(A+B) - \sin(A-B)]$
#5	$\sin(A - 90°) = -\cos(A)$
#6	$\cos(A - 90°) = \sin(A)$

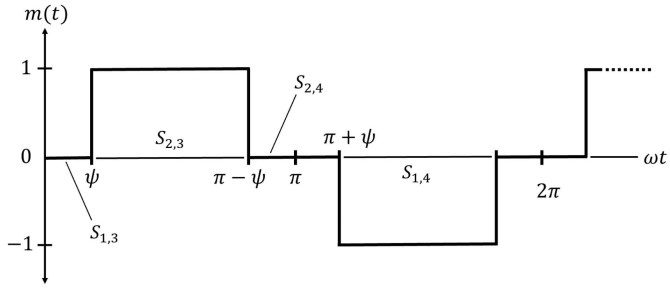

Fig. 3. Square wave modulation command for the main BDS inverter switches S_1–S_4. The angle ψ defines the length of "zero states" where the output of the main BDS inverter is short circuited. This angle is easily implemented by phase shifting two sets of 50% duty cycle complementary gating signals an angle ψ from one another.

A. Square Wave Modulation: The BDS Inverter

The full-bridge configuration of BDS devices S_1–S_4, which will be called the "main" BDS inverter for the remainder of this document, directly interface the ac port and are controlled as shown in Fig. 3. While there are many possibilities for modulating the ac voltage, this particular control sequence describes the familiar square wave modulation [4], where the function $m(t)$ describes the modulation command and is assumed to repeat cyclically at a frequency $\omega_{HF} \gg \omega_g$. The switching sequence shown in Fig. 3 ensures the minimum number of switching transitions per cycle and balanced conduction intervals such that loss is distributed evenly between the devices.

Since the modulation command represents a periodic signal obeying the Dirichlet conditions, it may be described by an equivalent Fourier Series Representation (FSR). Noting that Fig. 3 represents an odd and half-wave symmetric waveform, it may be written in terms of its FSR as

$$m(t) = \sum_{n=\text{odd}}^{\infty} a_n \sin(n\omega_{HF} t) \tag{3}$$

$$a_n = \frac{2}{T_{HF}} \int_0^{T_{HF}} m(t) \sin(n\omega_{HF} t) dt. \tag{4}$$

Solving (3) and (4) for $m(t)$ gives

$$m(t) = \sum_{n=\text{odd}}^{\infty} \frac{4}{n\pi} \cos(n\psi) \sin(n\omega_{HF} t). \tag{5}$$

The main BDS inverter output voltage can then be written as

$$v_{HF}(t) = v_{in}(t) \cdot m(t) = \sum_{n=\text{odd}}^{\infty} \frac{4V_g}{n\pi} \cos(n\psi) \sin(\omega_g t) \sin(n\omega_{HF} t). \quad (6)$$

Using ID #1 from Table I gives

$$v_{HF}(t) = \sum_{n=\text{odd}}^{\infty} \frac{2V_g}{n\pi} \cos(n\psi) \times [\cos((n\omega_{HF} - \omega_g)t) - \cos((n\omega_{HF} + \omega_g)t)]. \quad (7)$$

Equation (7) is representative of the familiar result found in AM radio [42], where the modulation (multiplication) of a low frequency "message" signal and a high frequency "carrier" signal results in sideband harmonic generation around the high frequency carrier. For the square wave modulation considered, there exists an infinite set of carrier signals which correspond to the harmonic content of the ω_{HF} square wave shown in Fig. 3 (odd nth harmonics of $1/n$ type descending amplitude). It is this harmonic content that generates the infinite set of sideband harmonics described by the summation in (7). If L_r and C_r are designed to resonate at the fundamental carrier frequency ω_{HF} with a high quality factor, the Fundamental Harmonic Approximation (FHA) may be employed ($n = 1$) such that the main BDS inverter output can be approximated as

$$v_{HF}(t) \approx \frac{2V_g}{\pi} \cos(\psi)[\cos((\omega_{HF} - \omega_g)t) - \cos((\omega_{HF} + \omega_g)t)]. \quad (8)$$

The BDS inverter can therefore be thought of as having inserted two voltage components to the rest of the system

$$v_-(t) = \frac{2V_g}{\pi} \cos(\psi) \cos((\omega_{HF} - \omega_g)t) \quad (9)$$

$$v_+(t) = -\frac{2V_g}{\pi} \cos(\psi) \cos((\omega_{HF} + \omega_g)t) \quad (10)$$

where the $-$ and $+$ subscripts denote the negative and positive sideband, respectively. For the remainder of this analysis the individual sideband harmonics will be treated separately.

The amplitude of the sideband harmonics is directly proportional to the fundamental amplitude of the modulation command $m(t)$, which is often denoted as M, and is seen from (5) to be

$$M(\psi) = \frac{4}{\pi} \cos(\psi). \quad (11)$$

The zero state angle ψ is observed to be a control variable enabling gain variation of the generated sideband harmonic amplitudes. It will be shown in Section II-E that this gain variability is one means of controlling the dc output voltage.

B. Instantaneous Power Flow

The main BDS inverter and resonant bandpass filter combine to insert a single pair of sideband harmonic voltages centered around the switching frequency ω_{HF}. As shown in Fig. 2, these voltage harmonics are to be partitioned such that v_- is dropped across a load consisting of the output of an additional BDS inverter in series with an inductor L_O and v_+ is to be dropped across the primary terminals of the $N_p : N_s$ transformer. For reasons that will be explained shortly, the loads maintaining v_- and v_+ are called the "orthogonal" and "direct" loads, respectively. Momentarily neglecting how the voltages v_- and v_+ are physically regulated, it is instructive to mathematically demonstrate how this system completely partitions dc and $2\omega_g$ instantaneous power flow while drawing current that enables unity power factor operation (e.g., 60 Hz plus higher frequency switching harmonics).

It is first assumed that only resistively loaded positive sideband harmonic current flows in the tank, or $i_{HF} = i_+ = v_+/R_e$, where the resistance R_e is to be defined shortly. This current flow can be shown to respect the conditions for unity power factor operation mentioned above. Referring to the sideband harmonic voltages (9) and (10), the instantaneous power flow at the orthogonal load can be written as

$$p_o(t) = v_-(t) \cdot i_+(t) = \frac{v_-(t) \cdot v_+(t)}{R_e} = -\frac{4V_g^2}{\pi^2 R_e} \cos^2(\psi) \cos((\omega_{HF} - \omega_g)t) \cos((\omega_{HF} + \omega_g)t). \quad (12)$$

Using ID #2 from Table I, (12) results in

$$p_o(t) = -\frac{2V_g^2}{\pi^2 R_e} \cos^2(\psi)[\cos(2\omega_g t) + \cos(2\omega_{HF} t)] \quad (13)$$

Similarly, the instantaneous power flow at the direct load can be written as

$$p_d(t) = v_+(t) \cdot i_+(t) = \frac{4V_g^2}{\pi^2 R_e} \cos^2(\psi) \cos^2((\omega_{HF} + \omega_g)t). \quad (14)$$

Using ID #3 from Table I, (14) results in

$$p_d(t) = \frac{2V_g^2}{\pi^2 R_e} \cos^2(\psi)[1 + \cos(2(\omega_{HF} + \omega_g)t)]. \quad (15)$$

Equation (13) shows that the orthogonal load processes only $2\omega_g$ and $2\omega_{HF}$ power, while (15) shows that the direct load processes only dc and $2(\omega_{HF} + \omega_g)$ power. While both loads process an unwanted high frequency power component, these harmonics can be easily accommodated by the EMI filter and relatively small output filter capacitors. The main takeaway from the above derivation is that there is complete partitioning of the dc and $2\omega_g$ power in the system. Therefore, the buffer capacitor C_B operating at the orthogonal load port may have no dc voltage regulation requirement and true minimum energy storage sizing while still respecting conditions for unity power factor operation and low dc output voltage ripple.

The specific power partitioning which occurs is clearly dependent upon which sideband harmonics are interacting at the port of interest. For example, it is seen that when the negative and positive sidebands interact, the power flow at that port is $2\omega_g$ plus higher order harmonics. Similarly, when the sidebands of interaction at the port are both positive, the power flow at the port will be dc plus higher order harmonics. The controlled mixing of sideband harmonics allows full power partitioning in the

converter and it is in this spirit that the names "orthogonal" and "direct" have been chosen for the harmonically partitioned loads. The "orthogonal" load represents the non-dc-power-processing element, and is called this to reflect that it inserts a voltage at a different frequency from that of the current in the branch (e.g., in Fig. 2, v_- and i_+ have different frequencies). The "direct" load represents the dc-power-processing element, and is called this to reflect that it inserts a voltage at the same frequency as the current in the branch (e.g., in Fig. 2, v_+ and i_+ have the same frequency).

C. Direct Load Implementation

The direct load shown in Fig. 2 consists of an $N_p : N_s$ transformer connected through a full-bridge diode rectifier to a load R_L in parallel with a filter capacitor[2] C_o. As in a conventional LLC with a full-bridge rectifier connected to the secondary of an $N_p : N_s$ transformer operating with a sinusoidal input current and a dc output voltage, the load resistance R_L can be mapped to the primary side of the transformer as an effective resistance [43] as

$$R_e = \frac{8}{\pi^2}\left(\frac{N_p}{N_s}\right)^2 R_L. \tag{16}$$

If the orthogonal load properly maintains a voltage $v_-(t)$, then by Kirchhoff's Voltage Law (KVL) the voltage across the direct load must be $v_+(t)$. By Ohm's Law, the current through the branch must then be $i_{HF}(t) = v_+(t)/R_e$. With these conditions satisfied, the power flow will respect that described in Section II-B. The fundamental design goal for this implementation is therefore to ensure that the orthogonal load maintains the desired voltage $v_-(t)$.

D. Orthogonal Load Implementation

For the particular implementation of the single-branch architecture described in this article, the orthogonal load is designed to maintain a voltage of $v_-(t)$. The orthogonal load as shown in Fig. 2 comprises a "buffer" capacitor C_B placed behind an additional BDS full-bridge inverter and a series "orthogonal" inductor L_O. As will be discussed in more detail, the capacitor and inductor are so named because their exclusive functionalities are to buffer the twice-line frequency power mismatch and to cancel an orthogonal voltage component inserted by the buffer BDS inverter. For the remainder of this document, the BDS full-bridge inverter associated with the orthogonal load will be called the "buffer" BDS inverter.

1) Terminal Relationships for $2\omega_g$ Buffering: It is necessary to find terminal behavior which allows the buffer capacitor to instantaneously process only the entire $2\omega_g$ power mismatch between the ac and dc ports. Consider that the buffer capacitor maintains the following voltage across its terminals:

$$v_{C_B}(t) = V_A \sin(\omega_g t + \alpha) \tag{17}$$

[2]It is important to note that because the twice-line frequency power will be entirely processed by the orthogonal load, the output capacitor C_o is implemented with the sole intention of filtering high frequency switching content from propagating into the dc port. As this capacitor does not partake in any $2\omega_g$ power buffering its size can be very small.

where V_A and α are the amplitude and phase of the capacitor voltage, respectively. These values are considered arbitrary and the phase α is referenced to that of the input voltage, which is taken to be 0°. From the constitutive relationship for a linear capacitor $i = C \cdot dv/dt$, the instantaneous power processed by the buffer capacitor is found as

$$p_{C_B}(t) = v_{C_B}(t) \cdot i_{C_B}(t) = v_{C_B}(t) \cdot C_B \frac{dv_{C_B}(t)}{dt}. \tag{18}$$

Integrating (17) and plugging the result into (18) gives

$$p_{C_B}(t) = \omega_g C_B V_A^2 \sin(\omega_g t + \alpha)\cos(\omega_g t + \alpha). \tag{19}$$

Using ID #4 from Table I, choosing $\alpha = -45°$, and using ID #5 from Table I, (19) reduces to

$$p_{C_B}(t) = -\frac{\omega_g C_B V_A^2}{2}\cos(2\omega_g t). \tag{20}$$

Comparing this expression to that of (1), it is seen that the buffer capacitor will process the correct $2\omega_g$ power during unity power factor operation if the following relationship holds

$$\frac{\omega_g C_B V_A^2}{2} = P_{dc}. \tag{21}$$

Therefore, once the amplitude of the capacitor voltage V_A is defined, the requisite buffer capacitance C_B to adequately process the $2\omega_g$ power mismatch can be found in terms of the desired dc output power P_{dc} and input frequency ω_g from (21).

2) Buffer BDS Inverter: Assuming that the voltage profile of (17) is maintained with V_A still arbitrary and $\alpha = -45°$, a modulation strategy that results in the voltage at the buffer inverter output being $v_-(t)$ is desired. It is chosen to operate the inverter with the following square wave modulation command, where the higher order harmonics are ignored under the FHA:

$$m_B(t) \approx \frac{4}{\pi}\cos(\psi_B)\sin(\omega_{HF} t + \rho). \tag{22}$$

This is achieved by operating the buffer BDS inverter in a manner exactly homologous to the main BDS inverter in Fig. 3 but with an independent zero state angle ψ_B and phase shifted by an angle ρ. The angle ρ is referenced to the main BDS inverter modulation command $m(t)$, which is chosen to have a phase of 0°. For simplicity, it will be assumed that $\psi_B = \psi$ for the remainder of this document. Following an analogous derivation as was given for the main BDS inverter in Section II-A, choosing $\rho = -45°$, and using ID #6 from Table I, the voltage produced by the buffer BDS inverter will be

$$v_B(t) = \frac{2V_A}{\pi}\cos(\psi)[\cos((\omega_{HF} - \omega_g)t) - \sin((\omega_{HF} + \omega_g)t)]. \tag{23}$$

The two sidebands generated in (23) can again be treated separately and decomposed as

$$v_{B-}(t) = \frac{2V_A}{\pi}\cos(\psi)\cos((\omega_{HF} - \omega_g)t) \tag{24}$$

$$v_{B+}(t) = -\frac{2V_A}{\pi}\cos(\psi)\sin((\omega_{HF} + \omega_g)t). \tag{25}$$

Choosing $V_A = V_g$, it is seen that (24) is the desired voltage $v_-(t)$ while (25) is a parasitic orthogonal term. If the orthogonal

voltage $v_{B+}(t)$ can be "canceled," the orthogonal load will successfully maintain $v_{-}(t)$.

3) Orthogonal Cancellation Element: The orthogonal voltage of (25) can be canceled by appropriate sizing of the orthogonal inductor L_O. Considering the current flow $i_{+}(t)$ in the branch and using the constitutive relationship for linear inductors $v = L \cdot di/dt$, the voltage across the inductor can be found as

$$\begin{aligned} v_{L_O}(t) &= L_O \cdot \frac{di_{+}(t)}{dt} \\ &= L_O \cdot \frac{d}{dt}\left[-\frac{2V_g}{\pi R_e}\cos(\psi)\cos((\omega_{HF}+\omega_g)t)\right] \\ &= \frac{2V_g L_O}{\pi R_e}\cos(\psi)(\omega_{HF}+\omega_g)\sin((\omega_{HF}+\omega_g)t). \end{aligned} \tag{26}$$

Comparing (26) to the parasitic orthogonal term of (25), it is seen that the orthogonal inductor voltage will provide the correct cancellation if the following relationship is maintained:

$$\frac{2V_g L_O}{\pi R_e}\cos(\psi)(\omega_{HF}+\omega_g) = \frac{2V_g}{\pi}\cos(\psi). \tag{27}$$

Solving for L_O gives

$$L_O = \frac{R_e}{(\omega_{HF}+\omega_g)}. \tag{28}$$

It is interesting to note that this analysis very closely mimics the underlying goal of single sideband (SSB) suppression in communication systems, where a dual sideband amplitude modulated signal is generated and one sideband is suppressed such that only a single sideband is transmitted [42].

4) Buffer Sizing: The twice-line frequency power buffering requirement of the buffer capacitor C_B is from (13)

$$p_{C_B}(t) = -\frac{2V_g^2}{\pi^2 R_e}\cos^2(\psi)\cos(2\omega_g t). \tag{29}$$

Comparing this to (20) and recalling that the buffer capacitor voltage amplitude must be $V_A = V_g$ for proper voltage insertion, the following relationship must be maintained to buffer the correct twice-line frequency power:

$$\frac{2V_g^2}{\pi^2 R_e}\cos^2(\psi) = \frac{\omega_g C_B V_g^2}{2}. \tag{30}$$

This provides a sizing requirement on the buffer capacitor of

$$C_B = \frac{4}{\pi^2 R_e \omega_g}\cos^2(\psi). \tag{31}$$

By sizing the buffer capacitor as in (31), the orthogonal inductor as in (28), and modulating the buffer inverter switches as described in Section II-D2, the system will result in full power pulsation decoupling with unity power factor.

E. Gain Variation

The dc output voltage V_o is a result of full-wave rectification of the transformer secondary. Therefore the voltage at the transformer secondary will be a 50% duty cycle square wave varying between $+V_o$ and $-V_o$ at a frequency $\omega_{HF}+\omega_g$. The voltage on the primary of the transformer is then the same shape with peak values of $n_t \cdot V_o$ where $n_t = N_p/N_s$ is the transformer turns ratio. The amplitude of the fundamental component of the square wave voltage at the primary can be found as

$$v_{p,1} = \frac{4}{\pi}V_p = \frac{4}{\pi}\left(\frac{N_p}{N_s}\right)V_o. \tag{32}$$

Recalling that the voltage $v_{+}(t)$ is the fundamental amplitude of a square wave voltage under the FHA, the value in (32) can be related to the amplitude of $v_{+}(t)$ in (10) as

$$\frac{4}{\pi}\left(\frac{N_p}{N_s}\right)V_o = \frac{2V_g}{\pi}\cos(\psi). \tag{33}$$

Solving for V_o yields

$$V_o = \frac{V_g}{2n_t}\cos(\psi). \tag{34}$$

The turns ratio n_t is a design parameter and is assumed to be constant while the ac voltage amplitude V_g is assumed to be a fixed value set by the ac port (e.g., the grid[3]). It is clear from (34) that the dc output voltage can be varied using the control variable ψ. In other words, by altering the length of the zero states in Fig. 3, the dc voltage can be controlled over a continuous range. This gain variability completes the single-branch architecture's realization of the four foundational characteristics of an ideal single-phase ac/dc conversion architecture with power factor requirements: 1) single-stage power conversion, 2) complete power pulsation decoupling, 3) continuous gain variation, and 4) galvanic isolation.

III. Experimental Verification

This section describes and demonstrates a 120 V_{rms} /60 Hz in, 250 V dc out, 250 W hardware prototype implemented to provide experimental evidence of the operating theory described in Section II. The prototype is shown in Fig. 4. The BDS inverters are designed as standalone boards and interconnected with a breakoff board containing the branch passives and direct load. This modularity allows flexibility in future testing of additional modulation strategies and multibranch topologies (to be discussed in Section IV). It is noted that this experimental prototype was not optimized to display state-of-the-art performance but is intended to provide the first experimental demonstration of the novel concepts described herein. Optimization and exhibition of the performance and miniaturization benefits enabled by this architecture will be the focus of a future work. The hardware prototype is designed to modulate a $f_g = 60$ Hz grid frequency voltage at $f_{HF} = 3500 \cdot f_g = 210$ kHz . To implement the BDS devices, two GaN HEMTs are connected in an anti-series configuration and are driven in unison. The source terminals of the devices are tied together such that they are driven from a single gating signal and driver IC. A readily available 12V computer

[3]While this paper considers the case of power flow from the grid to a dc load, the HPPC is in general an architecture with bidirectional power flow capability. For example, if the diode rectifier in Fig. 2 is instead implemented using synchronous rectifiers, the converter may deliver power to the grid from the dc port. The voltage conversion ratio in (34) can then be used to regulate the sinusoidal ac voltage amplitude V_g.

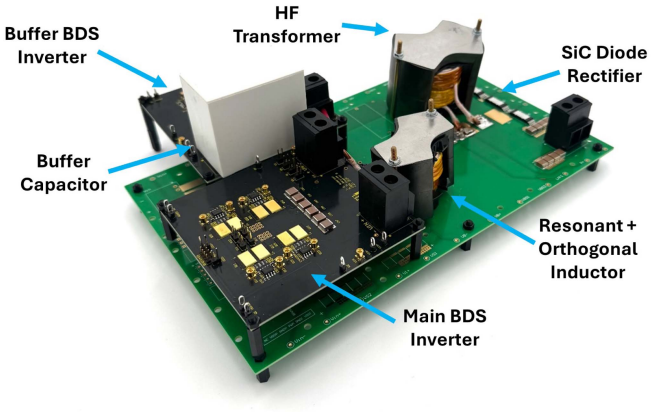

Fig. 4. Labeled single-branch experimental prototype. The resonant and orthogonal inductors are integrated into a single magnetic component and resonant capacitors are under the breakoff board.

TABLE II
HARDWARE COMPONENTS AND EQUIPMENT

Active Devices		
Item	**Manufacturer**	**Part Number**
GaN HEMT	GaN Systems	GS66516T
Gate Driver IC	Infineon	1EDB7275F
Isolated Power	Analog Devices	ADUM5010
SiC Schottky Diode	Infineon	IDDD08G65C6

Passive Components		
Item	**Value**	**Material/Technology**
Resonant Inductor L_r †	51.2μH	3C94
Resonant Capacitor C_r	11.02nF	Ceramic, C0G
Buffer Capacitor C_B ‡	46.0μF	Film
Orthogonal Inductor L_O †	17.65μH	3C94
Transformer Turns Ratio n_t *	1/3	3C94
Output Capacitor C_o	12μF	Ceramic, X7R
Load Resistor R_L	258Ω	Power Resistor

Test and Measurement		
Item	**Manufacturer**	**Part Number**
Digital Oscilloscope	Tektronix	MSO56B
Input Voltage Probe	Tektronix	THDP0200
Buffer Capacitor Voltage Probe	Tektronix	THDP0200
BDS Inverter Voltage Probe	Tektronix	TIVP1L
Output Voltage Probe	Tektronix	THDP0200
Input Current Probe	Tektronix	TCP0020
Resonant Current Probe	Tektronix	TCP003A

† Integrated into single magnetic component using 15 turns 435/#40 Litz wire on PM50/39 Ferroxcube 3C94 core.
‡ PNs C4ATFBW5400A3NJ (40μF); EZPQ33405LTA (4μF); C4ATFBU4200A3BJ (2μF).
* 5 primary, 15 secondary turns 435/#40 Litz wire on PM62/49 Ferroxcube 3C94 core.

fan is employed to force room temperature air over the GaN devices for cooling purposes. Table II provides relevant values and part numbers for the components and equipment utilized in the experimental prototype of Fig. 4.

A. Prototype Results

The low frequency operating waveforms from the experimental prototype are shown in Fig. 5[4] for $\psi = 0$ open loop operation

[4]The waveforms presented in Figs. 5 and 6 were collected directly from the oscilloscope, with enhanced axis labels added to improve readability. Complete oscilloscope screen captures are available in the supplementary material accompanying this manuscript.

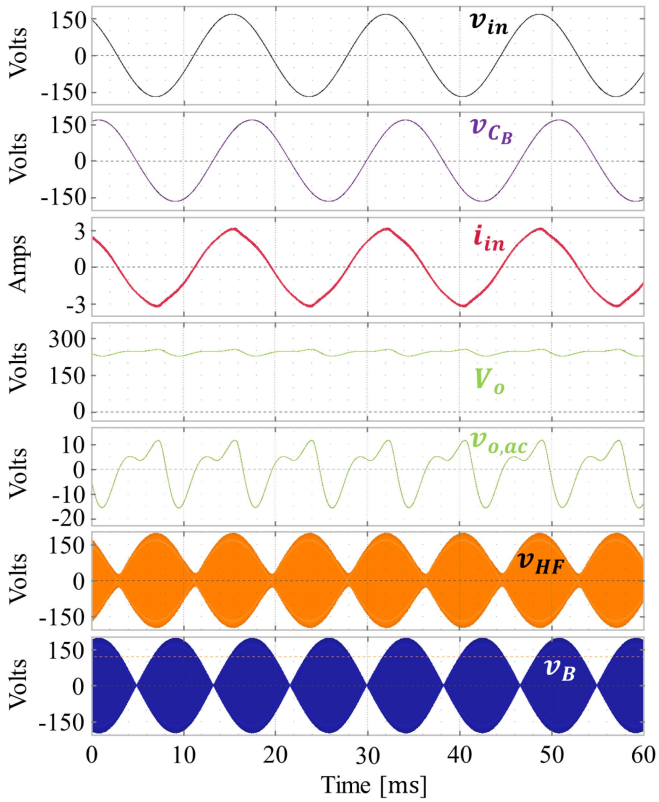

Fig. 5. Experimentally measured low frequency waveforms for $v_{in} = 120.2\,\mathrm{V}_{rms}$, $f_g = 60\,\mathrm{Hz}$, $P_{in} = 251.7\,\mathrm{W}$, $f_{HF} = 209.86\,\mathrm{kHz}$.

as described in Section II. The input current demonstrates the inherent unity power factor regulation of this converter: current is nearly perfectly in phase with the input voltage. The power factor at any port can be determined as the product of a distortion factor K_D, which indicates harmonic content in the current waveform and a displacement factor K_ϕ which indicates the relative phase shift between the voltage and current waveforms. The distortion factor associated with switching frequency harmonic currents would be mitigated by an EMI filter, but the displacement factor is what is regulated by a conventional PFC stage in the traditional ac/dc architecture of Fig. 1. The phase shift between the input voltage and current is observed to be 1.78°, which results in a displacement factor of $K_\phi = \cos(1.78°) = 0.9995$. Thus, automatic unity power factor capability of the architecture is clearly demonstrated. The buffer capacitor voltage is observed to be a 45.92° phase shifted version of the ac input, a condition for processing nearly all $2\omega_g$ instantaneous power in the system.

Fig. 5 displays the output voltage V_o and its corresponding ac component $v_{o,ac}$. This waveform has a $2\omega_g$ peak-to-average ripple ratio of $\mathcal{R} = 5.67\%$. The ideal value is $\mathcal{R} = 0$, corresponding to perfect absorption of the second-line harmonic power by the orthogonal load. This relatively low variation from the expected result is largely attributable to imperfect bandpass filtering of the resonant tank. A two-branch implementation of the HPPC represents an attractive means of reducing the dc output voltage ripple through its enablement of increased tank frequencies and thus relaxed filtering requirements, and this is discussed in Section IV. The waveforms of v_{HF} and

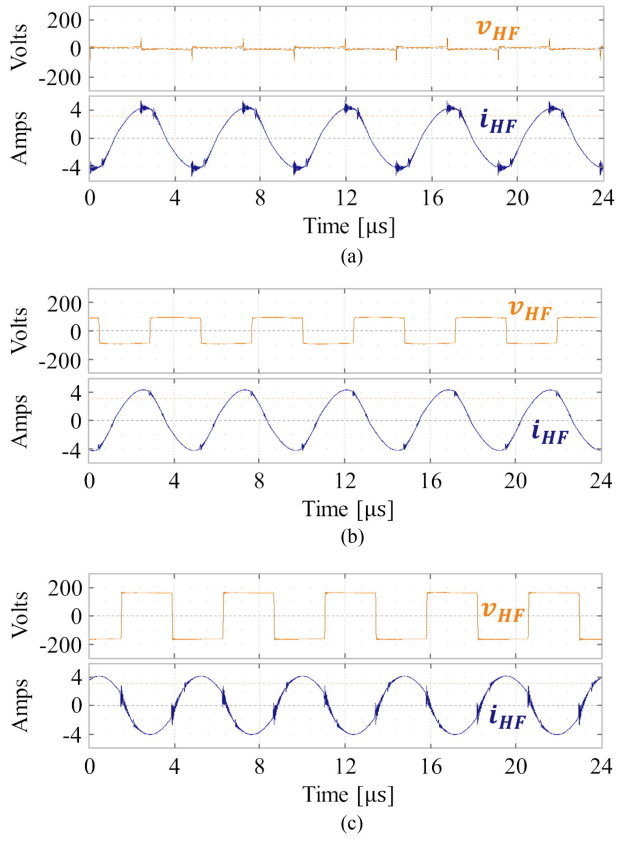

Fig. 6. Experimentally measured high frequency waveforms for $v_{in} = 120.2\,\mathrm{V}_{rms}$, $f_g = 60\,\mathrm{Hz}$, $P_{in} = 251.7\,\mathrm{W}$, $f_{HF} = 209.86\,\mathrm{kHz}$. The waveforms show a progression through the line cycle at angles (a) $\omega_g t \approx 3°$, (b) $\omega_g t \approx 35°$, and (c) $\omega_g t \approx 90°$.

v_B show the familiar beat frequency voltage profiles associated with the outputs of the BDS inverters and their corresponding low frequency envelopes. Fig. 6 illustrates the output voltage of the main BDS inverter v_{HF} and the tank current i_{HF} on a switching frequency time scale. The main BDS inverter output voltage is observed to be a high frequency square wave whose amplitude tracks the envelope of the grid while the tank current is approximately a pure tone of constant amplitude. It is seen that the phase of i_{HF} changes with respect to v_{HF} over the line cycle as a result of their slightly differing frequency content. This results in expected and quantifiable hard switching during some parts of the cycle [see Fig. 6(a)] and soft switching during others [see Fig. 6(b) and 6(c)], and is further addressed in Section IV-C.

A quantitative comparison between the model of Section II and experimental measurements is provided in Table III along with an estimate of the losses in the system. It is of note that over half of the losses are estimated to be a result of HEMT switching and conduction losses. The most compelling pathway to high efficiency for the HPPC is to employ a two-branch architecture owing to its ability to achieve ZVS throughout the entire line cycle. In addition, the availability of monolithic BDSs will aid in improving the figure of merit of these devices compared to their implementation as discrete anti-series connected devices. Recalling the buffer capacitance calculated in (2) for the same ripple ratio, this prototype demonstrates an approximately

TABLE III
COMPARISON OF MODEL PREDICTED AND EXPERIMENTALLY OBSERVED VALUES

Parameter	Model	Experiment	Percent Error
Input Power P_{in}	$250W$	$251.7W$	+0.68%
Output Voltage V_o	$254.6V_{\text{dc}}$	$241.8V_{\text{dc}}$	-5.03%
Buffer Capacitor Voltage v_{C_B}	$120V_{\text{rms}}$	$118.2V_{\text{rms}}$	-1.50%
Buffer Capacitor Phase α	45°	45.92°	+2.04%
Displacement Factor K_ϕ	1.0	0.9995	-0.05%
Efficiency η	91.3%	91.7%	+0.44%
Loss Estimate (Model Only):			
Branch Inductors†	4.7 W		
HF Transformer†	3.1 W		
SiC Diode Rectifier	2.6 W		
HEMT Switching	7.3 W		
HEMT Conduction‡	4.0 W		

† Assuming ac resistance factor $F_R = 2$.
‡ Using 1.5x multiplier for dynamic R_{dson}.

68.5% reduction in required bulk capacitance as compared to a conventional energy buffer which must perform dc voltage regulation. Further, a dc link film capacitor of 140μF with a voltage rating of $550\,V_{dc}$ has a typical box volume of about $142.3\,\mathrm{cm}^3$ [44]. In contrast, a 45μF film capacitor with a voltage rating of $250\,V_{ac}$ has a typical box volume of about $67.3\,\mathrm{cm}^3$ [45], representing a 2x reduction in capacitor physical volume for the same system specifications. Methods for decreasing the required capacitance further are possible through independent control of the buffer BDS inverter zero state angle ψ_B and will be the focus of a future work.

B. Comparison to Current Art

While it is difficult to directly compare single-phase ac/dc power converters without considering a comprehensive set of design details (e.g., port specifications, passive/active voltage and current stresses, control complexity), Table IV provides a high-level comparison between this and other single-stage single-phase ac/dc converters proposed in the literature. It is seen that the efficiency of the non-optimized experimental prototype presented in this work is comparable to current art. As the volume of a capacitor is dependent upon its capacitance and rated voltage, we have included an evaluation of the bulk capacitive energy storage requirement normalized to the rated power throughput of the converter. This metric is aimed at being a design-agnostic comparison of the buffer miniaturization potential of a single-phase ac/dc power converter. The required capacitive energy storage per unit power in this paper is found to be 2.4x less than the next lowest work in Table IV and 15.4x lower than the median, highlighting the benefit of true minimum energy storage sizing achieved in this work.

C. Distinguishing From Similar Topologies

A class of single-stage[5] single-phase ac/dc converters based on the DAB has found widespread interest in recent years

[5]While some authors refer to these converters as "quasi-single-stage" due to the front-end ac bridge (cycloconverter), we consider this as belonging to the single-stage in the same manner that a dc bridge is encapsulated in the single conversion stage of, e.g., an LLC converter.

TABLE IV
COMPARISON OF THE PROPOSED SINGLE-STAGE, SINGLE-PHASE ac/dc CONVERTER WITH PRIOR WORK

Proposed Work	ac Voltage (V_{rms})	dc Voltage (V_{dc})	Rated Power (W)	Efficiency[†]	Normalized Capacitive Energy Storage (mJ Installed/W Rated)	No. of Semiconductors	Switching Frequency (kHz)
[46]	90–265	55	150	81.5%	133.13	13	50
[47]	85–265	48	1000	84.5%	–	14	50
[48]	216–264	25–40	100	95.3%	20.37	10	100-500
[49]	207–253	370–470	3700	96.0%	238.85	12	75-150
[50]	85–265	150	100	91.5%	15.53	12	156
[51]	110	155	400	92.0%	13.42	10	15
[52]	90–265	20	330	92.2%	40.72	12	400
[53]	90–265	20	330	94.0%	44.79	15	300
[18]	90–110	100	100	92.5%	6.38	7	50
[54]	100–240	48	100	90.5%	42.65	11	35-75
This Work	120	250	250	91.7%	2.65	12[‡]	210

[†] Taken at rated power and $120V_{\text{rms}}$ where available.
[‡] Using monolithic BDS devices; 20 devices used in this work to emulate BDSs.

(e.g., [49], [55], [56], [57], [58], [59], [60]). The primary drawback of these converters is that they still rely upon large dc link capacitors to filter $2\omega_g$ ripple present during near unity power factor operation and subsequently this power must be processed by the high-frequency transformer. To reduce the size of the buffer capacitor and power throughput of the transformer, [48], [61], [62], [63] introduce a series-connected AEB to the high frequency tank of the DAB ac/dc converter, where [48], [61], [62] also include a series resonant filter. While the circuit structure of these works are very similar to that of Fig. 2, the power conversion processes are fundamentally distinct. Having described the operating principles of the single-branch HPPC in this and the previous section, we now provide insight into the differentiating characteristics of this and the work in [48], [61], [62], [63], which is corroborated by experimental measurements.

In the seminal work which introduced this method [48], the series buffer capacitor and the ac line are both modulated by a half-bridge configuration of unipolar devices (a half-wave cycloconverter is required for the ac interface) while the dc port is interfaced by a full-bridge. A complicated line-phase dependent control strategy is proposed, which implements time-varying phase shifts on the ac and buffer bridges and time-varying PWM on the dc bridge. This results in a PWM modulated switching frequency square wave on the primary of the transformer and a modulated switching frequency current in the tank. The buffer capacitor operates with a dc voltage and therefore does not achieve minimum energy buffering. In contrast, [61] replaces the half-bridges with full-bridges and operates with time-varying PWM on both the ac and series-buffer active bridges, and with fixed phase, constant duty cycle operation on the dc bridge (phase and duty cycle are used as setpoint variables to regulate the desired steady-state voltage and power conditions). The work proposed in [62] then implements similar modulation strategies as in [61] while using the topology of [48]. The result of [61] and [62] is a square wave on the primary of the transformer and a sinusoidal tank current, both at the switching frequency. These works achieve minimum energy storage buffering by maintaining a half-wave rectified sinusoid on the buffer capacitor with an appropriate phase shift to the grid voltage. The work in [63] interfaces the ac port with a BDS full-bridge inverter, and the series active buffer and dc port with a unipolar full-bridge. This results in a switching frequency square wave voltage at the transformer and a multisegment piece-wise linear current in the tank. The capacitor $2\omega_g$ buffering is imposed on a dc voltage and therefore does not achieve minimum energy storage buffering.

TABLE V
EXPERIMENTALLY MEASURED HARMONIC CONTENT IN KEY SINGLE-BRANCH HPPC STATE VARIABLES

	$f_{\text{HF}} - f_g = 209.80\text{kHz}$	$f_{\text{HF}} = 209.86\text{kHz}$	$f_{\text{HF}} + f_g = 209.92\text{kHz}$
$v_{HF}(t)$	$76.0V_{\text{rms}}$	0	$74.0V_{\text{rms}}$
$v_B(t)$	$73.5V_{\text{rms}}$	0	$74.0V_{\text{rms}}$
$v_+(t)$	$2.5V_{\text{rms}}$	0	$74.0V_{\text{rms}}$
$i_{HF}(t)$	$0.05A_{\text{rms}}$	0	$3.0A_{\text{rms}}$

In all of [48], [61], [62], and [63], the critical distinction from this work is that every switching network operates at the same square wave modulated switching frequency. Therefore, regardless of the additional modulation employed (e.g., phase, PWM), the dominant current harmonic in the tank is at the switching frequency. While all of these works generate and control sideband harmonic voltages, the partitioning and enforcement of these harmonics is fundamentally dissimilar from that proposed in this work, where the current in the tank and the voltage across the primary of the transformer are explicitly designed to be at one sideband harmonic of the switching frequency. This is exemplified by the harmonic content measured on the prototype of Fig. 4 and presented in Table V. It is seen that the voltages $v_{HF}(t)$ and $v_B(t)$ contain both 60 Hz sidebands of the switching frequency but the tank current and the voltage across the primary of the transformer are predominantly of the positive sideband. Further, this work presents a novel framework for time-domain analysis of these systems and a general architecture enabling synthesis of otherwise nontrivial topologies (to be discussed in

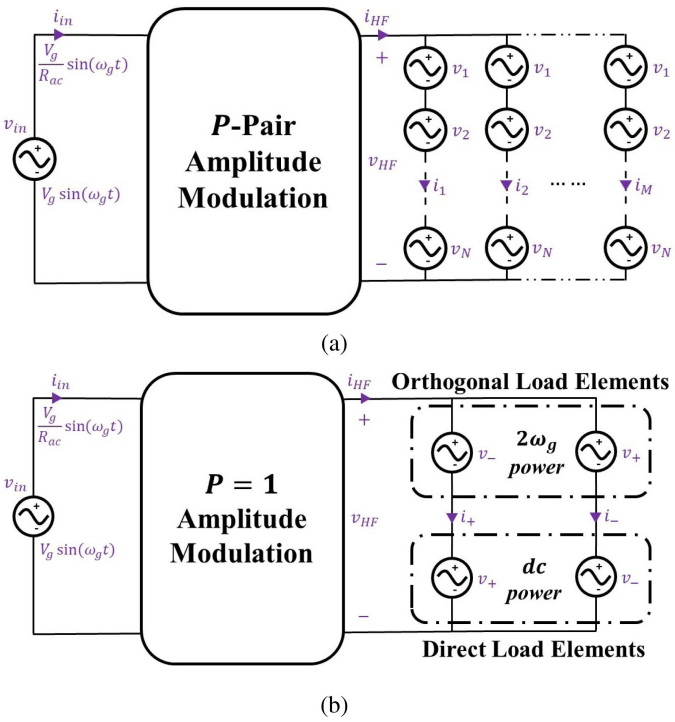

Fig. 7. Generalized HPPC for (a) an arbitrary integer P pairs of sideband harmonics, $N = 2P$ total voltage harmonics, and M branches, and (b) an example HPPC with a single $P = 1$ sideband harmonic pair, $N = 2$ voltage harmonics, and $M = 2$ branches.

Section IV). This is in contrast to prior art which has relied upon complicated switching-frequency-based averaged fundamental harmonic analyses that provide a limited framework for exploring alternative topologies that might offer different and beneficial design trade-offs.

IV. General HPPC Architecture

The previous section experimentally demonstrates the ability for a single-branch HPPC to achieve unity power factor, true-minimum energy buffering, dc output voltage conversion, and galvanic isolation in a single-stage architecture. The most general structure of the HPPC is shown in Fig. 7(a). The HPPC consists of a P-Pair amplitude modulation network connected directly to the ac port, and the output of this network feeds a configuration of harmonically partitioned loads. The P-Pair amplitude modulation network, hereinafter referred to as the modulation network, generates P pairs of sideband harmonic voltages totaling $N = 2P$ voltage harmonics. The configuration of harmonically partitioned loads consists of $M \geq 1$ parallel branches, where each branch consists of a series connection of orthogonal load elements and direct load elements whose total voltage drops must equal the N voltage harmonics inserted by the modulation network. In addition, each of the M branches must carry a current with the same frequency as one of the voltage harmonics inserted by the modulation network.

One particular embodiment of the general architecture, which demonstrates its salient benefits while enabling very high performance is shown in Fig. 7(b). This implementation generates a single pair ($P = 1$) of sideband harmonic voltages such that a total of $N = 2$ voltage harmonics are present in v_{HF}. The modulation command for this case is

$$m(t) = M \sin(\omega_{HF} t) \tag{35}$$

where $0 \leq M \leq 1$ is the controllable carrier amplitude enabling gain variation and $\omega_{HF} \gg \omega_g$ is the carrier frequency. As was described in Section II, the output of the BDS inverter can be found as

$$v_{HF}(t) = \frac{MV_g}{2}[\cos((\omega_{HF} - \omega_g)t) - \cos((\omega_{HF} + \omega_g)t)] \tag{36}$$

and the decomposed voltage harmonics are

$$v_-(t) = \frac{MV_g}{2}\cos((\omega_{HF} - \omega_g)t) \tag{37}$$

$$v_+(t) = -\frac{MV_g}{2}\cos((\omega_{HF} + \omega_g)t). \tag{38}$$

A. Instantaneous Power Flow

To ensure the converter will draw current that allows unity power factor operation, we can load the modulation network with an effective resistance R_e. For this case, the current $i_{HF}(t)$ is found as

$$\begin{aligned} i_{HF}(t) &= \frac{v_{HF}(t)}{R_e} = \frac{v_-(t)}{R_e} + \frac{v_+(t)}{R_e} \\ &= \frac{MV_g}{2R_e}[\cos((\omega_{HF} - \omega_g)t) - \cos((\omega_{HF} + \omega_g)t)]. \end{aligned} \tag{39}$$

This current has the same sideband harmonics as the voltage inserted by the modulation network. If the orthogonal and direct loads maintain the voltages shown in Fig. 7(b) and the current $i_{HF}(t)$ splits such that $i_-(t)$ flows in one branch while $i_+(t)$ flows in the other, the HPPC will draw unity power factor current while completely decoupling the dc and $2\omega_g$ instantaneous power in the system. Following the derivation provided in Section II-B, the orthogonal loads will process the following instantaneous power:

$$p_{o1}(t) = -\frac{M^2V_g^2}{4R_e}[\cos(2\omega_{HF}t) + \cos(2\omega_g t)] \tag{40}$$

$$p_{o2}(t) = -\frac{M^2V_g^2}{4R_e}[\cos(2\omega_{HF}t) + \cos(2\omega_g t)]. \tag{41}$$

Similarly, the instantaneous power flow at the direct loads is

$$p_{d1}(t) = \frac{M^2V_g^2}{4R_e}[1 + \cos(2(\omega_{HF} - \omega_g)t)] \tag{42}$$

$$p_{d2}(t) = \frac{M^2V_g^2}{4R_e}[1 + \cos(2(\omega_{HF} + \omega_g)t)]. \tag{43}$$

Equations (40) and (41) again show that the orthogonal load elements process only $2\omega_g$ and $2\omega_{HF}$ power, while (42) and (43) show that the direct load elements process only dc and $2(\omega_{HF} \pm \omega_g)$ power. The analysis for the general two-branch architecture of Fig. 7(b) further demonstrates the key mechanism

for power decoupling: similar sidebands process dc power while orthogonal sidebands process $2\omega_g$ power. With unity power factor, gain variation, and power decoupling demonstrated, galvanic isolation can be achieved by integrating transformers at the direct loads as was described in Section II.

B. Reduction to a Single-Branch

It is possible to omit one of the branches in Fig. 7(b) at the expense of losing ZVS over half of the line cycle and carrying increased currents in the branch for the same power transfer. This has already been demonstrated in Section II, where Fig. 2 corresponds to having removed the rightmost branch of Fig. 7(b) carrying the other sideband harmonic current i_-. The second branch of Fig. 7(b) can be implemented in Fig. 2 by adding an identical branch in parallel but controlling the new buffer BDS inverter to have $\rho = +45^\circ$ and replacing the orthogonal inductor L_O with an orthogonal capacitor C_O sized for

$$C_O = \frac{1}{R_e(\omega_{HF} + \omega_g)}. \tag{44}$$

Multiple branches can also be implemented to carry the same harmonic current with varying amplitudes, as may be of interest, e.g., in generating multiple dc outputs from the single ac source.

C. Zero Voltage Switching (ZVS)

The single-branch HPPC described in this paper only achieves ZVS for half of the line cycle, one of the primary drawbacks of the single-branch architecture in comparison to the dual-branch architecture. This can be observed by considering the effective ac resistance loading the modulation network. For example, in the single-branch implementation the current was defined such that $i_{HF} = i_+ = v_+/R_e$. The effective ac resistance loading the modulation network for this voltage and current profile is then found as

$$R_{ac} = \frac{v_{HF}(t)}{i_{HF}(t)} = R_e\left[1 + \frac{\cos((n\omega_{HF} - \omega_g)t)}{\cos((n\omega_{HF} + \omega_g)t)}\right]. \tag{45}$$

Equation (45) shows that the harmonically partitioned loads of the single-branch architecture appear to the BDS inverter as a nonlinear load and only enable ZVS during half of the line cycle. In contrast, the current for the two-branch implementation in Fig. 7(b) is defined as $i_{HF} = i_+ + i_- = v_{HF}/R_e$. The harmonically partitioned loads of this two-branch implementation therefore appear to the modulation network as an effective linear resistance and permit soft switching of all inverter switches throughout the duration of the line cycle.

V. Practical Considerations

Because the HPPC is a new general architecture, it is beneficial to further discuss some of the practical design opportunities and challenges associated with the single- and two-branch HPPC architecture.

A. Magnetic Design

A key advantage of the HPPC over the traditional architecture described in Fig. 1 is the removal of PFC inductors carrying dc currents. These are inherently difficult to miniaturize owing to the competing requirements of high saturation flux densities (associated with dc currents) and low core losses (associated with ac currents). The high frequency operation enabled by the two-branch architecture presents an opportunity for significant miniaturization of the magnetics as they are all relegated to the high frequency ac branch. In addition, certain waveshaping techniques (e.g., setting $\psi = 30^\circ$ to cancel third harmonic sideband generation) can further reduce the requirements of the resonant filter, and many other multilevel and harmonic reduction waveshaping techniques common to inverters [4] may be extended to the BDS inverter.

The purely sinusoidal high frequency current $i_+(t)$ carried by the branch inductances is also amenable to miniaturization, particularly with the emergence of low cost, automated high-frequency core loss testers which produce large data sets ideal for optimization [64], [65], [66]. Further, as the orthogonal and resonant inductances L_O and L_r can be integrated into a single inductance, only one inductor is required for a single-branch. At the higher switching frequencies available in the two-branch architecture, this can be done, e.g., by implementing the inductors as the leakage of the high-frequency transformer.

B. Variable Passive Components

One of the key challenges of the HPPC implementation described in this article is load dependence of the orthogonal inductor L_O. If the main BDS inverter is operated with a control angle ψ while the buffer BDS inverter is operated with an independent control angle ψ_B, the required buffer capacitance and orthogonal inductance are found as

$$C_B = \frac{4}{\pi^2\omega_g R_e}\cos^2(\psi_B) \tag{46}$$

$$L_O = \frac{R_e}{(\omega_{HF} + \omega_g)}. \tag{47}$$

The control angle ψ is used for output voltage regulation and the variable ψ_B in (46) can enable a constant capacitance over variations of load voltage and power. Equation (47), however, shows that the required orthogonal inductance must change with variations in load resistance to maintain unity power factor. This variable inductance (and capacitance for the two-branch architecture) represents a unique design challenge for the HPPCs described in this work, but there exists a myriad of literature on the synthesis of variable inductors and capacitors. For example, variable inductors [67], [68], [69], [70], [71], [72] and capacitors [73], [74], [75], [76] derived from ferromagnetic and ferroelectric materials represent a suitable option for power electronics applications, but a more comprehensive analysis as to their associated trade-offs on system functionality, loss, and volume is necessary. The strong miniaturization opportunity presented by the HPPC architecture motivates the advancement of improved high-performance variable passive components.

Another possibility for introducing an additional control variable in the system is the implementation of a variable turns ratio transformer. For example, since $R_L = V_o^2/P_o$, two independent control variables are needed for the two independent design

TABLE VI
ORTHOGONAL LOAD VOLTAGES, ENERGY BUFFERS, AND ORTHOGONAL CANCELLATION ELEMENTS FOR EXAMPLE SINGLE- OR TWO-BRANCH HPPC IMPLEMENTATIONS

Desired Voltage	Energy Buffer	Phase Cancellation Element
$v_-(t)$	Capacitor	Inductor
$v_-(t)$	Inductor	Capacitor
$v_+(t)$	Capacitor	Capacitor
$v_+(t)$	Inductor	Inductor

specifications V_o and P_o. Assuming a fixed turns ratio, the zero state angle ψ allows for output voltage regulation while a variable inductance L_O would be required to regulate the output power P_o. However, if the turns ratio of the transformer was variable, ψ could still regulate the output voltage while the turns ratio n_t is altered to ensure the effective resistance of (16) remained constant, thus allowing constant valued passive components as per (28) and (31). Such variable turns ratio transformers are in active development and would be particularly amenable to this type of system [39], [40], [41], [77].

C. Other Energy Buffers

While this article presented one implementation of the orthogonal load using a capacitive energy buffer C_B, the energy buffering element can also be an inductor[6] L_B. The required orthogonal cancellation element will then depend on not only what type of energy buffer is utilized, but also what orthogonal load voltage is desired to be maintained. Table VI shows the combinations of orthogonal loads that may be implemented when using square wave modulation of the BDS inverters. Furthermore, the architecture can build on the extensive work that has been done in dc-regulating AEBs [21], [80], [81], [82]. The orthogonal load in the HPPC is distinct in that it interfaces a low frequency buffer to a high frequency tank, but the robust dc AEB literature can motivate implementations of the orthogonal load. For example, the implementation in this article mimics the classic implementation in [16].

VI. FUTURE WORK

This article experimentally demonstrates the single-branch HPPC's ability to achieve unity power factor, complete power pulsation decoupling, and dc voltage regulation under open-loop operation. Practical deployment of the single- and two-branch HPPC described in this work necessitates further investigation into dynamic response and parameter optimization via closed-loop control, particularly due to voltage, frequency, and temperature fluctuations. The HPPC architecture described in this article additionally enables the synthesis of many possible single-stage single-phase ac/dc power conversion topologies. To fully leverage the benefit of the HPPC method across various applications, further research and development of the advantages and trade-offs of HPPC-based conversion topologies is required.

[6]It is very unlikely that an inductive buffer element would be considered as a result of the drastic energy density superiority of capacitor technologies at low frequency [78], [79].

VII. CONCLUSION

This article introduces a single-stage, single-phase ac/dc power conversion architecture called a "HPPC". By leveraging BDSs for direct modulation of the ac input, and employing a special "harmonically partitioned" loading network, the HPPC can achieve automatic unity power factor operation, continuous gain variation, galvanic isolation, and complete power pulsation decoupling in a single power conversion stage. Critically, this power conversion occurs entirely through a single high frequency ac tank (line-frequency ac $\rightarrow$ high-frequency ac $\rightarrow$ dc), rather than the traditional cascaded structure of single-phase ac/dc converters (which convert line-frequency ac $\rightarrow$ dc$\rightarrow$high-frequency ac $\rightarrow$ dc). By eliminating redundant conversion stages and relegating all magnetic components to the high frequency tank, the HPPC offers a substantial opportunity for miniaturization. The paper provides an analytical description of the general architecture and the underlying design equations. The core functionality of the proposed architecture is experimentally validated using a simple "single-branch" implementation, which demonstrates that unity power factor operation, true-minimum energy storage buffering, dc voltage conversion, and galvanic isolation are achieved in a single conversion stage. Several opportunities and challenges of the architecture are discussed, in addition to directions for future work. The proposed architecture is valuable for all single-phase ac/dc power conversion applications with power factor requirements on the ac port and offers strong potential for miniaturization and performance advances in this space.

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REFERENCES

[1] "IEC 61000-3-2: Electromagnetic Compatibility (EMC) – Part 3-2: Limits–Limits for Harmonic Current Emissions (Equipment up to and including 16 A Per Phase)," International Electrotechnical Commission (IEC), 2018, edition 5.0. [Online]. Available: https://webstore.iec.ch/en/publication/92799

[2] E. Candan, N. C. Brooks, A. Stillwell, R. A. Abramson, J. Strydom, and R. C. N. Pilawa-Podgurski, "A six-level flying capacitor multilevel converter for single-phase buck-type power factor correction," *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 6335–6348, Jun. 2022.

[3] S. S. Sayed and A. M. Massoud, "Review on state-of-the-art unidirectional non-isolated power factor correction converters for short-/long-distance electric vehicles," *IEEE Access*, vol. 10, pp. 11308–11340, 2022.

[4] J. G. Kassakian, D. J. Perreault, G. C. Verghese, and M. F. Schlect, *Principles of Power Electronics*, 2nd ed. New York, NY, USA: Cambridge Univ. Press, 2023.

[5] G. Moschopoulos and P. Jain, "Single-phase single-stage power-factor-corrected converter topologies," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 23–35, Feb. 2005.

[6] B. Singh, S. Singh, A. Chandra, and K. Al-Haddad, "Comprehensive study of single-phase AC-DC power factor corrected converters with high-frequency isolation," *IEEE Trans. Ind. Inform.*, vol. 7, no. 4, pp. 540–556, Nov. 2011.

[7] R. Kushwaha, V. Khadkikar, and A. Edpuganti, "Electric vehicle on-board fast charging through converter maximum switch utilization," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 998–1014, Jan. 2024.

[8] M. K. Ranjram, C. Zhang, and D. J. Perreault, "A two-stage universal input charger with wide output voltage range," *IEEE Open J. Power Electron.*, vol. 1, pp. 88–102, 2020.

[9] A. R. Gautam, D. M. Fulwani, R. R. Makineni, A. K. Rathore, and D. Singh, "Control strategies and power decoupling topologies to mitigate 2omega-ripple in single-phase inverters: A review and open challenges," *IEEE Access*, vol. 8, pp. 147533–147559, 2020.

[10] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "A review of power decoupling techniques for microinverters with three different decoupling capacitor locations in pv systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2711–2726, Jun. 2013.

[11] Y. Tang and F. Blaabjerg, "Power decoupling techniques for single-phase power electronics systems — an overview," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 2541–2548.

[12] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of active power decoupling topologies in single-phase systems," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4778–4794, Jul. 2016.

[13] S. Qin, Y. Lei, C. Barth, W.-C. Liu, and R. C. N. Pilawa-Podgurski, "A high power density series-stacked energy buffer for power pulsation decoupling in single-phase converters," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4905–4924, Jun. 2017.

[14] T. Shimizu, K. Wada, and N. Nakamura, "Flyback-type single-phase utility interactive inverter with power pulsation decoupling on the dc input for an ac photovoltaic module system," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1264–1272, Sep. 2006.

[15] Y. Tang and F. Blaabjerg, "A component-minimized single-phase active power decoupling circuit with reduced current stress to semiconductor switches," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 2905–2910, Jun. 2015.

[16] P. T. Krein, R. S. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4690–4698, Nov. 2012.

[17] H. Hu, S. Harb, N. H. Kutkut, Z. J. Shen, and I. Batarseh, "A single-stage microinverter without using eletrolytic capacitors," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2677–2687, Jun. 2013.

[18] H. Tian, M. Chen, C. Nie, G. Liang, and X. Xiao, "A more efficient single-phase ac/dc converter with automatic PFC and power decoupling capability," *IEEE Trans. Transport. Electrific.*, vol. 8, no. 3, pp. 3977–3988, Sep. 2022.

[19] M. Chen, K. K. Afridi, and D. J. Perreault, "Stacked switched capacitor energy buffer architecture," in *Proc. 27th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2012, pp. 1404–1413.

[20] C. McHugh et al., "A high power density single-phase inverter using stacked switched capacitor energy buffer," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 1947–1953.

[21] Y. Ni, S. Pervaiz, M. Chen, and K. K. Afridi, "Energy density enhancement of stacked switched capacitor energy buffers through capacitance ratio optimization," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6363–6380, Aug. 2017.

[22] A. J. Hanson, A. F. Martin, and D. J. Perreault, "Energy and size reduction of grid-interfaced energy buffers through line waveform control," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11442–11453, Nov. 2019.

[23] F. Giardine, N. C. Brooks, K. Fernandez, and R. C. Pilawa-Podgurski, "Utilizing harmonic injection to reduce energy storage and required capacitance in an active series-stacked energy buffer for single-phase systems," in *Proc. IEEE 23rd Workshop Control Model. Power Electron.*, 2022, pp. 1–7.

[24] T. Langbauer et al., "Third-harmonic-type modulation minimizing the dc-link energy storage requirement of isolated phase-modular three-phase PFC rectifier systems," *IEEE Access*, vol. 11, pp. 34359–34371, 2023.

[25] T. Morita et al., "650 V 3.1 mohmcm2 gan-based monolithic bidirectional switch using normally-off gate injection transistor," in *Proc. 2007 IEEE Int. Electron Devices Meeting*, 2007, pp. 865–868.

[26] Y. Kudoh et al., "Single to two-phase matrix converter using gan-based monolithic bidirectional switch for driving symmetrical two-phase motor," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 3186–3191.

[27] T. LaBella and J.-S. Lai, "A hybrid resonant converter utilizing a bidirectional GAN AC switch for high-efficiency PV applications," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3468–3475, Sep./Oct. 2014.

[28] Z. J. Shen et al., "First experimental demonstration of solid state circuit breaker (SSCB) using 650v gan-based monolithic bidirectional switch," in *Proc. 28th Int. Symp. Power Semicond. Devices*, 2016, pp. 79–82.

[29] C. Kuring, O. Hilt, J. Böcker, M. Wolf, S. Dieckerhoff, and J. Würfl, "Novel monolithically integrated bidirectional GAN hemt," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 876–883.

[30] H. Ueno et al., "A 3-phase t-type 3-level inverter using GAN bidirectional switch with very low on-state resistance," in *Proc. Europe Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2019, pp. 1–4.

[31] Y. Kinoshita, T. Ichiryu, A. Suzuki, and H. Ishida, "100 A solid state circuit breaker using monolithic GAN bidirectional switch with two-step gate-discharging technique," in *Proc. 2020 IEEE Appl. Power Electron. Conf. Expo.*, 2020, pp. 652–657.

[32] S. Musumeci, M. Panizza, F. Stella, and F. Perraud, "Monolithic bidirectional switch based on GAN gate injection transistors," in *Proc. IEEE 29th Int. Symp. Ind. Electron.*, 2020, pp. 1045–1050.

[33] F. Vollmaier, N. Nain, J. Huber, J. W. Kolar, K. K. Leong, and B. Pandya, "Performance evaluation of future t-type PFC rectifier and inverter systems with monolithic bidirectional 600 v GAN switches," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2021, pp. 5297–5304.

[34] N. Nain, S. Walser, J. Huber, K. K. Leong, and J. W. Kolar, "Self-reverse-blocking control of dual-gate monolithic bidirectional GAN switch with quasi-ohmic on-state characteristic," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 10091–10094, Sep. 2022.

[35] H. Dai, R. A. Torres, J. Gossmann, W. Lee, T. M. Jahns, and B. Sarlioglu, "A seven-switch current-source inverter using wide bandgap dual-gate bidirectional switches," *IEEE Trans. Ind. Appl.*, vol. 58, no. 3, pp. 3721–3737, May/Jun. 2022.

[36] J. Huber and J. W. Kolar, "Monolithic bidirectional power transistors," *IEEE Power Electron. Mag.*, vol. 10, no. 1, pp. 28–38, Mar. 2023.

[37] H. Dai, R. A. Torres, F. Chen, T. M. Jahns, and B. Sarlioglu, "An h8 current-source inverter using single-gate WBG bidirectional switches," *IEEE Trans. Transport. Electrific.*, vol. 9, no. 1, pp. 1311–1329, Mar. 2023.

[38] Q. Yu, D. Klikic, V. Aulagnier, E. Perrson, and J. Cerce, "Evaluation of monolithic AC GAN switch in a vienna rectifier for UPS," in *Proc. 2024 IEEE Appl. Power Electron. Conf. Expo.*, 2024, pp. 767–773.

[39] M. K. Ranjram, I. Moon, and D. J. Perreault, "Variable-inverter-rectifier-transformer: A hybrid electronic and magnetic structure enabling adjustable high step-down conversion ratios," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 6509–6525, Aug. 2018.

[40] M. K. Ranjram and D. J. Perreault, "A 380-12 v, 1-kw, 1-mhz converter using a miniaturized split-phase, fractional-turn planar transformer," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1666–1681, Feb. 2022.

[41] I. Willows, S. Radhakrishnan, and M. Ranjram, "Multi-level coupled electronic and magnetic system for wide-gain constant power conversion," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2024, pp. 7268–7275.

[42] R. E. Ziemer and W. H. Tranter, *Principles of Communications*, 7th ed. Massachusetts, USA: Wiley, 2014.

[43] H. Huang, "Designing an LLC resonant half-bridge power converter," Texas Instruments, Texas, USA, White Paper SLUP263, 2010, [Online]. Available: https://bbs.dianyuan.com/upload/community/2013/12/01/1385867010-65563.pdf

[44] E. Corporation, "Eaton efdks55j147f044dh film capacitor datasheet," 2025, Accessed: Feb. 19, 2025. [Online]. Available: https://www.eaton.com/us/en-us/skuPage.EFDKS55J147F044DH.pdf

[45] T. Electronics, "Epcos b32796g2456k 45 μf film capacitor 250v 630v polypropylene (pp), metallized radial," 2025, Accessed: Feb. 19, 2025. [Online]. Available: https://mm.digikey.com/Volume0/opasdata/d220001/medias/docus/1076/B32794-B32798.pdf

[46] M. Daniele, P. Jain, and G. Joos, "A single-stage power-factor-corrected AC/DC converter," *IEEE Trans. Power Electron.*, vol. 14, no. 6, pp. 1046–1055, Nov. 1999.

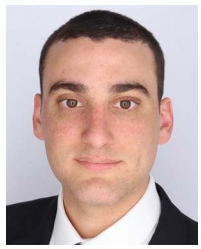
[47] M. Narimani and G. Moschopoulos, "A new single-phase single-stage three-level power-factor-correction AC–DC converter with phase-shift modulation," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3731–3735, Sep. 2013.

[48] B. J. Pierquet and D. J. Perreault, "A single-phase photovoltaic inverter topology with a series-connected energy buffer," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4603–4611, Oct. 2013.

[49] J. Everts, F. Krismer, J. Van den Keybus, J. Driesen, and J. W. Kolar, "Optimal zvs modulation of single-phase single-stage bidirectional dab ac–dc converters," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 3954–3970, Aug. 2014.

[50] Y. Qiu, L. Wang, H. Wang, Y.-F. Liu, and P. C. Sen, "Bipolar ripple cancellation method to achieve single-stage electrolytic-capacitor-less high-power led driver," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 3, pp. 698–713, Sep. 2015.

[51] X. Sun, H. Wang, L. Qi, and F. Liu, "Research on single-stage high-frequency-link SST topology and its optimization control," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8701–8711, Aug. 2020.
[52] M. Khatua, A. Kumar, S. Pervaiz, S. Chakraborty, and K. K. Afridi, "A single-stage isolated AC–DC converter based on the impedance control network architectureA single-stage isolated ac–dc converter based on the impedance control network architecture," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10366–10382, Sep. 2021.
[53] M. Khatua, A. Kumar, S. Pervaiz, S. Chakraborty, and K. K. Afridi, "Performance enhancement of ICN-based single-stage AC–DC converters using reconfigurable inverters," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8217–8231, Jul. 2022.
[54] J.-W. Yang and H.-L. Do, "Single-stage two-flyback PFC converter with low voltage stress on a switch," *IEEE Trans. Ind. Electron.*, vol. 72, no. 2, pp. 1466–1474, Feb. 2025.
[55] N. D. Weise, G. Castelino, K. Basu, and N. Mohan, "A single-stage dual-active-bridge-based soft switched AC–DC converter with open-loop power factor correction and other advanced features," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4007–4016, Aug. 2014.
[56] N. Patel, L. A. C. Lopes, A. Rathore, and V. Khadkikar, "A soft-switched single-stage single-phase PFC converter for bidirectional plug-in ev charger," *IEEE Trans. Ind. Appl.*, vol. 59, no. 4, pp. 5123–5135, Jul./Aug. 2023.
[57] P. Jena, R. K. Singh, and V. N. Lal, "A reduced carrier count asymmetric switching sequence based triangular modulation for quasi single stage ac-dc dual active bridge," *IEEE Trans. Ind. Appl.*, vol. 60, no. 6, pp. 8988–8997, Nov./Dec. 2024.
[58] D. Sha, D. Zhang, and J. Zhang, "A single-stage dual-active-bridge ac–dc converter employing mode transition based on real-time calculation," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10081–10088, Sep. 2021.
[59] F. Jauch and J. Biela, "Combined phase-shift and frequency modulation of a dual-active-bridge AC–DC converter with PFC," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8387–8397, Dec. 2016.
[60] R. Baranwal, G. F. Castelino, K. Iyer, K. Basu, and N. Mohan, "A dual-active-bridge-based single-phase AC to DC power electronic transformer with advanced features," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 313–331, Jan. 2018.
[61] D. Sal y Rosas, D. Frey, J.-L. Schanen, and J.-P. Ferrieux, "Isolated single stage bidirectional ac-dc converter with power decoupling and reactive power control to interface battery with the single phase grid," in *Proc. 2018 IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 631–636.
[62] D. Chavez and D. E. S. y. Rosas, "Isolated single-stage dabsr DC/AC converter with series-power decoupling to interface PV with the single-phase grid," in *Proc. IEEE 12th Int. Symp. Power Electron. Distrib. Gener. Syst.*, 2021, pp. 1–6.
[63] S. Barman, S. Chakraborty, and K. Chatterjee, "Series connected high frequency link ripple power compensation strategy for 1-phase bidirectional isolated AC- DC matrix converters," in *Proc. 2024 IEEE Int. Commun. Energy Conf.*, 2024, pp. 1–6.
[64] J. R. Anderson and M. K. Ranjram, "Automation of high-frequency magnetic core loss data collection," in *Proc. IEEE 24th Workshop Control Model. Power Electron.*, 2023, pp. 1–8.
[65] J. R. Anderson, N. J. Kirkby, and M. K. Ranjram, "Class-d amplifier-based core loss measurements for high frequency magnetic materials," in *Proc. IEEE Workshop Control Model. Power Electron.*, 2024, pp. 1–8.
[66] N. J. Kirkby and M. K. Ranjram, "Temperature control for automated high frequency core loss testing," in *Proc. 2024 IEEE Workshop Control Model. Power Electron.*, 2024, pp. 1–8.
[67] D. Tagare, S. Park, and M. K. Ranjram, "Emulation of plasma load reactances by saturation control of low-permeability inductors," in *Proc. 2024 IEEE Appl. Power Electron. Conf. Expo.*, 2024, pp. 416–423.
[68] P. N. Tawiah-Mensah, I. Hwang, S. Nagella, and A.-T. Avestruz, "Orthogonally variable inductors with poloidal AC currents and axial dc fields," in *Proc. 2024 IEEE Workshop Control Model. Power Electron.*, 2024, pp. 1–8.
[69] W. G. Hurley and W. H. Wolfle, "Variable inductance," in *Transformers and Inductors for Power Electronics*, 1st ed. Hoboken, NJ. USA: Wiley, 2013, pp. 301–341.
[70] D. Medini and S. Ben-Yaakov, "A current-controlled variable-inductor for high frequency resonant power circuits," in *Proc. 1994 IEEE Appl. Power Electron. Conf. Expo.*, 1994, pp. 219–225.
[71] P. Zacharias, T. Kleeb, F. Fenske, J. Wende, and J. Pfeiffer, "Controlled magnetic devices in power electronic applications," in *Proc. 19th Eur. Conf. Power Electron. Appl.*, 2017, pp. P.1–P.10.
[72] P. Mali, *Magnetic Amplifiers: Principles and Applications*. New York, NY, USA: John F. Rider Publisher, Inc., 1960.
[73] L. Zhou, J. Tian, S. Liu, R. Mai, L. Fu, and U. K. Madawala, "High-efficiency WPT systems for potable electronics based on DC-bias-voltage-controlled variable capacitor," *IEEE Trans. Ind. Electron.*, vol. 71, no. 5, pp. 4707–4718, May 2024.
[74] S. Tishechkin and S. Ben-Yaakov, "Adaptive capacitance impedance matching (acim) of WPT systems by voltage controlled capacitors," in *Proc. IEEE PELS Workshop Emerg. Technol.: Wireless Power Transfer*, 2019, pp. 396–400.
[75] H. Zeng and F. Z. Peng, "Non-linear capacitor based variable capacitor for self-tuning resonant converter in wireless power transfer," in *Proc. 2018 IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 1375–1379.
[76] I. Kolberg, D. Shmilovitz, and S. S. Ben-Yaakov, "Ceramic capacitor controlled resonant LLC converters," in *Proc. 2018 IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 2162–2167.
[77] M. K. Ranjram and D. J. Perreault, "A modeling approach for the virt and other coupled electronic and magnetic systems," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 6728–6741, Dec. 2022.
[78] Z. Liao, N. C. Brooks, Z. Ye, and R. C. N. Pilawa-Podgurski, "A high power density power factor correction converter with a multilevel boost front-end and a series-stacked energy decoupling buffer," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 7229–7235.
[79] C. B. Barth, T. Foulkes, I. Moon, Y. Lei, S. Qin, and R. C. N. Pilawa-Podgurski, "Experimental evaluation of capacitors for power buffering in single-phase power converters," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7887–7899, Aug. 2019.
[80] K. A. Kim, Y.-C. Liu, M.-C. Chen, and H.-J. Chiu, "Opening the box: Survey of high power density inverter techniques from the little box challenge," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 2, pp. 131–139, 2017.
[81] M. Chen, K. K. Afridi, and D. J. Perreault, "A multilevel energy buffer and voltage modulator for grid-interfaced microinverters," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1203–1219, Mar. 2015.
[82] H. Sarnago and O. Lucía, "High power density on-board charger featuring power pulsating buffer," *IEEE Open J. Power Electron.*, vol. 5, pp. 162–170, 2024.



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