Optimization Study of Parasitic Parameters in Parallel Interleaved Windings for High-Frequency PCB Transformers

Dejun Ba, Faxin Yu, *Senior Member, IEEE*, Yihe Wang, Xinran Chen, Yuxin Niu, and Xiaofeng Lyu, *Senior Member, IEEE*

***Abstract*—This study presents an innovative design approach using a parallel interleaved winding structure to reduce parasitic effects in high-frequency PCB transformers. Among the solutions provided, the multibranch parallel connection winding structure addresses high ac impedance and eddy current loss caused by the high-frequency skin effect of the conductor. The branch horizontal interleaved structure decreases the winding parasitic capacitance and suppresses the common mode current conduction path. The vertical interleaved winding structure improves the electromagnetic coupling between the primary and secondary windings, reducing the transformer's leakage inductance. The effectiveness of the proposed winding structure is supported by simulation and experimental results, which indicate reductions in parasitic capacitance by 37.20%, 43.54%, and 63.06%, and reductions in leakage inductance by 44.64%, 44.05%, and 44.79% at 1 MHz. In addition, the output efficiency of the 45 V–5 V/20 A prototype has been increased by 2.8%, 2.0%, and 1.5% at 1.1 MHz.**

***Index Terms*—High-frequency transformer, isolated power supply, leakage inductance, parallel interleaving, parasitic capacitance.**

NOMENCLATURE

Variables

δ	Skinning depth $[um]$.
μ	Permeability of the conductor material $[H/m]$.
σ	Conductivity of the conductor material $[S/m]$.
C_{AB}	Capacitance of primary winding structures $[F]$.
$C_{AD}, C_{BC}, C_{AC}, C_{BD}$	Capacitance between primary and secondary $[F]$.
C_{CD}	Capacitance of secondary winding structures $[F]$.
f	Frequency $[Hz]$.
L_p	Excitation inductance of primary windings $[H]$.
L_{r1}	Primary leakage inductance of the transformer $[H]$.
L_{r2}	Secondary leakage inductance of the transformer $[H]$.
L_{rT}	Equivalent leakage inductance of transformer $[H]$.
L_s	Excitation inductance of secondary windings $[H]$.
Q_{MC}	Mutual capacitance charge $[J]$.
Q_{SC}	Self capacitance charge $[J]$.
Q_T	Transformer parasitic capacitance charge $[J]$.
R_{DC}	DC impedance $[\Omega]$.
U_P	Primary voltage of the transformer $[V]$.
U_S	Secondary voltage of the transformer $[V]$.
Z_{AC}	AC impedance $[\Omega]$.
Z_{s1}	Equivalent impedance of primary windings $[\Omega]$.
Z_{s2}	Equivalent impedance of secondary windings $[\Omega]$.
Z_T	Equivalent impedance of transformer $[\Omega]$.

Abbreviations

HFT	High-frequency transformers.
PCB	Printed circuit board.
PIW	Parallel interleaved windings.
MBPC	Multibranch parallel connection winding structure.
BHI	Branch horizontal interleaved winding structure.
VIW	Vertical interleaved winding structure.

Received 22 October 2024; revised 28 February 2025 and 25 May 2025; accepted 17 June 2025. Date of publication 19 June 2025; date of current version 5 August 2025. Recommended for publication by Associate Editor F. Luo. *(Corresponding author: Xiaofeng Lyu.)*

The authors are with the The School of Aeronautics and Astronautics, Zhejiang University, Hangzhou 310058, China (e-mail: 12324061@zju.edu.cn; xiaofeng.lyu@zju.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3581515.

Digital Object Identifier 10.1109/TPEL.2025.3581515

I. INTRODUCTION

WITH the advent of third-generation wide-bandgap semiconductor materials such as SiC [1] and GaN [2], which support faster switching speeds and higher operating frequencies, the demand for high-frequency PCB transformers (HFT(PCB)) in commercial satellites, new energy vehicles, electric vehicles, and smart grids has significantly increased [3]. High-frequency transformers enhance energy transfer efficiency and core utilization, reduce core size and weight, and minimize the volume of passive components such as capacitors and inductors [4]. Consequently, the application of high-frequency PCB transformers in power electronic systems has become increasingly widespread [5].

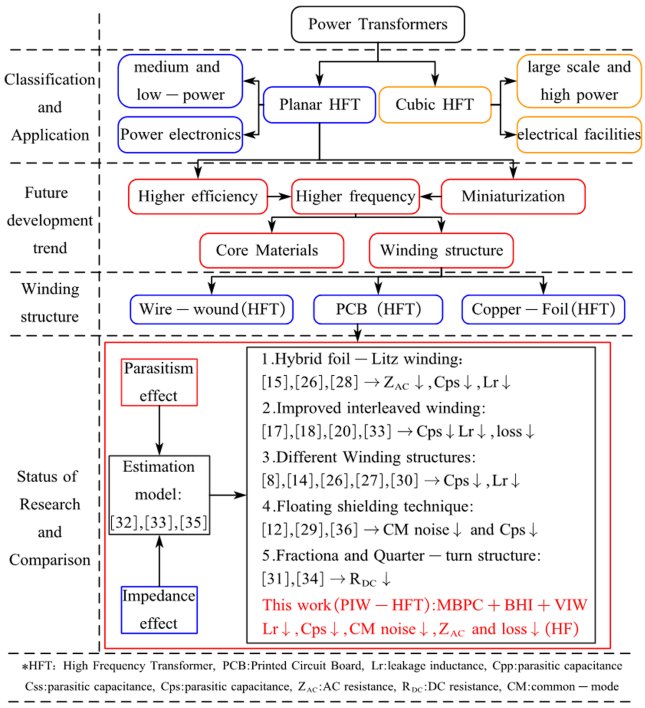


Fig. 1. Development trend and research progress of power transformer.

PCB transformers are extensively used in high-frequency applications due to their high window utilization, customization potential, reliability, large heat dissipation area, capacity to handle high current densities, simple manufacturing process, and low production cost. However, the progression toward higher frequencies introduces significant parasitic effects that impact transformer performance and stability. These effects include core losses at high frequencies [6], [7], parasitic effects in the windings [8], skin effect and proximity effect [9], [10], and challenges in high-frequency noise suppression and electromagnetic interference (EMI) optimization [11]. Specifically, increased high-frequency parasitic resistance (high-frequency ac impedance) leads to higher energy losses, reducing transformer efficiency. Increased parasitic capacitance between windings may cause circuit oscillations, crosstalk, and electromagnetic interference [12]. In addition, higher transformer leakage inductance can reduce efficiency and cause severe heating issues. Therefore, ensuring the consistency and reliability of high-frequency PCB transformers during long-term operation is crucial in high-frequency applications [13].

Studies on the suppression of parasitic parameters in HFT(PCB) have explored various approaches, as depicted in Fig. 1. Conventional solutions include layered winding arrangements to mitigate proximity effects [14], and litz wire and foil winding configurations to address skin effect limitations [15]. Although these methods reduce ac resistance by 15%–20%, they often compromise window utilization and increase manufacturing complexity. Advanced techniques like distributed air gap cores demonstrated reduction in leakage inductance 30%, but introduced additional core losses at MHz frequencies [16]. Comparative analysis of interleaved winding topologies revealed tradeoffs between parasitic capacitance and leakage inductance, highlighting the need for balanced optimization [17], [18]. Existing solutions fail to simultaneously address these interrelated challenges—multistrand parallel windings reduce ac resistance but increase interlayer capacitance [19], while vertical interleaving techniques achieve leakage inductance reduction at the cost of higher proximity losses [20].

Addressing the issues associated with HFT(PCB) necessitates deeper research and optimization. For example, optimizing winding design to reduce interwinding distances and selecting appropriate core materials and structures to minimize hysteresis and eddy current losses can significantly enhance performance and reliability [21], [22]. The hybrid core designs combining nanocrystalline and ferrite materials to suppress core losses by 37% [23]. However, these approaches require complex manufacturing processes incompatible with standard PCB fabrication.

This article proposes a novel parallel interleaved winding (PIW) structure that aims to simultaneously address high-frequency ac impedance, parasitic capacitance, and leakage inductance without significant trade-offs. The PIW structure leverages multibranch parallel connections (MBPC) to reduce ac impedance, branch horizontal interleaving (BHI) to minimize parasitic capacitance, and vertical interleaving winding (VIW) to enhance electromagnetic coupling and reduce leakage inductance. The proposed structure has been experimentally studied. Section II analyzes the electric field, parasitic capacitance, and high-frequency ac impedance models of high-frequency transformers. Section III presents the design method for the improved PIW structure. Section IV verifies the optimization effects on parasitic parameters through simulations and experiments. Finally, Section V concludes this article.

II. High-Frequency Transformer Modeling

A. Three-Capacitance Lumped Parameter Model

The six-capacitance transformer model is highly esteemed for its precise and detailed analysis in high-frequency characteristic simulations, insulation design, and partial discharge analysis. However, its complexity hinders its practical application in simulations. To tackle this issue, we suggest a simplified three-capacitance model derived from the six-capacitance model and the real electric field energy characteristics between windings, as depicted in Fig. 2. The potentials at each point are as follows:

$$\begin{cases} U_{AB} = U_P - (U_{Zs1} + U_{Lr1}) \\ U_{CD} = U_S - (U_{Zs2} + U_{Lr2}) \\ U_{AC} = U_{AB} + U_{BC} \\ U_{AD} = U_{AB} + U_{BC} + V_{CD} \\ U_{BD} = U_{BC} + U_{CD}. \end{cases} \tag{1}$$

In (1), we can determine the potentials at points A, B, C, and D by measuring U_{BC}. According to the six-capacitor model in Fig. 2(a), the total charge of the transformer's parasitic capacitance is given by

$$Q_T = U_{AB}\left(C_{AB} + C_{AC} + C_{AD}\right) + U_{CD}\left(C_{AD} + C_{BD} + C_{CD}\right)$$

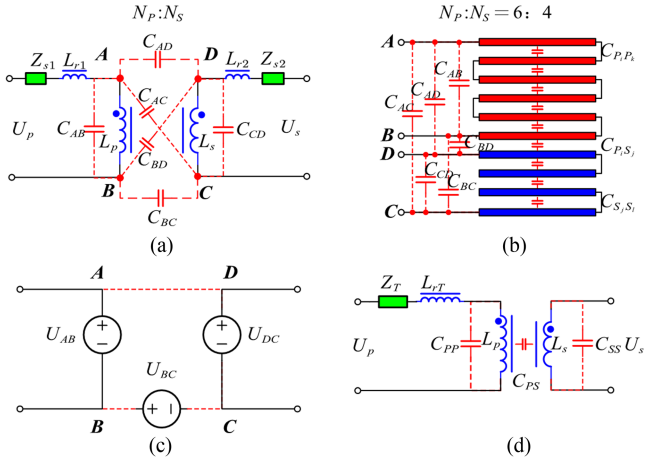


Fig. 2. Models of HFT capacitance. (a) the six-capacitor model, (b) the winding structure capacitance model, (c) equivalent potential model, and (d) the three-capacitance lumped parameter model.

$$+ U_{BC}\left(C_{AC} + C_{AD} + C_{BC} + C_{BD}\right). \tag{2}$$

From the six-capacitor model, we can derive the actual PCB transformer winding structure capacitance model in Fig. 2(b). Based on the electric field energy distribution within the transformer windings, the expression for the charge matrix of the parasitic capacitance in the model is

$$\mathbf{Q}_T = \mathbf{CV} \tag{3}$$

$$\mathbf{C} = \begin{bmatrix} C_{P_1P_1} & \cdots & C_{P_1P_j} & C_{P_1S_1} & \cdots & C_{P_1S_n} \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ C_{P_iP_1} & \cdots & C_{P_iP_j} & C_{P_iS_1} & \cdots & C_{P_iS_n} \\ C_{S_1P_1} & \cdots & C_{S_1P_j} & C_{S_1S_1} & \cdots & C_{S_1S_n} \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ C_{S_mP_1} & \cdots & C_{S_mP_j} & C_{S_mS_1} & \cdots & C_{S_mS_n} \end{bmatrix}$$

$$\mathbf{V} = \begin{bmatrix} v_{P_1P_1} & \cdots & v_{P_1P_j} & v_{P_1S_1} & \cdots & v_{P_1S_n} \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ v_{P_iP_1} & \cdots & v_{P_{P_iP_j}} & v_{P_iS_1} & \cdots & v_{P_{S_nS_n}} \\ v_{S_1P_1} & \cdots & v_{S_1P_j} & v_{S_1S_1} & \cdots & v_{S_1S_n} \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ v_{S_mP_1} & \cdots & v_{S_mP_j} & v_{S_mS_1} & \cdots & v_{S_mS_n} \end{bmatrix}^T.$$

In (3) ($i, j \in [1, N_P]; m, n \in [1, N_S]$), since the parasitic capacitance between nonadjacent windings in the transformer is relatively small, it can be neglected. Therefore, the total charge stored in the HFT is

$$Q_T = \begin{bmatrix} Q_{P_1P_1} + Q_{P_1P_2} + \cdots + Q_{P_1S_1} + \cdots + Q_{P_1S_n} \\ \vdots \\ Q_{P_iP_1} + Q_{P_iP_2} + \cdots + Q_{P_iS_1} + \cdots + Q_{P_iS_n} \\ Q_{S_1P_1} + Q_{S_1P_2} + \cdots + Q_{S_1S_1} + \cdots + Q_{S_1S_n} \\ \vdots \\ Q_{S_mP_1} + Q_{S_mP_2} + \cdots + Q_{S_mS_1} + \cdots + Q_{S_mS_n} \end{bmatrix}$$

$$= \begin{bmatrix} Q_{SC\_P_1} \\ \vdots \\ Q_{SC\_P_{(i=j)}} \\ Q_{SC\_S_1} \\ \vdots \\ Q_{SC\_S_{(m=n)}} \end{bmatrix} + \begin{bmatrix} Q_{MC\_P_1P_{j(j\neq1)}} \\ \vdots \\ Q_{MC\_P_iP_{j(j\neq i)}} \\ Q_{MC\_S_1S_{n(n\neq1)}} \\ \vdots \\ Q_{MC\_S_mS_{n(n\neq m)}} \end{bmatrix} + \begin{bmatrix} Q_{MC\_P_1S_n} \\ \vdots \\ Q_{MC\_P_iS_n} \\ Q_{MC\_S_1P_j} \\ \vdots \\ Q_{MC\_S_mP_j} \end{bmatrix}. \tag{4}$$

In (4), it is evident that the parasitic capacitance of the transformer is primarily composed of self-capacitance and mutual capacitance. The mutual capacitance further includes the inter-layer structural capacitance and the coupling capacitance between the primary and secondary windings, expressed as

$$Q_T = Q_{SC} + Q_{MC1} + Q_{MC2} \tag{5}$$

$$Q_{MC1} = Q_{PP} + Q_{SS} = \sum_{i=1}^{Np}\sum_{j=1}^{Np} C_{P_iP_j} v_{P_iP_j} + \sum_{m=1}^{Ns}\sum_{n=1}^{Ns} C_{S_mS_n} v_{S_mS_m} \tag{6}$$

$$Q_{MC2} = Q_{PS} + Q_{SP} = \sum_{i=1}^{Np}\sum_{n=1}^{Ns} C_{P_iS_n} v_{P_iS_n} + \sum_{m=1}^{Ns}\sum_{j=1}^{Np} C_{S_mP_j} v_{S_mP_j}. \tag{7}$$

Self-capacitance is an inherent property of the transformer windings and can be ignored. Thus, the three-capacitor model of the transformer is

$$Q_T = Q_{MC1} + Q_{MC2} = Q_{PP} + Q_{SS} + Q_{PS}(Q_{SP}). \tag{8}$$

The proportion of the three capacitors in the total parasitic capacitance is related to the transformer's winding configuration. In Fig. 2(d), the secondary side leakage inductance and the high-frequency impedances are transformed to the primary side. The resulting transformer leakage inductance and equivalent impedance are

$$L_{rT} = L_{r1} + L_{r2}\frac{N_P^2}{N_S^2} \tag{9}$$

$$Z_T = Z_{S_1} + Z_{S_2}\frac{N_P^2}{N_S^2}. \tag{10}$$

Under low-frequency operating conditions, the influence of PCB transformer parasitic parameters on the circuit is negligible and may be disregarded. However, under high-frequency conditions, the impact of high-frequency effects and parasitic parameters of PCB transformers is substantial, significantly affecting circuit stability, EMI, voltage-withstand capability, and component lifespan. Subsequent sections will comprehensively examine the parasitic capacitance, parasitic resistance, and leakage inductance under high-frequency conditions. We will present an optimized winding structure for PIW-HFT (PCB) transformers, and undertake experimental studies to corroborate the anticipated effects.

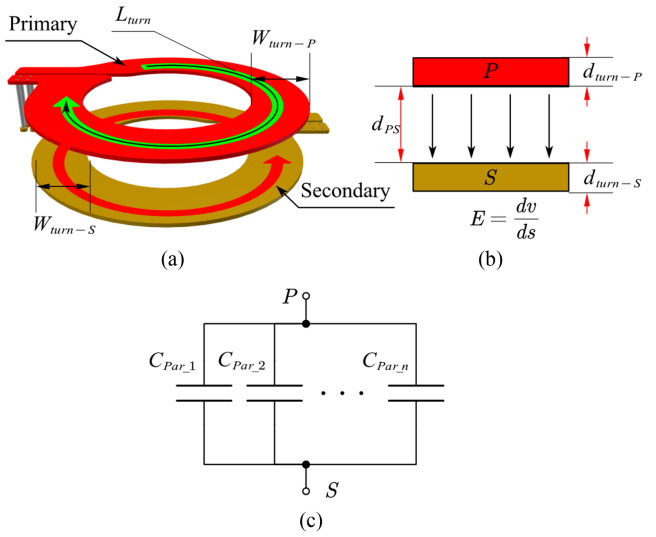


Fig. 3. Equivalent model of winding layers structure capacitance (a) 3-D model of the primary and secondary windings (b) parasitic plate capacitance model (c) equivalent circuit model.

B. Winding Layers Structure Capacitance

The parasitic capacitance generated by the winding layer structure of the HFT (PCB) is shown in Fig. 3.

As shown in Fig. 3(a), the windings of the PCB transformer are typically designed in a flattened configuration. The potential difference between the primary and secondary windings leads to an uneven distribution of electric field energy, thereby generating parasitic capacitance, as depicted in Fig. 3(c). These parasitic capacitances are primarily located between winding layers, turns, and between the windings and the shielding layer, thus affecting the transformer's performance. Therefore, altering the winding structure to prevent the formation of capacitive structures can effectively mitigate parasitic capacitance.

The parasitic capacitance of the winding structure can be calculated using the parallel plate capacitor model. The calculation principle is

$$\begin{cases} C_{ps} = \varepsilon_{ps} \frac{S_{ps}}{d_{ps}} \\ S_{ps} = L_{turn} W_{turn-P} \\ W_{turn-P} = W_{turn-S} \\ d_{turn-P} = d_{turn-S} \end{cases} \tag{11}$$

where L_{turn} and W_{turn} are the length and width of a single turn of the winding, respectively. d_{ps} is the distance between layers, and ε_{ps} is the dielectric constant of the material between the layers.

Increasing the distance between windings would result in an excessively thick PCB, affecting its usability. Therefore, under d_{ps} constant conditions, i.e., with the interlayer spacing and thickness of the PCB transformer fixed, the parasitic capacitance is proportional to S_{ps}. Consequently, the larger the overlapping area between the windings, the greater the parasitic capacitance.

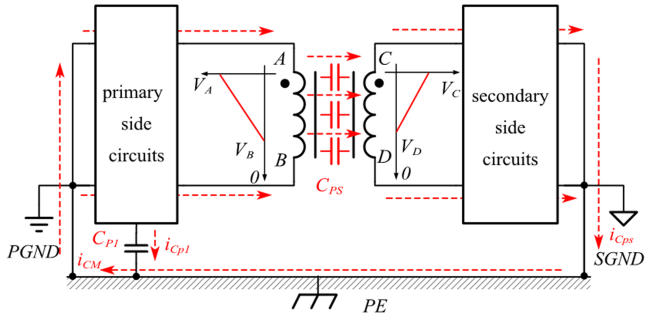


Fig. 4. Transmission path of common mode interference in transformers.

C. Common-Mode Current Conduction Model

High-frequency transformers experience rapid current fluctuations during operation, inducing high-frequency charge transfer in the parasitic capacitance, resulting in EMI. These interferences are mainly manifested as common-mode noise, originating from the uneven distribution of currents on different paths within the system. As shown in Fig. 4 [24], the existence of a ground or other common paths in the system will exacerbate this uneven current distribution, leading to the generation of common-mode currents.

In Fig. 4, the common-mode current mainly consists of the parasitic capacitance i_{Cp1} current formed by the high-frequency potential difference from the primary side to ground and the parasitic capacitance i_{Cps} current within the transformer winding

$$i_{CM} = i_{Cp1} + i_{Cps}. \tag{12}$$

This study only considers the parasitic capacitance currents of the transformer winding.

The potential at any point on the transformer winding is

$$v_{P\_R} = \frac{v_A - v_B}{l_{AB}} l_{pB} + v_B \tag{13}$$

$$v_{S\_R} = \frac{v_C - v_D}{l_{CD}} l_{RD} + v_D. \tag{14}$$

The parasitic capacitance current of the transformer winding is

$$\begin{aligned} i_{Cps} &= C_{ps} \frac{d}{dt} \left[\frac{1}{2}(v_A + v_B) - \frac{1}{2}(v_C + v_D) \right] \\ &= C_{ps} \frac{d}{dt} (\bar{v}_{AB} - \bar{v}_{CD}). \end{aligned} \tag{15}$$

When the parasitic capacitance of the winding is significant, the common-mode current generated by the primary winding of the transformer will be coupled to the secondary side, resulting in circuit output noise and instability. Under high-frequency conditions, common-mode noise interference not only disrupts the normal operation of the secondary side circuit, but it can also propagate outward as electromagnetic waves through other circuit components or connecting wires, causing damage to the surrounding environment and equipment. As a result, improving the transformer winding structure and lowering parasitic capacitance can efficiently decrease high-frequency common-mode noise interference.

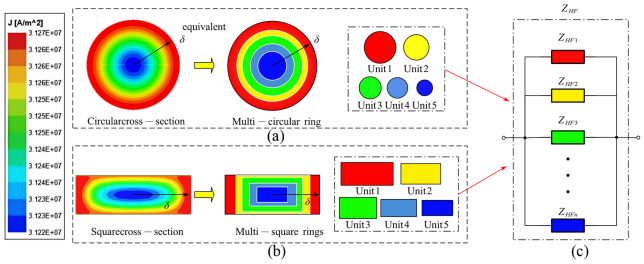


Fig. 5. High-frequency skin effect in conductors and the AC impedance model: (a) equivalent model of circular cross-section, (b) equivalent model of square cross-section, and (c) equivalent AC impedance circuit model.

D. High-Frequency Skin Effect and AC Impedance

At high frequencies, the skin effect and proximity effect within the transformer winding conductor become crucial, leading to significantly increased eddy current losses and ac impedance losses. Fig. 5 shows the current density affected by the skin effect in the cross-section of a copper conductor.

In Fig. 5, the skin effect causes high-frequency currents to concentrate in a thin layer at the surface of the conductor. The current density decreases nonlinearly from the surface towards the center of the conductor, increasing ac impedance. Specifically, the ac impedance is higher towards the interior of the conductor and lower near the surface. An equivalent model treats the conductor cross-section as multiple parallel conductor elements, each with different impedances, as shown in Figs. 5(a) and 5(b).

The skinning depth is calculated as

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} = \sqrt{\frac{1}{\pi f\mu\sigma}}. \tag{16}$$

From (16), it can be seen that as the frequency increases, the skin depth decreases and the ac impedance gradually increases. This means that at high frequencies, the ac losses in the windings become the main source of losses in high frequency transformers. The equivalent impedance of the winding at high frequency can be divided into two parts: The dc part and the ac part, as follows:

$$\begin{aligned} Z_{HF} &= \frac{\prod Z_{HF\_i}}{\sum Z_{HF\_i}} \\ &= Z_{HF,AC} + R_{HF,DC} = (1 + k_s + k_p)\frac{l}{\sigma A}. \end{aligned} \tag{17}$$

In (17), $R_{HF,DC}$ represents the dc resistance, while $Z_{HF,AC}$ is the ac resistance influenced by the skin effect coefficient k_s and the proximity effect coefficient k_p [25]

$$k_s = \frac{R_{AC,Skin}}{R_{DC}} = \frac{bh}{(b+h)}\frac{\sqrt{\pi f\mu\sigma}}{2} \tag{18}$$

$$k_p \approx \frac{R_{AC,prox}}{R_{DC}} = \pi^2 f^2 \mu^2 \sigma^2 \left(\frac{Nh^2}{3}\right)^2. \tag{19}$$

Combining (17)–(19) and considering the high-frequency inductive reactance of the winding, the high-frequency impedance model for the winding can be expressed as

$$\begin{aligned} Z_{HF,AC} = &\left(\frac{bh}{(b+h)}\frac{\sqrt{\pi f\mu\sigma}}{2} + f^2\mu^2\sigma^2N^2h^4\right)\frac{1}{\sigma bh} \\ &+ j2\pi fL \end{aligned} \tag{20}$$

where b is the wire width; h is the wire thickness; N is the number of winding turns.

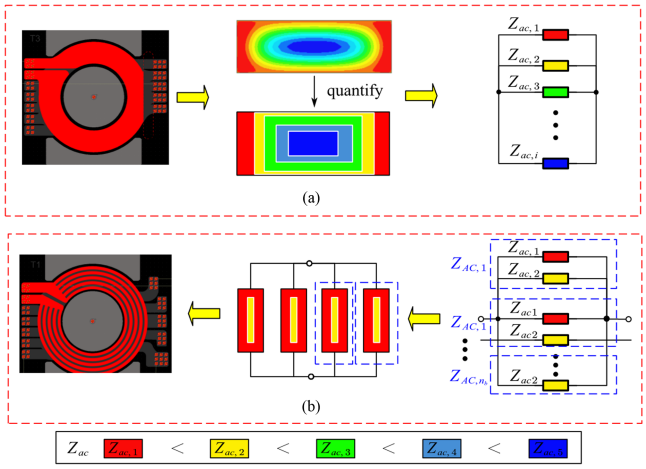


Fig. 6. MBPC Winding Structure (a) STSP cross-sectional equivalent impedance model (b) MBPC cross-sectional equivalent impedance model.

III. Improvement of Parallel Interleaved Winding Structure

A. Multibranch Parallel Connection Structure

The traditional HFT (PCB) winding structure suffers from severe skin effect, high ac impedance, and significant eddy current losses at high frequencies due to its single-turn, single-path (STSP) design. To address these issues, this work proposes a Multibranch Parallel Connection (MBPC) design, illustrated in Fig. 6.

A. MBPC Design Steps:

1) Calculate the skin depth δ at the given frequency using (16).
2) Based on the skin depth δ, calculate the design branch width w_i

$$w_i = 2k\delta \tag{21}$$

where k is the branch width scaling factor, designed according to the fabrication process and requirements.

3) Based on branch width w_i and the winding window width W, calculate the number of parallel branches n_b

$$n_b = \left\lceil \frac{W}{2w_i} \right\rceil. \tag{22}$$

4) Set the branch spacing $d = w_i$ to ensure that the primary and secondary windings are appropriately staggered.

The high-frequency equivalent impedance model for the STSP winding of the HFT (PCB) is illustrated in Fig. 6(a). The

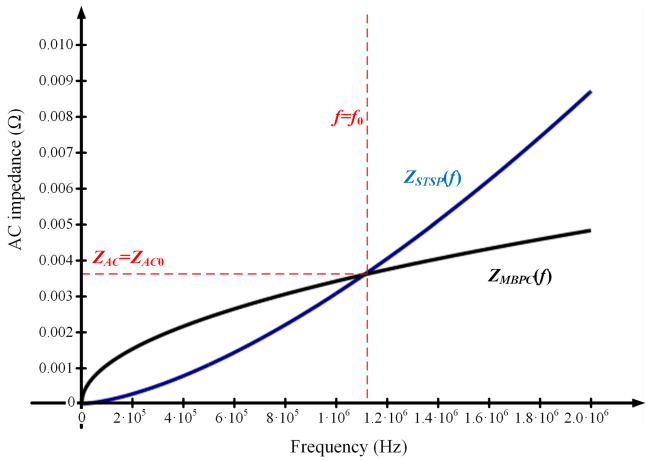


Fig. 7. AC impedance variation curves of STSP and MBPC structures.

high-frequency ac impedance of a STSP is

$$Z_{STSP} = \left(\frac{bh}{(b+h)}\frac{\sqrt{\pi f\mu\sigma}}{2} + f^2\mu^2\sigma^2N^2h^4\right)\frac{1}{\sigma bh} + j2\pi fL. \tag{23}$$

Dividing the flattened STSP winding into multiple winding branches and parallel connections forms the MBPC structure, resulting in the high-frequency equivalent circuit model shown in Fig. 6(b). The high-frequency ac impedance of the MBPC structure winding is

$$Z_{MBPC} = \left(\frac{bh}{(b+2n_bh)}\frac{\sqrt{\pi f\mu\sigma}}{2} + 2f^2\mu^2\sigma^2N^2h^4\right)\frac{2}{\sigma bh} + j2\pi fL. \tag{24}$$

Equating (23) and (24), the frequency is:

$$f_0 = \sqrt[3]{\frac{1}{3\mu^3\sigma^3h^4}\frac{b^2(2n_b-1)^2}{(b^2+bh(2n_b+1)+2n_bh^2)^2}}. \tag{25}$$

As shown in Fig. 7, when $f \geq f_0$, get $Z_{MBPC} \leq Z_{STSP}$. The ac impedance of the MBPC structure is less than the AC impedance of the STSP structure.

The MBPC structure optimizes the winding design to improve high-frequency current distribution, reduce conductor losses, and enhance overall transformer performance. By cleverly splitting the traditional STSP winding into multiple parallel branches, each branch is laid out and spaced to ensure uniform current flow, effectively mitigating the skin effect, proximity effect, and eddy current losses at high frequencies.

B. Branch Horizontal Interleaved Structure

To optimize the parasitic capacitance of HFT (PCB) windings, this work propose an improved branch horizontal interleaved structure (BHI) for primary and secondary windings based on the MBPC structure, as shown in Fig. 8.

Parasitic capacitance mainly exists between adjacent conductors. In HFT (PCB) transformers, the overlapping area between primary and secondary windings leads to parasitic capacitance, as shown in Fig. 8(a). By redesigning the layout of primary and secondary windings to minimize overlapping in the horizontal projection, the parasitic capacitance can be significantly reduced. This is achieved by ensuring that each primary winding branch is located in the gap between secondary winding branches, as shown in Fig. 8(b). This layout reduces the overlapping area, thereby decreasing parasitic capacitance.

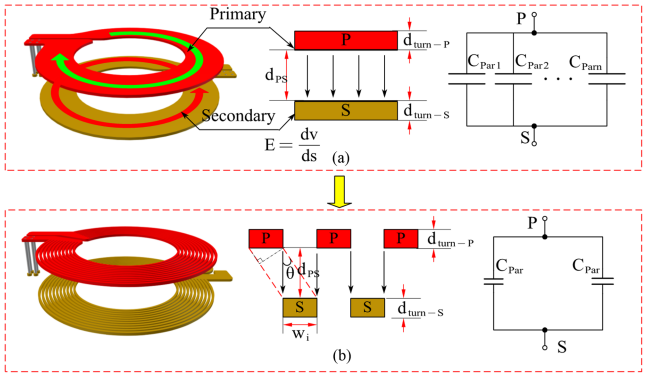


Fig. 8. Equivalent Parasitic Capacitance Model of Winding Structure. (a) Conventional Structure. (b) BHI Structure.

The parasitic capacitance between layers in the conventional structure is calculated according to (11). The calculation principle of the layers parasitic capacitance in the BHI structure is

$$d_{ps,BHI} = \sqrt{{d_{ps}}^2 + w_i^2} \tag{26}$$

$$S_{ps,BHI} = L_{turn}n_b\frac{w_i^2}{d_{ps}} \tag{27}$$

$$C_{BHI,ps} = \varepsilon_{ps}\frac{S_{ps,BHI}}{d_{ps,BHI}} = \varepsilon_{ps}\frac{L_{turn}n_b\frac{w_i^2}{d_{ps}}}{\sqrt{{d_{ps}}^2 + w_i^2}}. \tag{28}$$

The BHI structure effectively reduces parasitic capacitance and suppresses high-frequency common-mode noise. By minimizing parasitic capacitance and optimizing winding layout, the BHI design enhances the EMI performance, stability, and reliability of PCB transformers, which is crucial for the normal operation of electronic equipment in various electromagnetic environments.

C. Vertical Interleaved Winding Structure

To ensure tight electromagnetic coupling between primary and secondary windings, this work propose the segmented interleaved (SI) and completely intertwined (CI) structures, summarized as the Vertical Interleaved Winding (VIW) structure, based on the design principles in [20]. The two structures are illustrated in Fig. 9.

Two design principles for the VIW structure are outlined as follows:

C. Design Principle 1:

1) If the transformer is a step-up transformer

$$N_p < N_S$$

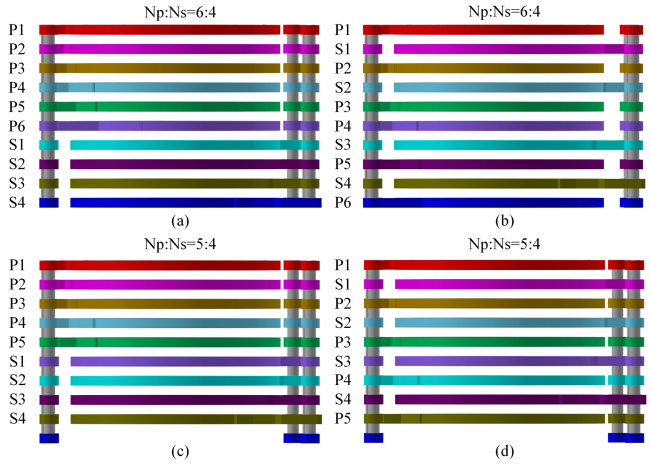


Fig. 9. Vertical interleaved winding structures (a) conventional structure (6:4) (b) SI structure (6:4) (c) conventional structure (5:4) (d) CI structure (5:4).

then the design principle is to place the secondary winding as the top and bottom layers.

2) If the transformer is a step-down transformer

$$N_p > N_S$$

then the design principle is to place the primary winding as the top and bottom layers.

C. Design Principle 2:

1) If the difference in turns is equal to 1

$$\max(N_p, N_S) - \min(N_p, N_S) = 1$$

the CI structure is adopted, as shown in Fig. 9(d).

2) If the difference in turns is greater than 1

$$\max(N_p, N_S) - \min(N_p, N_S) \neq 1$$

the SI structure is adopted, as shown in Fig. 9(b).

For the SI structure design, the segmentation number is determined first

$$n_{seg} = \max(N_p, N_S) - \min(N_p, N_S)(n \geq 2).$$

Then, each segment is designed using the completely intertwined structure sequentially. It can be observed that the CI structure is a special case within the SI structure.

D. Design Flow

Combining the MBPC, BHI, and VIW structures, this work proposes the Parallel Interleaved Winding High-Frequency PCB Transformer (PIW-HFT). The design process is shown in Fig. 10.

Take $N_p : N_S = 6 : 4, f$ =1MHz, EIR20 core structure as an example to design PIW-HFT, the design flow is shown in Fig. 11.

IV. Experimental Verifications

The experiment utilized Altium Designer to design PCB transformer windings, with the magnetic core material chosen as TP5E with an EIR20 structure. While ensuring consistency in the magnetic core material and structure, both conventional

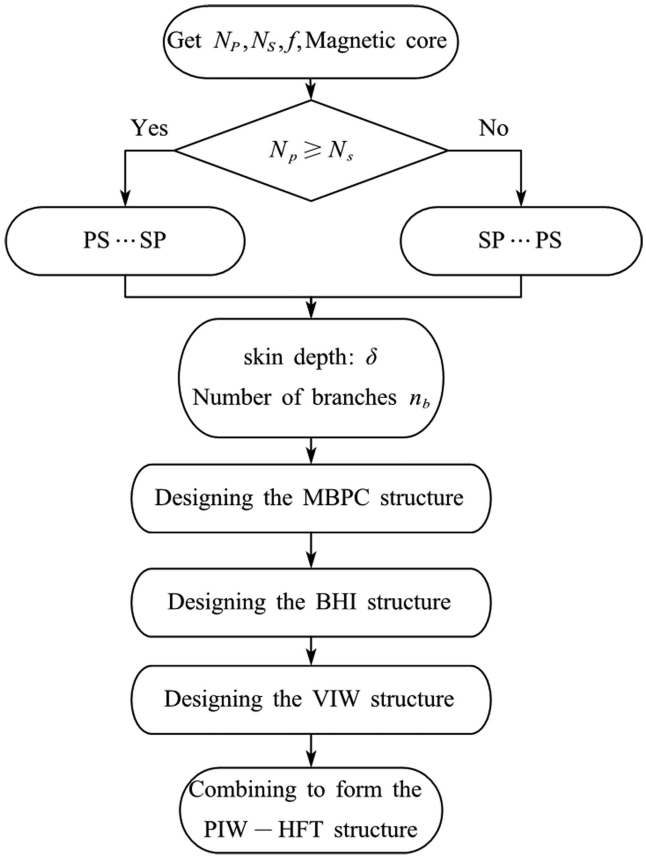


Fig. 10. PIW-HFT (PCB) Design Flow.

TABLE I
Transformer Design Parameters

Symbol	Description	Value
N_P	primary turns	6(5)
N_S	secondary turns	4
ρ	Winding resistivity	1.75×10^{-8} $\Omega \cdot m$
μ	Winding permeability	$4\pi \times 10^{-7}$ H/m
μ_i	Core initial permeability	1200 H/m
B_s	Saturation flux density	520 $mT(25°C)$
ρ_c	Electrical resistivity	9 $\Omega \cdot m$
A_e	Core effective cross-sectional area	60.09
V_e	Core effective volume	1416.70
f	Test frequency	$0.1 - 2$ MHz

HFT and PIW-HFT (PCB) were designed and fabricated for comparative experimental research. The winding structure of the experimental transformer is illustrated in Fig. 12. Table I contains a complete list of design parameters.

To investigate the parasitic parameters of PIW-HFT (PCB) under different branch width settings, three sets of transformers with different scaling factors were designed (T5, T6, T7). The design frequency was set to f =1MHz, and the branch width scaling factors were set to k=2, k=3, and k=5 for comparative experiments. Table II presents the winding parameters of PIW-HFT (PCB) at different k values.

A. Simulation of Near Field

The electric and magnetic fields of the proposed PIW-HFT (PCB) windings are simulated for single turn and for the winding

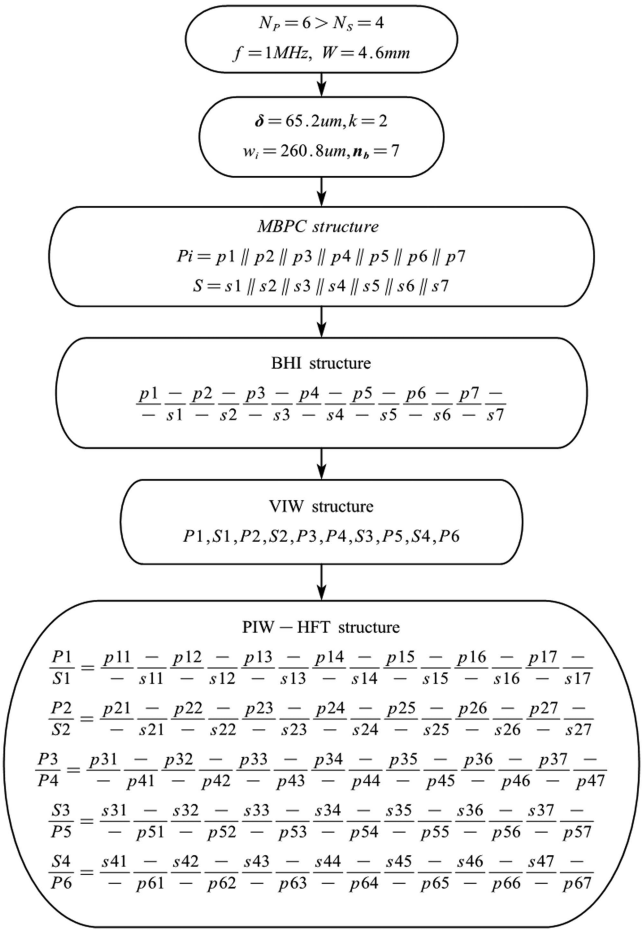


Fig. 11. PIW-HFT (6:4) Design Flow.

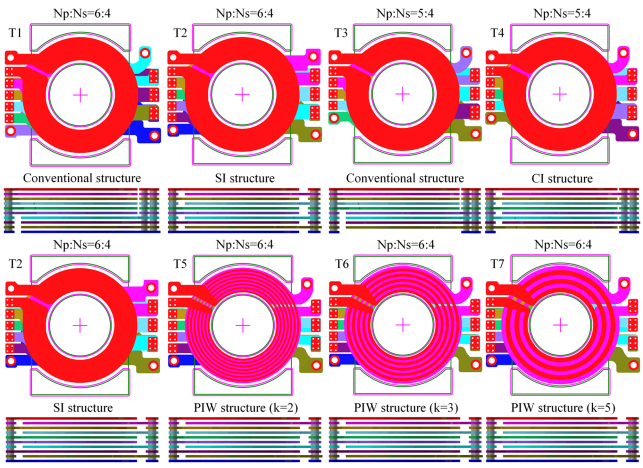


Fig. 12. Main view of experimental transformer winding design.

TABLE II
WINDING PARAMETERS OF WPI-HFT (PCB) WITH DIFFERENT K VALUES

Transformer	Scaling factors	Branch width	Number of branches
T5	2	10.2 mil	7
T6	3	15.4 mil	5
T7	5	25.6 mil	3

as a whole. As well as the current density of different transformer windings are simulated and the simulation results are shown in Figs. 13–17.

Fig. 13 shows the electric and magnetic field simulations for each turn of the T5 winding, and Figs. 14-15 show the near electric and magnetic field simulations for the windings of the SI structure (T2) and the PIW-HFT (PCB) structure (T5, T6, and T7) as a whole at an operating frequency of 2 MHz. The electric field distribution shows a uniform charge distribution in the conductors and a uniform current distribution inside each parallel branch. The magnetic field distribution reflects that each parallel branch has a small eddy current loss.

Figs. 16–17 shows that as the frequency increases, the skin effect becomes more pronounced in conventional transformer windings. The PIW-HFT (PCB) with k= 2 exhibits a more uniform current density due to the smaller branch width, and the current density remains stable at high frequencies. Conversely, the k=5 transformer shows uniform current density at low frequencies but a more significant skin effect at high frequencies. Thus, the branch width must be designed according to the operating frequency to achieve optimal performance.

B. Simulation of Parasitic Parameter

The parasitic capacitance, ac-$*$ impedance and dc impedance of the PIW-HFT winding structure are simulated and analyzed using ANSYS Q3D platform. The simulation results are shown in Figs. 18–20.

Fig. 18 shows that the SI structure (T2) and CI structure (T4) have higher parasitic capacitance and lower leakage inductance than conventional HFT structures (T1, T3). The PIW-HFT (PCB) structures (T5, T6, and T7) exhibit both lower parasitic capacitance and leakage inductance. At 1 MHz, the parasitic capacitance of T5, T6, and T7 is reduced by 28.62%, 38.77%, and 59.92%, respectively, compared to T2. Similarly, their leakage inductance is reduced by 74.12%, 65.68%, and 77.13% compared to T1. These results validate the advantages of the BHI structure and the VIW structure.

In Fig. 19, the PIW-HFT (PCB) structures (T5, T6, T7) show higher ACR at low frequencies, but as the frequency increases, the ACR growth rate is lower compared to conventional HFT (T1, T2) windings. The conventional HFT structures exhibit lower ACR at low frequencies but a higher growth rate. Within the frequency range of 0.1–2 MHz, T1 and T2 have ACR growth rates of 352.33% and 548.91%, respectively, while the PIW–HFT structures have growth rates of 231.53%, 245.27%, and 280.82% . These results confirm the high-frequency advantages of the MBPC structure.

Fig. 20 shows that the DCR parameter remains constant regardless of frequency. The PIW-HFT windings have a slightly higher initial DCR due to their smaller cross-sectional area compared to conventional HFTs, with a maximum difference of 15.257 mΩ (T5 vs. T1). The DCR values for T1 and T2, T3 and T4, are identical, aligning with actual conditions.

The simulation results align well with actual trends, demonstrating high reliability. From the simulations, it is clear that the

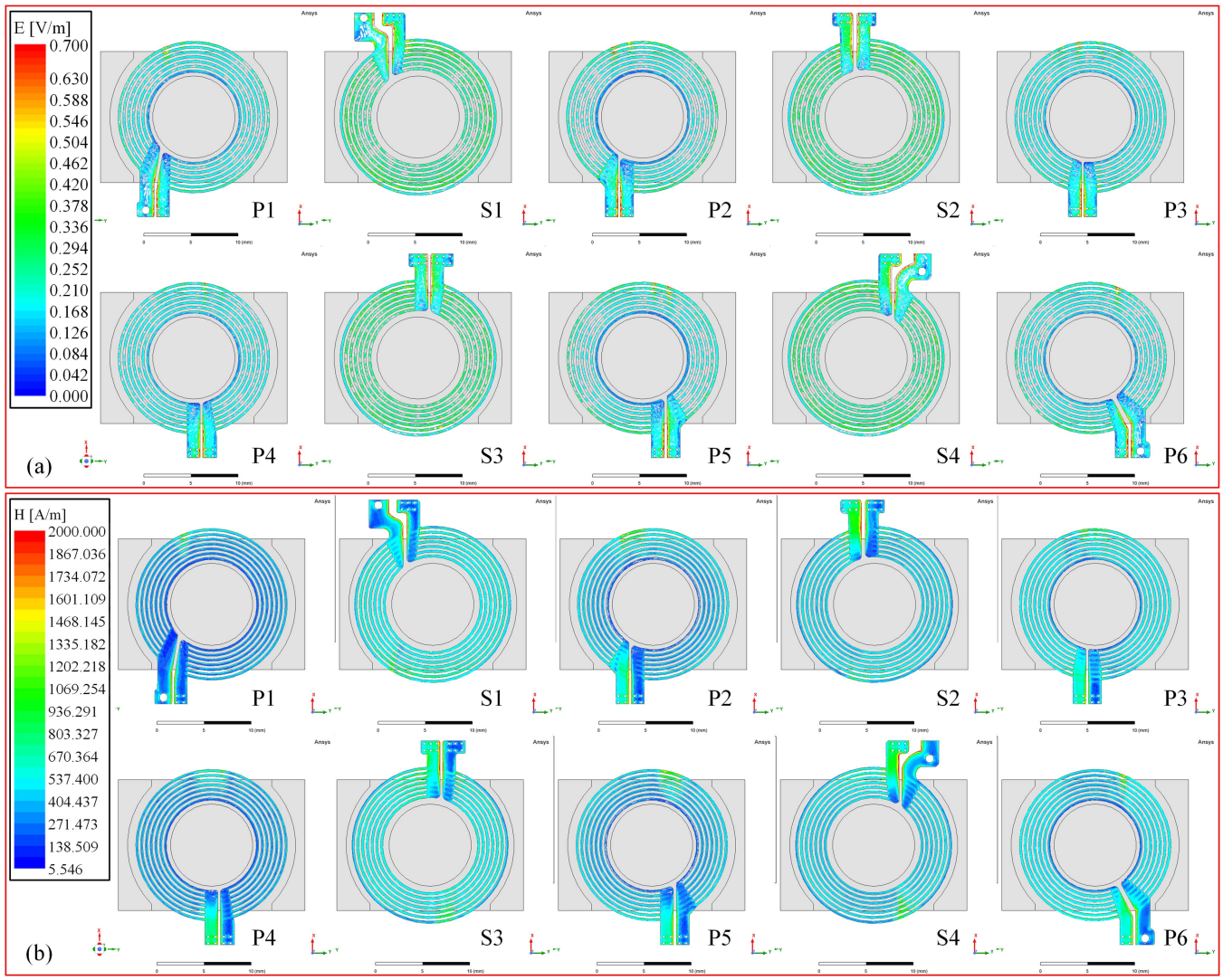


Fig. 13. Electric and magnetic field distribution per layer of winding at 2 MHz frequency of T5 (a) electric field (b) magnetic field.

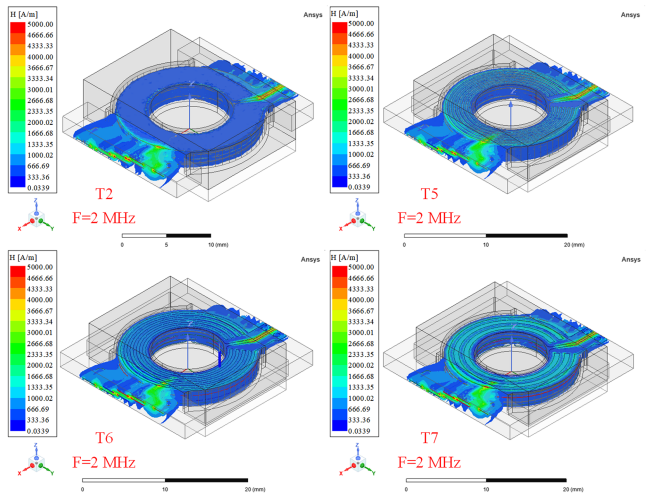


Fig. 14. Distribution of near-magnetic field at f=2 MHz frequency.

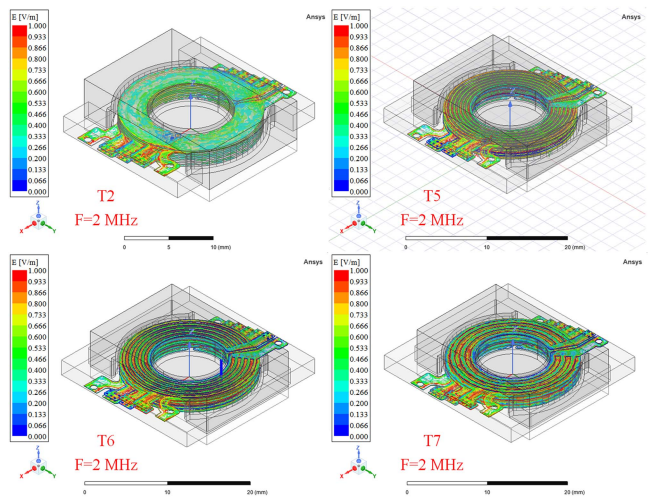


Fig. 15. Distribution of near-electric field at f=2 MHz frequency.

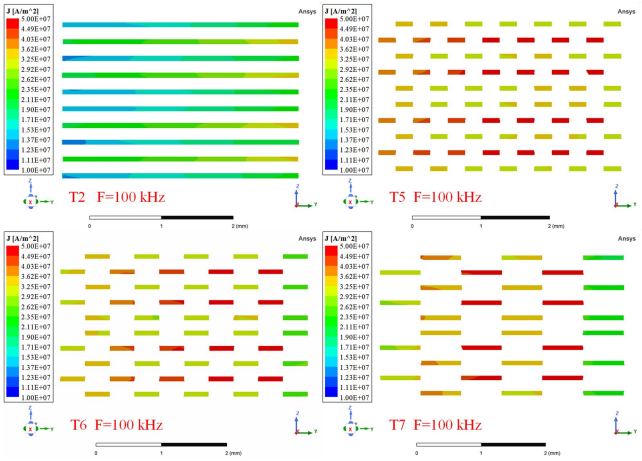


Fig. 16. Distribution of high-frequency current density at f=100 KHz.

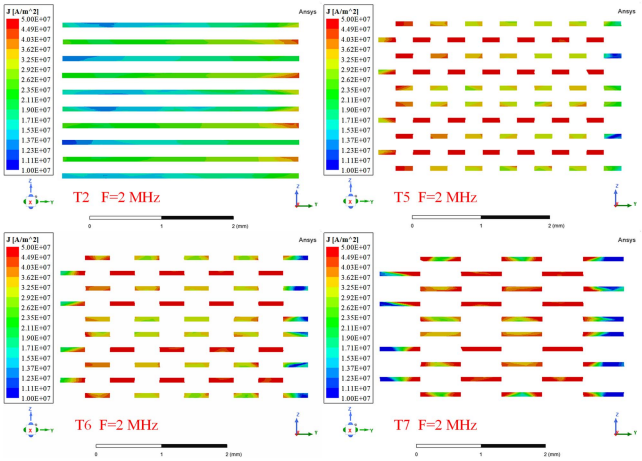


Fig. 17. Distribution of high-frequency current density at f=2 MHz.

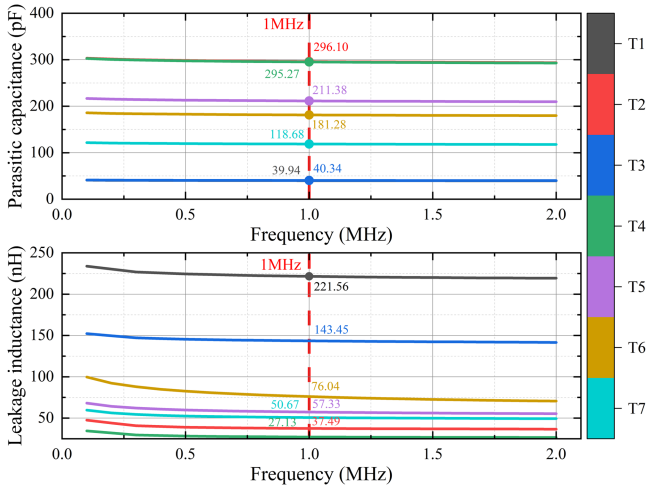


Fig. 18. Variation curves of HFT parasitic capacitance and leakage inductance with frequency.

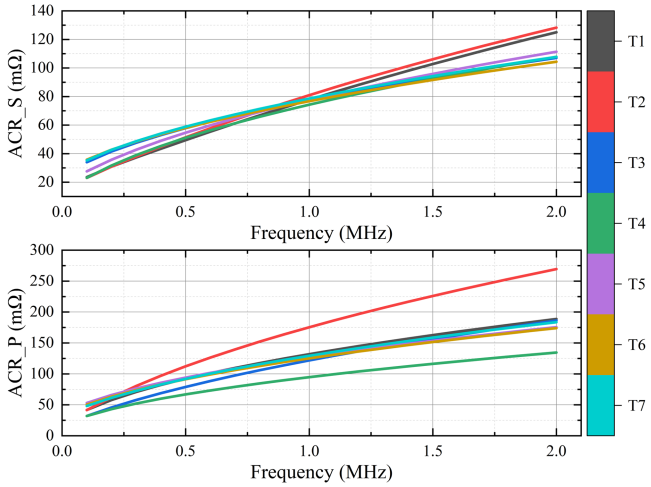


Fig. 19. Variation curve of ACR of primary and secondary windings with frequency.

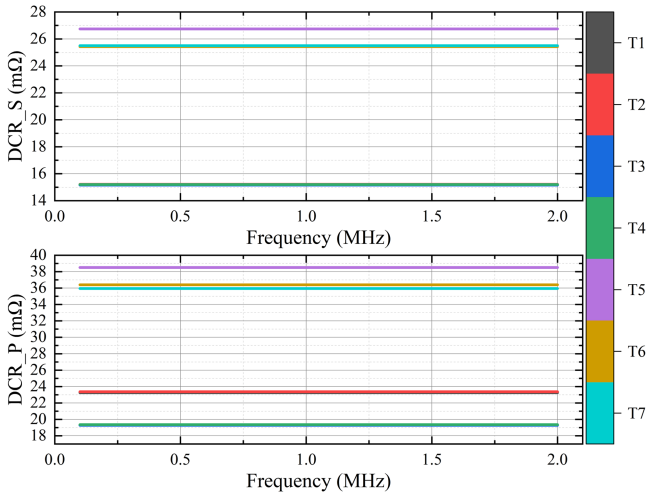


Fig. 20. Variation curve of DCR of primary and secondary windings with frequency.

PIW-HFT winding structure exhibits lower parasitic capacitance and leakage inductance at high frequencies.

C. Experimental Measurements of Parasitic Parameters

Practical transformers were fabricated and tested using the GWINSTEK LCR-8205 A meter to measure leakage inductance, magnetizing inductance, and parasitic capacitance.

Fig. 21 shows that the PIW-HFT winding structures (T5, T6, and T7) have lower parasitic capacitance compared to the SI structure (T2) and CI structure (T4). At 1 MHz, the parasitic capacitance of T5, T6, and T7 is reduced by 37.20%, 43.54%, and 63.06%, respectively, compared to T2.

Fig. 22 shows that the PIW-HFT winding structures (T5, T6, and T7) exhibit lower leakage inductance compared to conventional HFT structures (T1, T3). At 1 MHz, the leakage inductance of T5, T6, and T7 is reduced by 44.64%, 44.05%, and 44.79%, respectively, compared to T1.

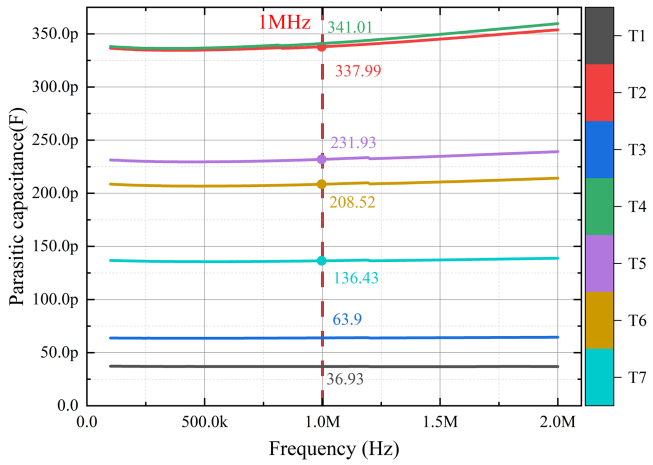


Fig. 21. Variation of HFT parasitic capacitance with frequency.

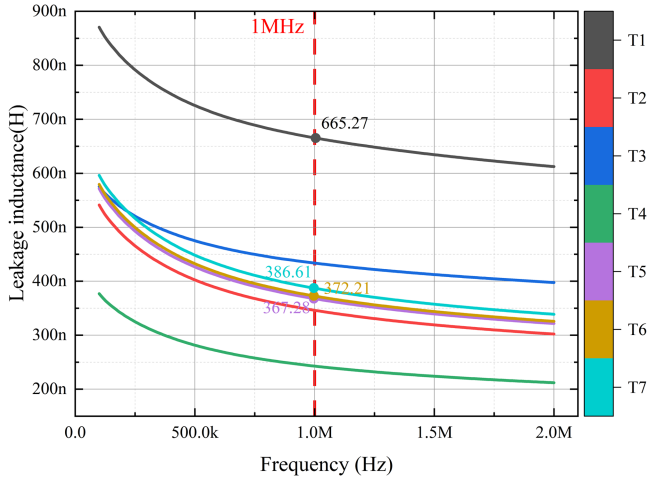


Fig. 22. Variation of transformer leakage inductance with frequency.

Fig. 23 shows that the magnetizing inductance of the PIW-HFT winding structures (T5, T6, and T7) is higher than that of conventional HFT windings as the frequency increases. A higher magnetizing inductance under the same input conditions indicates higher transformer efficiency, lower core losses, and no-load losses, maintaining more stable output voltage and better voltage regulation performance.

In summary, the proposed PIW-HFT winding structures (T5, T6, and T7) exhibit smaller leakage inductance and parasitic capacitance, with more stable high-frequency magnetizing inductance parameters. This helps improve the system's stability and reliability.

D. Application Test Analysis

The CM EMI and output performance of traditional transformers (T1, T2) and PIW-HFT winding structures transformers (T5, T6, T7) were tested through a dc/dc power module. The prototype topology and experimental setup are shown in Fig. 24.

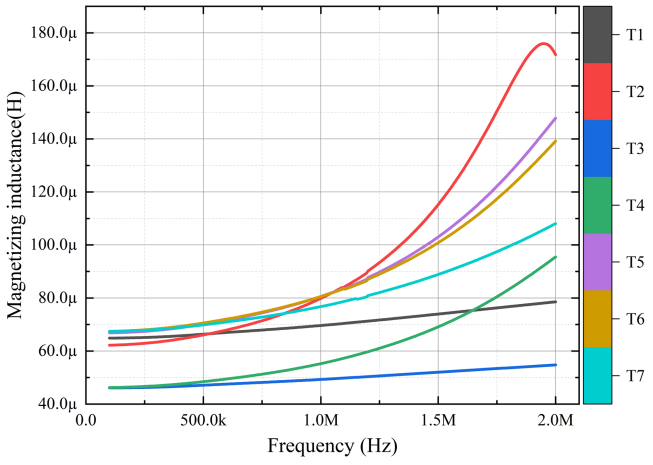


Fig. 23. Variation of transformer magnetizing inductance with frequency.

In order to prevent the magnetic core from affecting the experimental results, the same material, shape and the same batch of cores were used in the experiments. Only the transformer windings were replaced for the experiment, and the above transformer was designed as a half-bridge transformer in the form of magnetic integration and did not optimize the output efficiency of the power module; The results of the test are shown in Figs. 25–28.

Fig. 25 shows the voltage stress $Vpk-pk$ values of 46V, 42V, 41V, and 39V for the conventional winding (T2) and the PIW-HFT winding structures (T5, T6, and T7) at a frequency of f=1.124MHz. The voltage stress is reduced by a maximum of 15% . Fig. 26 CM EMI test results show that the optimized PIW-HFT windings transformer is effective in suppressing CM EMI noise in the mid- and high-frequency bands. In particular, T5,T6, and T7 reduce the maximum EMI high-frequency band amplitude by 3.13 dBuV, 4.31 dBuV, and 7.69 dBuV, respectively, relative to T2. Fig. 27 show that the proposed PIW-HFT winding structures (T5, T6, and T7) have slightly smaller losses than the common sandwich transformer (T2) at the operating frequency of F=1.124 MHz, which can be verified with the efficiency curves of the actual tests.

Fig. 28 shows that at a high frequency of 1.124 MHz, the overall output efficiency of the transformer is lower than that under the test condition of red480 KHz. At high frequencies, the switching losses of power devices, the magnetic losses of transformers, and the copper losses of PCB windings all increase, leading to a decrease in efficiency. This experiment mainly verifies the high - frequency losses of PCB windings. When the load current is 20 A, compared with T1, the efficiency of T5, T6, and T7 is increased by 2.8%, 2.0%, and 1.5% respectively; compared with T2, the efficiency of T5, T6, and T7 is increased by 1.7%, 0.9%, and 0.5% respectively. When the output current is greater than 8 A, the output efficiency of transformers T5, T6, and T7 gradually increases compared with T1 and T2. The experimental results show that in high-frequency larger current output, the improved transformer has higher efficiency than the conventional transformer. It can effectively enhance the output efficiency of the secondary isolated power supply.

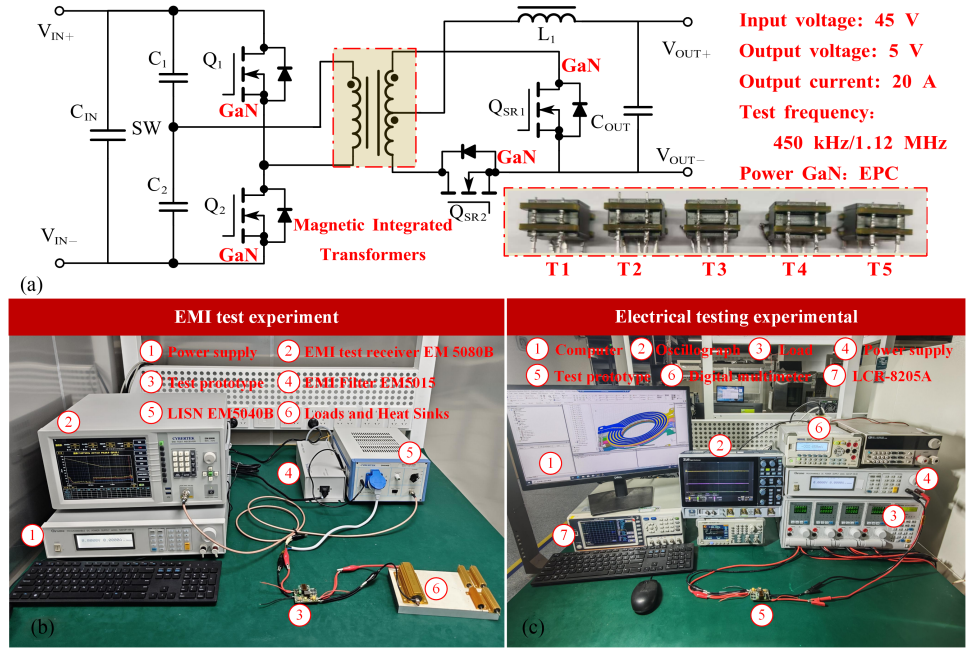


Fig. 24. (a) Final prototype and parameters (b) CM EMI testing setup (c) electrical performance testing setup.

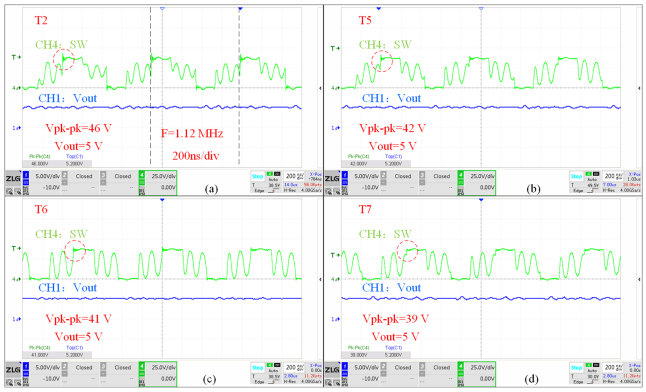


Fig. 25. SW Voltage stresses at f=1.124 MHz.

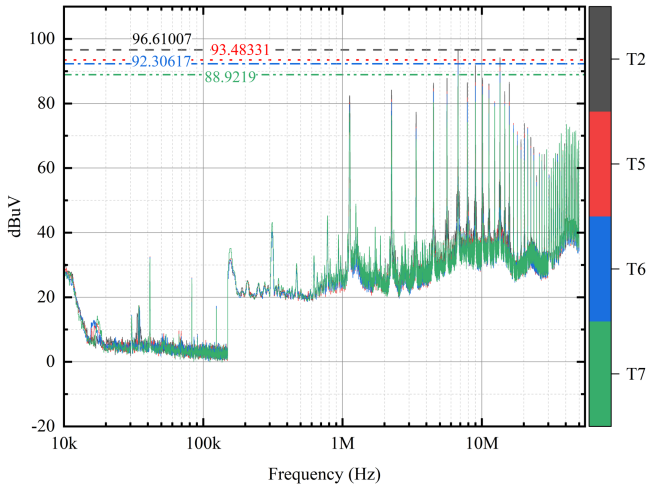


Fig. 26. CM EMI test curves.

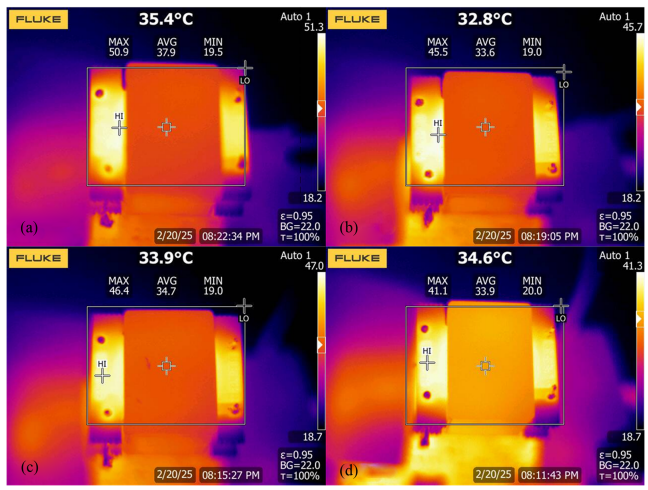


Fig. 27. Transformer heat distribution diagram (a) T2 (b) T5 (c) T6 (d) T7.

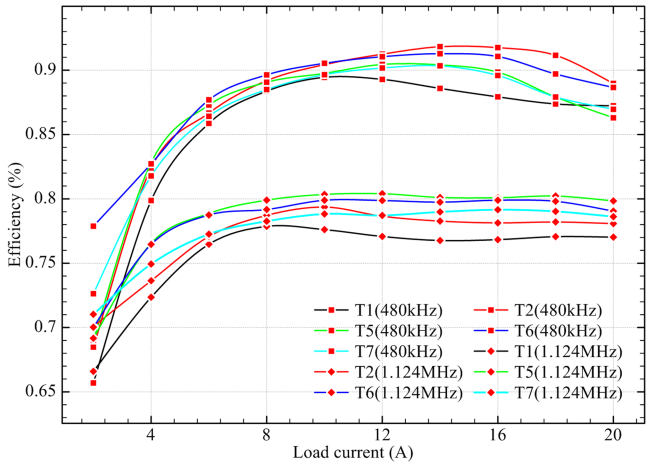


Fig. 28. Output efficiency test curve.

V. Conclusion

This article proposes a multibranch parallel interleaved high-frequency PCB transformer winding structure (PIW-HFT). The structure enhances the primary and secondary side winding coupling, reduces the transformer leakage inductance and winding structure parasitic capacitance, and optimises the high-frequency winding skin effect. This results in a high-frequency winding current density that is uniform and a reduction in winding high-frequency ac loss. Consequently, the HFT energy transfer efficiency is effectively improved. The structural parasitic parameters of the PIW-HFT winding were simulated and measured using the Ansys and LCR-8205 A testing apparatus, respectively. The results demonstrate a reduction in the parasitic capacitance of the PIW-HFT (T5, T6, and T7) by 37.20%, 43.54%, and 63.06%, respectively. In addition, there has been a notable decrease in the leakage inductance, with reductions of 44.64%, 44.05%, and 44.79% . Transformer application experiments were conducted using a 100 W half-bridge synchronous rectifier dc/dc prototype, and the results demonstrated that the efficiency of the PIW-HFT (T5, T6, and T7) was enhanced by 2.8%, 2.0%, and 1.5%, respectively, at high frequencies.

In power supply topologies, the parasitic parameters of high-frequency transformers have different effects in different modes of operation. Complete suppression is not always the best solution. Instead, it is crucial to effectively control these parasitic parameters using technical means such as interlayer insulation, shielding and PIW-HFT techniques to achieve circuit optimization goals.

References

[1] X. Yuan, I. Laird, and S. Walder, "Opportunities, challenges, and potential solutions in the application of fast-switching SiC power devices and converters," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3925–3945, Apr. 2021.

[2] A. I. Emon, A. B. Mustafeez-ul-Hassan, J. Mirza, S. S. Kaplun Vala, and F. Luo, "A review of high-speed GaN power modules: State of the art, challenges, and solutions," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 3, pp. 2707–2729, Jun. 2023.

[3] G. Li and X. Wu, "High power density 48–12V DCX with 3–D PCB winding transformer," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1189–1193, Feb. 2020.

[4] Z. Tang, Y. Yang, and F. Blaabjerg, "Power electronics: The enabling technology for renewable energy integration," *CSEE JPES*, vol. 8, no. 1, pp. 39–52, 2022.

[5] Y. Cao, K. Ngo, and D. Dong, "A scalable electronic-embedded transformer, a new concept toward ultra-high-frequency high-power transformer in DC–DC converters," *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 9278–9293, Aug. 2023.

[6] T. Wang and J. Yuan, "Improvement on loss separation method for core loss calculation under high-frequency sinusoidal and nonsinusoidal excitation," *IEEE Trans. Magn.*, vol. 58, no. 8, Aug. 2022, Art. no. 6301109.

[7] X. Lyu, Y. Li, N. Ren, C. Nan, D. Cao, and S. Jiang, "Optimization of high-density and high-efficiency switched-tank converter for data center applications," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1626–1637, Feb. 2020.

[8] L. Deng et al., "Modeling and analysis of parasitic capacitance of secondary winding in high-frequency high-voltage transformer using finite-element method," *IEEE Trans. Appl. Supercond*, vol. 28, no. 3, Apr. 2018, Art. no. 5500105.

[9] C. Bednarz, H. Schreiber, and M. Leone, "Efficient multiport equivalent circuit for skin and proximity effect in parallel conductors with arbitrary cross sections," *IEEE Trans Electromagn Compat.*, vol. 60, no. 6, pp. 2053–2056, Dec. 2018.

[10] O. de la Barrière et al., "Skin effect and losses in soft magnetic sheets: From low inductions to magnetic saturation," *IEEE Trans. Magn.*, vol. 59, no. 11, Nov. 2023, Art. no. 6301211.

[11] L. Makki et al., "Equivalent circuit model of a pulse planar transformer and endurance to abrupt dv/dt," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 10585–10593, Sep. 2022.

[12] H. Zhang, S. Wang, Y. Li, Q. Wang, and D. Fu, "Two-capacitor transformer winding capacitance models for common-mode EMI noise analysis in isolated DC–DC converters," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8458–8469, Nov. 2017.

[13] Z. Li, E. Hsieh, Q. Li, and F. C. Lee, "High-frequency transformer design with medium-voltage insulation for resonant converter in solid-state transformer," *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 9917–9932, Aug. 2023.

[14] J. Afsharian, N. Zhu, D. D. Xu, B. Gong, and Z. Yang, "Analytical modelling of current sharing and eddy current losses in PCB windings of stacked transformers," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, New Orleans, LA, USA, 2020, pp. 223–230.

[15] R. Yu, T. Chen, P. Liu, and A. Q. Huang, "A 3-D winding structure for planar transformers and its applications to LLC resonant converters," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 5, pp. 6232–6247, Oct. 2021.

[16] L. Keuck, F. Schafmeister, and J. Böcker, "Computer-aided design and optimization of an integrated transformer with distributed air gap and leakage path for an LLC resonant converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Anaheim, CA, USA, 2019, pp. 1415–1422.

[17] B. Zhao, Z. Ouyang, M. C. Duffy, M. A. E. Andersen, and W. G. Hurley, "An improved partially interleaved transformer structure for high-voltage high-frequency multiple-output applications," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 2691–2702, Apr. 2019.

[18] K. Kamran, A. Russo, F. Cammarata, C. Malannino, S. Y. Ciardo, and Z. Ouyang, "Investigation on impact of transformer parasitic capacitance on standby power consumption in power converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Atlanta, GA, USA, 2025, pp. 252–257.

[19] P. Mellor, J. Hoole, and N. Simpson, "Computationally efficient prediction of statistical variance in the AC losses of multi-stranded windings," in *Proc. IEEE Energy Convers. Congr. Expo.*, Vancouver, BC, Canada, 2021, pp. 3887–3894.

[20] X. Zhou et al., "A design method of partially interleaved winding structure with low leakage inductance for planar transformer application," *IEEE Trans. Power Electron.*, vol. 38, no. 5, pp. 6366–6379, May 2023.

[21] Z. Luo, X. Li, C. Jiang, and T. Long, "Characterization of nanocrystalline flake ribbon for high frequency magnetic cores," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 14011–14016, Dec. 2022.

[22] M. Lyu et al., "Development of a novel iron core of fe-based nanocrystalline strip for scanning magnet," *IEEE Trans. Appl. Supercond.*, vol. 34, no. 5, Aug. 2024, Art. no. 4401304.

[23] N. Xia et al., "Laminated nanocrystallineferrite high saturation magnetic flux density composite core for use in highfrequency transformers," *J. Power Electron*. vol. 24, no. 9, pp. 1374–1384, 2024.

[24] L. Xie and X. Yuan, "Non-isolated DC-DC converters with low common-mode noise by using split-winding configuration," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 452–461, Jan. 2022.

[25] R. P. Wojda and M. K. Kazimierczuk, "Proximity-effect winding loss in different conductors using magnetic field averaging," *COMPEL*, vol. 31, no 6, pp: 1793–1814, 2012.

[26] A. Muneeb, A. B. Mirza, M. Ul Hassan, A. Anwar, A. Castiblanco, and F. Luo, "Parasitic capacitances in high step ratio planar transformers for dual active bridge converters: Cause and effect," in *Proc. 50th Annu. Conf. IEEE Ind. Electron. Soc.*, Chicago, IL, USA, 2024, pp. 1–6, doi: 10.1109/IECON55916.2024.10905246.

[27] S. Lee and J. -W. Shin, "Decreasing parasitic capacitances of planar transformers in high-frequency operation," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Long Beach, CA, USA, 2024, pp. 3210–3215.

[28] A. Cremasco, D. Rothmund, M. Curti, and E. A. Lomonova, "Hybrid foil-litz windings for highly efficient and compact medium-frequency transformers," in *IEEE Open J. Power Electron.*, vol. 4, pp. 137–147, 2023.

[29] K.-D. Le, Q.-H. Nguyen, M.-Q. Nguyen, T.-T. Le, T.-N. Quang, and D.-D. Nguyen, "Novel shielding method for planar transformers to suppress common-mode EMI noise and improve soft-switching range," *IEEE Trans. Ind. Electron*., early access, Mar., 4, 2025, doi: 10.1109/TIE.2025.3536537.

[30] X. Zhao, C. -W. Chen, J. -S. Lai, and O. Yu, "Circuit design considerations for reducing parasitic effects on GaN-Based 1-MHz high-power-density high-step-up/down isolated resonant converters," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 2, pp. 695–705, Jun. 2019.
[31] K. Wang, Q. Gao, G. Wei, and X. Yang, "Integrated fractional-turn planar transformer for MHz and high-current applications," *IEEE Trans. Power Electron.*, vol. 38, no. 6, pp. 7374–7384, Jun. 2023.
[32] L. Pniak, L. Quéval, B. Revol, J.-S. N. Teu, C. Gautier, and O. Béthoux, "AC resistance and leakage inductance estimation for planar transformers with parallel-connected windings," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 728–738, Jan. 2023.
[33] M. D'Antonio, S. Chakraborty, and A. Khaligh, "Planar transformer with asymmetric integrated leakage inductance using horizontal air gap," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 14014–14028, Dec. 2021.
[34] Y. -C. Liu et al., "Quarter-turn transformer design and optimization for high power density 1-MHz LLC resonant converter," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1580–1591, Feb. 2020.
[35] Z. Ouyang, W. G. Hurley, and M. A. E. Andersen, "Improved analysis and modeling of leakage inductance for planar transformers," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 4, pp. 2225–2231, Dec. 2019.
[36] Z. Ge, H. Wu, and Y. Liu, "Low-loss segmented shielding technique for PCB-Winding planar transformers," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 12–16, Jan. 2023.

Dejun Ba received the B.S. degree in measurement and instrumentation technology and the M.S. degree in control science and engineering from Lanzhou Jiaotong University, Lanzhou, China, in 2020 and 2023, respectively. He is currently working toward the Ph.D. degree in electronic information with the School of Aeronautics and Astronautics, Zhejiang University, Hangzhou, China.

His current research interests include high power density and high efficiency isolated dc/dc converters.

Faxin Yu (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees in communication and information systems from the School of Electronics and Information Engineering, Harbin Institute of Technology, Harbin, China, in 1997, 1999, and 2002, respectively.

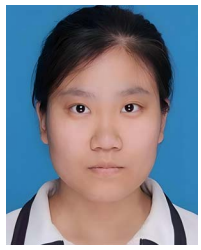
From 2002 to 2005, he was a System Architect with UTStarcom, San Jose, CA, USA. In 2006, he joined the School of Aeronautics and Astronautics, Zhejiang University, Hangzhou, China, as a Postdoctoral Researcher, became an Associate Professor in 2007, and a Professor in 2011. His research interests include MMICs and 3-D HI microsystems.

Yihe Wang received the B.S. degree in electrical engineering from North China Electric Power University, Baoding, China, in 2018, and the M.S. degree in electrical engineering from the Taiyuan University of Technology, Taiyuan, China, in 2021. He is currently working toward the Ph.D. degree in electronic information with the School of Aeronautics and Astronautics, Zhejiang University, Hangzhou, China.

His current research interests include high efficiency and high power density POL converters based on switching capacitor converter.

Xinran Chen received the B.S. degree in electronics and electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2023. He is currently working toward the Ph.D. degree in electronic information with the School of Aeronautics and Astronautics, Zhejiang University, Hangzhou, China.

His research interests include dc–dc converter, power semiconductor, and reliability of GaN HEMT.



Yuxin Niu received the B.S. degree in electronic information engineering from Jilin University, Changchun, China, in 2022. The author is currently working toward the Ph.D. degree in electronic information with the School of Aeronautics and Astronautics, Zhejiang University, Hangzhou, China.

Xiaofeng Lyu (Senior Member, IEEE) received the B.S. degree from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2010, the M.S. degree in power electronics from Zhejiang University, Hangzhou, China, in 2013, and the Ph.D. degree in electronic and computer engineering from North Dakota State University, Fargo, USA, in 2017.

From 2018 to 2022, he was Senior Applications Manager with Navitas Semiconductor, LA, USA. He is currently an Assistant Professor with Zhejiang University, Hangzhou, Cshina. He has authored or coauthored more than 50 papers. His research interests include wide-band gap based high-density power converters.

Dr. Lyu is Guest Editor for IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN INDUSTRIAL ELECTRONICS.